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INTELLIGENT DISCRETES

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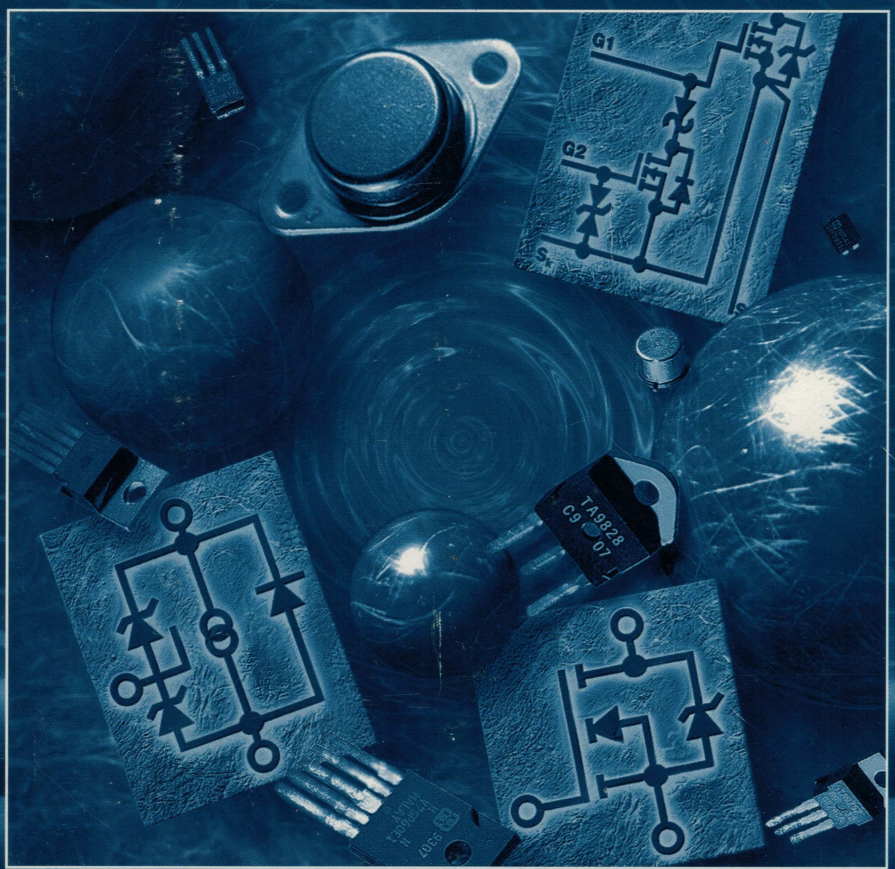

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1. Do you have access to CD-ROM capabilities?
   ❑ At Work ❑ At Home ❑ No
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   ❑ At Work ❑ At Home ❑ No
3. What is your preferred source of product data sheets? (select one)
   ❑ Data Books ❑ CD-ROM ❑ Internet
   ❑ AnswerFAX ❑ Stand-Alone Data Sheets
4. Would you prefer to have a CD-ROM Data Book, a printed Data Book, or both?
   ❑ CD-ROM Book ❑ Printed Book ❑ Both
5. Which best describes your current design stage (select one):
   ❑ Info Collection ❑ Initial Production
   ❑ Prototyping ❑ Breadboarding
   ❑ Design Concept ❑ Full Production
6. When will your design be finalized?
   Month _____ Year _____
7. Expected Annual Volume at full production (select one):
   ❑ 1 to 999 ❑ 5K to 100K
   ❑ 1K to 4999 ❑ > 100K
8. This location has as its primary function (select one)
   ❑ Manufacturing ❑ Design
   ❑ Both

Which category best describes your primary end market? (Select One) [ ]

1100 Video/Imaging
1101 - Desktop Multimedia
1102 - Prof/Broadcast Video
1103 - Medical Imaging
1104 - Cable TV
1105 - Video Conferencing
1199 - Other Video/Imaging

1200 Wireless Communication
1201 - Base Stations
1202 - Wireless LAN/PCS/PB
1203 - Handset/Terminals
1204 - Satellite Communication
1205 - Wireless Local Loop
1299 - Other Wireless Comm.

1300 Government/Military
1301 - Space
1302 - Guidance/Control
1303 - Radar
1304 - Communications
1305 - Avionics
1399 - General Gov't/Military

1400 Telecom
1401 - PBX or CO Line Cards
1402 - Fiber-in-the-Loop
1403 - Wireless Local Loop
1404 - Fiber Optics
1405 - ADSL/HDSL
1406 - Other High Speed Datacomm
1499 - Other Telecom

1500 Computers/Peripherals
1501 - Laptops/Palmtops
1502 - Desktop PCs
1503 - Workstation/File Server
1504 - Disk/Tape Drives
1505 - Printers/Plotter/Scanner
1506 - Datacomm
1599 - General Computer/EDP

1600 Transportation/Consumer
1601 - Power Train
1602 - Vehicle Control
1603 - Safety & Convenience
1604 - Driver Information
1605 - Entertainment
1606 - Electric Vehicles
1607 - Consumer
1699 - Other Transportation

1700 Power Supply/Power Mgmt
1701 - UPS (Uninterruptible Power Supplies)
1702 - AC-DC Power Supplies
1703 - DC-DC Power Supplies
1704 - Transmission Lines
1705 - Utility Substations
1706 - Panel Boxes
1707 - General Protection
1799 - Other Power Supplies/Mgmt

1800 Motor Control
1801 - AC Motors
1802 - 3 Phase Motors
1803 - Brushless
1804 - DC Motors
1805 - Stepper Motors
1899 - Other Motor Control

1900 Industrial Controls & Instrumentation
1901 - Manufacturing System
1902 - High Speed Instrumentation
1903 - Handheld Instruments
1904 - Medical Electronics
1905 - HVAC
1906 - Automatic Test Equipment (ATE)
1999 - General Industrial & Instrumentation

2000 Other Electronics, Not Listed Above

Which best describes your job function? (select one):
❑ Consultant
❑ Corporate/Operating Management
❑ Documentation
❑ Education
❑ Engineering
❑ Manufacturing
❑ Marketing
❑ Purchasing
❑ Quality Assurance
❑ Sales
❑ Systems

What is your primary product interest? (select one):
❑ Analog
❑ Protection Devices
❑ Power Control
❑ Converter
❑ Digital
❑ DSP
❑ Telecom
❑ Rad Hard
❑ Power Discrete
❑ Multimedia
❑ Wireless

Which best describes your job responsibility (select one):
❑ President/Owner
❑ Vice-President/Director
❑ Manager/Section Head
❑ Engineer
❑ Assistant
❑ Independent Contractor

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Harris Semiconductor is a pioneer in developing and producing Discrete Power products for the most demanding Commercial applications in this world and beyond.

This databook fully describes Harris Semiconductor's Power MOSFET product line. It includes a complete set of datasheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program. A New AnswerFAX section has been added to allow Users to request the latest datasheets and have them delivered immediately to your FAX machine. A detailed listing of product Packaging dimensions provides a wide variety of information at your fingertips.

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POWER MOSFET PRODUCTS

This MOSFET Databook offers an extensive line of power MOSFET products for use in a wide range of consumer, industrial and high-reliability applications. This databook contains detailed technical information on the broad line of MOSFETs, including standard power MOSFETs (the popular RF-series types, the IRF-series of industry replacement types, and JEDEC types), MegaFETs, logic-level power MOSFETs (L^2FETs), ruggedized power MOSFETs, advanced discrete, high-reliability and radiation-hardened power MOSFETs.

Separate data sections provide definitive ratings and characteristics for each major category of devices. Data pages for individual devices are organized in numeric/alphanumeric sequence for each section. Because some devices are grouped together to show similarity of function or data, some individual types numbers may be out of sequence. If you have difficulty finding a type number, check the General Information Index, Section 1.

It is our intention to provide you with the most up-to-date information on Power MOSFET Products. For complete, current and detailed technical specifications on any Harris devices please contact the nearest Harris sales, representative or distributor office, listed at the end of the databook; or direct literature requests to:

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HARRIS SEMICONDUCTOR

POWER MOSFETs

FOR COMMERCIAL AND HIGH RELIABILITY APPLICATIONS

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POWER MOSFETs 2

POWER MOSFET CROSS REFERENCE

PRODUCT	HARRIS TYPE
2N6756	2N6756
2N6758	IRF232
2N6758	IRF232R
2N6759	2N6759
2N6759	IRF333
2N6759	IRF333R
2N6760	2N6760
2N6760	IRF330
2N6760	IRF330R
2N6762	2N6762
2N6762	IRF430
2N6762	IRF430R
2N6764	2N6764
2N6764	IRF150
2N6764	IRF150R
2N6764	RFK35N10
2N6766	2N6766
2N6766	IRF250
2N6766	IRF250R
2N6768	2N6768
2N6768	IRF350
2N6768	IRF350R
2N6770	2N6770
2N6770	IRF450
2N6770	IRF450R
2N6782	2N6782
2N6782	IRFF110
2N6782	IRFF110R

PRODUCT	HARRIS TYPE
2N6784	2N6784
2N6784	IRFF210
2N6784	IRFF210R
2N6786	2N6786
2N6786	IRFF310
2N6786	IRFF310R
2N6788	2N6788
2N6788	IRFF120
2N6788	IRFF120R
2N6790	2N6790
2N6790	IRFF220
2N6790	IRFF220R
2N6792	2N6792
2N6792	IRFF320
2N6792	IRFF320R
2N6794	2N6794
2N6794	IRFF420
2N6794	IRFF420R
2N6796	2N6796
2N6796	IRFF130
2N6796	IRFF130R
2N6798	IRFF230
2N6798	IRFF230R
2N6800	2N6800
2N6800	IRFF330
2N6800	IRFF330R
2N6802	2N6802
2N6802	IRFF430

PRODUCT	HARRIS TYPE
2N6802	IRFF430R
2N6804	2N6804
2N6804	IRF9130
2N6804	IRF9142
2N6804	RFM12P10
2N6806	IRF9230
2N6845	IRFF9120
2N6847	IRFF9220
2N6849	2N6849
2N6849	IRFF9130
2N6851	2N6851
2N6851	IRFF9230
BUK452-10	BUZ72A
BUK452-60	RFP3055
BUK453-10	IRF530
BUK453-10	IRF530R
BUK453-10	BUZ20
BUK453-10	RFP12N10
BUK454-20	BUZ32
BUK454-20	IRF630
BUK454-20	IRF630R
BUK454-40	BUZ76
BUK454-40	IRF720
BUK454-40	IRF720R
BUK455-10	RFP22N10
BUK455-10	BUZ21
BUK455-10	IRF542
BUK455-10	IRF542R

Power MOSFET Cross Reference

PRODUCT	HARRIS TYPE
BUK455-40	BUZ60
BUK455-40	IRF730
BUK455-40	IRF730R
BUK455-50	BUZ41A
BUK455-50	IRF830
BUK455-50	IRF830R
BUK456-60	RFP45N06
BUK457-60	IRFBC40R
BUK552-60	RFP3055RL
BUK553-60	RFP25N06L
BUK553-60	RFP17N06L
BUK554-20	RFP8N20L
BUZ10A	BUZ71A
BUZ11	BUZ11
BUZ20	BUZ20
BUZ20	RFP12N10
BUZ21	BUZ21
BUZ21	IRF542
BUZ21	IRF542R
BUZ32	BUZ32
BUZ32	IRF630
BUZ32	IRF630R
BUZ330	RFH10N50
BUZ353	RFH10N50
BUZ41A	BUZ41A
BUZ41A	IRF830
BUZ41A	IRF830R
BUZ42	BUZ42
BUZ42	IRF832
BUZ42	IRF832R
BUZ45	BUZ45
BUZ45	RFM10N50
BUZ45A	BUZ45A
BUZ60	BUZ60
BUZ60	IRF730
BUZ60	IRF730R

PRODUCT	HARRIS TYPE
BUZ60B	BUZ60B
BUZ60B	IRF732
BUZ60B	IRF732R
BUZ71	BUZ71
BUZ71	RFP14N05
BUZ71A	BUZ71A
BUZ72A	BUZ72A
BUZ73	BUZ32
BUZ73	IRF630
BUZ73	IRF630R
BUZ74	IRF820
BUZ74	IRF820R
BUZ74	RFP3N50
BUZ74A	IRF822
BUZ74A	IRF822R
BUZ76	BUZ76
BUZ76	IRF720
BUZ76	IRF720R
BUZ76A	BUZ76A
BUZ76A	IRF722
BUZ76A	IRF722R
IRF120	IRF120
IRF121	IRF121
IRF122	IRF122
IRF123	IRF123
IRF130	IRF130
IRF130	IRF130R
IRF131	IRF131
IRF131	IRF131R
IRF132	IRF132
IRF132	IRF132R
IRF133	IRF133
IRF133	IRF133R
IRF140	IRF140
IRF140	IRF140R
IRF141	IRF141

PRODUCT	HARRIS TYPE
IRF141	IRF141R
IRF142	IRF142
IRF142	IRF142R
IRF143	IRF143
IRF143	IRF143R
IRF150	IRF150
IRF150	IRF150R
IRF150	2N6764
IRF150	RFK35N10
IRF151	IRF151
IRF151	IRF151R
IRF152	IRF152
IRF152	IRF152R
IRF153	IRF153
IRF153	IRF153R
IRF153	2N6763
IRF220	IRF220
IRF221	IRF221
IRF222	IRF222
IRF223	IRF223
IRF230	IRF230
IRF230	IRF230R
IRF230	2N6758
IRF231	IRF231
IRF231	IRF231R
IRF232	IRF232
IRF232	IRF232R
IRF233	IRF233
IRF233	IRF233R
IRF233	2N6757
IRF234	IRF234
IRF235	IRF235
IRF240	IRF240
IRF240	IRF240R
IRF241	IRF241
IRF241	IRF241R

Power MOSFET Cross Reference (Continued)

PRODUCT	HARRIS TYPE
IRF242	IRF242
IRF242	IRF242R
IRF243	IRF243
IRF243	IRF243R
IRF244	IRF244
IRF245	IRF245
IRF250	IRF250
IRF250	IRF250R
IRF250	2N6766
IRF251	IRF251
IRF251	IRF251R
IRF252	IRF252
IRF252	IRF252R
IRF253	IRF253
IRF253	IRF253R
IRF253	2N6765
IRF254	IRF254
IRF255	IRF255
IRF320	IRF320
IRF321	IRF321
IRF322	IRF322
IRF323	IRF323
IRF330	IRF330
IRF330	IRF330R
IRF330	2N6760
IRF331	IRF331
IRF331	IRF331R
IRF332	IRF332
IRF332	IRF332R
IRF333	IRF333
IRF333	IRF333R
IRF333	2N6759
IRF340	IRF340
IRF340	IRF340R
IRF341	IRF341
IRF341	IRF341R

PRODUCT	HARRIS TYPE
IRF342	IRF342
IRF342	IRF342R
IRF343	IRF343
IRF343	IRF343R
IRF350	IRF350
IRF350	IRF350R
IRF350	2N6768
IRF351	IRF351
IRF351	IRF351R
IRF352	IRF352
IRF352	IRF352R
IRF353	IRF353
IRF353	IRF353R
IRF353	2N6767
IRF360	IRF360
IRF362	IRF362
IRF420	IRF420
IRF420	RFM3N50
IRF421	IRF421
IRF421	RFM3N45
IRF422	IRF422
IRF423	IRF423
IRF430	IRF430
IRF430	IRF430R
IRF430	2N6762
IRF431	IRF431
IRF431	IRF431R
IRF432	IRF432
IRF432	IRF432R
IRF433	IRF433
IRF433	IRF433R
IRF433	2N6761
IRF440	IRF440
IRF440	IRF440R
IRF441	IRF441
IRF441	IRF441R

PRODUCT	HARRIS TYPE
IRF442	IRF442
IRF442	IRF442R
IRF443	IRF443
IRF443	IRF443R
IRF448	BUZ45
IRF448	RFM10N50
IRF450	IRF450
IRF450	IRF450R
IRF450	2N6770
IRF451	IRF451
IRF451	IRF451R
IRF452	BUZ45B
IRF452	IRF452
IRF452	IRF452R
IRF453	IRF453
IRF453	IRF453R
IRF453	2N6769
IRF460	IRF460
IRF462	IRF462
IRF510	IRF510
IRF510	IRF510R
IRF511	IRF511
IRF511	IRF511R
IRF512	IRF512
IRF512	IRF512R
IRF513	IRF513
IRF513	IRF513R
IRF520	IRF520
IRF520	IRF520R
IRF521	IRF521
IRF521	IRF521R
IRF522	IRF522
IRF522	IRF522R
IRF523	IRF523
IRF523	IRF523R
IRF530	IRF530

Power MOSFET Cross Reference (Continued)

PRODUCT	HARRIS TYPE
IRF530	IRF530R
IRF531	IRF531
IRF531	IRF531R
IRF532	IRF532
IRF532	IRF532R
IRF533	IRF533
IRF533	IRF533R
IRF540	IRF540
IRF540	IRF540R
IRF541	IRF541
IRF541	IRF541R
IRF542	BUZ21
IRF542	IRF542
IRF542	IRF542R
IRF543	IRF543
IRF543	IRF543R
IRF543	RFP18N08
IRF610	IRF610
IRF610	IRF610R
IRF611	IRF611
IRF611	IRF611R
IRF612	IRF612
IRF612	IRF612R
IRF613	IRF613
IRF613	IRF613R
IRF614	IRF614
IRF620	IRF620
IRF620	IRF620R
IRF621	IRF621
IRF621	IRF621R
IRF622	IRF622R
IRF623	IRF623
IRF623	IRF623R
IRF624	IRF624
IRF625	IRF625
IRF630	BUZ32

PRODUCT	HARRIS TYPE
IRF630	IRF630
IRF630	IRF630R
IRF631	IRF631R
IRF632	BUZ73A
IRF632	IRF632
IRF632	IRF632R
IRF633	IRF633
IRF633	IRF633R
IRF634	IRF634
IRF635	IRF635
IRF640	IRF640
IRF640	IRF640R
IRF641	IRF641
IRF641	IRF641R
IRF642	BUZ31
IRF642	IRF642
IRF642	IRF642R
IRF643	IRF643
IRF643	IRF643R
IRF644	IRF644
IRF645	IRF645
IRF710	IRF712
IRF710	IRF712R
IRF711	IRF711
IRF711	IRF711R
IRF712	IRF710
IRF712	IRF710R
IRF713	IRF713
IRF713	IRF713R
IRF720	BUZ76
IRF720	IRF720
IRF720	IRF720R
IRF721	IRF721
IRF721	IRF721R
IRF722	BUZ76A
IRF722	IRF722

PRODUCT	HARRIS TYPE
IRF722	IRF722R
IRF723	IRF723
IRF723	IRF723R
IRF730	BUZ60
IRF730	IRF730
IRF730	IRF730R
IRF731	IRF731
IRF731	IRF731R
IRF732	BUZ60B
IRF732	IRF732
IRF732	IRF732R
IRF733	IRF733
IRF733	IRF733R
IRF740	IRF740
IRF740	IRF740R
IRF741	IRF741
IRF741	IRF741R
IRF742	IRF742
IRF742	IRF742R
IRF743	IRF743
IRF743	IRF743R
IRF820	IRF820
IRF820	IRF820R
IRF820	RFP3N50
IRF821	IRF821
IRF821	IRF821R
IRF821	RFP3N45
IRF822	IRF822
IRF822	IRF822R
IRF823	IRF823
IRF823	IRF823R
IRF82O	IRF820
IRF82O	IRF820R
IRF82O	RFP3N50
IRF830	BUZ41A
IRF830	IRF830

Power MOSFET Cross Reference (Continued)

PRODUCT	HARRIS TYPE
IRF830	IRF830R
IRF831	IRF831
IRF831	IRF831R
IRF832	BUZ42
IRF832	IRF832
IRF832	IRF832R
IRF833	IRF833
IRF833	IRF833R
IRF840	IRF840
IRF840	IRF840R
IRF841	IRF841
IRF841	IRF841R
IRF842	IRF842
IRF842	IRF842R
IRF843	IRF843
IRF843	IRF843R
IRF9130	2N6804
IRF9130	IRF9130
IRF9130	IRF9142
IRF9130	RFM12P10
IRF9131	IRF9131
IRF9131	IRF9143
IRF9131	RFM12P08
IRF9132	IRF9132
IRF9132	RFM8P10
IRF9133	IRF9133
IRF9133	RFM8P08
IRF9140	IRF9140
IRF9141	IRF9141
IRF9142	2N6804
IRF9142	IRF9130
IRF9142	IRF9142
IRF9142	RFM12P10
IRF9143	IRF9131
IRF9143	IRF9143
IRF9143	RFM12P08

PRODUCT	HARRIS TYPE
IRF9230	IRF9230
IRF9231	IRF9231
IRF9232	IRF9232
IRF9233	IRF9233
IRF9240	IRF9240
IRF9241	IRF9241
IRF9241	RFM10P15
IRF9242	IRF9242
IRF9243	IRF9243
IRF9510	IRF9510
IRF9511	IRF9511
IRF9512	IRF9512
IRF9513	IRF9513
IRF9520	IRF9520
IRF9520	RFP6P10
IRF9521	IRF9521
IRF9521	RFP6P08
IRF9522	IRF9522
IRF9523	IRF9523
IRF9530	IRF9530
IRF9530	IRF9542
IRF9530	RFP12P10
IRF9531	IRF9531
IRF9531	IRF9543
IRF9531	RFP12P08
IRF9532	IRF9532
IRF9532	RFP8P10
IRF9533	IRF9533
IRF9533	RFP8P08
IRF9540	IRF9540
IRF9541	IRF9541
IRF9542	IRF9530
IRF9542	IRF9542
IRF9542	RFP12P10
IRF9543	IRF9531
IRF9543	IRF9543

PRODUCT	HARRIS TYPE
IRF9543	RFP12P08
IRF9620	IRF9620
IRF9621	IRF9621
IRF9622	IRF9622
IRF9623	IRF9623
IRF9630	IRF9630
IRF9631	IRF9631
IRF9632	IRF9632
IRF9633	IRF9633
IRF9640	IRF9640
IRF9641	IRF9641
IRF9641	RFP10P15
IRF9642	IRF9642
IRF9643	IRF9643
IRFAC40	IRFAC40R
IRFAC42	IRFAC42R
IRFBC40	IRFBC40R
IRFBC42	IRFBC42R
IRFD113	IRFD113
IRFD113	IRFD113R
IRFD123	IRFD123
IRFD123	IRFD123R
IRFD1Z0	IRFD1Z0
IRFD210	IRFD210
IRFD210	IRFD210R
IRFD213	IRFD213
IRFD213	IRFD213R
IRFD220	IRFD220
IRFD220	IRFD220R
IRFD223	IRFD223
IRFD223	IRFD223R
IRFD9110	IRFD9110
IRFD9113	IRFD9113
IRFD9120	IRFD9120
IRFD9123	IRFD9123
IRFD9220	IRFD9220

Power MOSFET Cross Reference (Continued)

PRODUCT	HARRIS TYPE
IRFD9223	IRFD9223
IRFF110	2N6782
IRFF110	IRFF110
IRFF110	IRFF110R
IRFF111	IRFF111
IRFF111	IRFF111R
IRFF112	IRFF112
IRFF112	IRFF112R
IRFF113	IRFF113
IRFF113	IRFF113R
IRFF120	IRFF120
IRFF120	IRFF120R
IRFF120	2N6788
IRFF121	IRFF121
IRFF121	IRFF121R
IRFF122	IRFF122
IRFF122	IRFF122R
IRFF122	2N6798
IRFF123	IRFF123
IRFF123	IRFF123R
IRFF130	IRFF130
IRFF130	IRFF130R
IRFF130	2N6796
IRFF131	IRFF131
IRFF131	IRFF131R
IRFF132	IRFF132
IRFF132	IRFF132R
IRFF133	IRFF133
IRFF133	IRFF133R
IRFF210	IRFF210
IRFF210	IRFF210R
IRFF210	2N6784
IRFF211	IRFF211
IRFF211	IRFF211R
IRFF212	IRFF212
IRFF212	IRFF212R

PRODUCT	HARRIS TYPE
IRFF213	IRFF213
IRFF213	IRFF213R
IRFF220	IRFF220
IRFF220	IRFF220R
IRFF220	2N6790
IRFF221	IRFF221
IRFF221	IRFF221R
IRFF222	IRFF222
IRFF222	IRFF222R
IRFF223	IRFF223
IRFF223	IRFF223R
IRFF230	IRFF230
IRFF230	IRFF230R
IRFF231	IRFF231
IRFF231	IRFF231R
IRFF231	RFL4N15
IRFF232	IRFF232
IRFF232	IRFF232R
IRFF233	IRFF233
IRFF233	IRFF233R
IRFF310	IRFF310
IRFF310	IRFF310R
IRFF310	2N6786
IRFF311	IRFF311
IRFF311	IRFF311R
IRFF312	IRFF312
IRFF312	IRFF312R
IRFF313	IRFF313
IRFF313	IRFF313R
IRFF320	IRFF320
IRFF320	IRFF320R
IRFF320	2N6792
IRFF321	IRFF321
IRFF321	IRFF321R
IRFF322	IRFF322
IRFF322	IRFF322R

PRODUCT	HARRIS TYPE
IRFF323	IRFF323
IRFF323	IRFF323R
IRFF330	IRFF330
IRFF330	IRFF330R
IRFF330	2N6800
IRFF331	IRFF331
IRFF331	IRFF331R
IRFF332	IRFF332
IRFF332	IRFF332R
IRFF333	IRFF333
IRFF333	IRFF333R
IRFF420	IRFF420
IRFF420	IRFF420R
IRFF420	2N6794
IRFF421	IRFF421
IRFF421	IRFF421R
IRFF422	IRFF422
IRFF422	IRFF422R
IRFF423	IRFF423
IRFF423	IRFF423R
IRFF430	IRFF430
IRFF430	IRFF430R
IRFF430	2N6802
IRFF431	IRFF431
IRFF431	IRFF431R
IRFF432	IRFF432
IRFF432	IRFF432R
IRFF433	IRFF433
IRFF433	IRFF433R
IRFF9120	IRFF9120
IRFF9121	IRFF9121
IRFF9122	IRFF9122
IRFF9123	IRFF9123
IRFF9130	IRFF9130
IRFF9130	2N6849
IRFF9131	IRFF9131

Power MOSFET Cross Reference (Continued)

PRODUCT	HARRIS TYPE
IRFF9132	IRFF9132
IRFF9133	IRFF9133
IRFF9220	IRFF9220
IRFF9221	IRFF9221
IRFF9222	IRFF9222
IRFF9223	IRFF9223
IRFF9230	2N6851
IRFF9230	IRFF9230
IRFF9231	IRFF9231
IRFF9232	IRFF9232
IRFF9233	IRFF9233
IRFP044	RFG45N06
IRFP054	RFG70N06
IRFP140	IRFP140R
IRFP141	IRFP141R
IRFP142	IRFP142R
IRFP143	IRFP143R
IRFP150	IRFP150
IRFP150	IRFP150R
IRFP152	IRFP140R
IRFP153	IRFP141R
IRFP240	IRFP240R
IRFP241	IRFP241R
IRFP242	IRFP242R
IRFP243	IRFP243R
IRFP244	IRFP244
IRFP245	IRFP245
IRFP250	IRFP250
IRFP250	IRFP250R
IRFP251	IRFP251
IRFP251	IRFP251R
IRFP252	IRFP252
IRFP252	IRFP252R
IRFP253	IRFP253
IRFP253	IRFP253R
IRFP254	IRFP254

PRODUCT	HARRIS TYPE
IRFP255	IRFP255
IRFP340	IRFP340R
IRFP341	IRFP341R
IRFP342	IRFP342R
IRFP343	IRFP343R
IRFP350	IRFP350
IRFP350	IRFP350R
IRFP351	IRFP351
IRFP351	IRFP351R
IRFP352	IRFP352
IRFP352	IRFP352R
IRFP353	IRFP353
IRFP353	IRFP353R
IRFP360	IRFP360
IRFP362	IRFP362
IRFP440	IRFP440R
IRFP441	IRFP441R
IRFP442	IRFP442R
IRFP443	IRFP443R
IRFP450	IRFP450
IRFP450	IRFP450R
IRFP451	IRFP451
IRFP451	IRFP451R
IRFP452	IRFP452
IRFP452	IRFP452R
IRFP453	IRFP453
IRFP453	IRFP453R
IRFP460	IRFP460
IRFP462	IRFP462
IRFP9140	IRFP9140
IRFP9141	IRFP9141
IRFP9142	IRFP9142
IRFP9143	IRFP9143
IRFP9240	IRFP9240
IRFP9241	IRFP9241
IRFP9242	IRFP9242

PRODUCT	HARRIS TYPE
IRFP9243	IRFP9243
IRFPC40	IRFPC40R
IRFPG40	IRFPG40
IRFPG42	IRFPG42
IRFR020	RFD14N05S
IRFR110	IRFR110
IRFR120	IRFR120
IRFR121	IRFR121
IRFR214	IRFR214
IRFR220	IRFR220
IRFR222	IRFR222
IRFR320	IRFR320
IRFR420	IRFR420
IRFR9022	RFD8P05SM
IRFU020	RFD14N05
IRFU110	IRFU110
IRFU120	IRFU120
IRFU121	IRFU121
IRFU214	IRFU214
IRFU220	IRFU220
IRFU222	IRFU222
IRFU320	IRFU320
IRFU420	IRFU420
IRFU9022	RFD8P05
IRFZ20	BUZ71
IRFZ20	RFP14N05
IRFZ22	BUZ71A
IRFZ35	RFP25N06
IRFZ44	RFP45N06
IRLZ24	RFP17N06L
ITXP7N45	IRF843
ITXP7N45	IRF843R
IXFH12N5	IRFP452
IXFH12N5	IRFP452R
IXFH13N5	IRFP450
IXFH13N5	IRFP450R

Power MOSFET Cross Reference (Continued)

PRODUCT	HARRIS TYPE
IXFM12N5	BUZ45B
IXFM12N5	IRF452
IXFM12N5	IRF452R
IXFM13N5	2N6770
IXFM13N5	IRF450
IXFM13N5	IRF450R
IXTH12N4	IRFP453
IXTH12N4	IRFP453R
IXTH12N4	IRFP451
IXTH12N4	IRFP451R
IXTH12N5	IRFP452
IXTH12N5	IRFP452R
IXTH12N5	IRFP450
IXTH12N5	IRFP450R
IXTH15N4	IRFP451
IXTH15N4	IRFP451R
IXTH15N5	IRFP450
IXTH15N5	IRFP450R
IXTM12N4	2N6769
IXTM12N4	IRF453
IXTM12N4	IRF453R
IXTM12N4	IRF451
IXTM12N4	IRF451R
IXTM15N5	2N6770
IXTM15N5	IRF450
IXTM15N5	IRF450R
IXTM6N60	IRFAC40R
IXTP4N45	IRF833
IXTP4N45	IRF833R
IXTP4N45	IRF831
IXTP4N45	IRF831R
IXTP4N50	BUZ42
IXTP4N50	IRF832
IXTP4N50	IRF832R
IXTP4N50	BUZ41A
IXTP4N50	IRF830

PRODUCT	HARRIS TYPE
IXTP4N50	IRF830R
IXTP6N60	IRFBC40R
IXTP7N45	IRF841
IXTP7N45	IRF841R
IXTP7N50	IRF842
IXTP7N50	IRF842R
IXTP7N50	IRF840
IXTP7N50	IRF840R
MLP1N06CL	RLP1N06CL
MTD10N05E	RFD14N05
MTD2N50	IRFU410
MTD2N50	IRFU422
MTD3055E	RFD3055
MTD3055EL	RFD3055RL
MTD3055EL	RFD3055RL
MTH20P08	RFH25P08
MTH20P10	RFH25P10
MTM10N12L	RFM10N12L
MTM10N15L	RFM10N15L
MTM10N35	IRF234
MTM12N08L	RFM12N08L
MTM12N10	2N6756
MTM12N10L	2N6902
MTM12N10L	RFM12N10L
MTM12P08	IRF9131
MTM12P08	IRF9143
MTM12P08	RFM12P08
MTM12P10	2N6804
MTM12P10	IRF9130
MTM12P10	IRF9142
MTM12P10	RFM12P10
MTM13N50E	2N6770
MTM13N50E	IRF450
MTM13N50E	IRF450R
MTM15N35	IRF351
MTM15N35	IRF351R

PRODUCT	HARRIS TYPE
MTM15N40	2N6768
MTM15N40	IRF350
MTM15N40	IRF350R
MTM15N40E	2N6768
MTM15N40E	IRF350
MTM15N40E	IRF350R
MTM15N45	IRF451
MTM15N45	IRF451R
MTM15N50	2N6770
MTM15N50	IRF450
MTM15N50	IRF450R
MTM2N50	IRF422
MTM4N45	IRF431
MTM4N45	IRF431R
MTM4N50	2N6762
MTM4N50	IRF430
MTM4N50	IRF430R
MTM5N35	IRF331
MTM5N35	IRF331R
MTM5N40	2N6760
MTM5N40	IRF330
MTM5N40	IRF330R
MTM6N60	IRFAC40R
MTM7N50	BUZ45A
MTM8N20	2N6758
MTM8N20	IRF230
MTM8N20	IRF230R
MTM8N40	IRF340
MTM8N40	IRF340R
MTM8P08	IRF9133
MTM8P08	RFM8P08
MTM8P10	IRF9132
MTM8P10	RFM8P10
MTM8P20	IRF9242
MTP10N10E	BUZ72A
MTP10N12L	RFP10N12LD

Power MOSFET Cross Reference (Continued)

PRODUCT	HARRIS TYPE
MTP10N15	RFP10N15
MTP10N15L	RFP10N15L
MTP10N25	IRF634
MTP10N35	IRF741
MTP10N35	IRF741R
MTP10N40E	IRF740
MTP10N40E	IRF740R
MTP12N05E	BUZ71A
MTP12N08L	RFP12N08L
MTP12N10E	IRF530
MTP12N10E	IRF530R
MTP12N10L	RFP12N10L
MTP12P05	RFP8P05
MTP12P08	IRF9533
MTP12P08	RFP8P08
MTP12P10	IRF9530
MTP12P10	IRF9542
MTP12P10	RFP12P10
MTP15N05E	BUZ71
MTP15N05E	RFP14N05
MTP15N05L	RFP15N05L
MTP2N25	RFP4N35
MTP2N35	IRF713
MTP2N35	IRF713R
MTP2N40	IRF710
MTP2N40	IRF710R
MTP2N45	IRF823
MTP2N45	IRF823R
MTP2N50	IRF822
MTP2N50	IRF822R
MTP3055E	RFP3055
MTP3055EL	RFP3055RL
MTP3N10L	RFP2N10L
MTP3N45	IRF821
MTP3N45	IRF821R
MTP3N45	RFP3N45

PRODUCT	HARRIS TYPE
MTP3N50E	IRF820
MTP3N50E	IRF820R
MTP3N50E	RFP3N50
MTP4N40E	BUZ76
MTP4N40E	IRF720
MTP4N40E	IRF720R
MTP4N45	IRF831
MTP4N45	IRF831R
MTP4N50E	BUZ41A
MTP4N50E	IRF830
MTP4N50E	IRF830R
MTP5N35	IRF731
MTP5N35	IRF731R
MTP5N40E	BUZ60
MTP5N40E	IRF730
MTP5N40E	IRF730R
MTP6N60	IRFBC40R
MTP6N60E	IRFBC40R
MTP8N20	BUZ32
MTP8N20	IRF630
MTP8N20	IRF630R
MTP8P08	IRF9533
MTP8P08	RFP8P08
MTP8P10	IRF9532
MTP8P10	RFP8P10
MTW10N40E	IRFP340R
MTW14N05E	IRFP450
MTW14N05E	IRFP450R
MTW16N40E	IRFP350
MTW16N40E	IRFP350R
MTW20N50E	IRFP460
MTW23N25E	IRFP254
MTW24N40E	IRFP360
MTW32N20E	IRFP250
MTW32N20E	IRFP250R
MTW33N10E	IRFP150

PRODUCT	HARRIS TYPE
MTW33N10E	IRFP150R
MTW45N10E	RFG40N10
SGSP330	IRF821
SGSP330	IRF821R
SGSP330	RFP3N45
SGSP332	IRF723
SGSP332	IRF723R
SGSP362	IRF543
SGSP362	IRF543R
SGSP362	RFP18N08
SGSP364	IRF831
SGSP364	IRF831R
SGSP369	BUZ41A
SGSP369	IRF830
SGSP369	IRF830R
SGSP575	IRF340
SGSP575	IRF340R
SMD15N05	RFD14N05S
SMP20P10	IRF9540
SMP3P10	IRF9510
SMP40N10	RFP40N10
SMP50N06	RFP45N06
SMP60N06-14	RFP70N06
SMU15N05	RFD14N05
SMV1P10	IRFD9110
SMW12P20	IRFP9240
SMW20P10	IRFP9140
SMW45N10	RFG40N10
SMW70N06-14	RFG70N06
STLT20	RFP3055
STP50N06	RFP45N06

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R MOSFETs

1. R X X XX X XX XXX

FEATURE SUFFIX
- R: Rugged Capabilities Guaranteed
- L: Logic Level 5V Gate
- SM: Surface Mount Leadform (TO-252)
- E: ESD Protected Device
- CS: Current Sensing
- C: Voltage Clamping
- B: Integral Turn-Off Driver

VOLTAGE RATING/10
i.e., .05 = 50V, 10 = 100V, 20 = 200V, etc.

POLARITY
- N: N-Channel
- P: P-Channel

CURRENT RATING
1 = 1A, 10 = 10A, 25 = 25A, etc.

PACKAGE DESIGNATION
- A: MO-093AA
- B: TS-001
- D: TO-251, TO-252 (D-PAK)
- G: TO-247
- H: TO-218AC
- K: TO-204AE (TO-3 with 60 MIL Leads)
- L: TO-205AF (TO-39 with Low Profile Cap)
- M: TO-204AA (TO-3 with 40 MIL Leads)
- P: TO-220AB
- V: 5 Lead TO-247

DEVICE TYPE
- F: Standard MOSFET
- L: Current Limited MOSFET

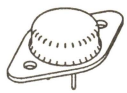
Example: RLP1N08LE ESD Protected, Current Limited, TO-220, 1A, N-Channel, 80V Logic Level MOSFET

RFD15N05SM D-PAK, 15A, N-Channel, 50V, Surface Mount Leadform MOSFET

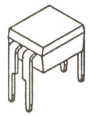
RFP12N06RLE TO-220, 12A N-Channel, 60V, Rugged, Logic Level, ESD Protected MOSFET

TO-205AF

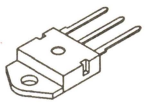
TO-204AA/AE



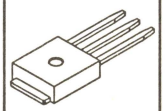
4-LEAD DIP



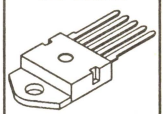
TO-218AC



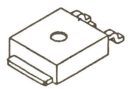
TO-251AA



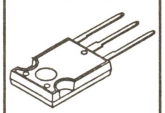
MO-093AA



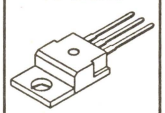
TO-252AA



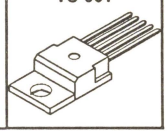
TO-247



TO-220AB



TS-001



IRF MOSFETs

I R XX XXX X

R: Ruggedized (Early Indicator for Avalanche Capability. All Devices now have EAS Ratings)

HEX DIE SIZE, Voltage Polarity and Electrical Selection

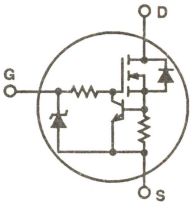
PACKAGE DESIGNATION:
- C: 5 Lead TO-220, Current Sensing
- FA: TO-204AA
- FD: 4 Lead DIP
- FF: TO-205AF (TO-39)
- FP: TO-247
- FR: TO-252
- FU: TO-251
- F1-F4: TO-204AA
- F5-F8: TO-220

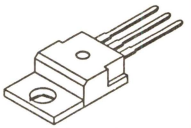
Current Limiting MOSFETs

Features

- Current Limits to a Pre-Set Level in a Shorted Load Condition
- "Logic-Level" Gate Input Allows Fully on Condition at 5V
- Monolithic Device Incorporates a Bipolar Transistor, 2 Resistors, a Zener Diode and a Power MOSFET
- ESD Protected to 2kV

TERMINAL DIAGRAM



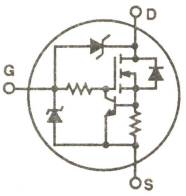
MAXIMUM RATINGS				PACKAGE
BV_{DSS} (V)	$I_{DS(LIM)}$ (A)	$R_{DS(ON)}$ (Ω)	ESD (kV)	 TO-220
80	1	0.75	2	RLP1N08LE
80	5.5	0.12	2	RLP5N08LE

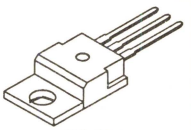
Voltage Clamping, Current Limiting MOSFETs

Features

- Excessive Drain-Source Voltage Clamped by Active Region Turn-On, Clamp Voltage Level: 60 - 70V
- Current Limits to a Pre-Set Level in a Shorted Load Condition
- Monolithic Device Incorporates a Bipolar Transistor, 2 Resistors, 2 Zener Diodes and a Power MOSFET

TERMINAL DIAGRAM



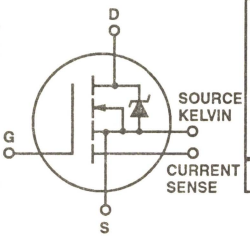
MAXIMUM RATINGS				PACKAGE
BV_{DSS} (V)	$I_{DS(LIM)}$ (A)	$R_{DS(ON)}$ (Ω)	ESD (kV)	 TO-220
55	1	0.75	2	RLP1N06CLE

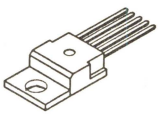
Current Sensing MOSFETs

Features

- Built-In Current Sensing Function to be Used as a Feed-Back Signal for Control and/or Protection
- Low $R_{DS(ON)}$ = 0.1Ω max
- Current Sensing Ratio = 1500 ±10%
- Avalanche Energy Rated for Ruggedness

TERMINAL DIAGRAM



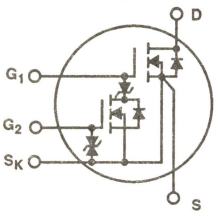
MAXIMUM RATINGS			PACKAGE
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	 TS-001
100	18	0.10	RFB18N10CS

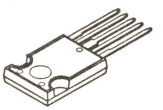
Buffered FET

Features

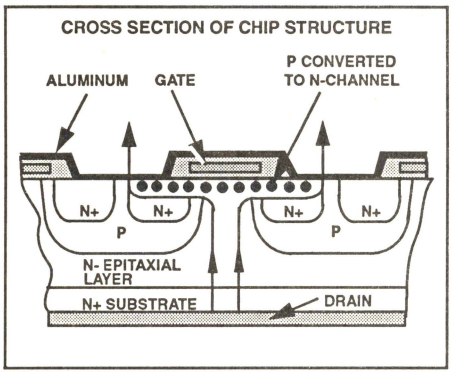
- Fall Time t_F <5ns
- Similar Electrical Performance of an IRF450
- $R_{DS(ON)}$ 0.48Ω max
- Avalanche Rated to I_{DM} at +25°C and +150°C
- ESD Protected Gates -2KV

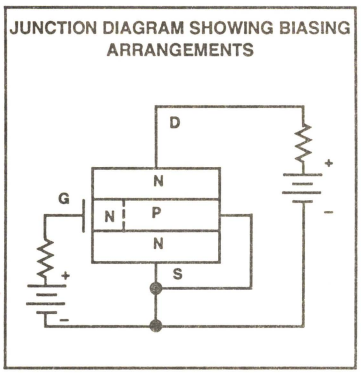
TERMINAL DIAGRAM

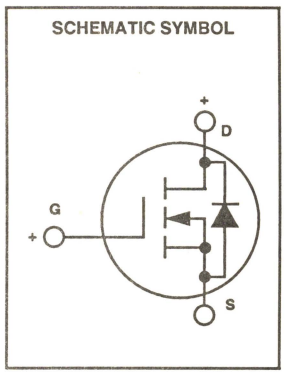


MAXIMUM RATINGS				PACKAGE
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	t_F (ns)	 TO-247
500	10	0.48	5	RFV10N50BE

N-Channel Power MOSFET







Rugged and Standard IRF-Series Power MOSFETs

Features

- **Single Pulse Avalanche Energy Rated**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Allows Reduced Protection Circuitry**
- **Reduced Drive Requirements**
- **Increased System Reliability**

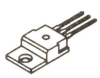
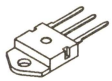
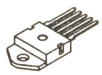
Description

The Rugged Series of Power MOSFETs are designed, tested, and guaranteed to withstand a specified level of circuit induced electrical stress in the breakdown avalanche mode of operation. These are n-channel enhancement mode polysilicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor and relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power.

Using state-of-the-art integrated circuit processing techniques, these Rugged MOSFETs provide superior performance in inductive switching applications. The design is optimized to suppress the parasitic bipolar transistor and improve system reliability. These types can be driven directly from integrated circuits.

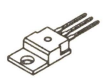
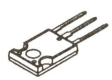
Rugged Series devices are identified by the suffix letter R following the type number or by the inclusion of a UIS SOA rating chart on the datasheet. This chart provides the user with a broad range of application usages for this capability. Application notes AN9321 and AN9322 detail this rating system.

MegaFET Product Series

MAXIMUM RATINGS				PACKAGE					
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-251	TO-252	 TO-220AB	TO-247	 TO-218	 MO-093
N-CHANNEL									
30	70	0.010	†			RFP70N03			
50	14	0.100	100	RFD14N05	RFD14N05SM	RFP14N05			
	16	0.047	200	RFD16N05	RFD16N05SM				
	25	0.047	200			RFP25N05			
	50	0.022	400			RFP50N05	RFG50N05		
	75	0.008	800				RFG75N05E	RFH75N05E	
	100	0.008	800						RFA100N05E
60	12	0.150	†	RFD3055	RFD3055SM	RFP3055			
	45	0.028	†			RFP45N06	RFG45N06		
	50	0.022	†			RFP50N06	RFG50N06		
	70	0.014	†			RFP70N06	RFG70N06		
100	22	0.080	†			RFP22N10			
	40	0.040	†			RFP40N10	RFG40N10		
P-CHANNEL									
50	8	0.300	†	RFD8P05	RFD8P05SM	RFP8P05			
	15	0.150	†	RFD15P05	RFD15P05SM	RFP15P05			
	30	0.065	†			RFP30P05	RFG30P05		
	60	0.026	†				RFG60P05E		
60	30	0.075	†			RFP30P06	RFG30P06		
	60	0.030	†				RFG60P06E		

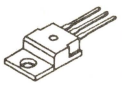
NOTE: † = More complete ruggedness capability now specified; UIS current vs time in avalanche graph on data sheet.

Logic Level MegaFET Product Series

MAXIMUM RATINGS				PACKAGE				
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-251	TO-252	 TO-220AB	 TO-247	4 LEAD DIP
N-CHANNEL								
50	14	0.100	100	RFD14N05L	RFD14N05LSM	RFP14N05L		
	16	0.047	200	RFD16N05L	RFD16N05LSM			
	25	0.047	200			RFP25N05L		
	50	0.022	400			RFP50N05L	RFG50N05L	
60	2	0.160	†					RFW2N06RLE
	12	0.135	†	RFD12N06RLE	RFD12N06RLESM	RFP12N06RLE		
P-CHANNEL								
30	10	0.225	†	RFD10P03L	RFD10P03LSM	RFP10P03L		

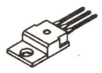
NOTE: † = More complete ruggedness capability now specified; UIS current vs time in avalanche graph on data sheet.

Logic Level Product Series

MAXIMUM RATINGS				PACKAGE						
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204AA	TO-251	TO-252	 TO-220AB	TO-247	4 LEAD DIP
N-CHANNEL										
50	2	0.950	N.R.	RFL2N05L						
	4	0.800	N.R.					RFP4N05L		
	14	0.100	100			RFD14N05L	RFD14N05LSM	RFP14N05L		
	15	0.140	N.R.		RFM15N05L			RFP15N05L		
	16	0.047	200			RFD16N05L	RFD16N05LSM			
	25	0.047	200					RFP25N05L		
	50	0.022	†					RFP50N05L	RFG50N05L	
60	2	0.950	N.R.	RFL2N06L						
	2	0.160	†							RFW2N06RLE
	4	0.800	N.R.			RFD4N06L	RFD4N06LSM	RFP4N06L		
	12	0.135	†			RFD12N06RLE	RFD12N06RLESM	RFP12N06RLE		
	15	0.140	N.R.		RFM15N06L			RFP15N06L		
	16	0.047	†			RFD16N06LE	RFD16N06LESM			
	17	0.100	N.R.					RFP17N06L		
	25	0.085	N.R.					RFP25N06L		
	30	0.047	†					RFP30N06LE		
80	1	1.200	N.R.	RFL1N08L						
	2	1.050	N.R.					RFP2N08L		
	3	0.800	N.R.			RFD3N08L	RFD3N08LSM			
	12	0.200	N.R.		RFM12N08L			RFP12N08L		
	15	0.140	N.R.					RFP15N08L		
100	1	1.200	N.R.	RFL1N10L						
	1.69	1.400	N.R.	2N6901††						
	2	1.050	N.R.					RFP2N10L		
	7	0.300	†			RFD7N10LE	RFD7N10LESM	RFP7N10LE		
	12	0.200	N.R.		RFM12N10L			RFP12N10L		
	12	0.200	N.R.		2N6902††					
120	1	1.900	N.R.	RFL1N12L						
	2	1.750	N.R.					RFP2N12L		
	10	0.300	N.R.		RFM10N12L			RFP10N12L		
150	1	1.900	N.R.	RFL1N15L						
	2	1.750	N.R.					RFP2N15L		
	10	0.300	N.R.		RFM10N15L			RFP10N15L		
180	1	3.650	N.R.	RFL1N18L						
	2	3.500	N.R.					RFP2N18L		
	8	0.500	N.R.		RFM8N18L			RFP8N18L		
200	0.98	3.650	N.R.	2N6903††						
	1	3.650	N.R.	RFL1N20L						
	2	3.500	N.R.					RFP2N20L		
	8	0.500	N.R.		RFM8N20L			RFP8N20L		
	8	0.600	N.R.		2N6904††					
P-CHANNEL										
30	10	0.225	†			RFD10P03L	RFD10P03LSM	RFP10P03L		

NOTE: † = More complete ruggedness capability now specified; UIS current vs time in avalanche graph on data sheet. BOLD indicates Developmental Products. N.R. Not Rated for UIS capability. †† = QPL Approved Types.

IR Equivalent N-Channel Product Series

MAXIMUM RATINGS				PACKAGE						
										
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	4 LEAD DIP
60	0.40	3.2	N.R.							IRFD1Z3
	0.50	2.4	N.R.							IRFD1Z1
	33.0	0.08	150		IRF153(R)					
	34.0	0.08	150						IRFP153(R)	
	40.0	0.055	150		IRF151(R)				IRFP151(R)	
80	0.8	0.8	19							IRFD113(R)
	1.0	0.6	19							IRFD111(R)
	1.1	0.4	36							IRFD123(R)
	1.3	0.3	36							IRFD121(R)
	3.0	0.8	19	IRFF113(R)						
	3.5	0.6	19	IRFF111(R)						
	4.9	0.74	19					IRF513(R)		
	5.0	0.4	36	IRFF123(R)						
	5.6	0.54	19					IRF511(R)		
	6.0	0.3	36	IRFF121(R)						
	7.0	0.25	69	IRFF133(R)						
	8.0	0.36	N.R.		IRF123					
	8.0	0.36	36					IRF523(R)		
	8.0	0.18	69	IRFF131(R)						
	8.4	0.27	36			IRFU121	IRFR121			
	9.2	0.27	N.R.		IRF121					
	9.2	0.27	36					IRF521(R)		
	12.0	0.23	50		IRF133(R)					
	12.0	0.23	69					IRF533(R)		
	14.0	0.16	50		IRF131(R)					
	14.0	0.16	69					IRF531(R)		
	25.0	0.1	100		IRF143(R)					
	25.0	0.1	230					IRF543(R)		
	27.0	0.099	100						IRFP143R	
	28.0	0.077	100		IRF141(R)					
	28.0	0.077	230					IRF541(R)		
	31.0	0.077	100						IRFP141R	

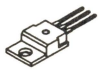
IR Equivalent N-Channel Product Series (Continued)

MAXIMUM RATINGS				PACKAGE						
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	4 LEAD DIP
100	0.4	3.2	N.R.							IRFD1Z2
	0.5	2.4	N.R.							IRFD1Z0
	0.8	0.8	19							IRFD112(R)
	1.0	0.6	19							IRFD110(R)
	1.1	0.4	36							IRFD122(R)
	1.3	0.3	36							IRFD120(R)
	3.0	0.8	19	IRFF112(R)						
	3.5	0.6	19	IRFF110(R)						
	4.7	0.54	19			IRFU110	IRFR110			
	4.9	0.74	19					IRF512(R)		
	5.0	0.4	36	IRFF122(R)						
	5.6	0.54	19					IRF510(R)		
	6.0	0.3	36	IRFF120(R)						
	7.0	0.25	69	IRFF132(R)						
	8.0	0.36	36					IRF522(R)		
	8.0	0.18	69	IRFF130(R)						
	8.0	0.36	N.R.		IRF122					
	8.4	0.27	36			IRFU120	IRFR120			
	9.2	0.27	36					IRF520(R)		
	9.2	0.27	N.R.		IRF120					
	12.0	0.23	50		IRF132(R)					
	12.0	0.23	69					IRF532(R)		
	14.0	0.16	50		IRF130(R)					
	14.0	0.16	69					IRF530(R)		
	25.0	0.1	100		IRF142(R)					
	25.0	0.1	230					IRF542(R)		
	27.0	0.099	100						IRFP142R	
	28.0	0.077	100		IRF140(R)					
	28.0	0.077	230					IRF540(R)		
	31.0	0.077	100						IRFP140R	
	33.0	0.08	150		IRF152(R)					
	34.0	0.08	150						IRFP152(R)	
	40.0	0.055	150		IRF150(R)				IRFP150(R)	

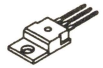
IR Equivalent N-Channel Product Series (Continued)

MAXIMUM RATINGS				PACKAGE						
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	4 LEAD DIP
150	0.30	6.5	N.R.							IRFD2Z3
	0.32	5.0	N.R.							IRFD2Z1
	0.45	2.4	30							IRFD213(R)
	0.60	1.5	30							IRFD211(R)
	0.70	1.2	85							IRFD223(R)
	0.80	0.8	85							IRFD221(R)
	1.8	2.4	30	IRFF213(R)						
	2.2	1.5	30	IRFF211(R)						
	2.6	2.4	46					IRF613(R)		
	3.0	1.2	85	IRFF223(R)						
	3.3	1.5	46					IRF611(R)		
	3.5	0.8	85	IRFF221(R)						
	4.0	1.2	N.R.		IRF223					
	4.0	1.2	85					IRF623(R)		
	4.5	0.6	85	IRFF233(R)						
	4.6	0.8	85			IRFU221	IRFR221			
	5.0	0.8	N.R.		IRF221					
	5.0	0.8	85					IRF621(R)		
	5.5	0.4	85	IRFF231(R)						
	8.0	0.6	150		IRF233(R)			IRF633(R)		
	9.0	0.4	150		IRF231(R)			IRF631(R)		
	18.0	0.22	510						IRFP243R	
	16.0	0.22	580		IRF243(R)			IRF643(R)		
	20.0	0.18	510						IRFP241R	
	18.0	0.18	580		IRF241(R)			IRF641(R)		
	25.0	0.12	910		IRF253(R)					
	27.0	0.12	810						IRFP253(R)	
	30.0	0.085	910		IRF251(R)					
	33.0	0.085	810						IRFP251(R)	
200	0.30	6.5	N.R.							IRFD2Z2
	0.32	5.0	N.R.							IRFD2Z0
	0.45	2.4	30							IRFD212(R)
	0.60	1.5	30							IRFD210(R)
	0.70	1.2	85							IRFD222(R)
	0.80	0.8	85							IRFD220(R)
	1.8	2.4	30	IRFF212(R)						
	2.2	1.5	30	IRFF210(R)						
	2.6	2.4	46					IRF612(R)		
	3.0	1.2	85	IRFF222(R)						
	3.3	1.5	46					IRF610(R)		
	3.5	0.8	85	IRFF220(R)						
	3.8	1.2	85			IRFU222	IRFR222			
	4.0	1.2	N.R.		IRF222					
	4.0	1.2	85					IRF622(R)		
	4.5	0.6	85	IRFF232(R)						
	4.6	0.8	85			IRFU220	IRFR220			
	5.0	0.8	N.R.		IRF220					
	5.0	0.8	85					IRF620(R)		
	5.5	0.4	85	IRFF230(R)						
	8.0	0.6	150		IRF232(R)			IRF632(R)		
	9.0	0.4	150		IRF230(R)			IRF630(R)		
	18.0	0.22	510						IRFP242R	
	16.0	0.22	580		IRF242(R)			IRF642(R)		
	20.0	0.18	510						IRFP240R	
	18.0	0.18	580		IRF240(R)			IRF640(R)		
	25.0	0.12	910		IRF252(R)					
	27.0	0.12	810						IRFP252(R)	
	30.0	0.085	910		IRF250(R)					
	33.0	0.085	810						IRFP250(R)	

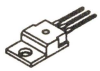
IR Equivalent N-Channel Product Series (Continued)

MAXIMUM RATINGS				PACKAGE						
										
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	4 LEAD DIP
250	2.0	2.0	61					**IRF614**		
	2.2	2.0	61			**IRFU214**	**IRFR214**			
	3.3	1.5	120					IRF625		
	3.8	1.1	120					IRF624		
	6.5	0.68	180		IRF235			IRF635		
	8.1	0.45	180		IRF234			IRF634		
	13.0	0.34	550		IRF245			IRF645		
	14.0	0.34	550						IRFP245	
	14.0	0.28	550		IRF244			IRF644		
	15.0	0.28	550						IRFP244	
	20.0	0.17	1000		IRF255					
	21.0	0.17	1000						IRFP255	
	22.0	0.14	1000		IRF254					
	23.0	0.14	1000						IRFP254	
275	3.3	1.5	120					IRF627		
	3.8	1.1	120					IRF626		
	6.5	0.68	180		IRF237			IRF637		
	8.1	0.45	180		IRF236			IRF636		
	13.0	0.34	550		IRF247			IRF647		
	14.0	0.34	550						IRFP247	
	14.0	0.28	550		IRF246			IRF646		
	15.0	0.28	550						IRFP246	
	20.0	0.17	1000		IRF257					
	21.0	0.17	1000						IRFP257	
	22.0	0.14	1000		IRF256					
	23.0	0.14	1000						IRFP256	
350	0.3	5.0	45							IRFD313(R)
	0.4	3.6	45							IRFD311(R)
	0.4	2.5	100							IRFD323(R)
	0.5	1.8	100							IRFD321(R)
	1.15	5.0	150	IRFF313(R)						
	1.35	3.6	150	IRFF311(R)						
	1.7	5.0	120					IRF713(R)		
	2.0	3.6	120					IRF711(R)		
	2.0	2.5	100	IRFF323(R)						
	2.5	1.8	100	IRFF321(R)						
	2.8	2.5	190					IRF723(R)		
	2.8	2.5	N.R.		IRF323					
	3.0	1.5	300	IRFF333(R)						
	3.1	1.8	190			IRFU321	IRFR321			
	3.3	1.8	190					IRF721(R)		
	3.3	1.8	N.R.		IRF321					
	3.5	1.0	300	IRFF331(R)						
	4.5	1.5	300		IRF333(R)			IRF733(R)		
	5.5	1.0	300		IRF331(R)			IRF731(R)		
	8.0	0.8	520					IRF743(R)		
	8.3	0.8	520		IRF343(R)					
	8.7	0.8	480						IRFP343R	
	10.0	0.55	520		IRF341(R)			IRF741(R)		
	11.0	0.55	480						IRFP341R	
	13.0	0.4	700		IRF353(R)					
	14.0	0.4	700						IRFP353(R)	
	15.0	0.3	700		IRF351(R)					
	16.0	0.3	700						IRFP351(R)	

IR Equivalent N-Channel Product Series (Continued)

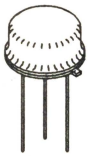
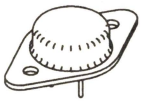
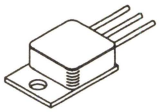
MAXIMUM RATINGS				PACKAGE						
										
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mJ)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	4 LEAD DIP
400	0.3	5.0	45							IRFD312(R)
	0.4	3.6	45							IRFD310(R)
	0.4	2.5	100							IRFD322(R)
	0.5	1.8	100							IRFD320(R)
	1.15	5.0	150	IRFF312(R)						
	1.35	3.6	150	IRFF310(R)						
	1.7	5.0	120					IRF712(R)		
	2.0	3.6	120					IRF710(R)		
	2.0	2.5	100	IRFF322(R)						
	2.5	1.8	100	IRFF320(R)						
	2.6	2.5	190			IRFU322	IRFR322			
	2.8	2.5	190					IRF722(R)		
	2.8	2.5	N.R.		IRF322					
	3.0	1.5	300	IRFF332(R)						
	3.1	1.8	190			IRFU320	IRFR320			
	3.3	1.8	190					IRF720(R)		
	3.3	1.8	N.R.		IRF320					
	3.5	1.0	300	IRFF330(R)						
	4.5	1.5	300		IRF332(R)			IRF732(R)		
	5.5	1.0	300		IRF330(R)			IRF730(R)		
	8.0	0.8	520					IRF742(R)		
	8.3	0.8	520		IRF342(R)					
	8.7	0.8	480						IRFP342R	
	10.0	0.55	520		IRF340(R)			IRF740(R)		
	11.0	0.55	480						IRFP340R	
	13.0	0.4	700		IRF352(R)					
	14.0	0.4	700						IRFP352(R)	
	15.0	0.3	700		IRF350(R)					
	16.0	0.3	700						IRFP350(R)	
	20.0	0.25	1200						IRFP362	
	22.0	0.25	980		IRF362					
	23.0	0.2	1200						IRFP360	
	25.0	0.2	980		IRF360					
450	1.4	4.0	210	IRFF423(R)						
	1.6	3.0	210	IRFF421(R)						
	2.2	4.0	210					IRF823(R)		
	2.2	4.0	N.R.		IRF423					
	2.25	2.0	300	IRFF433(R)						
	2.5	3.0	210			IRFU421	IRFR421	IRF821(R)		
	2.5	3.0	N.R.		IRF421					
	2.75	1.5	300	IRFF431(R)						
	4.0	2.0	300		IRF433(R)			IRF833(R)		
	4.5	1.5	300		IRF431(R)			IRF831(R)		
	7.0	1.1	510		IRF443(R)			IRF843(R)		
	7.0	1.1	480						IRFP443R	
	8.0	0.85	510		IRF441(R)			IRF841(R)		
	8.0	0.85	480						IRFP441R	
	11.0	0.5	860		IRF453(R)					
	12.0	0.5	860						IRFP453(R)	
	13.0	0.4	860		IRF451(R)					
	14.0	0.4	860						IRFP451(R)	

IR Equivalent N-Channel Product Series (Continued)

MAXIMUM RATINGS				PACKAGE						
										
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-251	TO-252	TO-220AB	TO-247	4 LEAD DIP
500	1.4	4.0	210	IRFF422(R)						
	1.5	7.0	45			IRFU410	IRFR410			
	1.6	3.0	210	IRFF420(R)						
	2.0	4.0	210					IRF822(R)		
	2.2	4.0	210			IRFU422	IRFR422			
	2.2	4.0	N.R.		IRF422					
	2.25	2.0	300	IRFF432(R)						
	2.5	3.0	210			IRFU420	IRFR420	IRF820(R)		
	2.5	3.0	N.R.		IRF420					
	2.75	1.5	300	IRFF430(R)						
	4.0	2.0	300		IRF432(R)			IRF832(R)		
	4.5	1.5	300		IRF430(R)			IRF830(R)		
	7.0	1.1	510		IRF442(R)			IRF842(R)		
	7.0	1.1	480						IRFP442R	
	8.0	0.85	510		IRF440(R)			IRF840(R)		
	8.0	0.85	480						IRFP440R	
	11.0	0.5	860		IRF452(R)					
	12.0	0.5	860						IRFP452(R)	
	13.0	0.4	860		IRF450(R)					
	14.0	0.4	860						IRFP450(R)	
	17.0	0.35	960						IRFP462	
	19.0	0.35	1200		IRF462					
	20.0	0.27	960						IRFP460	
	21.0	0.27	1200		IRF460					
600	5.4	1.6	570		IRFAC42R			IRFBC42R		
	5.9	1.6	410						IRFPC42R	
	6.2	1.2	570		IRFAC40R			IRFBC40R		
	6.8	1.2	410						IRFPC40R	
1000	3.9	4.2	490						IRFPG42	
	4.3	3.5	490						IRFPG40	

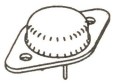
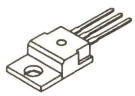
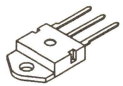
NOTE: N.R. = Not Avalanche Rated. R = Rugged ONLY Available. (R) = Rugged AND Non-Rugged Available. E_{AS} = Column Applies Only to Rugged MOSFETs. BOLD indicates Developmental Products.

JEDEC N-Channel

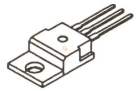
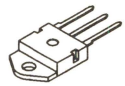
MAXIMUM RATINGS			PACKAGE		
					
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204	TO-254
60	12.0	0.25		2N6755	
	31.0	0.08		2N6763	
100	3.5	0.6	2N6782†		
	6.0	0.3	2N6788†		
	8.0	0.18	2N6796†		
	14.0	0.18		2N6756†	
	38.0	0.055		2N6764†	
150	8.0	0.6		2N6757	
	25.0	0.12		2N6765	
180	34	0.07			2N7224†
200	2.25	1.5	2N6784†		
	3.5	0.8	2N6790†		
	5.5	0.4	2N6798†		
	9.0	0.4		2N6758†	
	27.4	0.100			2N7225†
	30.0	0.085		2N6766†	
350	4.5	1.5		2N6759	
	12.0	0.4		2N6767	
400	1.25	3.6	2N6786†		
	2.0	1.8	2N6792†		
	3.0	1.0	2N6800†		
	5.5	1.0		2N6760†	
	14.0	0.315			2N7227†
	14.0	0.3		2N6768†	
450	4.0	2.0		2N6761	
	11.0	0.5		2N6769	
500	1.5	3.0	2N6794†		
	3.5	1.5	2N6802†		
	4.5	1.5		2N6762†	
	12.0	0.415			2N7228†
	12.0	0.4		2N6770†	

NOTE: † = QPL - Approved Types

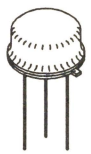
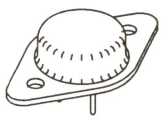
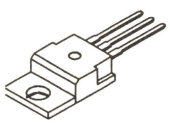
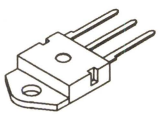
RF and BUZ Series MOSFETs

MAXIMUM RATINGS			PACKAGE			
						
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204	TO-220AB	TO-218
50	2.0	0.95	RFL2N05			
	4.0	0.8			RFP4N05	
	13.0	0.12			BUZ71A	
	14.0	0.1			BUZ71	
	15.0	0.14		RFM15N05	RFP15N05	
	30.0	0.04			BUZ11	
	45.0	0.04		RFK45N05		RFH45N05
60	2.0	0.95	RFL2N06			
	4.0	0.8			RFP4N06	
	15.0	0.14		RFM15N06	RFP15N06	
	25.0	0.07		RFM25N06	RFP25N06	
	45.0	0.04		RFK45N06		RFH45N06
80	1.0	1.2	RFL1N08			
	2.0	1.05			RFP2N08	
	12.0	0.2		RFM12N08	RFP12N08	
	18.0	0.1		RFM18N08	RFP18N08	
	35.0	0.055		RFK35N08		RFH35N08
100	1.0	1.2	RFL1N10			
	2.0	1.05			RFP2N10	
	9.0	0.25			BUZ72A	
	12.0	0.2		RFM12N10	RFP12N10,BUZ20	
	18.0	0.1		RFM18N10	RFP18N10	
	19.0	0.1			BUZ21	
	35.0	0.055		RFK35N10		RFH35N10
120	1.0	1.9	RFL1N12			
	2.0	1.75			RFP2N12	
	4.0	0.4	RFL4N12			
	10.0	0.3		RFM10N12	RFP10N12	
	15.0	0.15		RFM15N12	RFP15N12	
	30.0	0.075		RFK30N12		RFH30N12
150	1.0	1.9	RFL1N15			
	2.0	1.75			RFP2N15	
	4.0	0.4	RFL4N15			
	10.0	0.3		RFM10N15	RFP10N15	
	15.0	0.15		RFM15N15	RFP15N15	
	30.0	0.075		RFK30N15		RFH30N15
180	1.0	3.65	RFL1N18			
	2.0	3.5			RFP2N18	
	8.0	0.5		RFM8N18	RFP8N18	
	12.0	0.25		RFM12N18	RFP12N18	
	25.0	0.15		RFK25N18		RFK25N18
200	1.0	3.65	RFL1N20			
	2.0	3.5			RFP2N20	
	5.8	0.6			BUZ73A	
	8.0	0.5		RFM8N20	RFP8N20	
	9.5	0.4			BUZ32	
	12.0	0.25		RFM12N20	RFP12N20	
	25.0	0.15		RFK25N20		RFK25N20

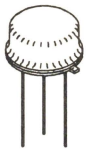
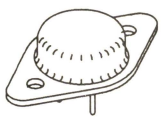
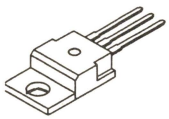
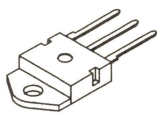
RF and BUZ Series MOSFETs (Continued)

MAXIMUM RATINGS			PACKAGE			
						
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204	TO-220AB	TO-218
350	4.0	2.0		RFM4N35	RFP4N35	
	7.0	0.75		RFM7N35	RFP7N35	
	12.0	0.38				RFH12N35
	12.0	0.5		RFM12N35		
400	2.6	2.5			BUZ76A	
	3.0	1.8			BUZ76	
	4.0	2.0		RFM4N40	RFP4N40	
	4.5	1.5			BUZ60B	
	5.5	1.0			BUZ60	
	7.0	0.75		RFM7N40	RFP7N40	
	11.5	0.4				BUZ351
	12.0	0.38				RFH12N40
	12.0	0.5		RFM12N40		
450	3.0	3.0		RFM3N45	RFP3N45	
	6.0	1.25		RFM6N45	RFP6N45	
	10.0	0.6		RFM10N45		RFH10N45
500	3.0	3.0		RFM3N50	RFP3N50	
	4.0	2.0			BUZ42	
	4.5	1.5			BUZ41A	
	6.0	1.25			RFP6N50	
	8.3	0.8		BUZ45A		
	9.6	0.6		BUZ45		
	10.0	0.6		RFM10N50		RFH10N50
	10.0	0.5		BUZ45B		
1000	4.3	3.5			RFP4N100	

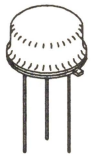
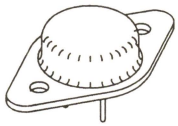
RF and BUZ Series P-Channel MOSFETs

MAXIMUM RATINGS			PACKAGE			
						
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204	TO-220AB	TO-218
80	1.0	3.65	RFL1P08			
	2.0	3.5			RFP2P08	
	6.0	0.6		RFM6P08	RFP6P08	
	8.0	0.4		RFM8P08	RFP8P08	
	12.0	0.3		RFM12P08	RFP12P08	
	25.0	0.15		RFK25P08		RFH25P08

RF and BUZ Series P-Channel MOSFETs (Continued)

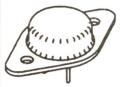
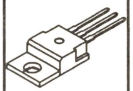
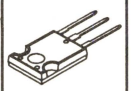
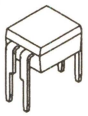
MAXIMUM RATINGS			PACKAGE			
						
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204	TO-220AB	TO-218
100	1.0	3.65	RFL1P10			
	2.0	3.5			RFP2P10	
	6.0	0.6			RFP6P10	
	8.0	0.4		RFM8P10	RFP8P10	
	12.0	0.3		RFM12P10	RFP12P10	
	25.0	0.15		RFK25P10		RFH25P10
120	5.0	1.0		RFM5P12	RFP5P12	
	10.0	0.5		RFM10P12	RFP10P12	
150	5.0	1.0		RFM5P15	RFP5P15	
	10.0	0.5		RFM10P15	RFP10P15	

JEDEC P-Channel

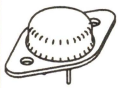
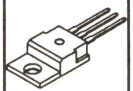
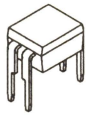
MAXIMUM RATINGS			PACKAGE	
				
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	TO-205AF	TO-204
100	1.16	3.65	2N6895†	
	6.0	0.6		2N6896†
	6.5	0.3	2N6849†	
	11.0	0.3		2N6804
	12.0	0.3		2N6897†
	25.0	0.2		2N6898†
200	4.0	0.8	2N6851†	

NOTE: † = QPL - Approved Types

IR Equivalent P-Channel Product Series

MAXIMUM RATINGS				PACKAGE				
								
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	TO-204	TO-220AB	TO-247	4 LEAD DIP
80	0.6	1.6	190					IRFD9113
	0.8	0.8	370					IRFD9123
	2.5	1.6	190			IRF9513		
	3.0	1.2	190			IRF9511		
	3.5	0.8	370	IRFF9123				
	4.0	0.6	370	IRFF9121				
	5.0	0.8	370			IRF9523		
	5.5	0.4	500	IRFF9133				
	6.0	0.6	370			IRF9521		
	6.5	0.3	500	IRFF9131				
	10.0	0.4	500		IRF9133	IRF9533		
	12.0	0.3	500		IRF9131	IRF9531		
	15.0	0.3	960		IRF9143	IRF9543		
	16.0	0.3	960				IRFP9143R	
	19.0	0.2	960		IRF9141	IRF9541	IRFP9141R	
	25.0	0.15	1300		IRF9151		IRFP9151	
100	0.7	1.2	190					IRFD9110
	1.0	0.6	370					IRFD9120
	2.5	1.6	190			IRF9512		
	3.0	1.2	190			IRF9510		
	3.5	0.8	370	IRFF9122				
	4.0	0.6	370	IRFF9120				
	5.0	0.8	370			IRF9522		
	5.5	0.4	500	IRFF9132				
	6.0	0.6	370			IRF9520		
	6.5	0.3	500	IRFF9130				
	10.0	0.4	500		IRF9132	IRF9532		
	12.0	0.3	500		IRF9130	IRF9530		
	15.0	0.3	960		IRF9142	IRF9542		
	16.0	0.3	960				IRFP9142R	
	19.0	0.2	960		IRF9140	IRF9540	IRFP9140R	
	25.0	0.15	1300		IRF9150		IRFP9150	
150	0.45	2.4	290					IRFD9223
	2.0	2.4	290	IRFF9223				
	2.5	1.5	290	IRFF9221				
	3.0	2.4	290			IRF9623		
	3.5	1.5	290			IRF9621		
	3.5	1.2	500	IRFF9233				
	4.0	0.8	500	IRFF9231				
	5.5	1.2	500		IRF9233	IRF9633		
	6.5	0.8	500		IRF9231	IRF9631		
	9.0	0.7	790		IRF9243	IRF9643		
	10.0	0.7	790				IRFP9243R	
	11.0	0.5	790		IRF9241	IRF9641		
	12.0	0.5	790				IRFP9241R	

IR Equivalent P-Channel Product Series (Continued)

MAXIMUM RATINGS				PACKAGE				
BV_{DSS} (V)	I_{DS} (A)	$R_{DS(ON)}$ (Ω)	E_{AS} (mj)	TO-205AF	 TO-204	 TO-220AB	TO-247	 4 LEAD DIP
200	0.6	1.5	290					IRFD9220
	2.0	2.4	290	IRFF9222				
	2.5	1.5	290	IRFF9220				
	3.0	2.4	290			IRF9622		
	3.5	1.5	290			IRF9620		
	3.5	1.2	500	IRFF9232				
	4.0	0.8	500	IRFF9230				
	5.5	1.2	500		IRF9232	IRF9632		
	6.5	0.8	500		IRF9230	IRF9630		
	9.0	0.7	790		IRF9242	IRF9642		
	10.0	0.7	790				IRFP9242R	
	11.0	0.5	790		IRF9240	IRF9640		
	12.0	0.5	790				IRFP9240R	

NOTE: All P-Channel MOSFETs are avalanche rated whether indicated by an R suffix or not.

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RFK45N05, RFK45N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-746
RFP50N05, RFG50N05	N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	4-750
RFG50N06, RFP50N06	50A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)	4-755
RFP70N03	70A, 30V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFET (MegaFET)	4-761
RFG70N06, RFP70N06	N-Channel Enhancement-Mode Power Field-Effect Transistors	4-767
RFG75N05E, RFH75N05E	N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)	4-773
RFA100N05E	N-Channel Enhancement-Mode Power Field-Effect Transistor (MegaFET)	4-778

HARRIS

2N6755
2N6756

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 12A and 14A, 60V - 100V
- $r_{DS(on)}$ = 0.18Ω and 0.25Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

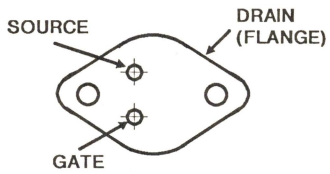
Description

The 2N6755 and 2N6756 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

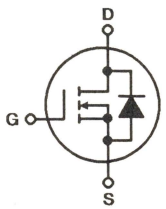
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6755	2N6756	UNITS
Drain-Source Voltage	V_{DS}	60*	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	60*	100*	V
Continuous Drain Current				
T_C = +25°C	I_D	12*	14*	A
T_C = +100°C	I_D	8.0*	9.0*	A
Pulsed Drain Current	I_{DM}	25	30	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Fig. 11)	P_D	75*	75*	W
T_C = +100°C (See Fig. 11)	P_D	30*	30*	W
Linear Derating Factor (See Fig. 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	25	30	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1586.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, T_C = 125°C
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 36V, I_D = 9A, Z_o = 15Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	
t_f	Fall Time	ALL	–	–	45*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage ①	2N6755	0.85*	–	1.7*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

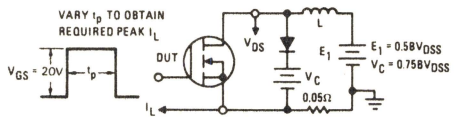

Fig. 1 – Clamped Inductive Test Circuit

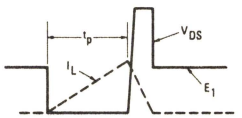

Fig. 2 – Clamped Inductive Waveforms

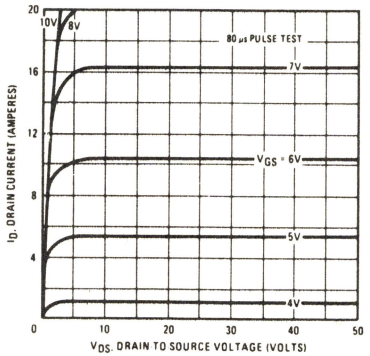

Fig. 3 – Typical Output Characteristics

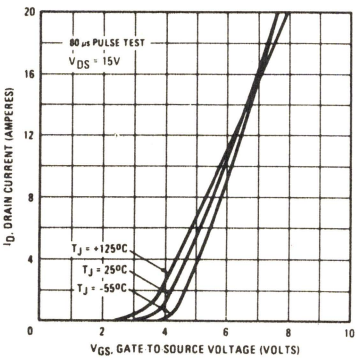

Fig. 4 – Typical Transfer Characteristics

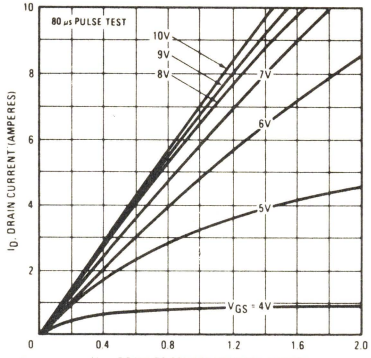

Fig. 5— Typical Saturation Characteristics (2N6755)

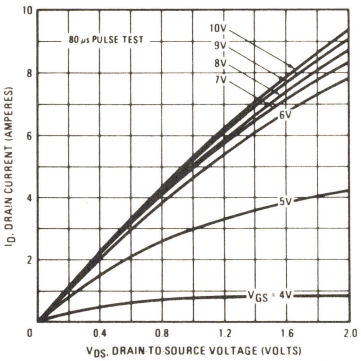

Fig. 6— Typical Saturation Characteristics (2N6756)

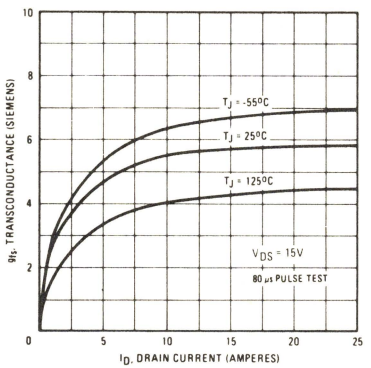

Fig. 7 — Typical Transconductance Vs. Drain Current

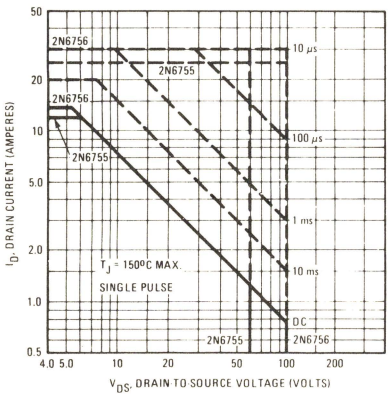

Fig. 8 — Maximum Safe Operating Area

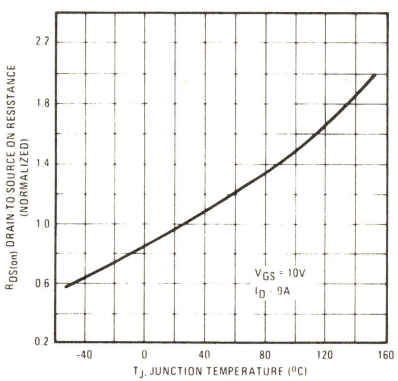

Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

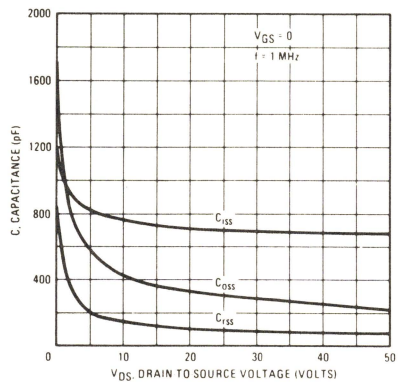

Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

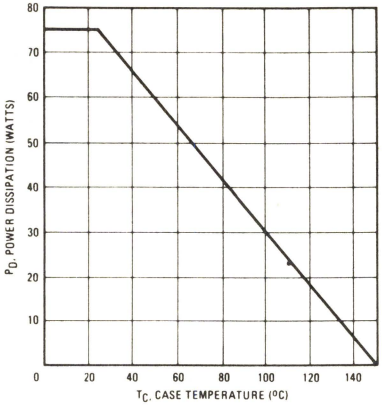

Fig. 11 – Power Vs. Temperature Derating Curve

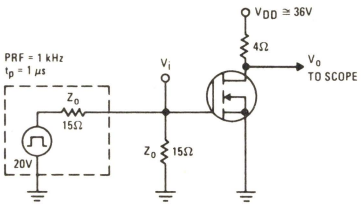

Fig. 13 – Switching Time Test Circuit

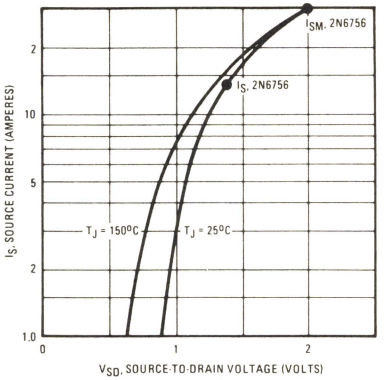

Fig. 12 – Typical Body-Drain Diode Forward Voltage

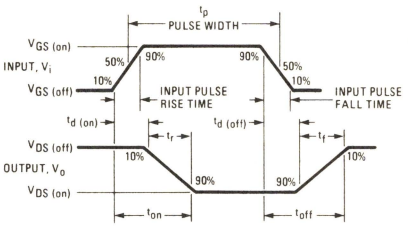

Fig. 14 – Switching Time Waveforms

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2N6757
2N6758

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 8A and 9A, 150V - 200V
- $r_{DS(on)}$ = 0.4Ω and 0.6Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

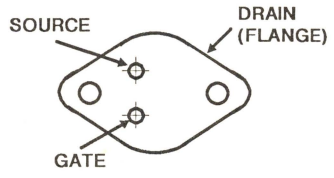
Description

The 2N6757 and 2N6758 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

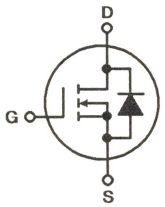
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6757	2N6758	UNITS
Drain-Source Voltage	V_{DS}	150*	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	150*	200*	V
Continuous Drain Current				
T_C = +25°C	I_D	8.0*	9.0*	A
T_C = +100°C	I_D	5.0*	6.0*	A
Pulsed Drain Current	I_{DM}	12	15	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	75*	75*	W
T_C = +100°C (See Figure 11)	P_D	30*	30*	W
Linear Derating Factor (See Figure 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	12	15	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1587.1

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	V_{GS} = 0
		2N6758	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6757	–	–	4.6*	V	V_{GS} = 10V, I_D = 8A
		2N6758	–	–	3.6*	V	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6757	–	0.4	0.6*	Ω	V_{GS} = 10V, I_D = 5A
		2N6758	–	0.25	0.4*	Ω	V_{GS} = 10V, I_D = 6A
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6757	–	–	1.13*	Ω	V_{GS} = 10V, I_D = 5A, $T_C = 125^oC$
		2N6758	–	–	0.75*	Ω	V_{GS} = 10V, I_D = 6A, $T_C = 125^oC$
g_{fs}	Forward Transconductance (1)	ALL	3.0*	5.0	9.0*	S (℧)	V_{DS} = 15V, I_D = 6A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	100*	250	450*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 90V$, I_D = 6A, $Z_o = 15\Omega$
t_r	Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	40*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6758	–	–	9.0*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V_{SD}	Diode Forward Voltage (1)	2N6757	0.75*	–	1.50*	V	$T_C = 25^oC$, I_S = 8A, V_{GS} = 0
		2N6758	0.80*	–	1.60*	V	$T_C = 25^oC$, I_S = 9A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

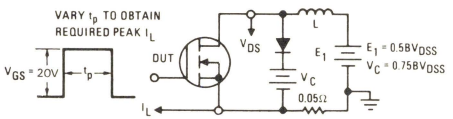


Fig. 1 – Clamped Inductive Test Circuit

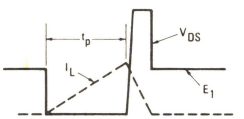


Fig. 2 – Clamped Inductive Waveforms

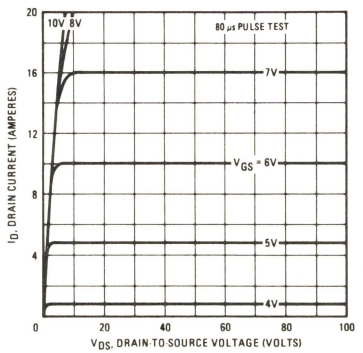


Fig. 3 – Typical Output Characteristics

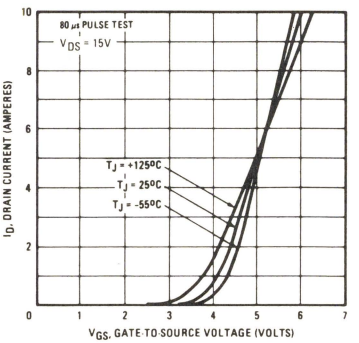


Fig. 4 – Typical Transfer Characteristics

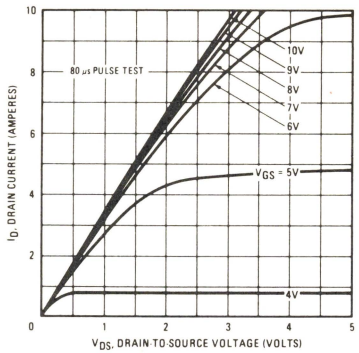


Fig. 5— Typical Saturation Characteristics (2N6757)

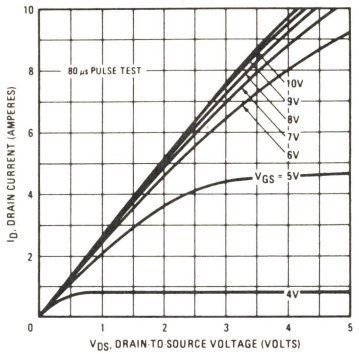


Fig. 6— Typical Saturation Characteristics (2N6758)

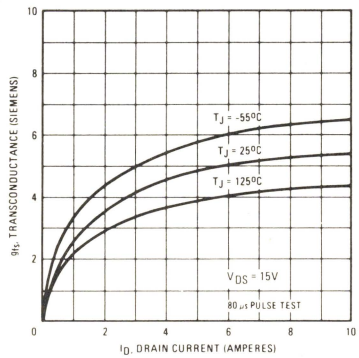


Fig. 7 — Typical Transconductance Vs. Drain Current

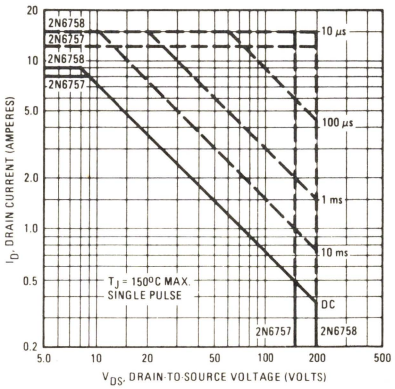


Fig. 8 — Maximum Safe Operating Area

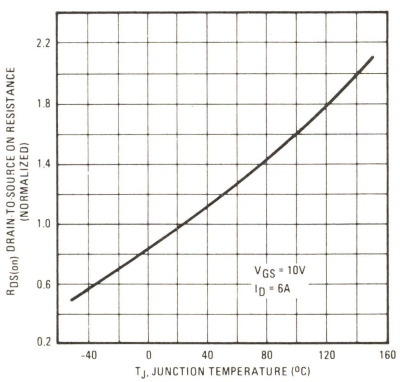


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

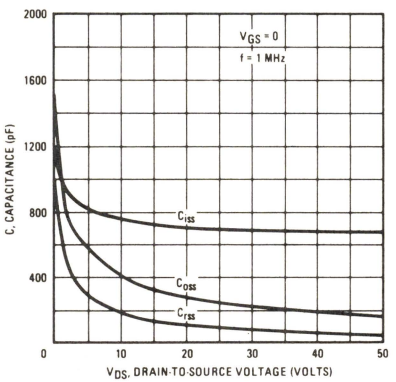


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

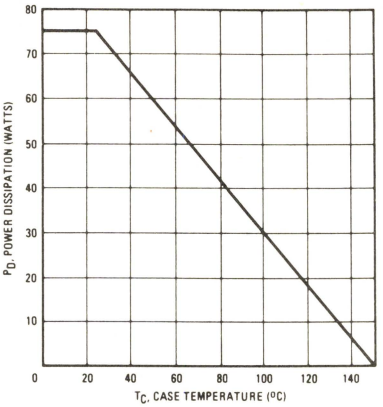


Fig. 11 – Power Vs. Temperature Derating Curve

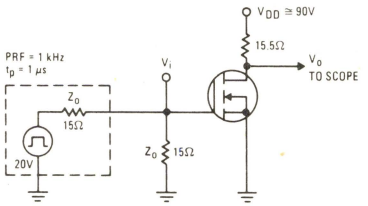


Fig. 13 – Switching Time Test Circuit

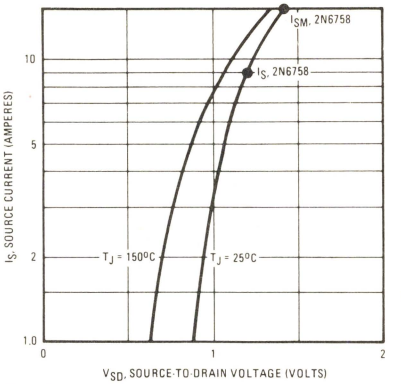


Fig. 12 – Typical Body-Drain Diode Forward Voltage

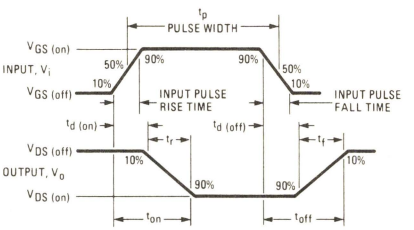


Fig. 14 – Switching Time Waveforms

HARRIS

2N6759
2N6760

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.5A and 5.5A, 350V - 400V
- $r_{DS(on)}$ = 1.0Ω and 1.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

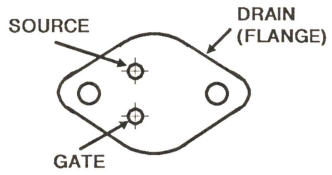
Description

The 2N6759 and 2N6760 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

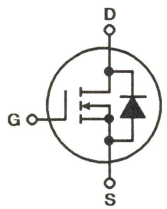
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6759	2N6760	UNITS
Drain-Source Voltage	V_{DS}	350*	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	350*	400*	V
Continuous Drain Current				
T_C = +25°C	I_D	4.5*	5.5*	A
T_C = +100°C	I_D	3.0*	3.5*	A
Pulsed Drain Current	I_{DM}	7.0	8.0	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	75*	75*	W
T_C = +100°C (See Figure 11)	P_D	30*	30*	W
Linear Derating Factor (See Figure 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	7.0	8.0	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1588.1**

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6759	350	–	–	V	V_{GS} = 0
		2N6760	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6759	–	–	7.0*	V	V_{GS} = 10V, I_D = 4.5A
		2N6760	–	–	6.7*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 3A
		2N6760	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3A, T_C = 125°C
		2N6760	–	–	2.2*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	3.0*	4.5	9.0*	S (℧)	V_{DS} = 15V, I_D = 3.5A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	50*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 175V$, I_D = 3.5A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	35*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6760	–	–	5.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
		2N6760	–	–	8.0		
V_{SD}	Diode Forward Voltage ①	2N6759	0.70*	–	1.4*	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0
		2N6760	0.75*	–	1.5*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

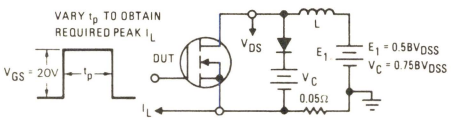


Fig. 1 – Clamped Inductive Test Circuit

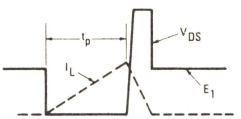


Fig. 2 – Clamped Inductive Waveforms

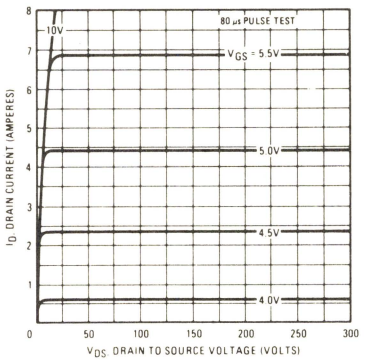


Fig. 3 – Typical Output Characteristics

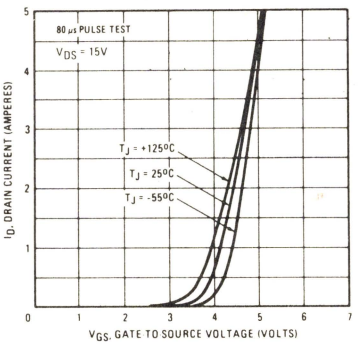


Fig. 4 – Typical Transfer Characteristics

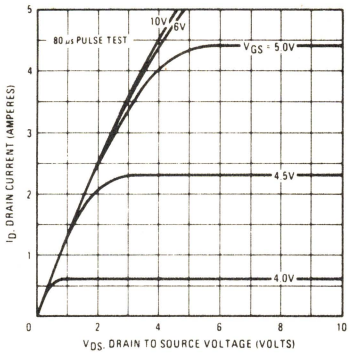


Fig. 5– Typical Saturation Characteristics (2N6759)

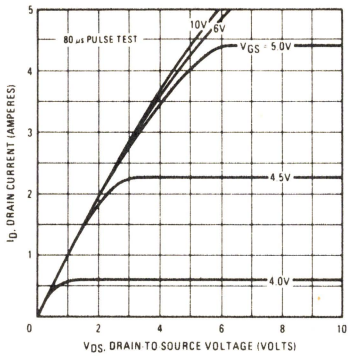


Fig. 6– Typical Saturation Characteristics (2N6760)

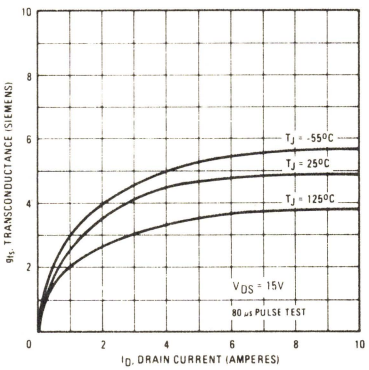


Fig. 7 – Typical Transconductance Vs. Drain Current

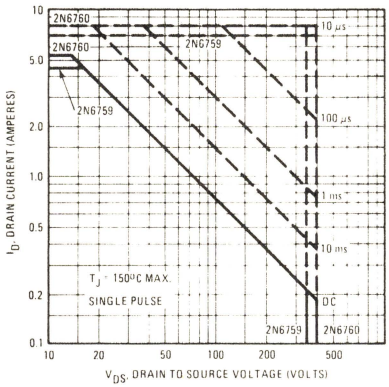


Fig. 8 – Maximum Safe Operating Area

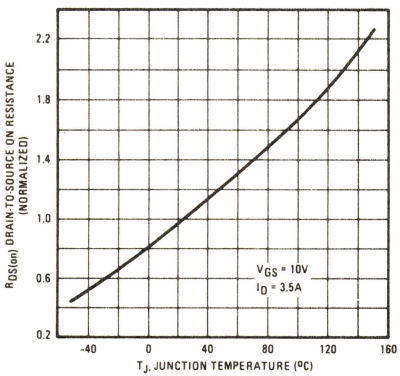


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

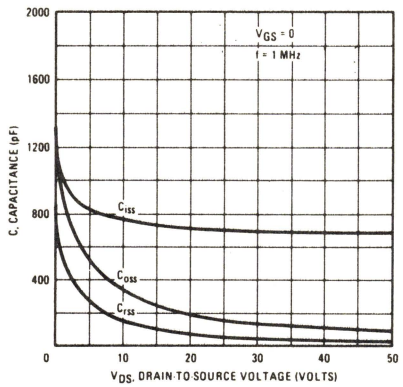


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

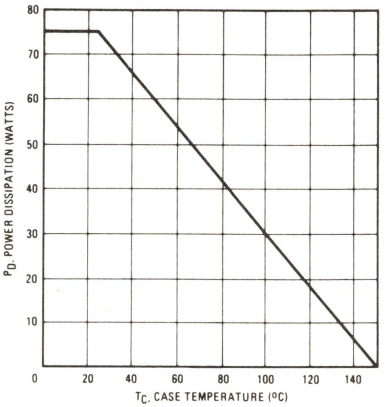


Fig. 11 – Power Vs. Temperature Derating Curve

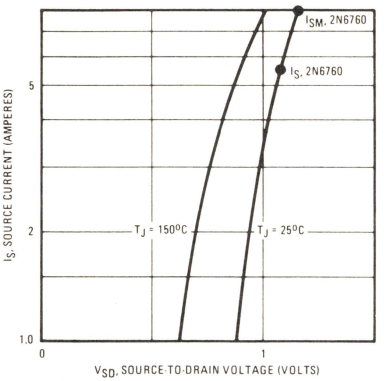


Fig. 12 – Typical Body-Drain Diode Forward Voltage

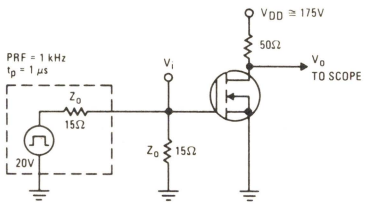


Fig. 13 – Switching Time Test Circuit

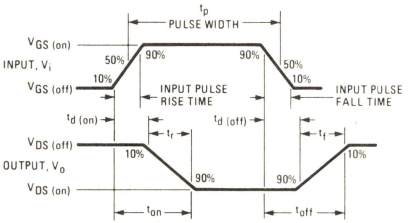


Fig. 14 – Switching Time Waveforms

HARRIS

2N6761
2N6762

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.0A, 5.5A and 450V - 500V
- $R_{DS(ON)} = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

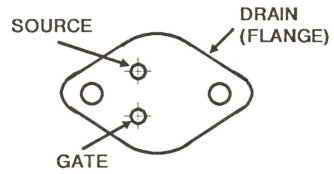
Description

The 2N6761 and 2N6762 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

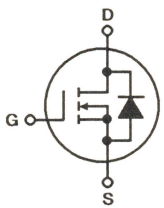
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6761	2N6762	UNITS
Drain-Source Voltage	V_{DS}	450*	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	450*	500*	V
Continuous Drain Current				
T_C = +25°C	I_D	4.0*	5.5*	A
T_C = +100°C	I_D	2.5*	3.0*	A
Pulsed Drain Current	I_{DM}	6.0	7.0	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	75*	75*	W
T_C = +100°C (See Figure 11)	P_D	30*	30*	W
Linear Derating Factor (See Figure 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	6.0	7.0	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1589.1

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6761	450	–	–	V	V_{GS} = 0
		2N6762	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_C = 25^oC$ to 125^oC
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6761	–	–	8.0*	V	V_{GS} = 10V, I_D = 4A
		2N6762	–	–	7.7*	V	V_{GS} = 10V, I_D = 4.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	1.5	2.0*	Ω	V_{GS} = 10V, I_D = 2.5A
		2N6762	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	–	4.4*	Ω	V_{GS} = 10V, I_D = 2.5A, $T_C = 125^oC$
		2N6762	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3.0A, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	2.5*	3.5	7.5*	S (℧)	V_{DS} = 16V, I_D = 3A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	25*	100	200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 225V$, I_D = 3A, $Z_o = 15\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	
t_f	Fall Time	ALL	–	–	30*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6762	–	–	4.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
		2N6762	–	–	7.0		
V_{SD}	Diode Forward Voltage ①	2N6761	0.65*	–	1.3*	V	$T_C = 25^oC$, I_S = 4A, V_{GS} = 0
		2N6762	0.7*	–	1.4*	V	$T_C = 25^oC$, I_S = 4.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.0	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

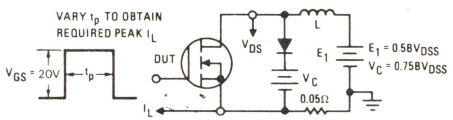


Fig. 1 – Clamped Inductive Test Circuit

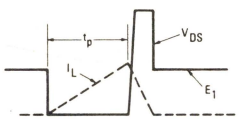


Fig. 2 – Clamped Inductive Waveforms

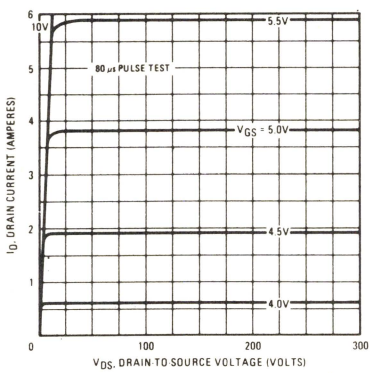


Fig. 3 – Typical Output Characteristics

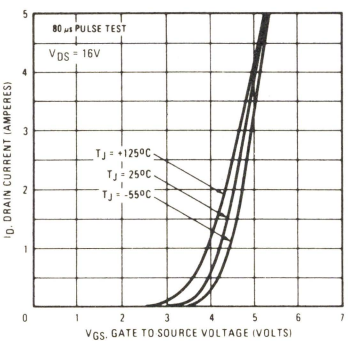


Fig. 4 – Typical Transfer Characteristics

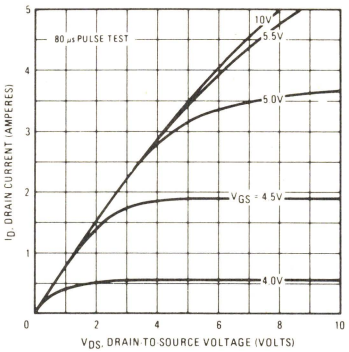


Fig. 5— Typical Saturation Characteristics (2N6761)

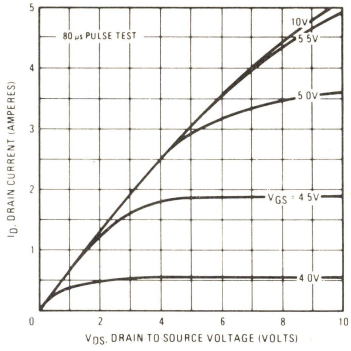


Fig. 6— Typical Saturation Characteristics (2N6762)

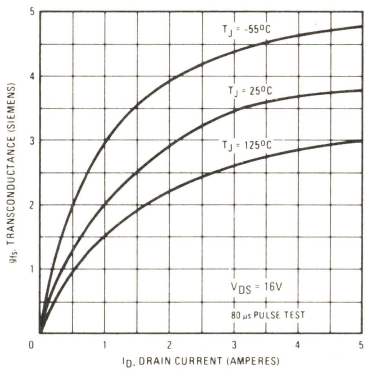


Fig. 7 — Typical Transconductance Vs. Drain Current

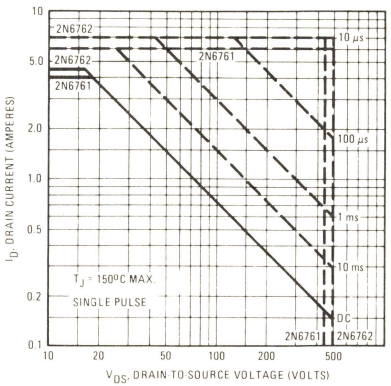


Fig. 8 — Maximum Safe Operating Area

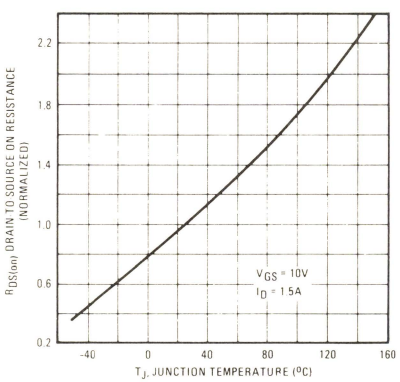


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

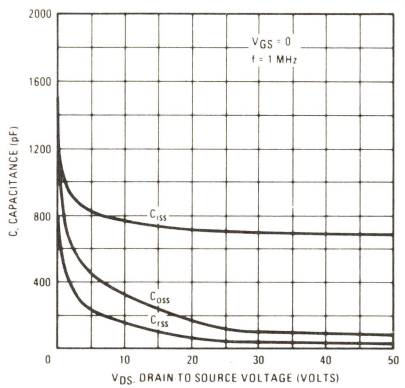


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

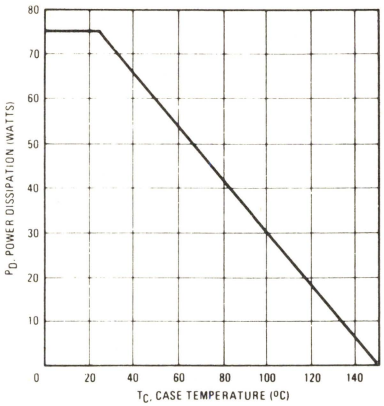


Fig. 11 — Power Vs. Temperature Derating Curve

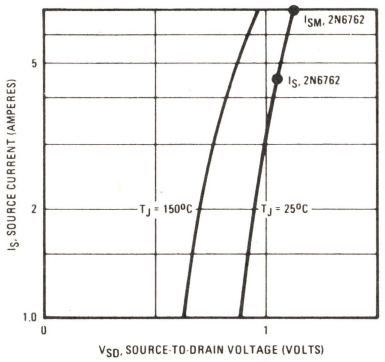


Fig. 12 — Typical Body-Drain Diode Forward Voltage

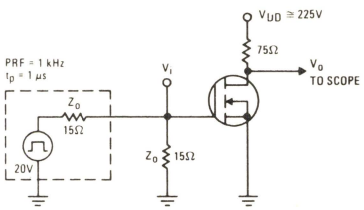


Fig. 13 — Switching Time Test Circuit

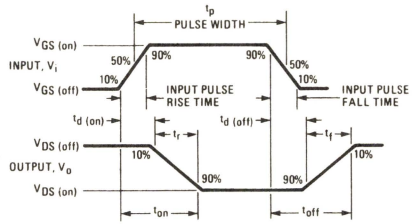


Fig. 14 — Switching Time Waveforms

HARRIS

2N6763
2N6764

N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- 31A and 38A, 60V - 100V
- $r_{DS(on)}$ = 0.08Ω and 0.055Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

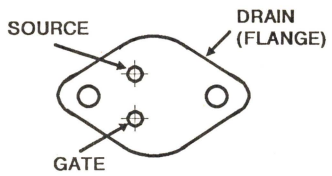
Description

The 2N6763 and 2N6764 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AE steel package.

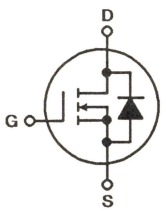
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6763	2N6764	UNITS
Drain-Source Voltage	V_{DS}	60*	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	60*	100*	V
Continuous Drain Current				
T_C = +25°C	I_D	31	38	A
T_C = +100°C	I_D	20	24	A
Pulsed Drain Current	I_{DM}	60	70	A
Gate-Source Voltage	V_{GS}	±20*	±20*	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	150*	150*	W
T_C = +100°C (See Figure 11)	P_D	60*	60*	W
Linear Derating Factor (See Figure 11)		1.2	1.2	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	60	70	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1590.1

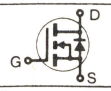
ELECTRICAL CHARACTERISTICS @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6763	60	–	–	V	V_{GS} = 0
		2N6764	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6763	–	–	2.48*	V	V_{GS} = 10V I_D = 31A
		2N6764	–	–	2.09*	V	V_{GS} = 10V, I_D = 38A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	0.06	0.08*	Ω	V_{GS} = 10V, I_D = 20A
		2N6764	–	0.045	0.055*	Ω	V_{GS} = 10V, I_D = 24A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	–	0.136*	Ω	V_{GS} = 10V, I_D = 20A, T_C = 125°C
		2N6764	–	–	0.094*	Ω	V_{GS} = 10V, I_D = 24A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	12.5	27*	S (℧)	V_{DS} = 15V, I_D = 24A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	500*	1000	1500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 24V, I_D = 24A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

THERMAL RESISTANCE

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

BODY-DRAIN DIODE RATINGS AND CHARACTERISTICS

I_S	Continuous Source Current (Body Diode)	2N6763	–	–	31*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6764	–	–	38*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6763	–	–	60	A	
		2N6764	–	–	70		
V_{SD}	Diode Forward Voltage ①	2N6763	0.90*	–	1.8*	V	T_C = 25°C, I_S = 31A, V_{GS} = 0
		2N6764	0.95*	–	1.9*	V	T_C = 25°C, I_S = 38A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

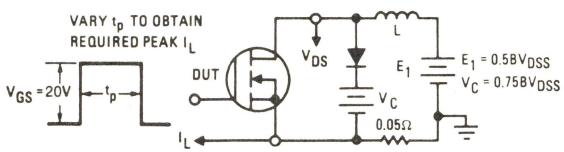


Fig. 1 - Clamped inductive test circuit.

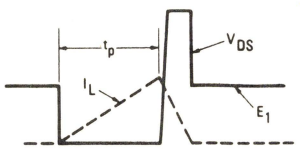


Fig. 2 - Clamped inductive waveforms.

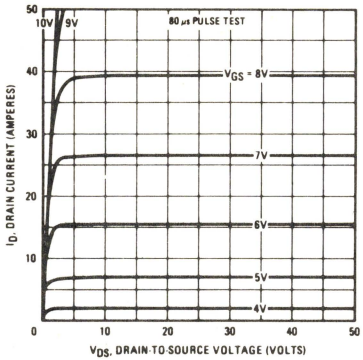


Fig. 3 - Typical output characteristics.

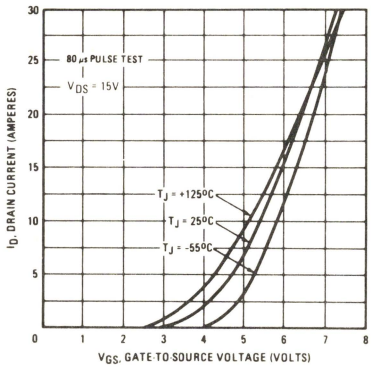


Fig. 4 - Typical transfer characteristics.

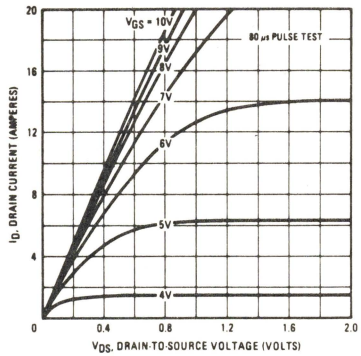


Fig. 5 - Typical saturation characteristics for the 2N6763.

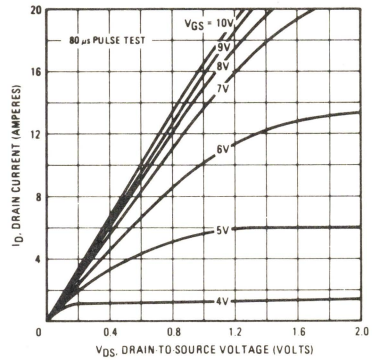


Fig. 6 - Typical saturation characteristics for the 2N6764.

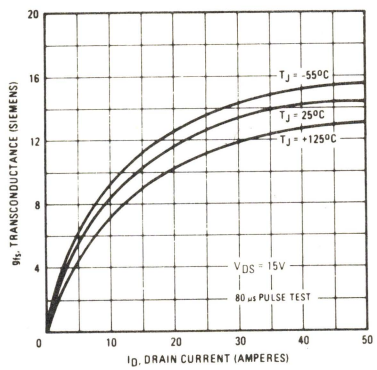


Fig. 7 - Typical transconductance vs. drain current.

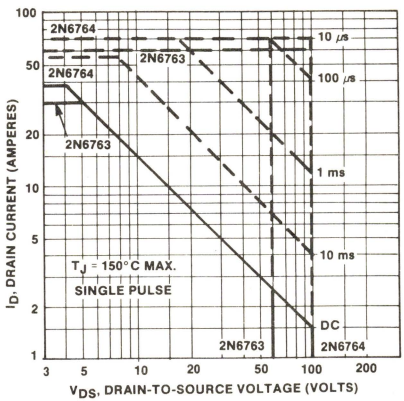


Fig. 8 - Maximum safe operating areas.

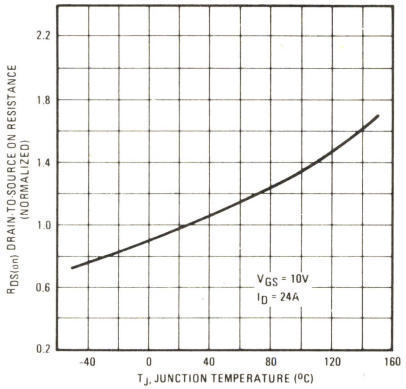


Fig. 9 - Typical normalized on-resistance vs. temperature.

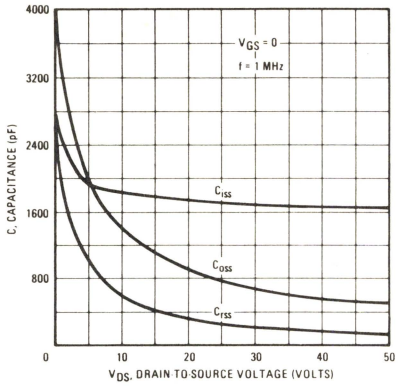


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

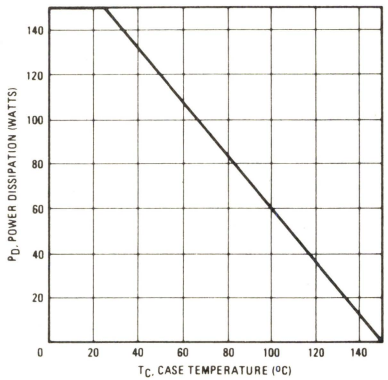


Fig. 11 - Power vs. temperature derating curve.

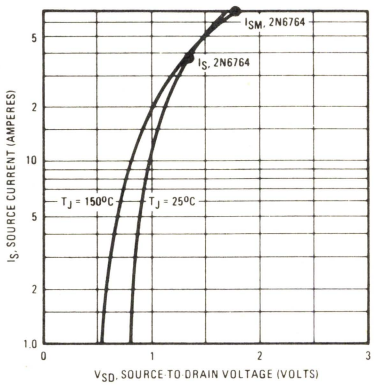


Fig. 12 - Typical body-drain diode forward voltage.

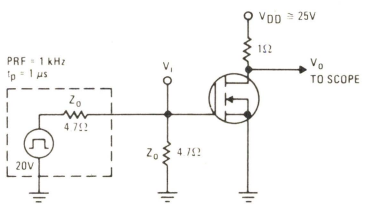


Fig. 13 - Switching time test circuit.

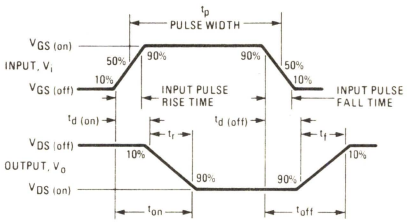


Fig. 14 - Switching time waveforms.

HARRIS

2N6765
2N6766

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 25A and 30A, 150V - 200V
- $r_{DS(on)}$ = 0.085Ω and 0.12Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

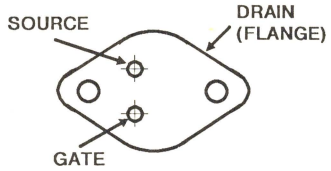
Description

The 2N6765 and 2N6766 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AE steel package.

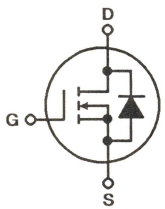
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	2N6765	2N6766	UNITS
Drain-Source Voltage ..... V_{DS}	150*	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) ..... V_{DGR}	150*	200*	V
Continuous Drain Current			
T_C = +25°C ..... I_D	25*	30*	A
T_C = +100°C ..... I_D	16*	19*	A
Pulsed Drain Current ..... I_{DM}	50	60	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C (See Figure 11) ..... P_D	150*	150*	W
T_C = +100°C (See Figure 11) ..... P_D	60*	60*	W
Linear Derating Factor (See Figure 11)	1.2*	1.2*	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figures 1 and 2, L = 100μH)	50	60	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1591.1

Electrical Characteristics @ T_C = 25° C (Unless Otherside Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6765	150	–	–	V	V_{GS} = 0
		2N6766	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6765	–	–	3.0*	V	V_{GS} = 10V, I_D = 25A
		2N6766	–	–	2.7*	V	V_{GS} = 10V, I_D = 30A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	0.09	0.12*	Ω	V_{GS} = 10V, I_D = 16A
		2N6766	–	0.07	0.085*	Ω	V_{GS} = 10V, I_D = 19A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	–	0.216*	Ω	V_{GS} = 10V, I_D = 16A, T_C = 125°C
		2N6766	–	–	0.153*	Ω	V_{GS} = 10V, I_D = 19A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	15.5	27*	S (℧)	V_{DS} = 15V, I_D = 19A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	450*	800	1200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 95V, I_D = 19A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Typical socket mount

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6765	–	–	25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6766	–	–	30*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6765	–	–	50	A	
		2N6766	–	–	60		
V_{SD}	Diode Forward Voltage ①	2N6765	0.85*	–	1.7*	V	T_C = 25°C, I_S = 25A, V_{GS} = 0
		2N6766	0.9*	–	1.8*	V	T_C = 25°C, I_S = 30A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

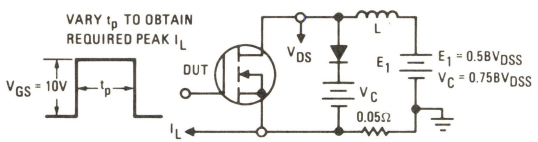


Fig. 1 — Clamped Inductive Test Circuit

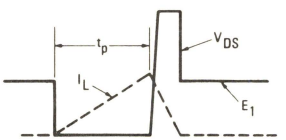


Fig. 2 — Clamped Inductive Waveforms

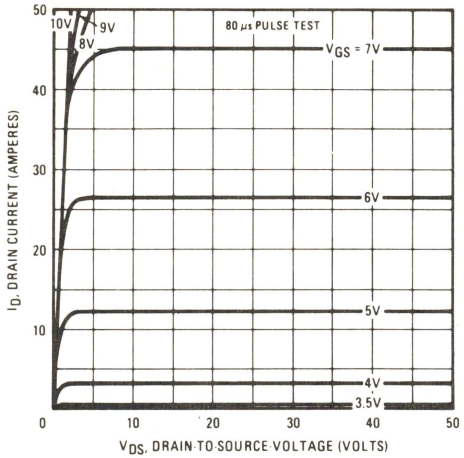


Fig. 3 — Typical Output Characteristics

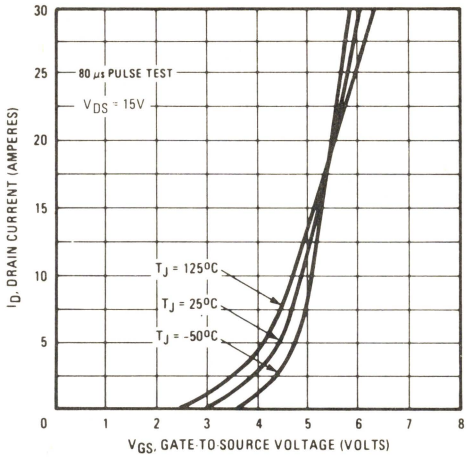


Fig. 4 — Typical Transfer Characteristics

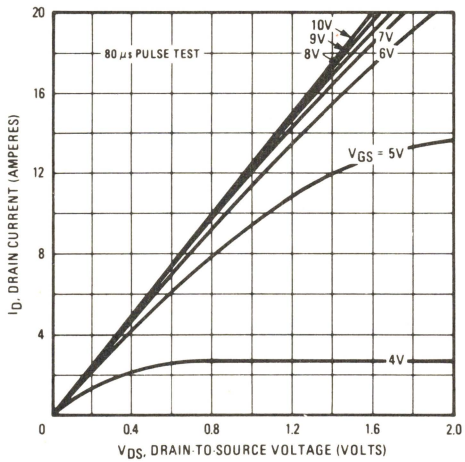


Fig. 5— Typical Saturation Characteristics (2N6765)

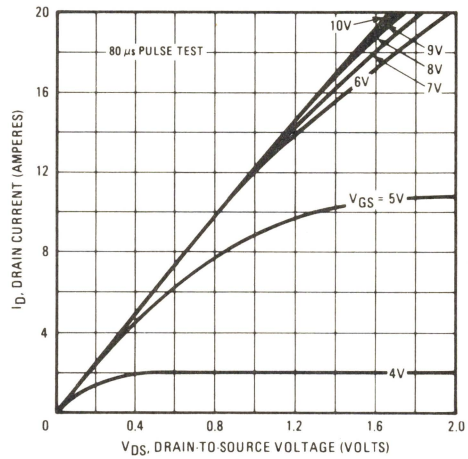


Fig. 6— Typical Saturation Characteristics (2N6766)

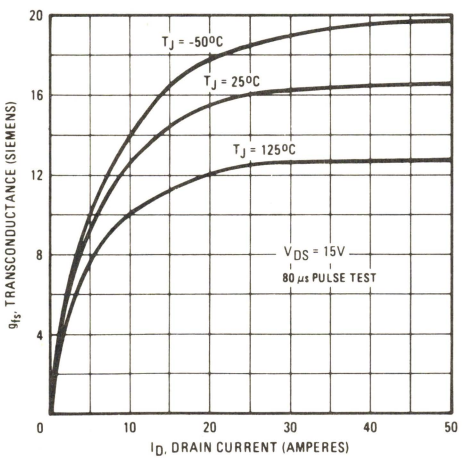


Fig. 7 — Typical Transconductance Vs. Drain Current

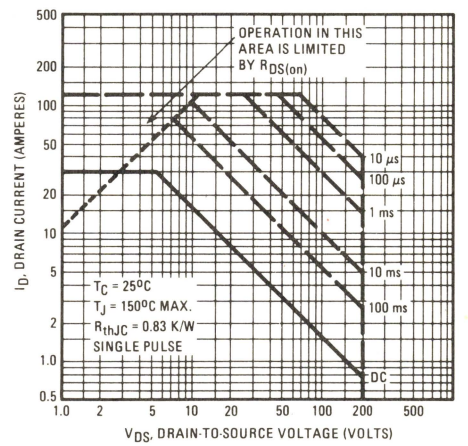


Fig. 8 — Maximum Safe Operating Area

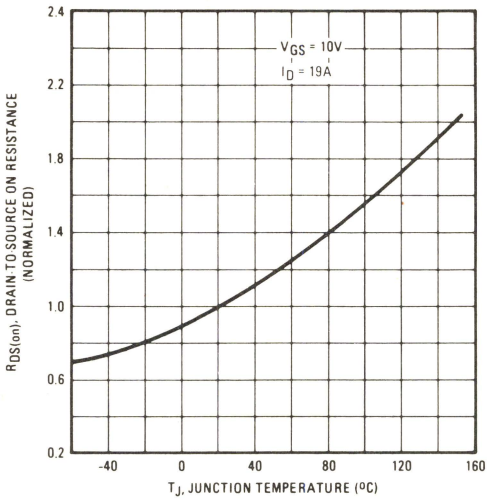


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

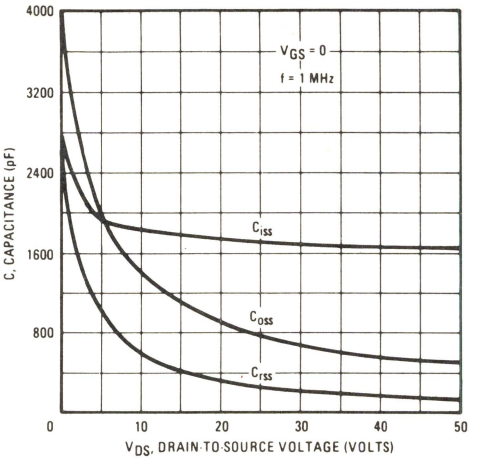


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

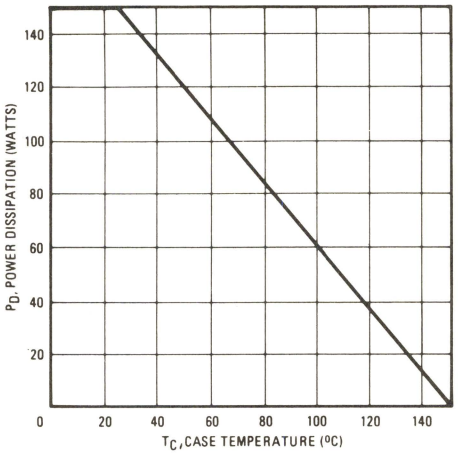


Fig. 11 — Power Vs. Temperature Derating Curve

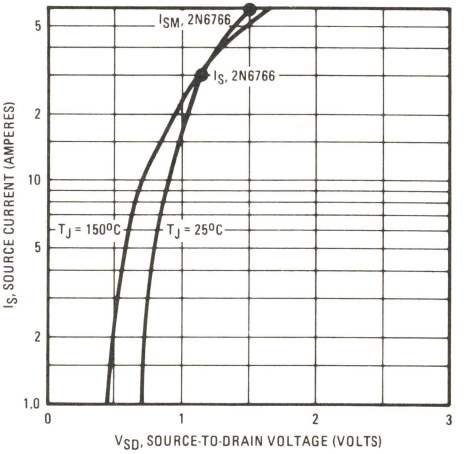


Fig. 12 — Typical Body-Drain Diode Forward Voltage

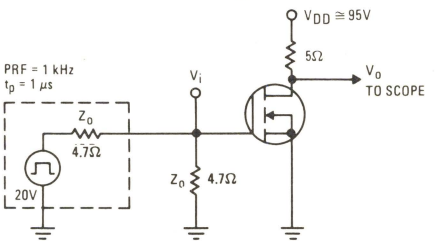


Fig. 13 — Switching Time Test Circuit

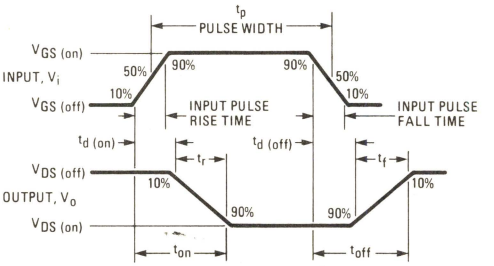


Fig. 14 — Switching Time Waveforms

HARRIS

2N6767
2N6768

N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- 12A and 14A, 350V - 400V
- $r_{DS(on)}$ = 0.4Ω and 0.3Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

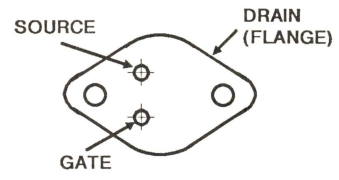
Description

The 2N6767 and 2N6768 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

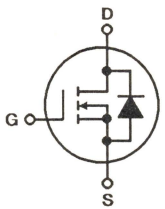
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6767	2N6768	UNITS
Drain-Source Voltage	V_{DS}	350*	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	350*	400*	V
Continuous Drain Current				
T_C = +25°C	I_D	12*	14*	A
T_C = +100°C	I_D	7.75*	9*	A
Pulsed Drain Current	I_{DM}	20	25	A
Gate-Source Voltage	V_{GS}	±20*	±20*	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	150*	150*	W
Above T_C = +25°C, Derate Linearly		1.2*	1.2*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	20	25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1898.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6767	350	–	–	V	V_{GS} = 0
		2N6768	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6767	–	–	5.4*	V	V_{GS} = 10V, I_D = 12A
		2N6768	–	–	5.6*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
		2N6768	–	0.25	0.3*	Ω	V_{GS} = 10V, I_D = 9.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
		2N6768	–	–	0.66*	Ω	V_{GS} = 10V, I_D = 9.0A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	8.0*	11.0	24*	S (℧)	V_{DS} = 15V, I_D = 9.0A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 180V, I_D = 9.0A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	65*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	75*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6767	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6768	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6767	–	–	20	A	
		2N6768	–	–	25		
V_{SD}	Diode Forward Voltage ①	2N6767	0.8*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6768	0.85*	–	1.7*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	25	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

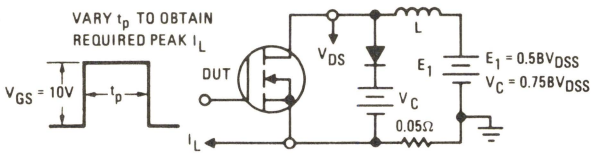


Fig. 1 - Clamped inductive test circuit.

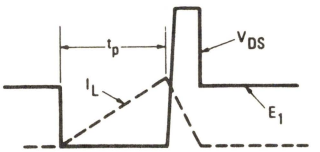


Fig. 2 - Clamped inductive waveforms.

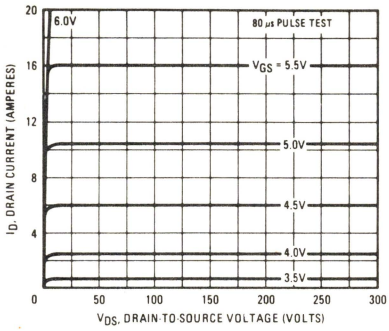


Fig. 3 - Typical output characteristics for both types.

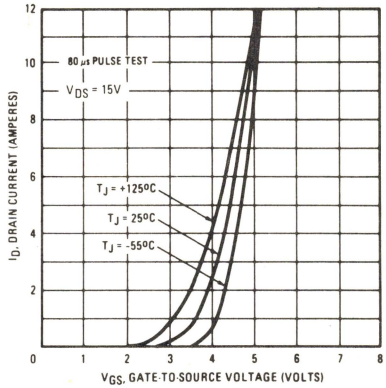


Fig. 4 - Typical transfer characteristics for both types.

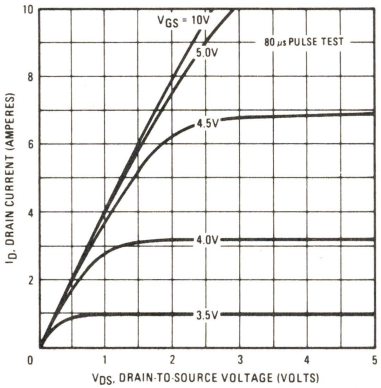


Fig. 5 - Typical saturation characteristics for the 2N6767.

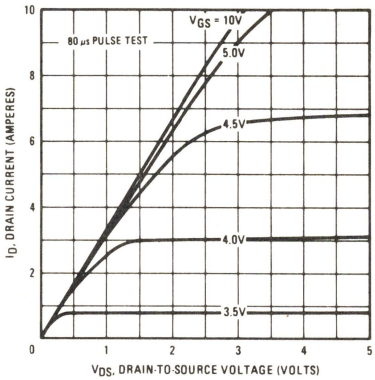


Fig. 6. - Typical saturation characteristics for the 2N6768.

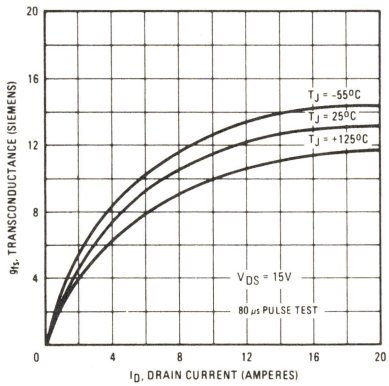


Fig. 7 - Typical transconductance versus drain current for both types.

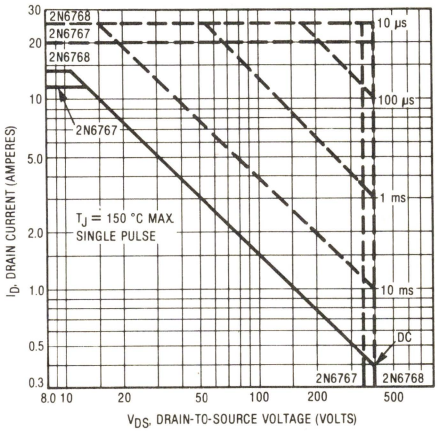


Fig. 8 - Maximum safe operating area for both types.

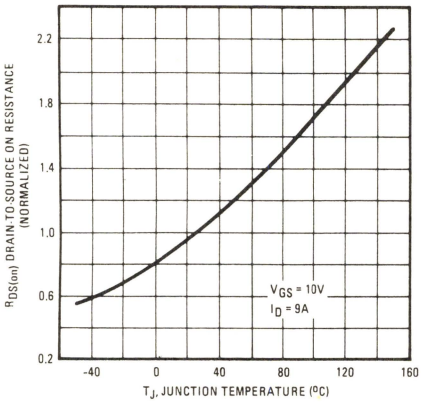


Fig. 9 - Typical normalized on-resistance versus temperature for both types.

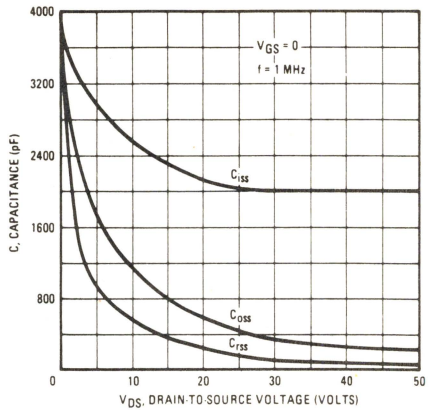


Fig. 10 - Typical capacitance versus drain-to-source voltage for both types.

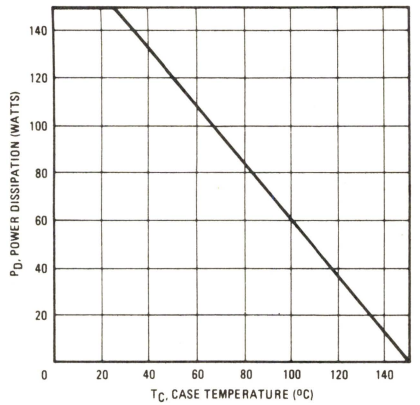


Fig. 11 - Power versus temperature derating curve for both types.

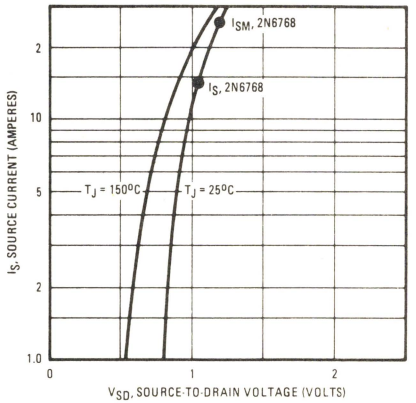


Fig. 12 - Typical body-drain diode forward voltage for both types.

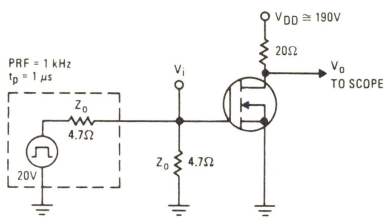


Fig. 13 - Switching time test circuit.

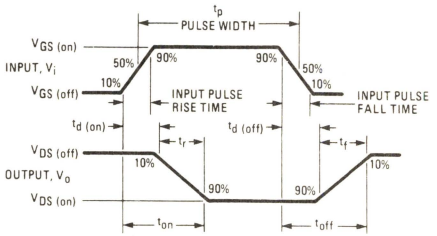


Fig. 14 - Switching time waveforms

HARRIS

2N6769
2N6770

N-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- 11A and 12A, 450V - 500V
- $r_{DS(on)}$ = 0.5Ω and 0.4Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

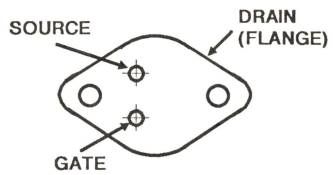
Description

The 2N6769 and 2N6770 are n-channel enhancement-mode silicon-gate power MOS field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

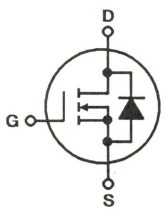
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6769	2N6770	UNITS
Drain-Source Voltage	V_{DS}	450*	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	450*	500*	V
Continuous Drain Current				
T_C = +25°C	I_D	11	12	A
T_C = +100°C	I_D	7	7.75	A
Pulsed Drain Current	I_{DM}	20	25	A
Gate-Source Voltage	V_{GS}	±20*	±20*	V
Maximum Power Dissipation				
T_C = +25°C (See Figure 11)	P_D	150*	150*	W
Above T_C = +25°C, Derate Linearly (See Figure 11)		1.2*	1.2*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	20	25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1899.1**

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6769	450	–	–	V	$V_{GS} = 0$
		2N6770	500	–	–	V	$I_D = 4.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	$V_{DS} = 0.8$ x Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 25^oC$ to 125^oC
$V_{DS(on)}$	Static Drain-Source On-State Voltage (1)	2N6769	–	–	6.0*	V	$V_{GS} = 10V$, $I_D = 11A$
		2N6770	–	–	6.0*	V	$V_{GS} = 10V$, $I_D = 12A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6769	–	0.4	0.5*	Ω	$V_{GS} = 10V$, $I_D = 7A$
		2N6770	–	0.3	0.4*	Ω	$V_{GS} = 10V$, $I_D = 7.75A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance (1)	2N6769	–	–	1.1*	Ω	$V_{GS} = 10V$, $I_D = 7.0A$, $T_C = 125°C$
		2N6770	–	–	0.88*	Ω	$V_{GS} = 10V$, $I_D = 7.75A$, $T_C = 125°C$
g_{fs}	Forward Transconductance (1)	ALL	8.0*	12.0	24*	S (℧)	$V_{GS} = 10V$ $I_D = 7.75A$
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong 210V$, $I_D = 7.75A$, $Z_o = 4.7\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50*	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	
t_f	Fall Time	ALL	–	–	70*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6769	–	–	11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6770	–	–	12*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6769	–	–	20	A	
		2N6770	–	–	25		
V_{SD}	Diode Forward Voltage (1)	2N6769	0.75*	–	1.5*	V	$T_C = 25^oC$, $I_S = 11A$, $V_{GS} = 0$
		2N6770	0.80*	–	1.6*	V	$T_C = 25^oC$, $I_S = 12A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	1300	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.4	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. (1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

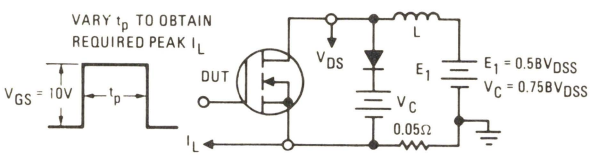


Fig. 1 - Clamped inductive test circuit.

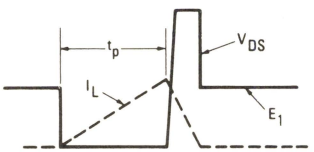


Fig. 2 - Clamped inductive waveforms.

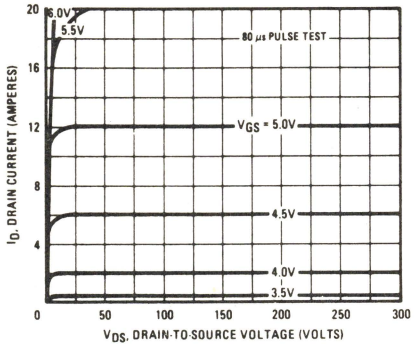


Fig. 3 - Typical output characteristics for both types.

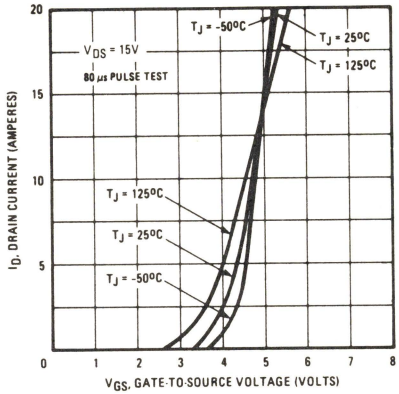


Fig. 4 - Typical transfer characteristics for both types.

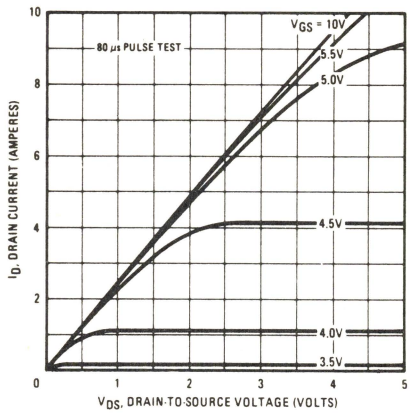


Fig. 5 - Typical saturation characteristics for the 2N6769.

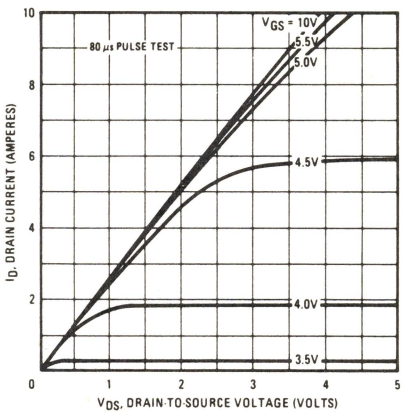


Fig. 6. - Typical saturation characteristics for the 2N6770.

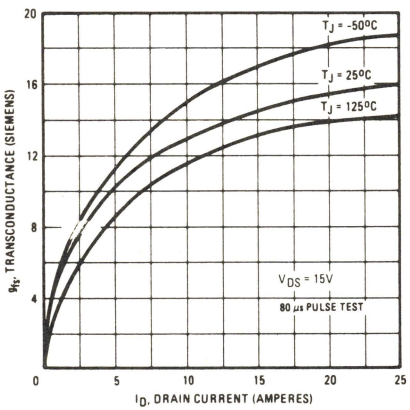


Fig. 7 - Typical transconductance versus drain current for both types.

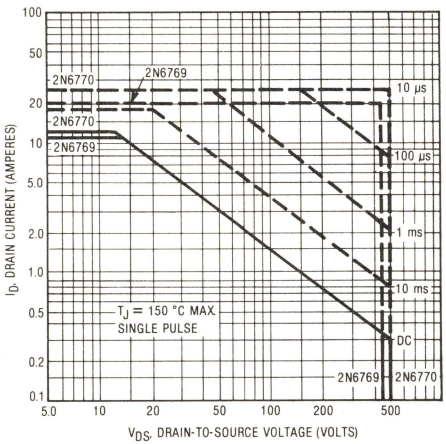


Fig. 8 - Maximum safe operating area for both types.

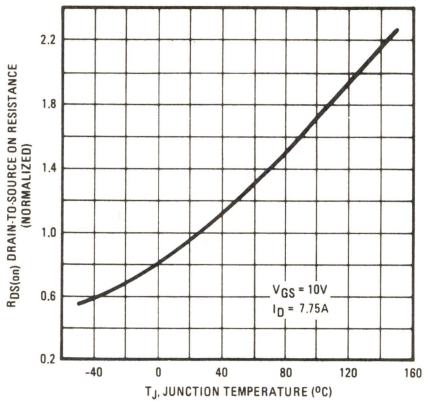


Fig. 9 - Typical normalized on-resistance versus temperature for both types.

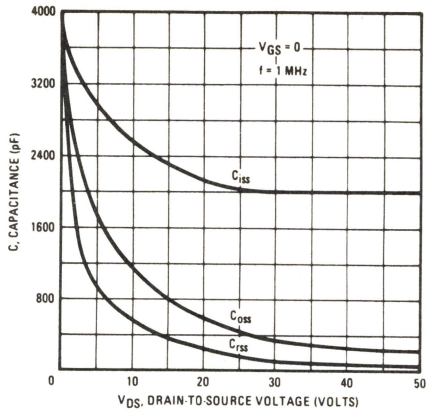


Fig. 10 - Typical capacitance versus drain-to-source voltage for both types.

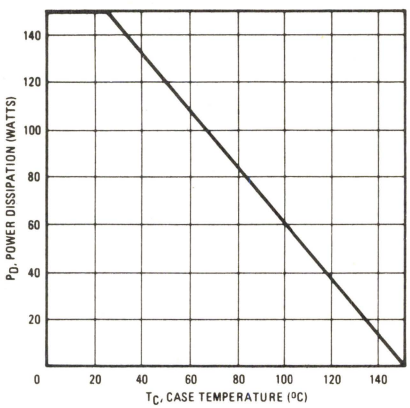


Fig. 11 - Power versus temperature derating curve for both types.

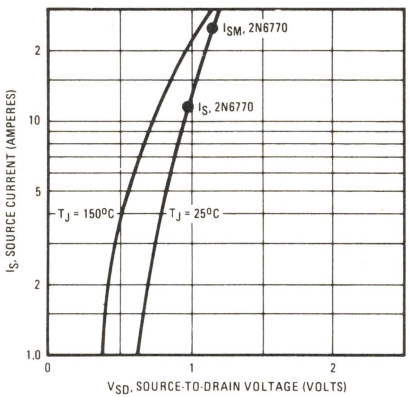


Fig. 12 - Typical body-drain diode forward voltage for both types.

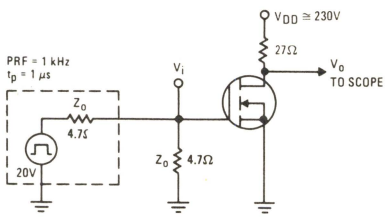


Fig. 13 - Switching time test circuit.

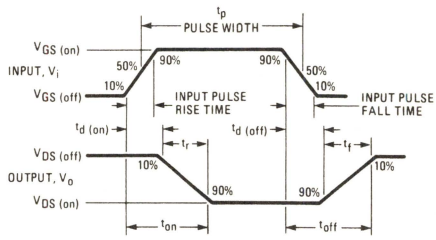


Fig. 14 - Switching time waveforms

HARRIS

2N6782

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 3.5A, 100V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

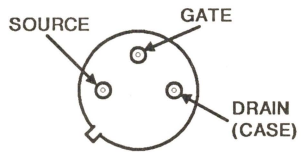
Description

The 2N6782 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6782 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

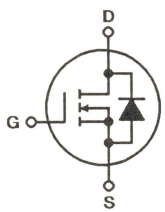
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6782	UNITS
Drain-Source Voltage (Note 1)	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	3.5*	A
T_C = +100°C	I_D	2.25*	A
Pulsed Drain Current (Note 2)	I_{DM}	14*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	3.50*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	14*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	15*	W
Linear Derating Factor (See Figure 14)		0.12*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	14	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

NOTES:

1. T_J = +25°C to +150°C
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1592.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	2.1*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.5	0.6*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 25°C
		–	–	1.08*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.0*	1.5	3.0*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	80	100*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	10*	20	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	15*	ns	V_{DD} ≅ 34V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	–	–	25*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	25*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	20*	ns	of operating temperature.)
SOA	Safe Operating Area	15	–	–	W	V_{DS} = 80V, I_D = 188 mA, See Fig. 16.
		15	–	–	W	V_{DS} = 4.28V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	200	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.0	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

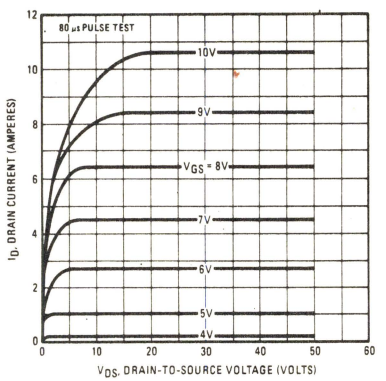


Fig. 1 – Typical Output Characteristics

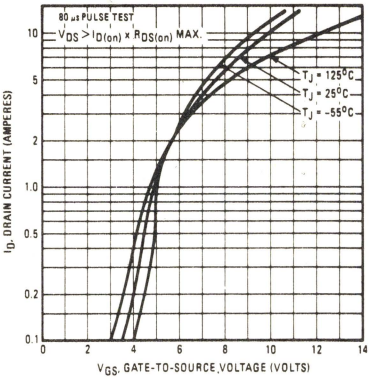


Fig. 2 – Typical Transfer Characteristics

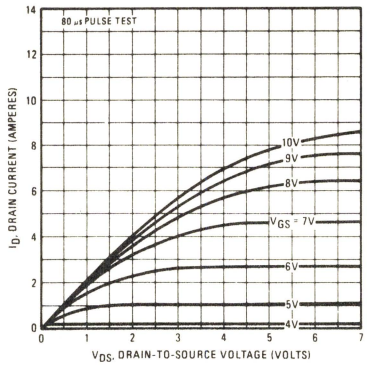


Fig. 3 – Typical Saturation Characteristics

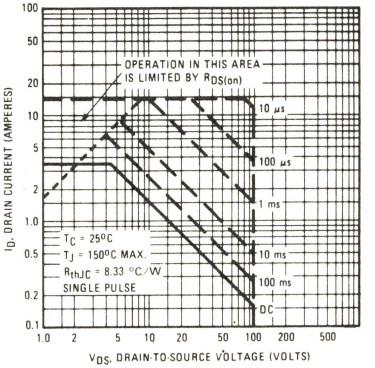


Fig. 4 – Maximum Safe Operating Area

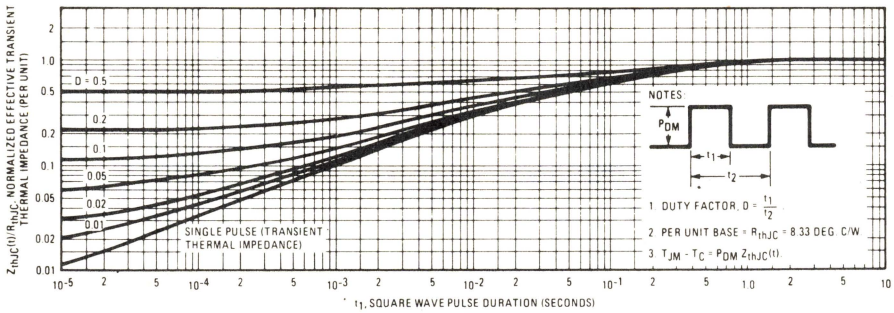


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

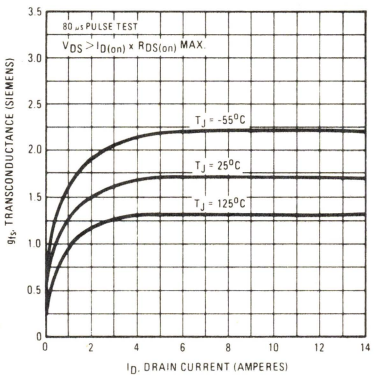


Fig. 6 – Typical Transconductance Vs. Drain Current

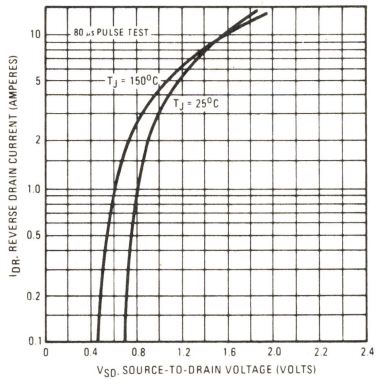


Fig. 7 – Typical Source-Drain Diode Forward Voltage

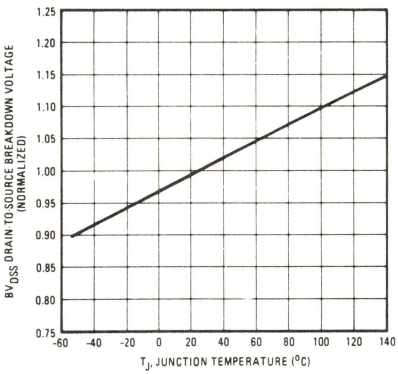


Fig. 8 – Breakdown Voltage Vs. Temperature

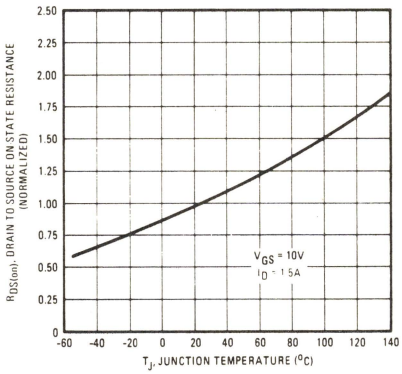


Fig. 9 – Normalized On-Resistance Vs. Temperature

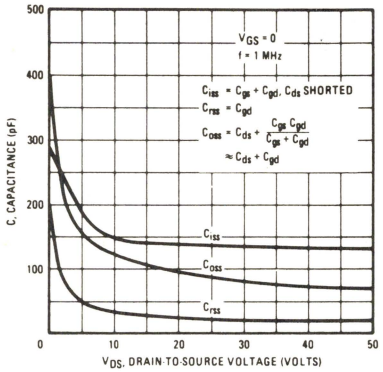


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

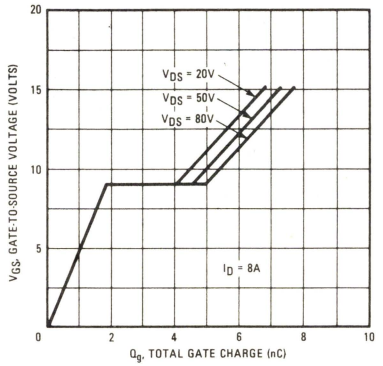


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

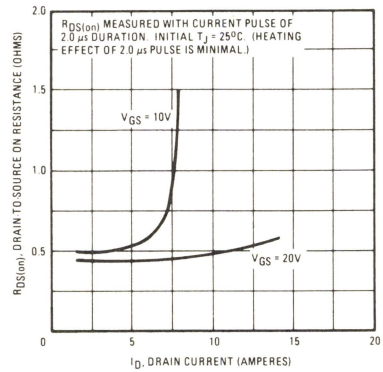


Fig. 12 – Typical On-Resistance Vs. Drain Current

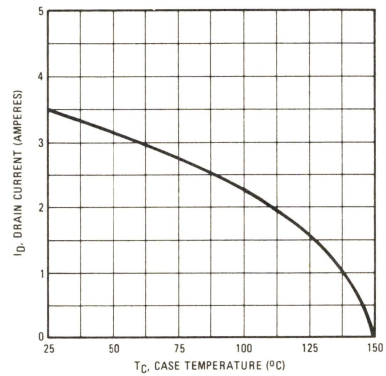


Fig. 13 – Maximum Drain Current Vs. Case Temperature

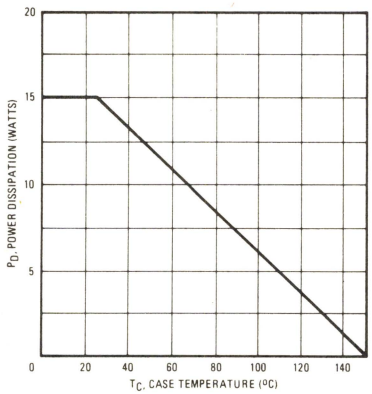
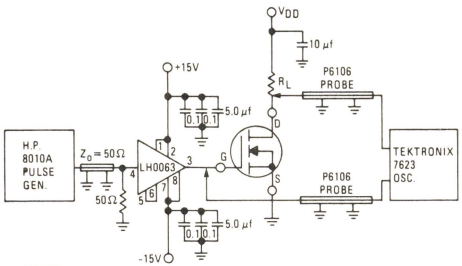
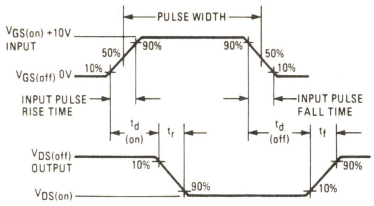


Fig. 14 – Power Vs. Temperature Derating Curve

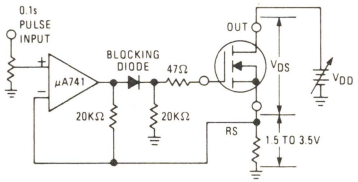


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

HARRIS

2N6784

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 2.25A, 200V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

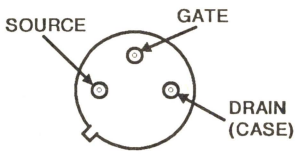
Description

The 2N6784 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6784 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

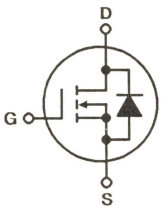
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6784	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200*	V
Continuous Drain Current			
T_C = +25°C	I_D	2.25*	A
T_C = +100°C	I_D	1.5*	A
Pulsed Drain Current (Note 2)	I_{DM}	9*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	2.25*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	9*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	15*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.12*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	9	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1906.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	—	—	3.37*	V	V_{GS} = 10V, I_D = 2.25A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	—	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 25°C
		—	—	2.81*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.7*	—	1.5*	V	T_C = 25°C, I_S = 2.25A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	0.9*	1.3	2.7*	S(℧)	V_{DS} = 5V, I_D = 1.5A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	20*	60	80*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	16	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	15*	ns	$V_{DD} \cong$ 75V, I_D = 1.5A, Z_o = 50Ω
t_r	Rise Time	—	—	20*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	30*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	—	20*	ns	
SOA	Safe Operating Area	15	—	—	W	V_{DS} = 160V, I_D = 94 mA, See Fig. 16.
		15	—	—	W	V_{DS} = 6.67V, I_D = 2.25A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	290	ns	T_J = 150°C, I_F = 2.25A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	2.0	μC	T_J = 150°C, I_F = 2.25A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

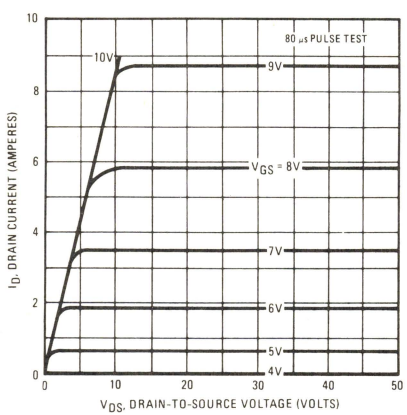


Fig. 1 - Typical output characteristics.

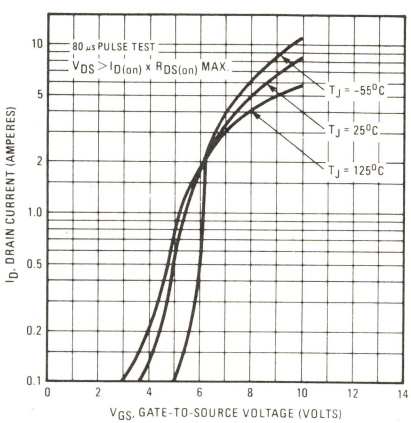


Fig. 2 - Typical transfer characteristics.

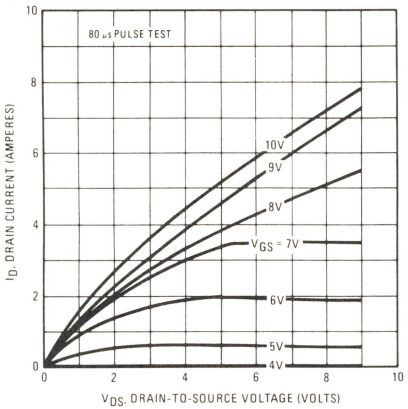


Fig. 3 - Typical saturation characteristics.

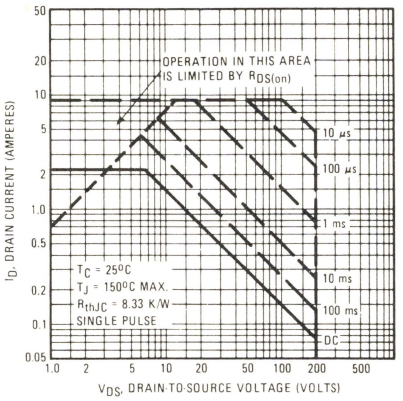


Fig. 4 - Maximum safe operating area.

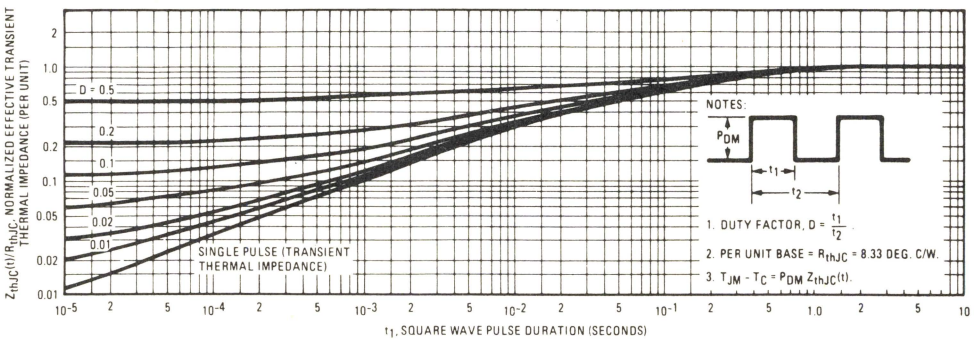


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

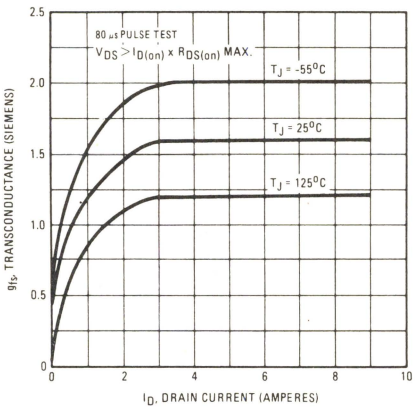


Fig. 6 - Typical transconductance versus drain current.

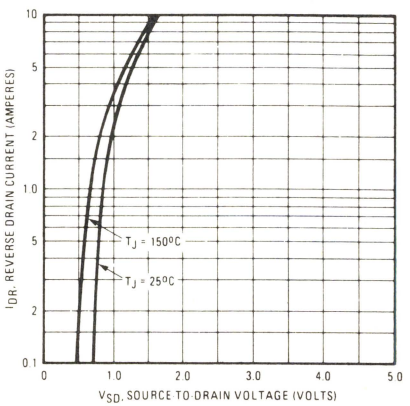


Fig. 7 - Typical source-drain diode forward voltage.

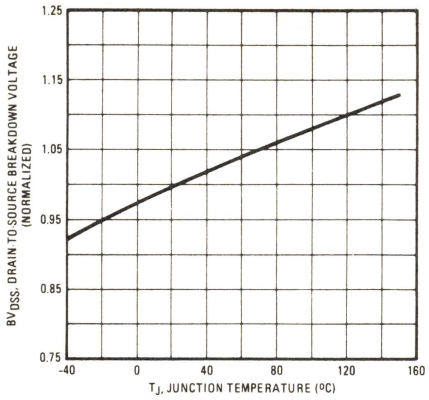


Fig. 8 - Breakdown voltage versus temperature.

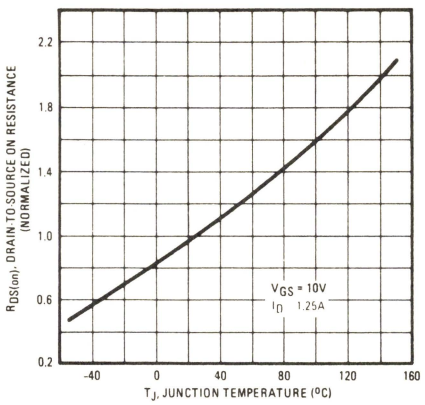


Fig. 9 - Typical normalized on-resistance versus temperature.

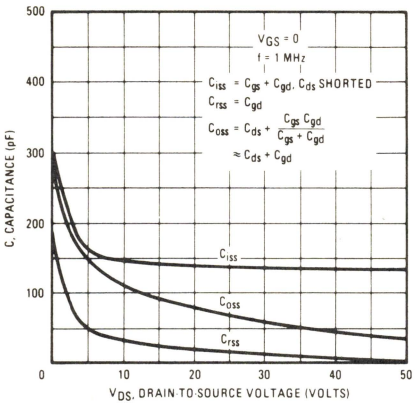


Fig. 10 - Typical capacitance versus drain-to-source voltage.

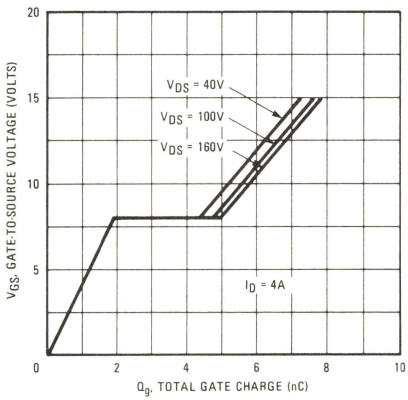


Fig. 11 - Typical gate charge versus gate-to-source voltage.

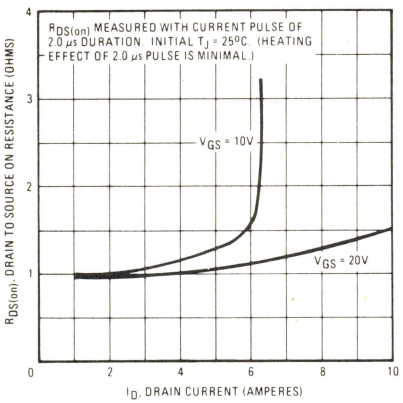


Fig. 12 - Typical on-resistance versus drain current.

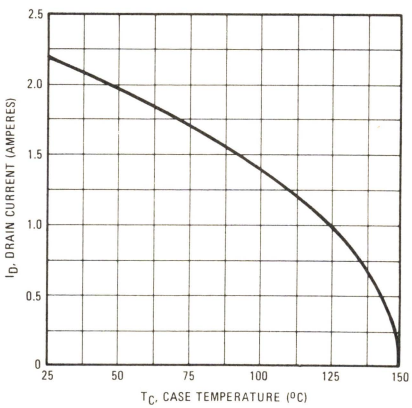


Fig. 13 - Maximum drain current versus case temperature.

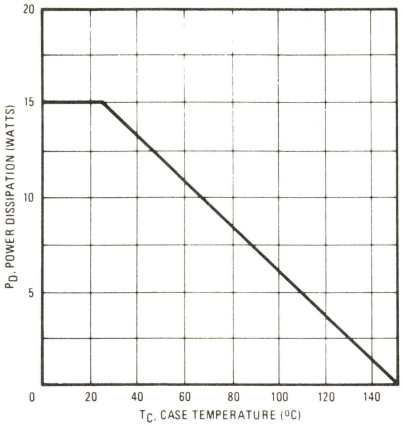
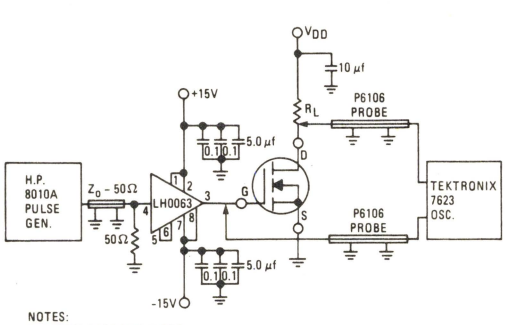
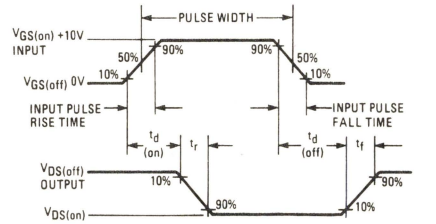


Fig. 14 - Power versus temperature derating curve.

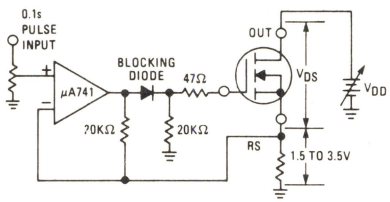


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6786

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 1.25A, 400V
- $r_{DS(on)} = 3.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

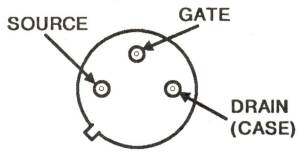
Description

The 2N6786 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6786 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

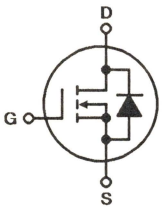
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6786	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	1.25*	A
T_C = +100°C	I_D	0.8*	A
Pulsed Drain Current	I_{DM}	5.5*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	1.25*	A
Pulse Source Current	I_{SM}	5.5*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	15*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.12*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	5.5	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2207.1**

ELECTRICAL CHARACTERISTICS at T_C = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	400*	—	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.5 mA	2.0*	—	4.0*	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	—	100*	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	—	—	100*	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	—	—	250*	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_C = 125°C	—	—	1000*	μA
On-State Voltage[a]	$V_{DS(on)}$	V_{GS} = 10 V, I_D = 1.25 A	—	—	4.5*	V
Static Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 0.8 A, T_A = 25°C	—	3.3	3.6*	Ω
		V_{GS} = 10 V, I_D = 0.8 A, T_A = 125°C	—	—	7.92*	Ω
Diode Forward Voltage[a]	V_{SD}	T_C = 25°C, I_S = 1.25 A, V_{GS} = 0 V	0.6*	—	1.4*	V
Forward Transconductance[a]	g_{fs}	V_{DS} = 5 V, I_D = 0.8 A	0.7*	1.2	2.1*	S(℧)
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz See Fig. 10	60*	135	200*	pF
Output Capacitance	C_{oss}		15*	35	50*	pF
Reverse Transfer Capacitance	C_{rss}		2*	8	15*	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} ≅ 170 V, I_D = 0.8 A, Z_O = 50 Ω See Fig. 15. (MOSFET switching times are essentially independent of operating temperature.)	—	—	15*	ns
Rise Time	t_r		—	—	20*	ns
Turn-Of Delay Time	$t_{d(off)}$		—	—	35*	ns
Fall Time	t_f		—	—	30*	ns
Safe Operating Area	SOA	V_{DS} = 200 V, I_D = 75 mA, See Fig. 16.	15	—	—	W
		V_{DS} = 12 V, I_D = 1.25 A, See Fig. 16.	15	—	—	W

THERMAL RESISTANCE

Junction-to-Case	$R_{\theta JC}$		—	—	8.33*	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	—	—	175	°C/W

SOURCE-DRAIN DIODE SWITCHING CHARACTERISTICS (TYPICAL)

Reverse Recovery Time	t_{rr}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	380	ns
Reverse Recovered Charge	Q_{RR}	T_J=150°C, I_F=1.25 A, di_F/dt=100 A/μs	2.7	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value.

[a]Pulse Test: Pulse width ≤ 300 μs, duty cycle ≤ 2%.

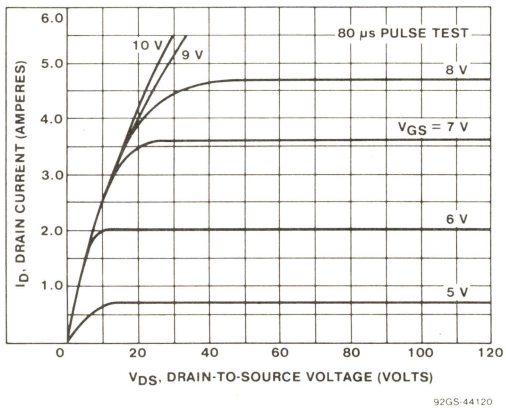


Fig. 1 - Typical output characteristics.

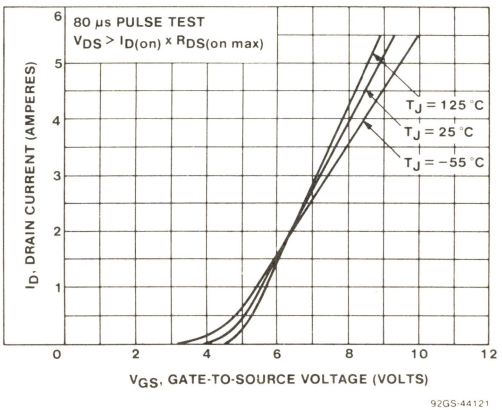


Fig. 2 - Typical transfer characteristics.

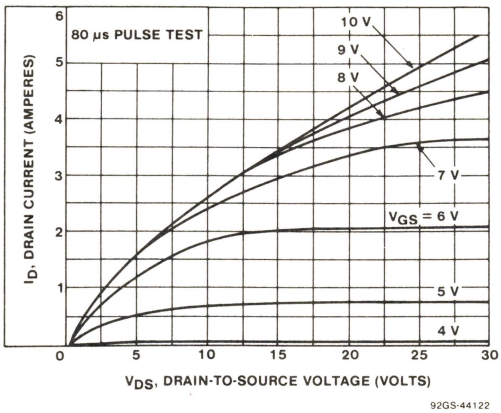


Fig. 3 - Typical saturation characteristics.

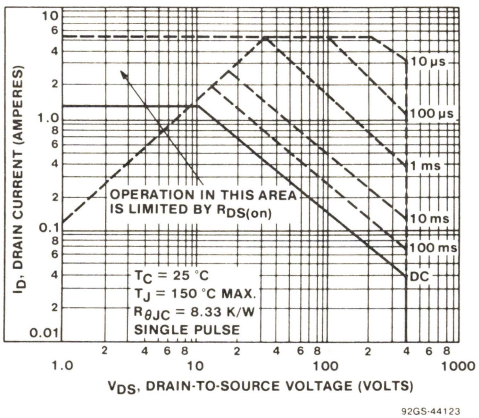


Fig. 4 - Maximum safe operating area.

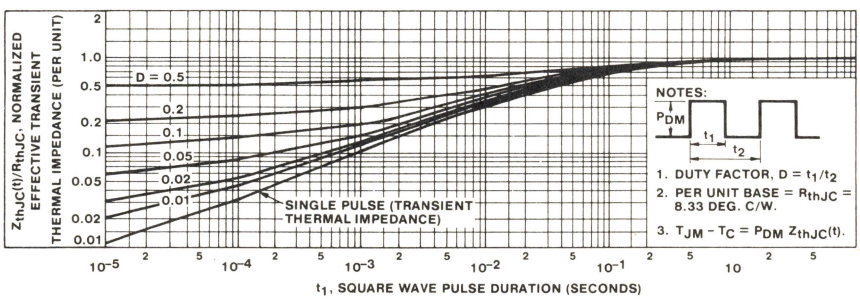


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

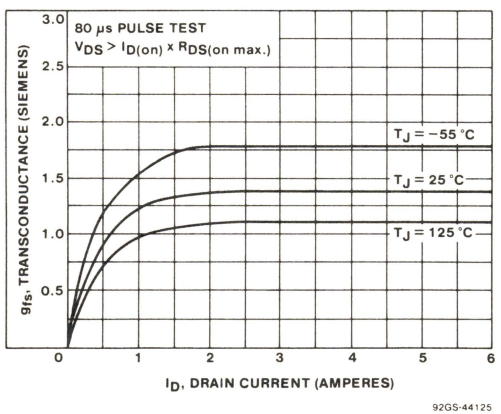


Fig. 6 - Typical transconductance vs. drain current.

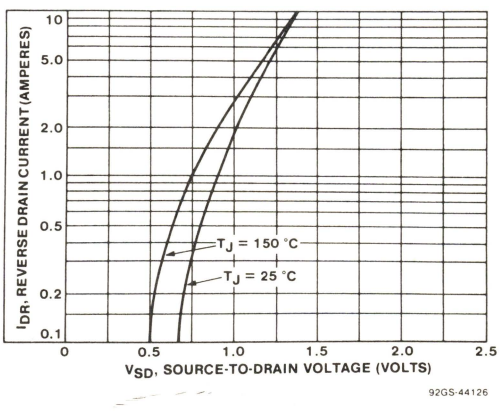


Fig. 7 - Typical source-drain diode forward voltage.

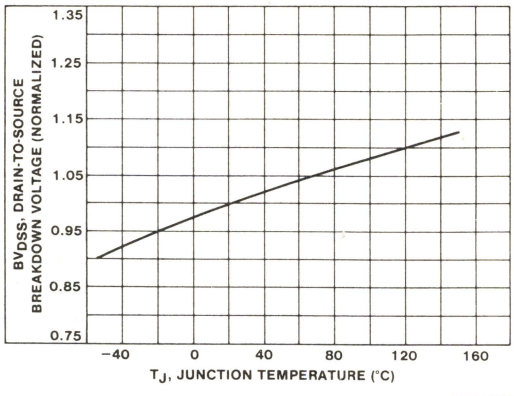


Fig. 8 - Breakdown voltage vs. temperature.

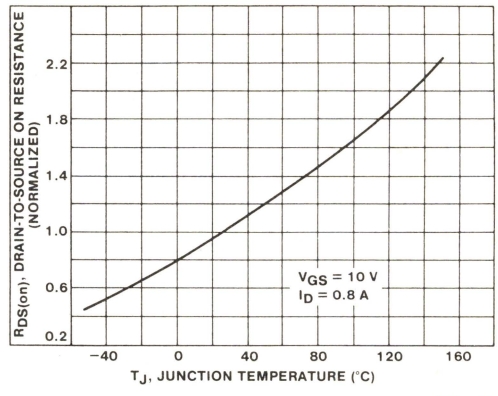


Fig. 9 - Normalized on-resistance vs. temperature.

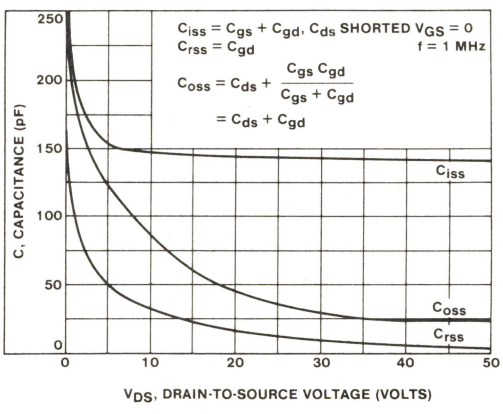


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

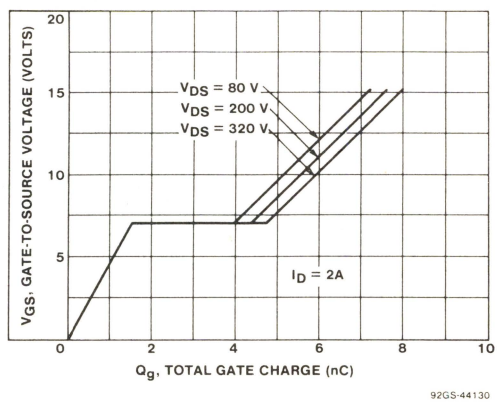


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

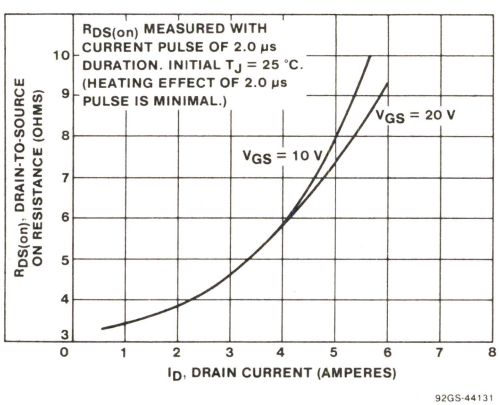


Fig. 12 - Typical on-resistance vs. drain current.

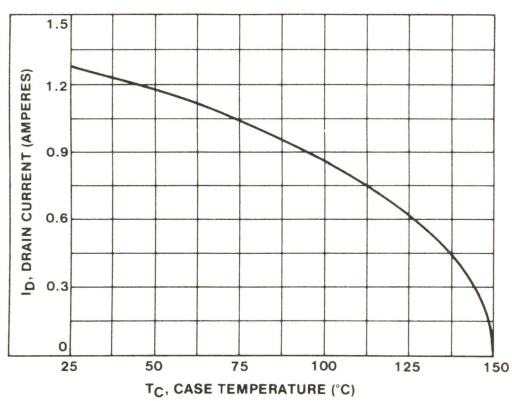


Fig. 13 - Maximum drain current vs. case temperature.

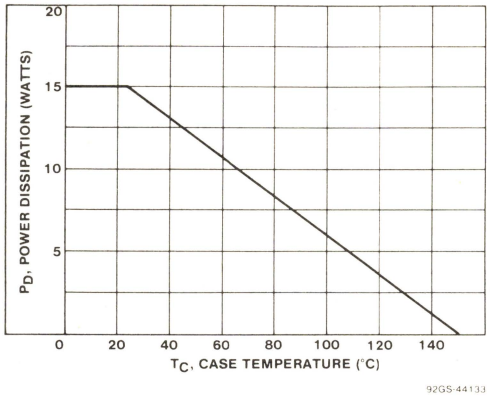
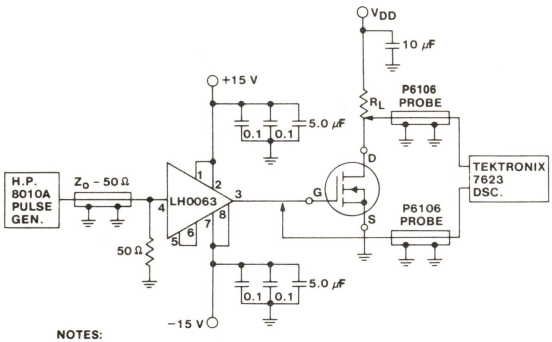


Fig. 14 - Power vs. temperature derating curve.



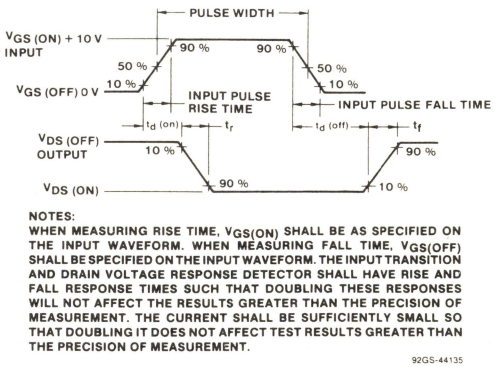
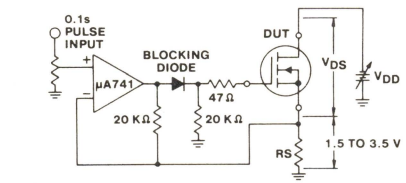


Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1-s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1$ Vdc.

92GS-44136

Fig. 16 - Safe operating test circuit.

HARRIS

2N6788

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 6.0A, 100V
- $r_{DS(on)} = 0.30\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

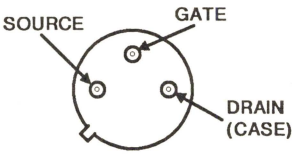
Description

The 2N6788 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6788 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

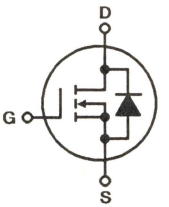
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		2N6788	UNITS
Drain-Source Voltage (Note 1)	V_{DS}	100*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	100*	V
Continuous Drain Current			
$T_C = +25^oC$	I_D	6.0*	A
$T_C = +100^oC$	I_D	3.5*	A
Pulsed Drain Current (Note 2)	I_{DM}	24*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	6.0*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	24*	A
Maximum Power Dissipation			
$T_C = +25^oC$ (See Figure 14)	P_D	20*	W
Linear Derating Factor (See Figure 14)		0.16*	W/^{o}C
Inductive Current, Clamped (L = 100μH)	I_{LM}	24	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	^{o}C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	^{o}C

*JEDEC registered values

NOTES:

1. $T_J = +25^oC$ to $+150^oC$
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1593.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	2.10*	V	V_{GS} = 10V, I_D = 6.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.25	0.30*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 25°C
		–	–	0.54*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.8*	–	1.8*	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.5*	2.9	4.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	200	400*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	50	100*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 35V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	–	–	70*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	70*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 80V, I_D = 250 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 3.3V, I_D = 60A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	C W	
R_{thJA}	Junction-to-Ambient	–	–	175	C W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	230	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.2	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

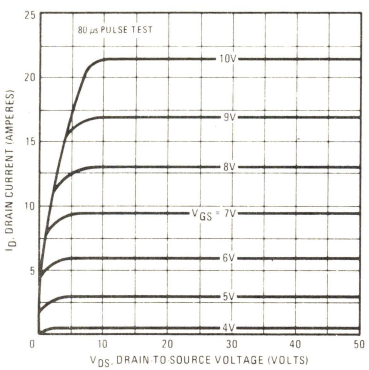


Fig. 1 – Typical Output Characteristics

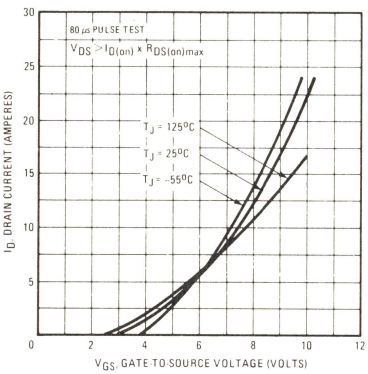


Fig. 2 – Typical Transfer Characteristics

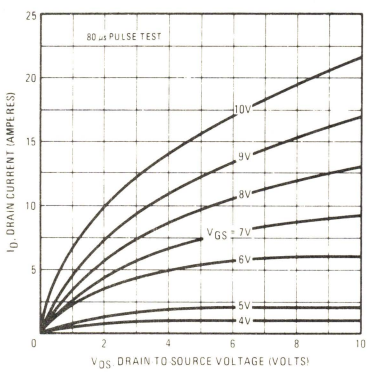


Fig. 3 – Typical Saturation Characteristics

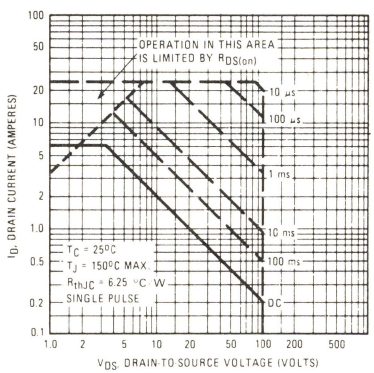


Fig. 4 – Maximum Safe Operating Area

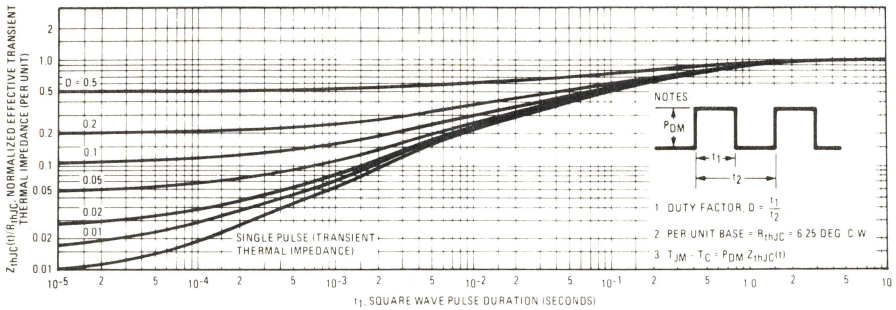


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

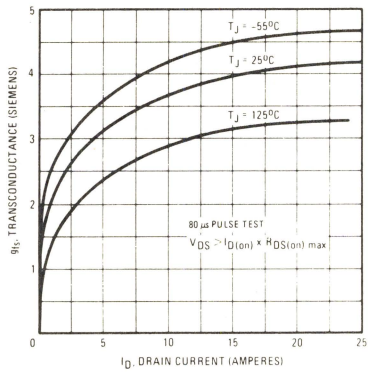


Fig. 6 – Typical Transconductance Vs. Drain Current

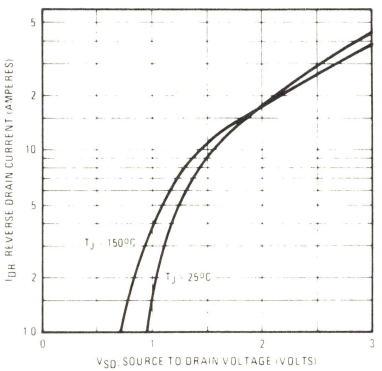


Fig. 7 – Typical Source-Drain Diode Forward Voltage

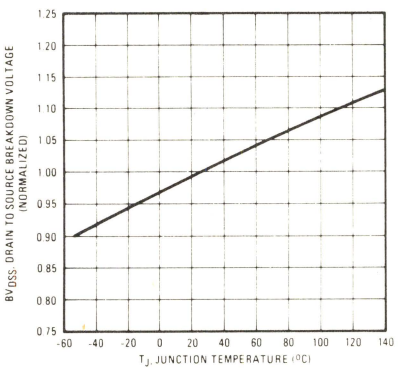


Fig. 8 – Breakdown Voltage Vs. Temperature

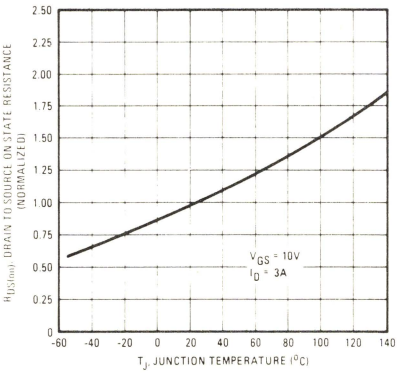


Fig. 9 – Normalized On-Resistance Vs. Temperature

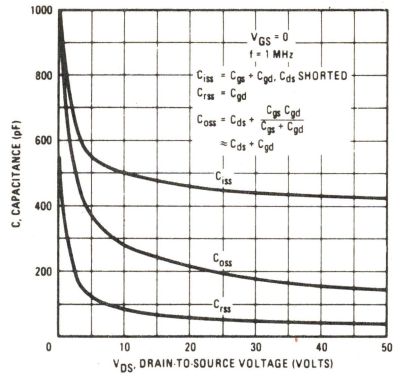


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

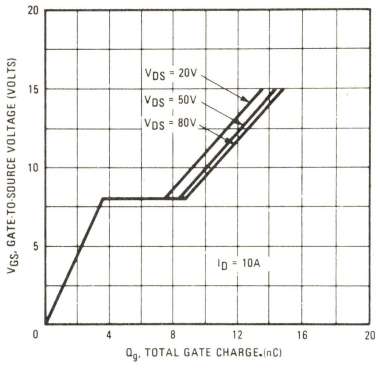


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

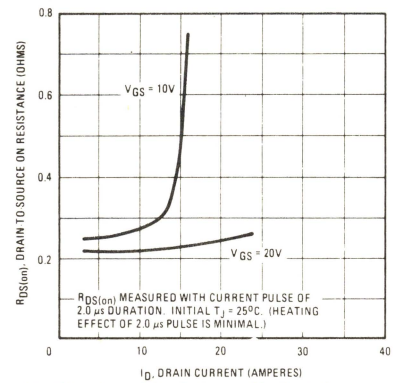


Fig. 12 – Typical On-Resistance Vs. Drain Current

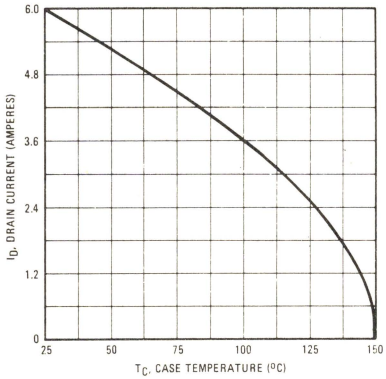


Fig. 13 – Maximum Drain Current Vs. Case Temperature

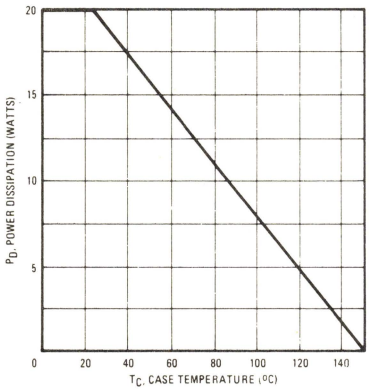
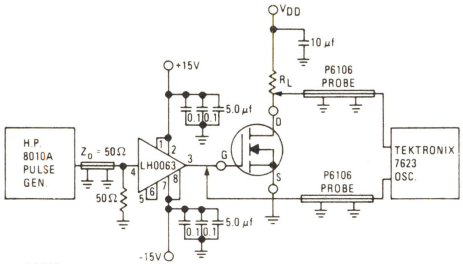
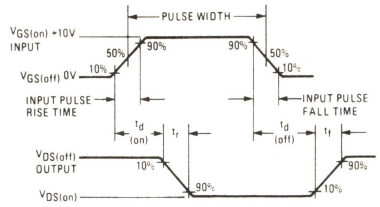


Fig. 14 – Power Vs. Temperature Derating Curve

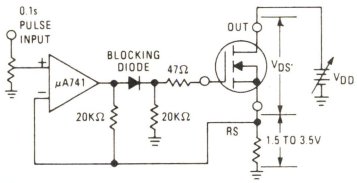


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

HARRIS

2N6790

August 1991

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 3.5A, 200V
- $r_{DS(on)} = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

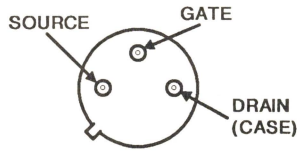
Description

The 2N6790 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6790 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

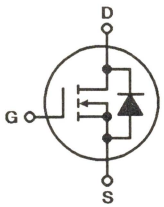
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		2N6790	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	V_{DGR}	200*	V
Continuous Drain Current			
$T_C = +25^oC$	I_D	3.5*	A
$T_C = +100^oC$	I_D	2.25*	A
Pulsed Drain Current	I_{DM}	14*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	3.5*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	14*	A
Maximum Power Dissipation			
$T_C = +25^oC$ (See Figure 14)	P_D	20*	W
Above $T_C = +25^oC$, Derate Linearly (See Figure 14)		0.16*	$W/^oC$
Inductive Current, Clamped (L = 100μH)	I_{LM}	14	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	^oC
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	^oC

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **1900.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	—	—	2.8*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	—	0.50	0.80*	Ω	V_{GS} = 10V, I_D = 2.25A, T_A = 25°C
		—	—	1.50*	Ω	V_{GS} = 10V, I_D = 2.25A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.7*	—	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.5*	2.25	4.5*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	60*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	15*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	40*	ns	V_{DD} ≅ 74V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	—	—	50*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	50*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	50*	ns	of operating temperature.)
SOA	Safe Operating Area	20	—	—	W	V_{DS} = 160V, I_D = 125 mA, See Fig. 16.
		20	—	—	W	V_{DS} = 5.7V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	350	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	2.3	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

aPulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

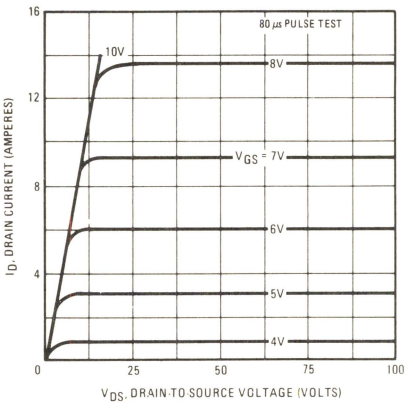


Fig. 1 - Typical output characteristics.

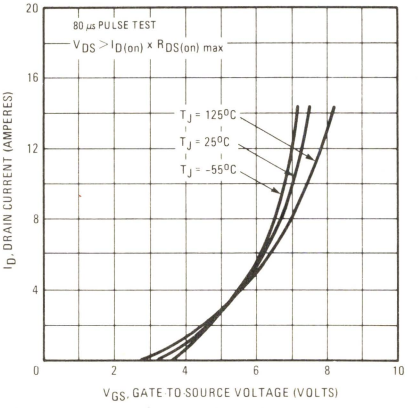


Fig. 2 - Typical transfer characteristics.

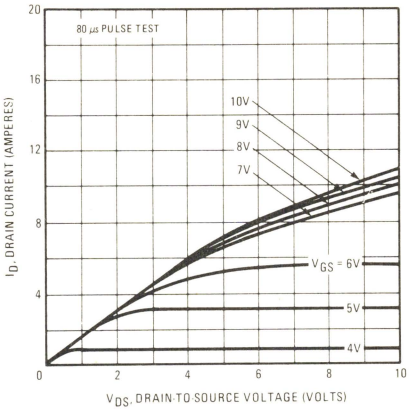


Fig. 3 - Typical saturation characteristics.

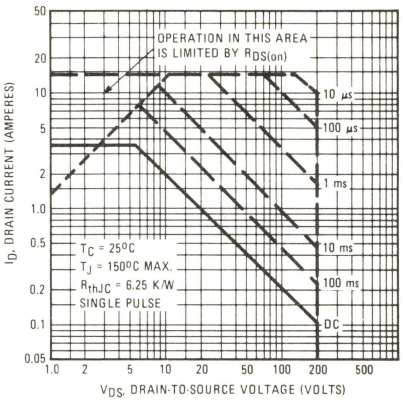


Fig. 4 - Maximum safe operating area.

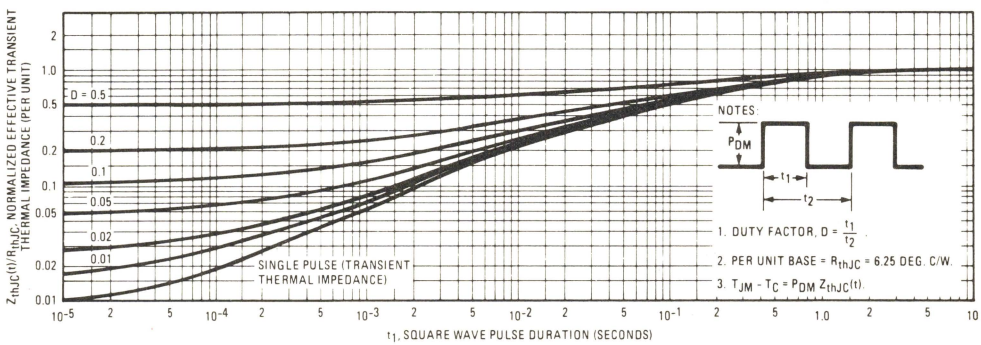


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

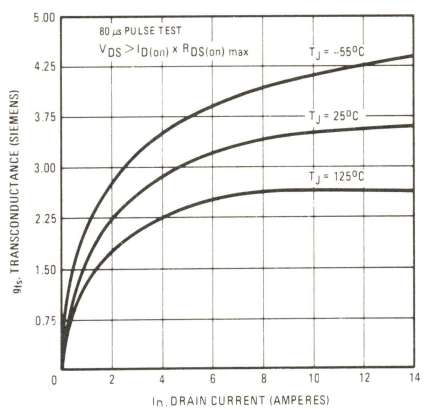


Fig. 6 - Typical transconductance versus drain current.

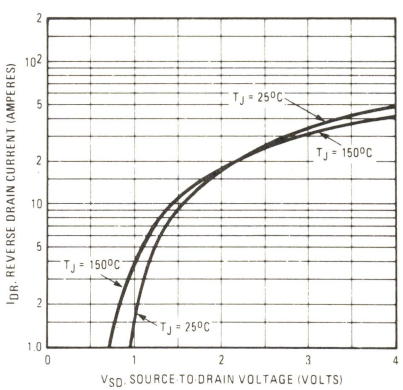


Fig. 7 - Typical source-drain diode forward voltage.

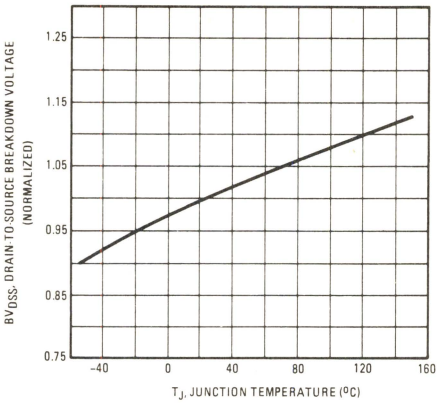


Fig. 8 - Breakdown voltage versus temperature.

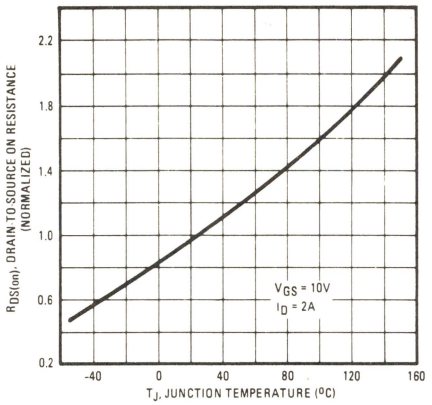


Fig. 9 - Typical normalized on-resistance versus temperature.

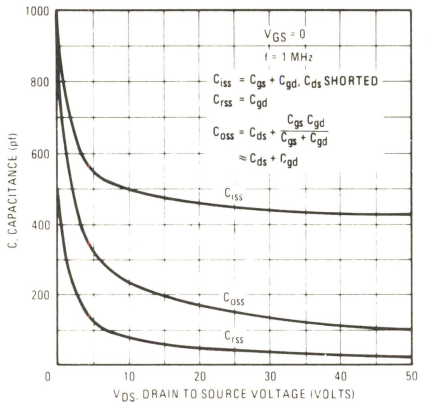


Fig. 10 - Typical capacitance versus drain-to-source voltage.

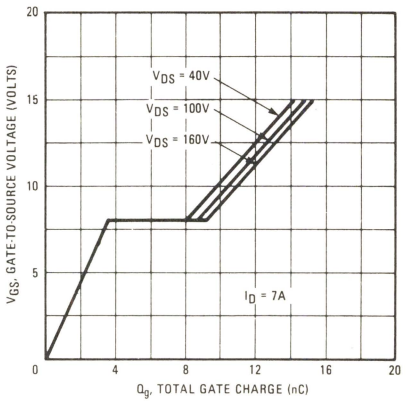


Fig. 11 - Typical gate charge versus gate-to-source voltage.

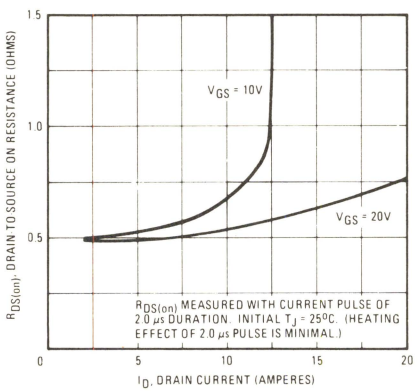


Fig. 12 - Typical on-resistance versus drain current.

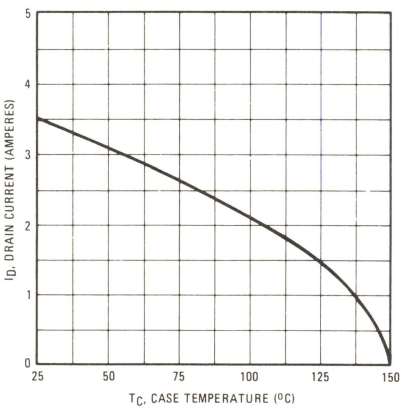


Fig. 13 - Maximum drain current versus case temperature.

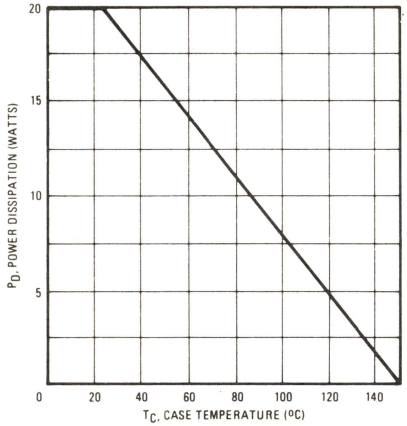
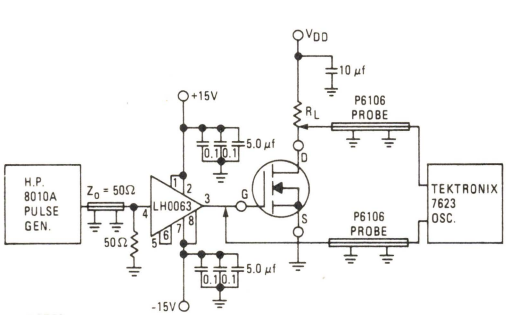


Fig. 14 - Power versus temperature derating curve.



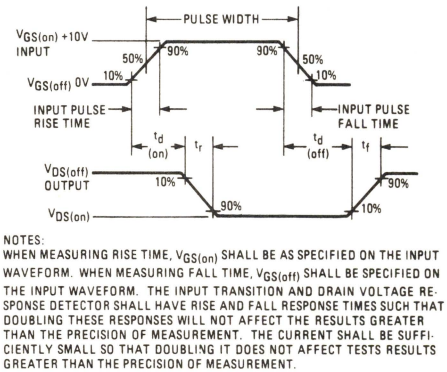
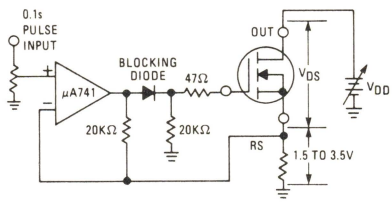


Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating area test circuit.

HARRIS

2N6792

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 2A, 400V
- $r_{DS(on)} = 1.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

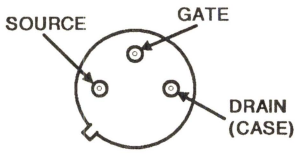
Description

The 2N6792 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6792 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

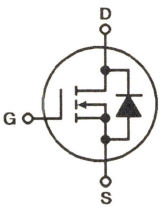
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6792	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	2*	A
T_C = +100°C	I_D	1.25*	A
Pulsed Drain Current	I_{DM}	10*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	2*	A
Pulse Source Current	I_{SM}	10*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	20*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.16*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	10	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1901.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage [a]	—	—	3.6*	V	V_{GS} = 10V, I_D = 2.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance [a]	—	1.50	1.80*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 25°C
		—	—	4.00*	Ω	V_{GS} = 10V, I_D = 1.25A, T_A = 125°C
V_{SD}	Diode Forward Voltage [a]	0.6*	—	1.4*	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance [a]	1.0*	2.0	3.0*	S(℧)	V_{DS} = 5V, I_D = 1.25A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	20	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	40*	ns	V_{DD} ≅ 175V, I_D = 1.25A, Z_o = 50Ω
t_r	Rise Time	—	—	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	60*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	35*	ns	of operating temperature.)
SOA	Safe Operating Area	20	—	—	W	V_{DS} = 200V, I_D = 100 mA, See Fig. 16.
		20	—	—	W	V_{DS} = 10V, I_D = 2.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	450	ns	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.1	μC	T_J = 150°C, I_F = 2.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

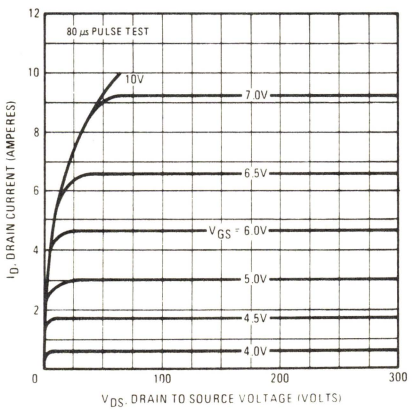


Fig. 1 - Typical output characteristics.

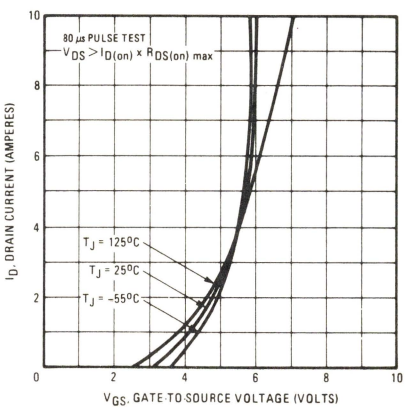


Fig. 2 - Typical transfer characteristics.

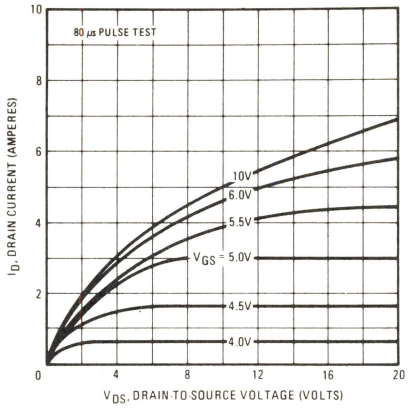


Fig. 3 - Typical saturation characteristics.

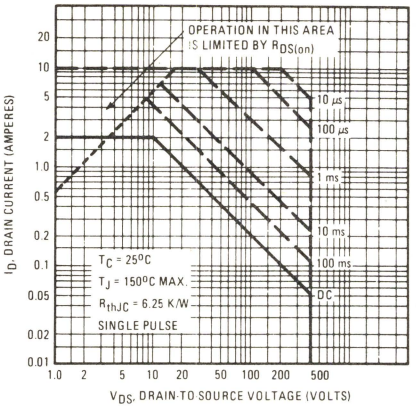


Fig. 4 - Maximum safe operating area.

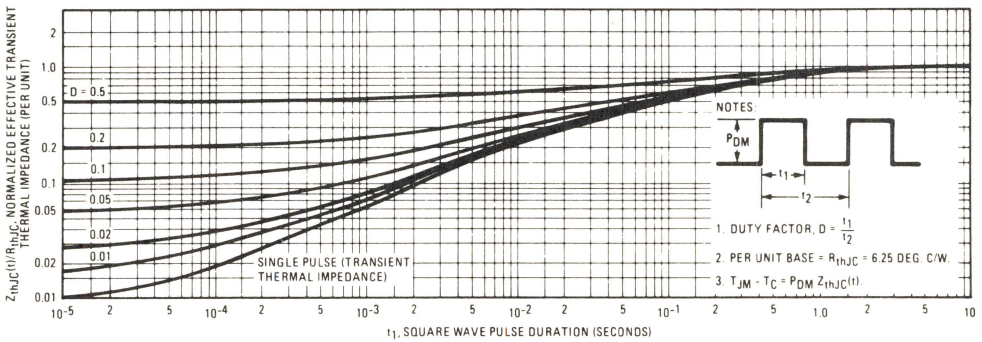


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

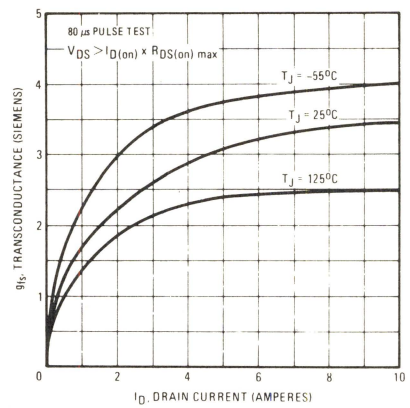


Fig. 6 - Typical transconductance versus drain current.

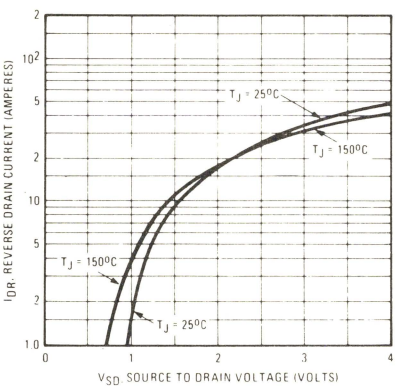


Fig. 7 - Typical source-drain diode forward voltage.

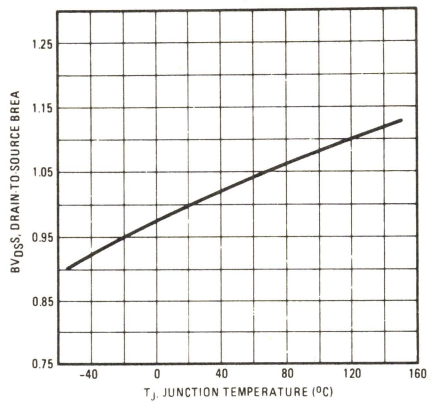


Fig. 8 - Breakdown voltage versus temperature.

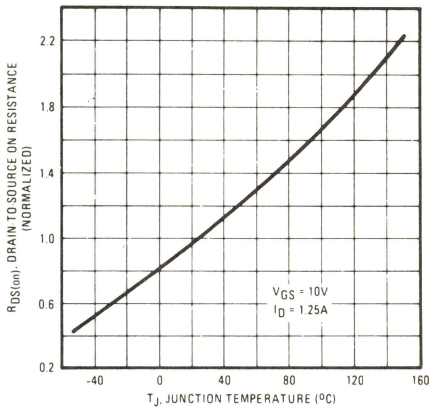


Fig. 9 - Typical normalized on-resistance versus. temperature.

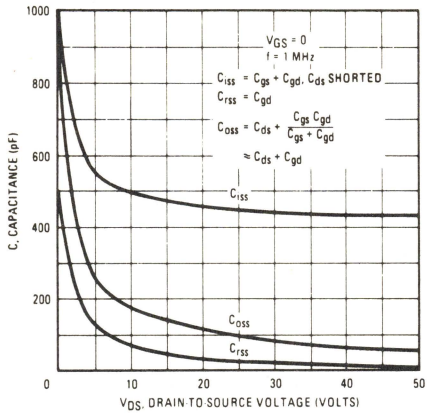


Fig. 10 - Typical capacitance versus drain-to-source. voltage.

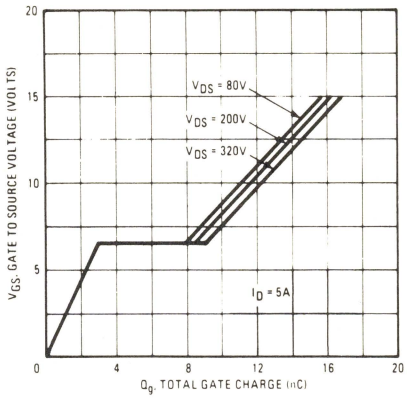


Fig. 11 - Typical gate charge versus gate-to-source. voltage.

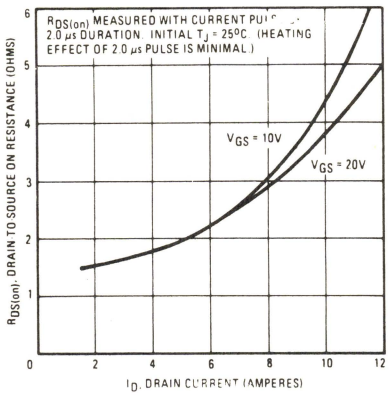


Fig. 12 - Typical on-resistance versus drain current.

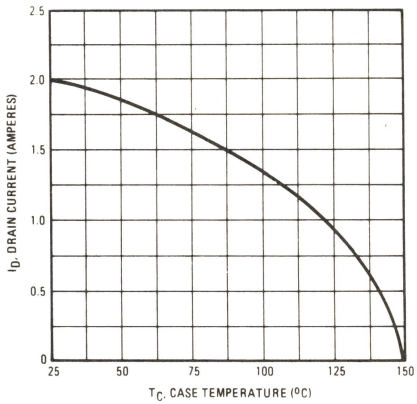


Fig. 13 - Maximum drain current versus case. temperature.

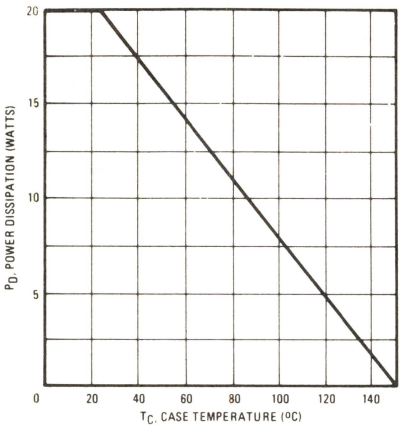
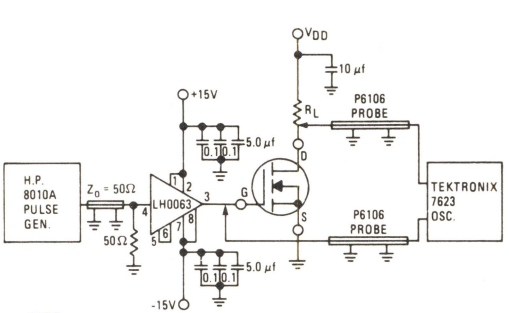
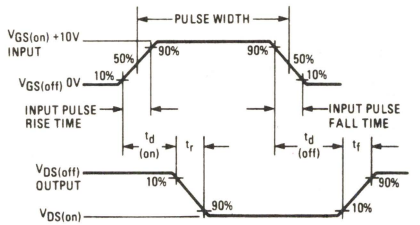


Fig. 14 - Power versus temperature derating curve.

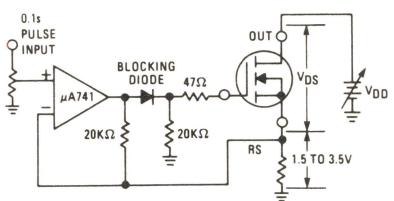


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating area test circuit.

HARRIS

2N6794

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 1.5A, 500V
- $r_{DS(on)} = 3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

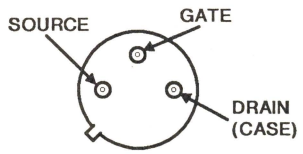
Description

The 2N6794 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6794 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

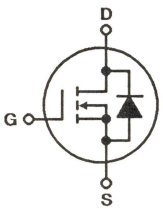
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6794	UNITS
Drain-Source Voltage	V_{DS}	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500*	V
Continuous Drain Current			
T_C = +25°C	I_D	1.5*	A
T_C = +100°C	I_D	1*	A
Pulsed Drain Current	I_{DM}	6.5*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	1.5*	A
Pulse Source Current	I_{SM}	6.5*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	20*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.16*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	6.5	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1902.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	500*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 500V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	4.5*	V	V_{GS} = 10V, I_D = 1.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	2.5	3.0*	Ω	V_{GS} = 10V, I_D = 1.0A, T_A = 25°C
		–	–	6.6*	Ω	V_{GS} = 10V, I_D = 1.0A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.6*	–	1.2*	V	T_C = 25°C, I_S = 1.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.0*	1.75	3.0*	S(℧)	V_{DS} = 5V, I_D = 1.00A
C_{iss}	Input Capacitance	200*	300	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	30*	75	150*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	5.0*	20	40*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	40*	ns	V_{DD} ≅ 225V, I_D = 1.0A, Z_o = 50Ω
t_r	Rise Time	–	–	30*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	60*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	30*	ns	of operating temperature.)
SOA	Safe Operating Area	20	–	–	W	V_{DS} = 200V, I_D = 100 mA, See Fig. 16.
		20	–	–	W	V_{DS} = 13.3V, I_D = 1.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	600	ns	T_J = 150°C, I_F = 1.50A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.5	μC	T_J = 150°C, I_F = 1.50A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

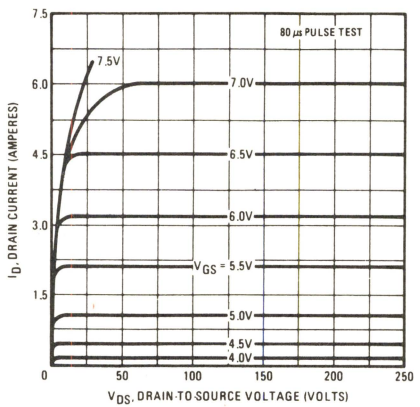


Fig. 1 - Typical output characteristics.

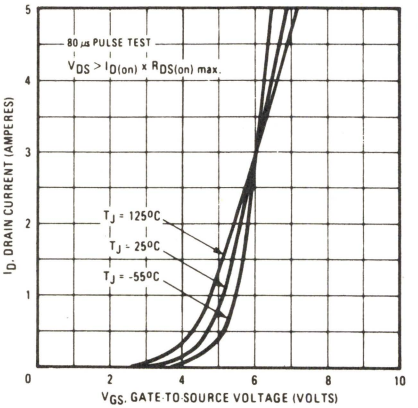


Fig. 2 - Typical transfer characteristics.

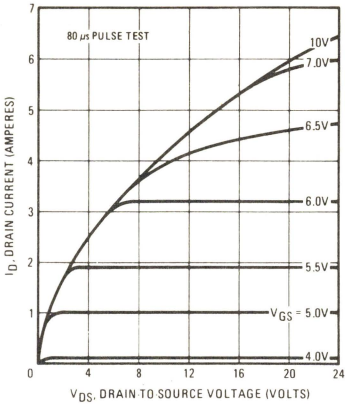


Fig. 3 - Typical saturation characteristics.

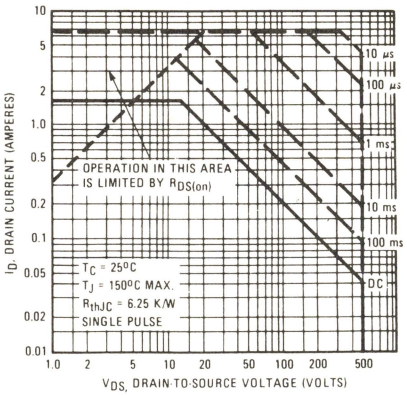


Fig. 4 - Maximum safe operating area.

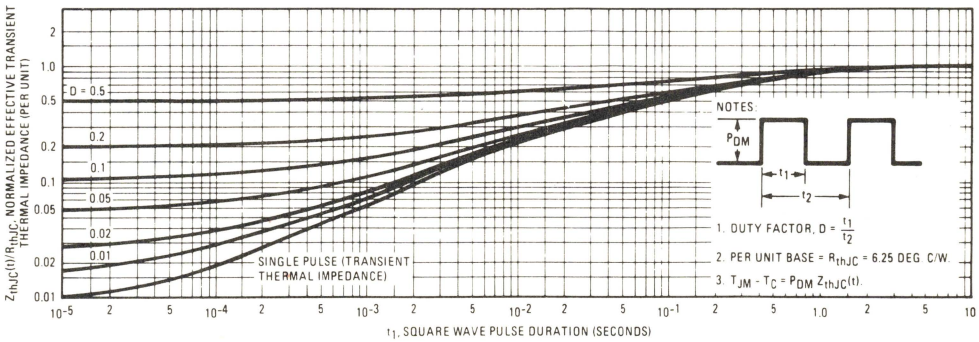


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

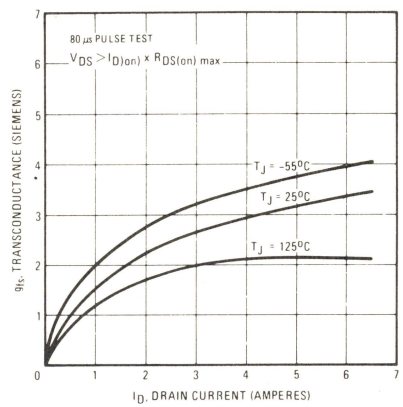


Fig. 6 - Typical transconductance versus drain current.

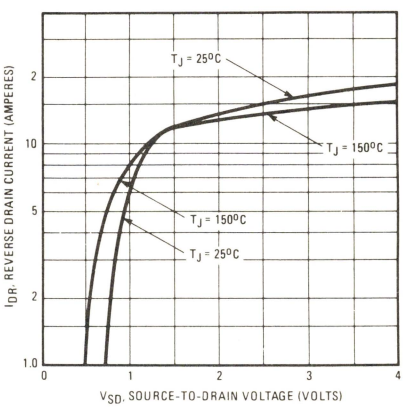


Fig. 7 - Typical source-drain diode forward voltage.

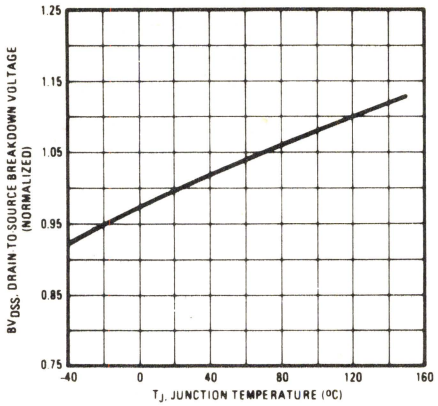


Fig. 8 - Breakdown voltage versus temperature.

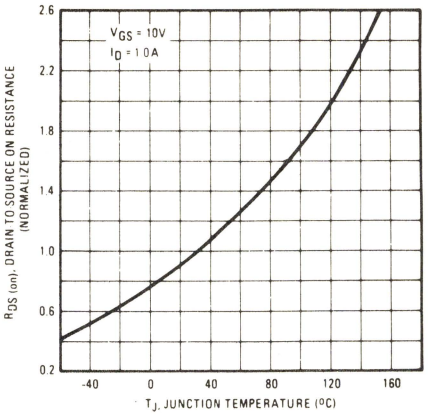


Fig. 9 - Typical normalized on-resistance versus temperature.

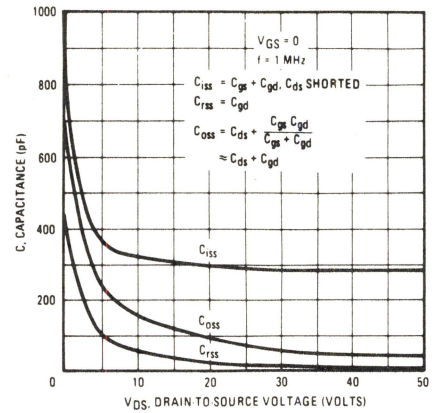


Fig. 10 - Typical capacitance versus drain-to-source voltage.

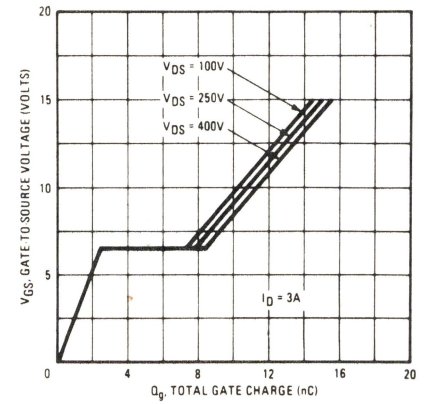


Fig. 11 - Typical gate charge versus gate-to-source voltage.

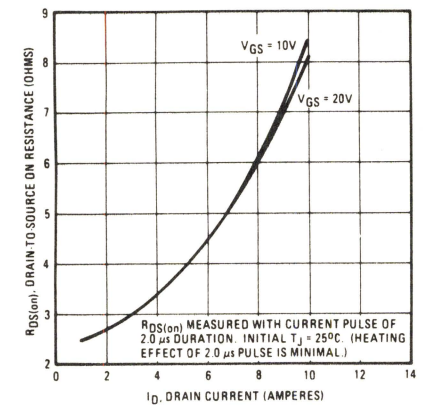


Fig. 12 - Typical on-resistance versus drain current.

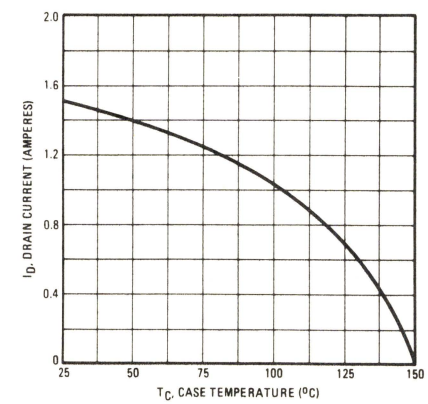


Fig. 13 - Maximum drain current versus case temperature.

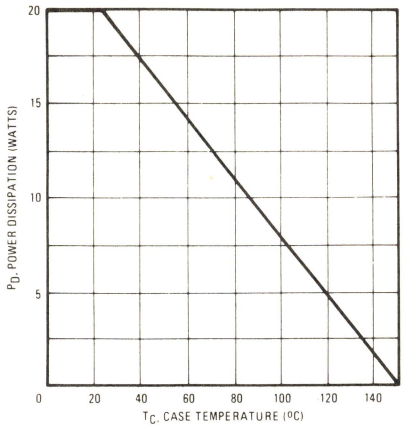
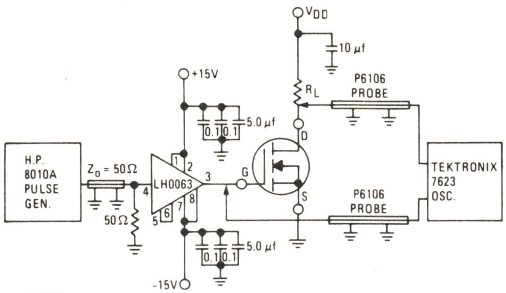
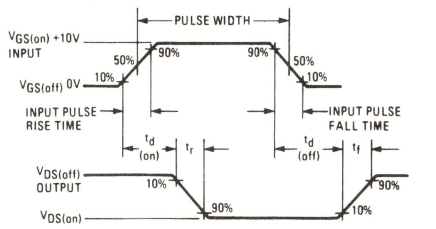


Fig. 14 - Power versus temperature derating curve.

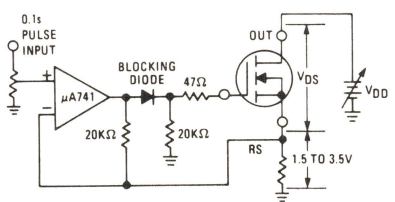


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6796

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 8.0A, 100V
- $r_{DS(on)}$ = 0.18Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

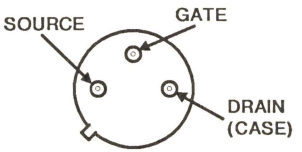
Description

The 2N6796 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6796 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

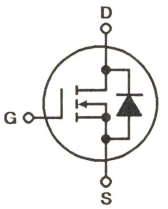
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6796	UNITS
Drain-Source Voltage (Note 1)	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	8.0*	A
T_C = +100°C	I_D	5.0*	A
Pulsed Drain Current (Note 2)	I_{DM}	32*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current (Body Diode)	I_S	8.0*	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}	32*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Linear Derating Factor (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	32	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

NOTES:

1. T_J = +25°C to +150°C
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1594.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	1.56*	V	V_{GS} = 10V, I_D = 8.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 25°C
		–	–	0.35*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	3.0*	5.5	9.0*	S(℧)	V_{DS} = 5V, I_D = 5.0A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	150*	300	500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 30V, I_D = 5.0A, Z_o = 50Ω
t_r	Rise Time	–	–	75*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	45*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 80V, I_D = 310 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 3.12V, I_D = 8.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	300	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.5	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

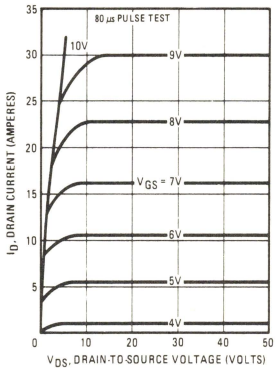


Fig. 1 – Typical Output Characteristics

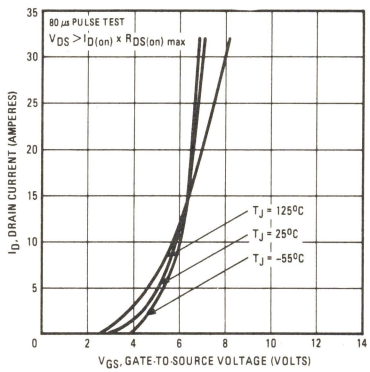


Fig. 2 – Typical Transfer Characteristics

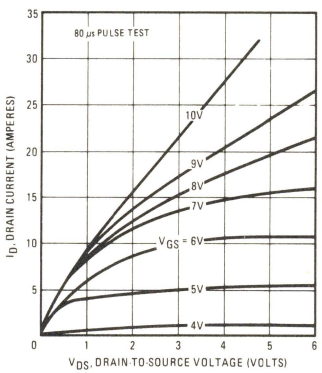


Fig. 3 – Typical Saturation Characteristics

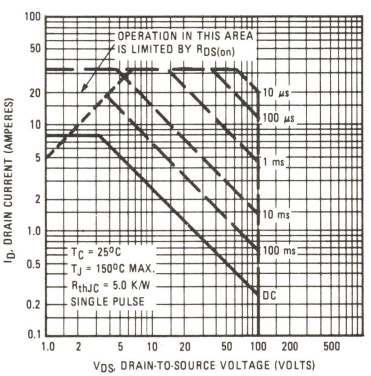


Fig. 4 – Maximum Safe Operating Area

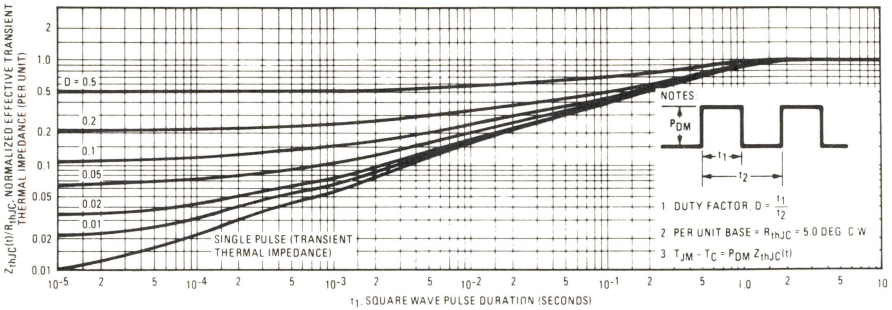


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

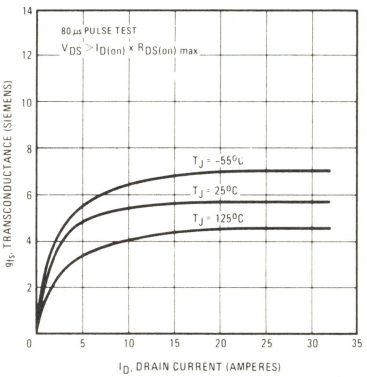


Fig. 6 – Typical Transconductance Vs. Drain Current

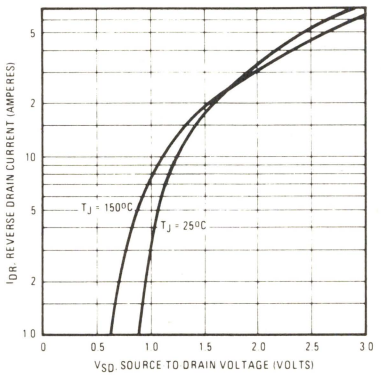


Fig. 7 – Typical Source-Drain Diode Forward Voltage

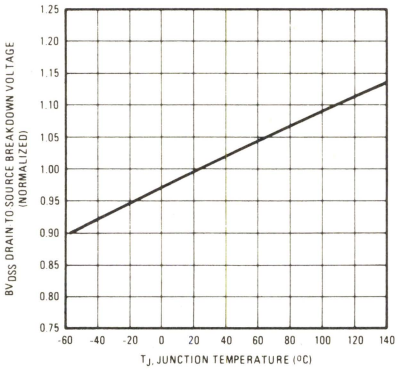


Fig. 8 – Breakdown Voltage Vs. Temperature

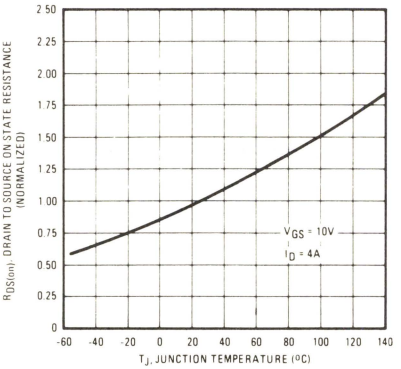


Fig. 9 – Normalized On-Resistance Vs. Temperature

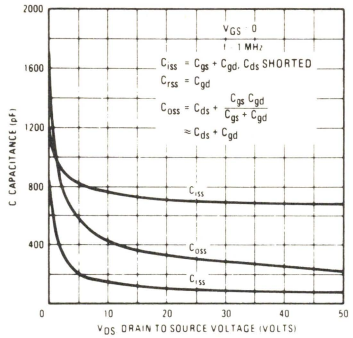


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

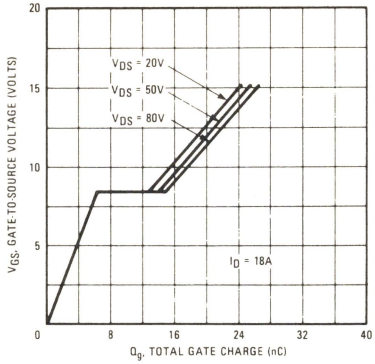


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

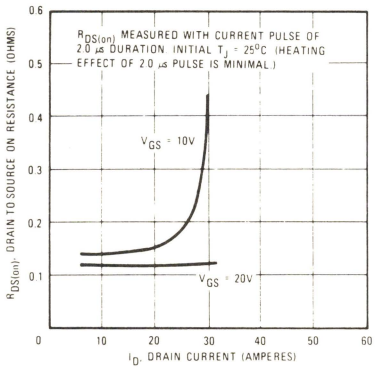


Fig. 12 – Typical On-Resistance Vs. Drain Current

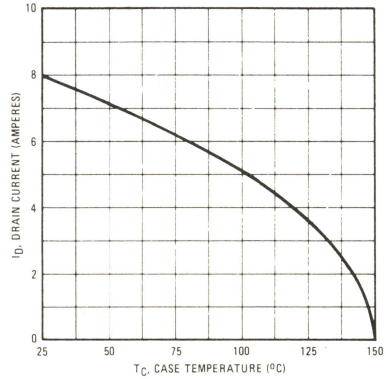


Fig. 13 – Maximum Drain Current Vs. Case Temperature

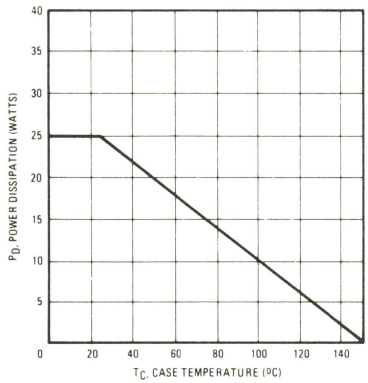
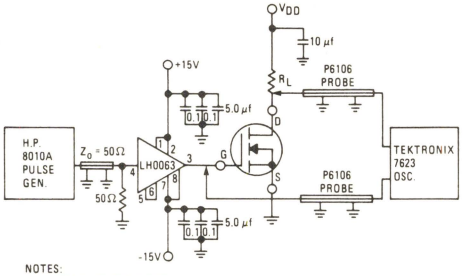
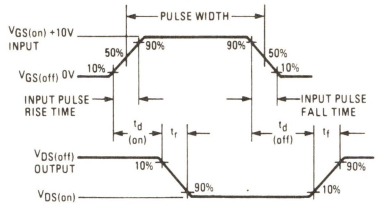


Fig. 14 – Power Vs. Temperature Derating Curve

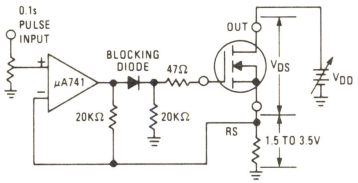


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

HARRIS

2N6798

August 1991

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 5.5A, 200V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

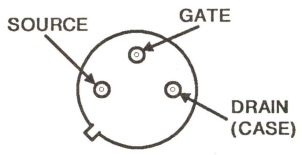
Description

The 2N6798 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6798 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

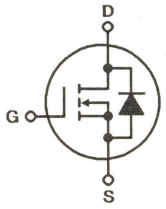
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6798	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200*	V
Continuous Drain Current			
T_C = +25°C	I_D	5.5*	A
T_C = +100°C	I_D	3.5*	A
Pulsed Drain Current	I_{DM}	22*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	5.5*	A
Pulse Source Current	I_{SM}	22*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	22	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1903.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	200*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 200V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 160V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	—	—	2.20*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	—	0.25	0.4*	Ω	V_{GS} = 10V, I_D = 3.5A, T_A = 25°C
		—	—	0.75*	Ω	V_{GS} = 10V, I_D = 3.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	—	1.4*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	2.5*	4.5	7.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	250	450*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30*	ns	$V_{DD} \cong$ 77V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	—	—	50*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	50*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	40*	ns	of operating temperature.)
SOA	Safe Operating Area	25	—	—	W	V_{DS} = 160V, I_D = 155 mA, See Fig. 16.
		25	—	—	W	V_{DS} = 4.5V, I_D = 5.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	450	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	3.0	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ⩽ 300μs, Duty Cycle ⩽ 2%.

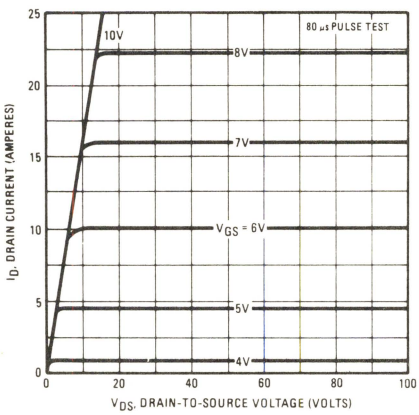


Fig. 1 - Typical output characteristics.

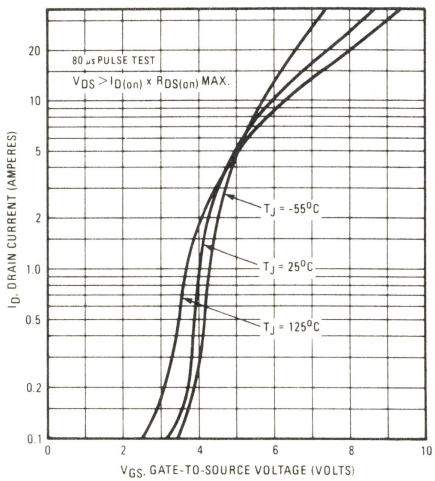


Fig. 2 - Typical transfer characteristics.

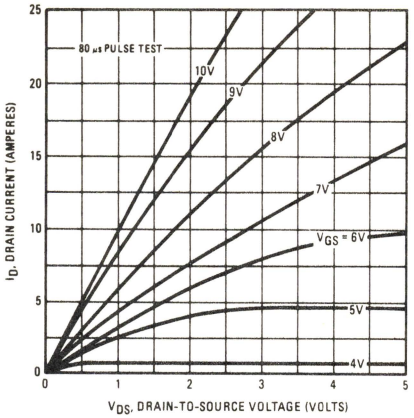


Fig. 3 - Typical saturation characteristics.

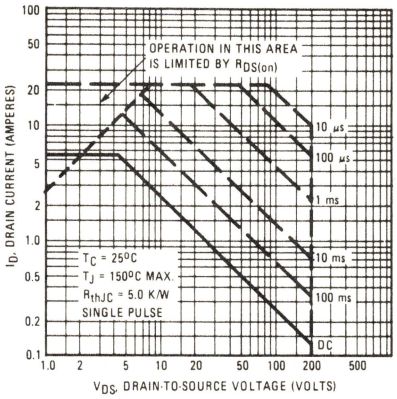


Fig. 4 - Maximum safe operating area.

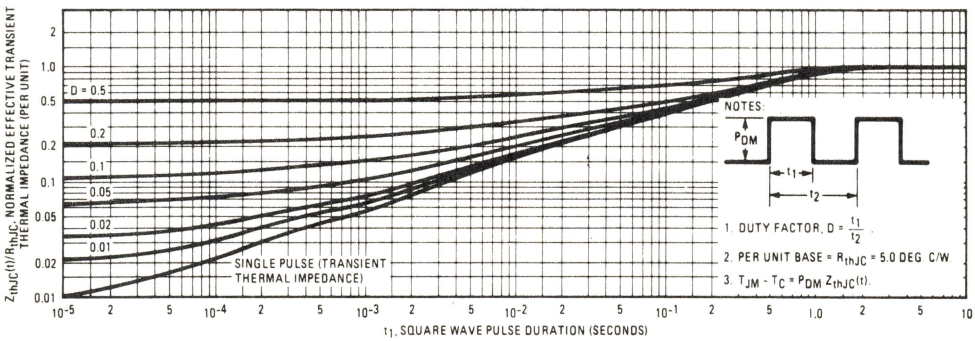


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

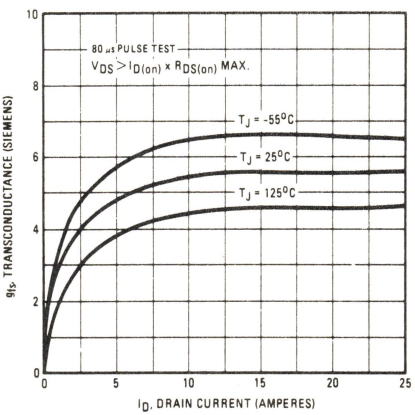


Fig. 6 - Typical transconductance versus drain current.

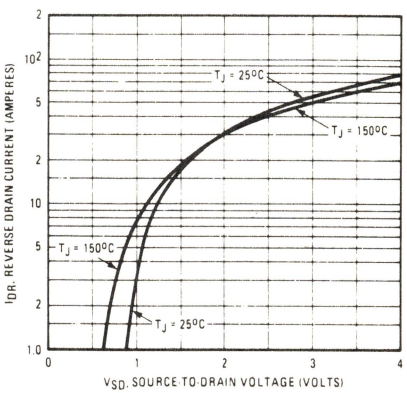


Fig. 7 - Typical source-drain diode forward voltage.

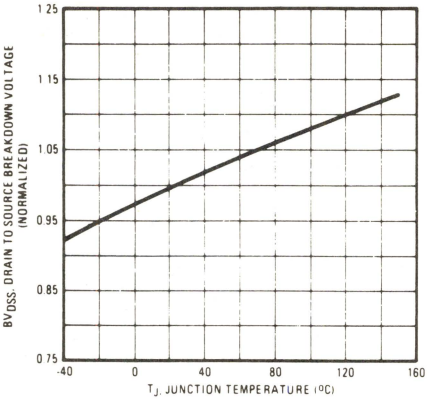


Fig. 8 - Breakdown voltage versus temperature.

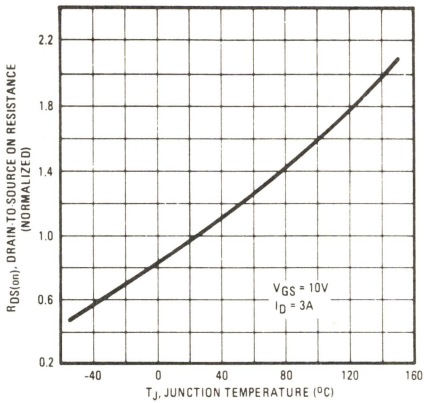


Fig. 9 - Typical normalized on-resistance versus temperature.

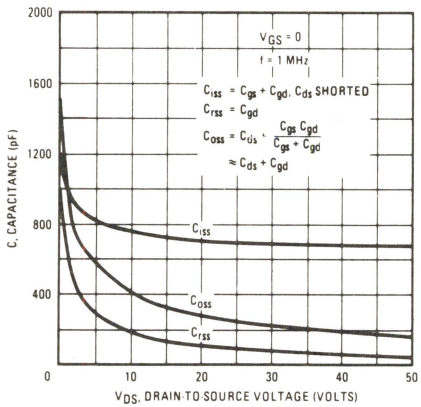


Fig. 10 - Typical capacitance versus drain-to-source voltage.

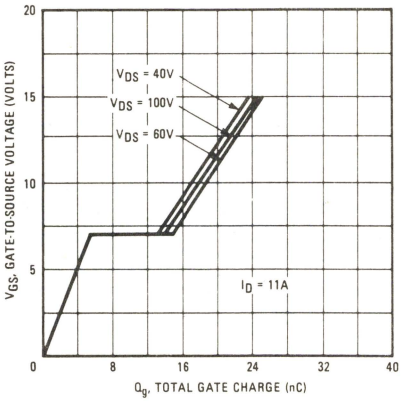


Fig. 11 - Typical gate charge versus gate-to-source voltage.

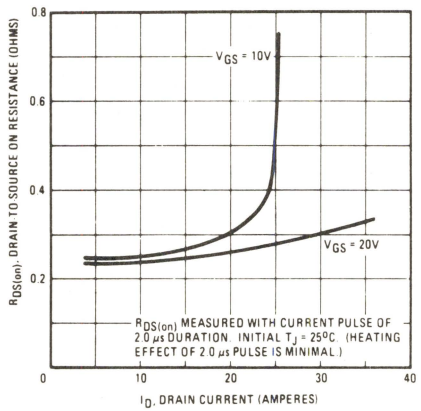


Fig. 12 - Typical on-resistance versus drain current.

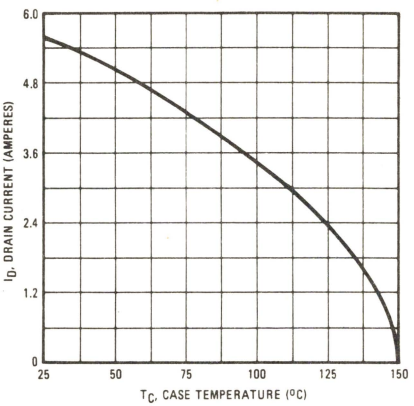


Fig. 13 - Maximum drain current versus case temperature.

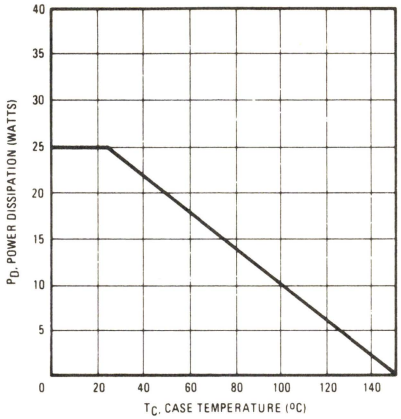
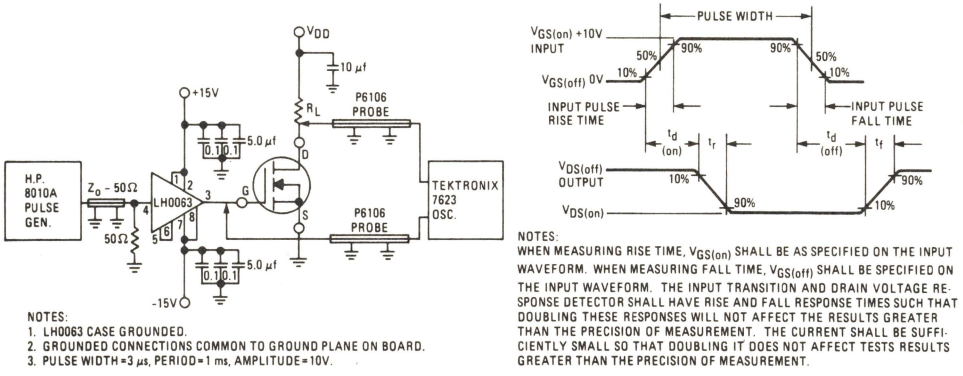


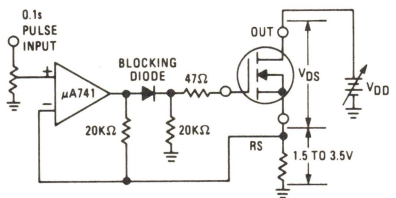
Fig. 14 - Power versus temperature derating curve.



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.

NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6800

August 1991

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

Features

- 3A, 400V
- $r_{DS(on)} = 1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

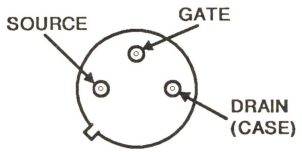
Description

The 2N6800 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6800 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

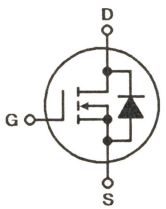
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6800	UNITS
Drain-Source Voltage	V_{DS}	400*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400*	V
Continuous Drain Current			
T_C = +25°C	I_D	3*	A
T_C = +100°C	I_D	2*	A
Pulsed Drain Current	I_{DM}	14*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	3*	A
Pulse Source Current	I_{SM}	14*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	14	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1904.1**

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	400*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 400V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 320V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	–	–	3.0*	V	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 25°C
		–	–	2.4*	Ω	V_{GS} = 10V, I_D = 2.0A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	–	1.4*	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	2.0*	3.5	6.0*	S(℧)	V_{DS} = 5V, I_D = 2.0A
C_{iss}	Input Capacitance	350*	700	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	50*	150	300*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 176V, I_D = 2.0A, Z_o = 50Ω
t_r	Rise Time	–	–	35*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	55*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	35*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 8.3V, I_D = 3.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	600	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	4.0	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a] Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

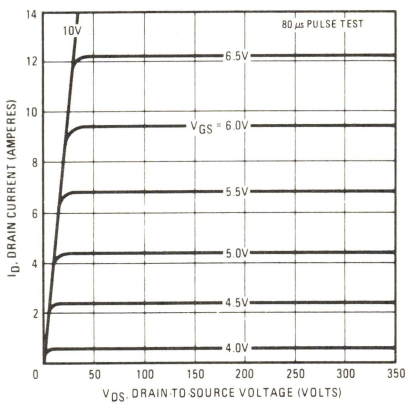


Fig. 1 - Typical output characteristics.

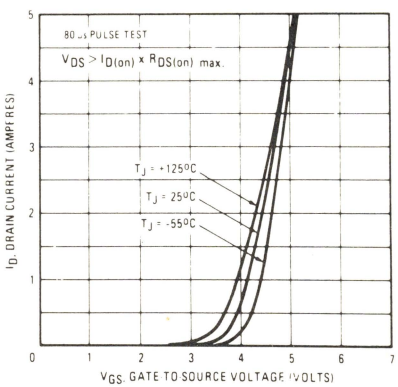


Fig. 2 - Typical transfer characteristics.

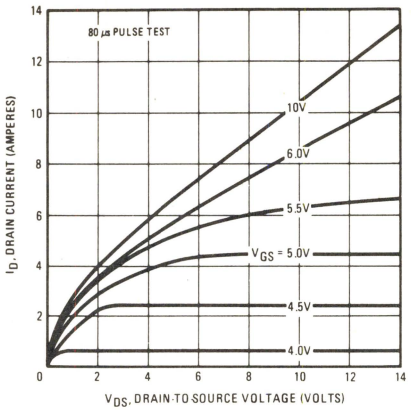


Fig. 3 - Typical saturation characteristics.

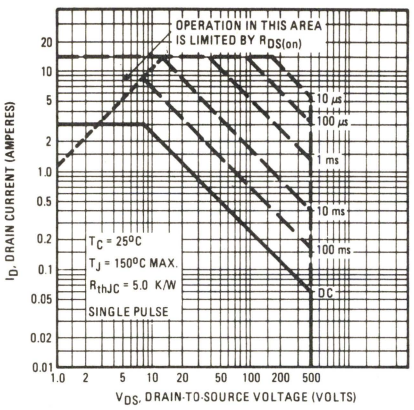


Fig. 4 - Maximum safe operating area.

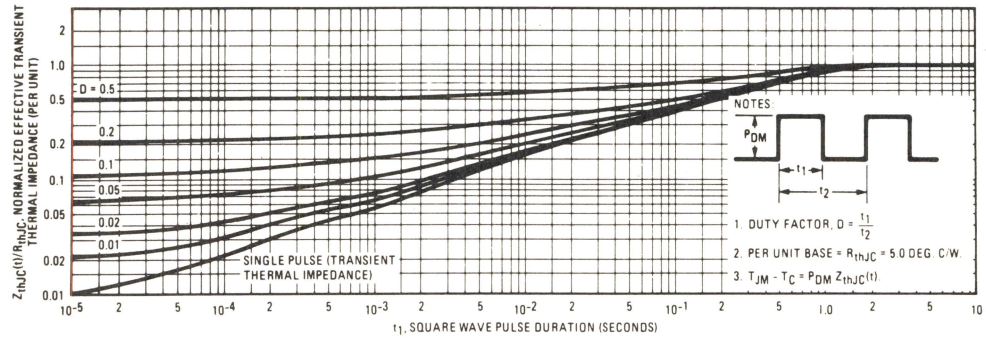


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

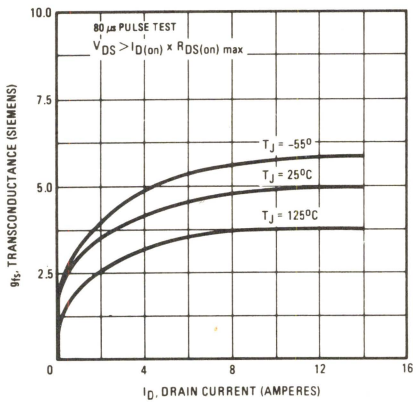


Fig. 6 - Typical transconductance versus drain current.

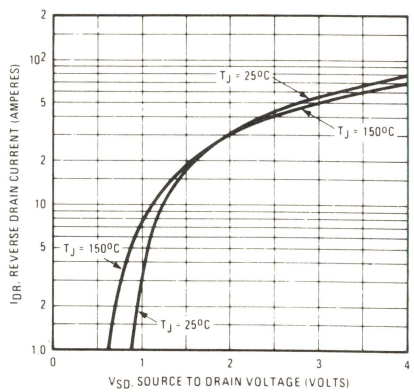


Fig. 7 - Typical source-drain diode forward voltage.

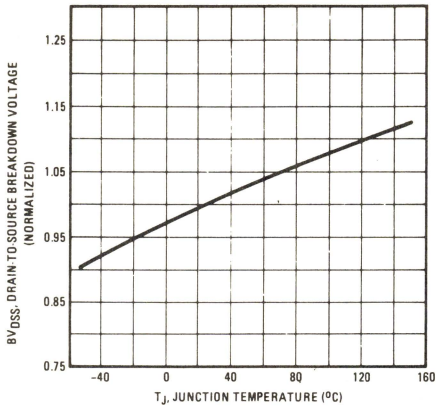


Fig. 8 - Breakdown voltage versus temperature.

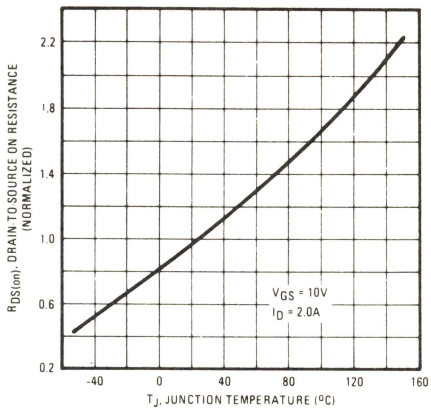


Fig. 9 - Typical normalized on-resistance versus temperature.

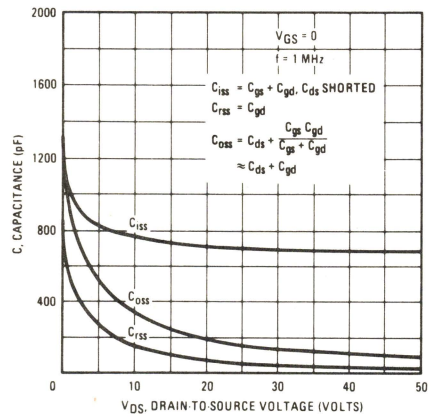


Fig. 10 - Typical capacitance versus drain-to-source voltage.

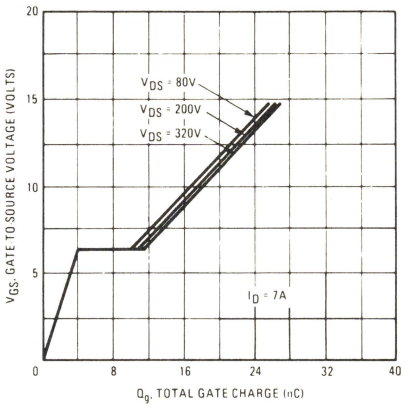


Fig. 11 - Typical gate charge versus gate-to-source voltage.

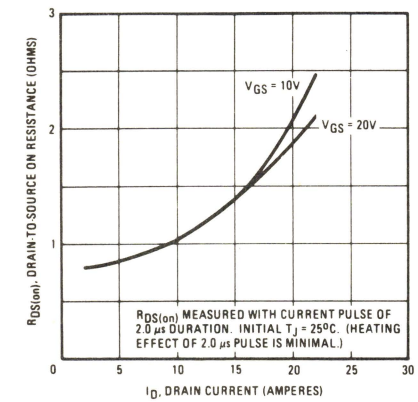


Fig. 12 - Typical on-resistance versus drain current.

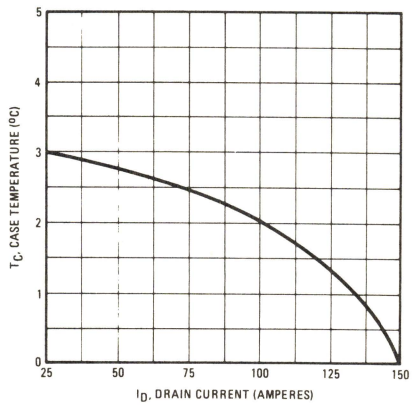


Fig. 13 - Maximum drain current versus case temperature.

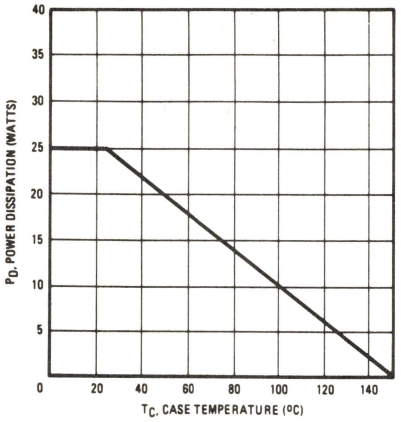
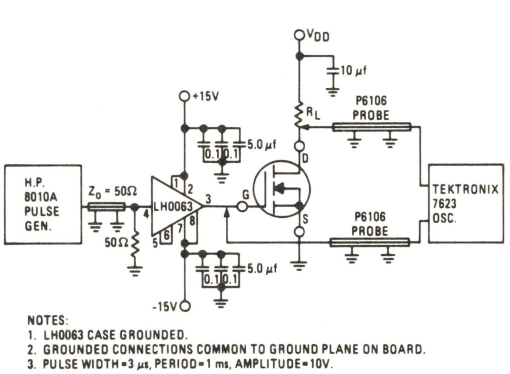
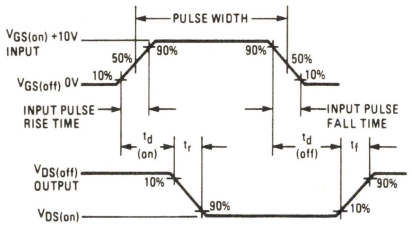


Fig. 14 - Power versus temperature derating curve.

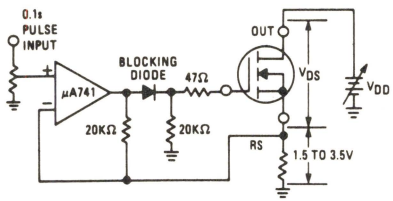


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

2N6802

N-Channel Enhancement-Mode Power MOS Field-Effect Transistor

August 1991

Features

- 3.5A, 500V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

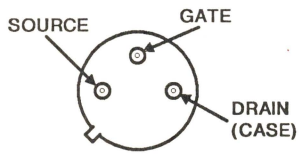
Description

The 2N6802 is an n-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The 2N6802 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

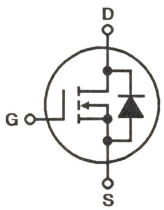
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6802	UNITS
Drain-Source Voltage	V_{DS}	500*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500*	V
Continuous Drain Current			
T_C = +25°C	I_D	3.5*	A
T_C = +100°C	I_D	1.5*	A
Pulsed Drain Current	I_{DM}	11*	A
Gate-Source Voltage	V_{GS}	±20*	V
Continuous Source Current	I_S	2.5*	A
Pulse Source Current	I_{SM}	11*	A
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.20*	W/°C
Inductive Current, Clamped (L = 100μH)	I_{LM}	11	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1905.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	500*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 500V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage[a]	—	—	3.75*	V	V_{GS} = 10V, I_D = 2.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance[a]	—	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 25°C
		—	—	3.5*	Ω	V_{GS} = 10V, I_D = 1.5A, T_A = 125°C
V_{SD}	Diode Forward Voltage[a]	0.70*	—	1.4*	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance[a]	1.5*	2.5	4.5*	S(℧)	V_{DS} = 5V, I_D = 1.5A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	25*	100	200*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	15*	30	60*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	30*	ns	$V_{DD} \cong$ 225V, I_D = 1.5A, Z_o = 50Ω
t_r	Rise Time	—	—	30*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	55*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	30*	ns	of operating temperature.)
SOA	Safe Operating Area	25	—	—	W	V_{DS} = 200V, I_D = 125 mA, See Fig. 16.
		25	—	—	W	V_{DS} = 10V, I_D = 2.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	800	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	4.6	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

*JEDEC registered value

[a]Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

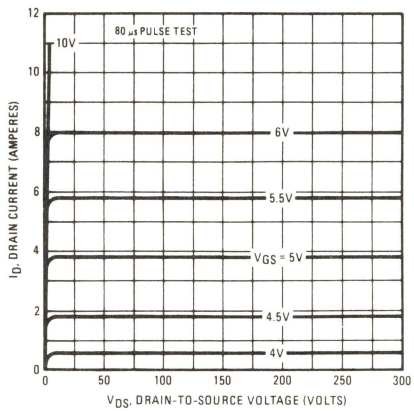


Fig. 1 - Typical output characteristics.

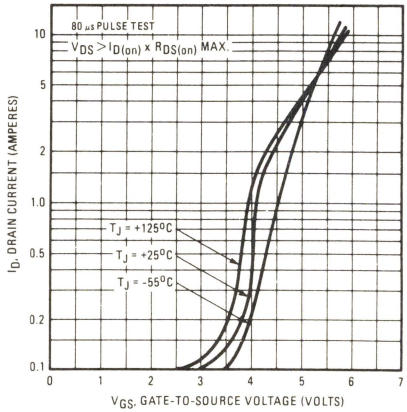


Fig. 2 - Typical transfer characteristics.

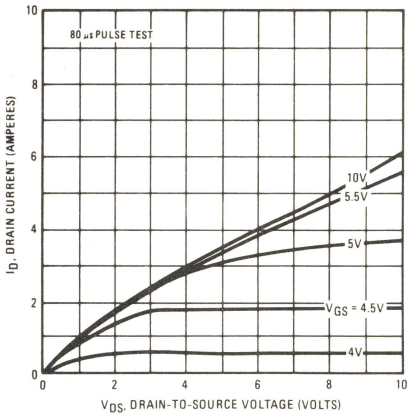


Fig. 3 - Typical saturation characteristics.

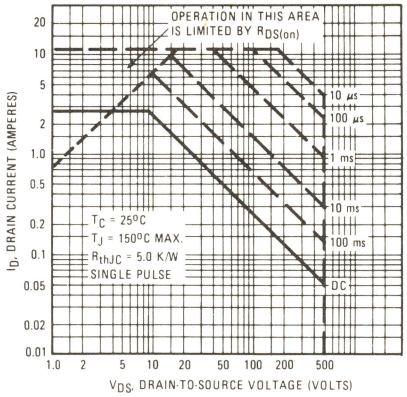


Fig. 4 - Maximum safe operating area.

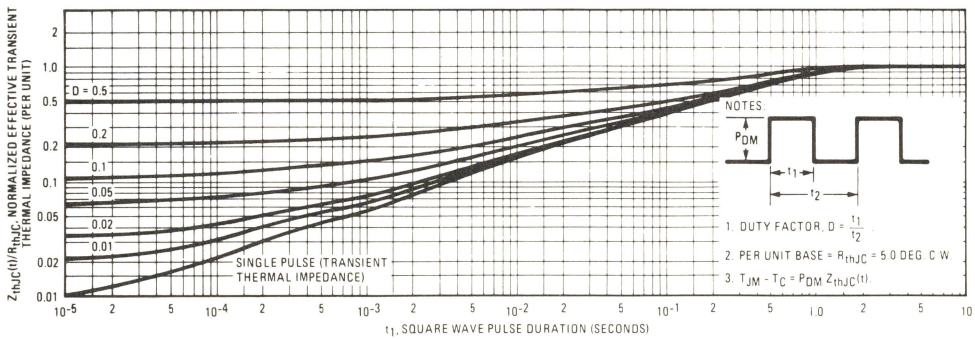


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case versus pulse duration.

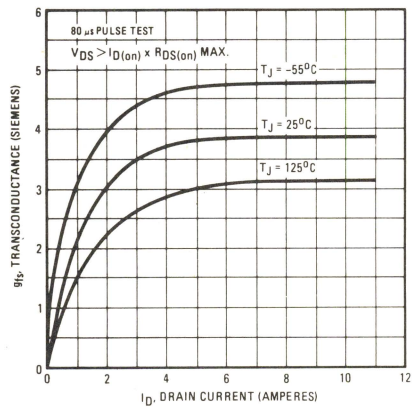


Fig. 6 - Typical transconductance versus drain current.

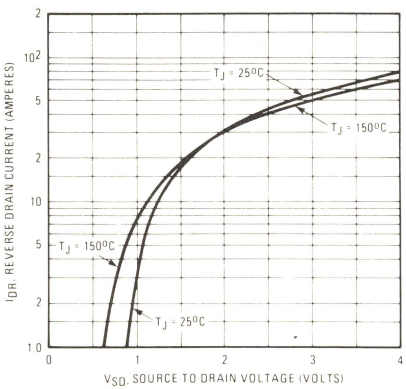


Fig. 7 - Typical source-drain diode forward voltage.

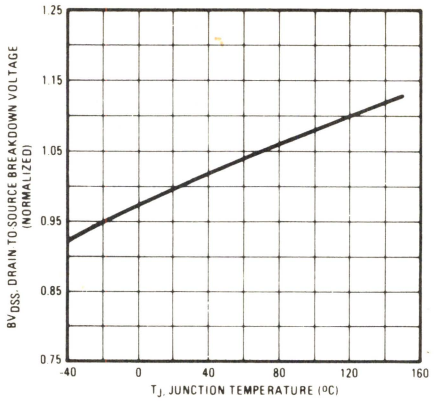


Fig. 8 - Breakdown voltage versus temperature.

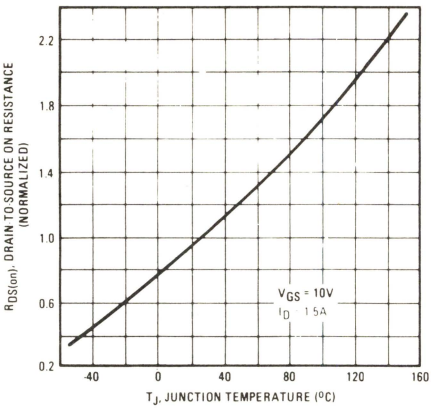


Fig. 9 - Typical normalized on-resistance versus temperature.

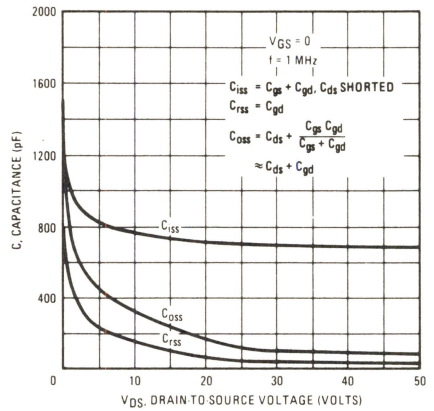


Fig. 10 - Typical capacitance versus drain-to-source voltage.

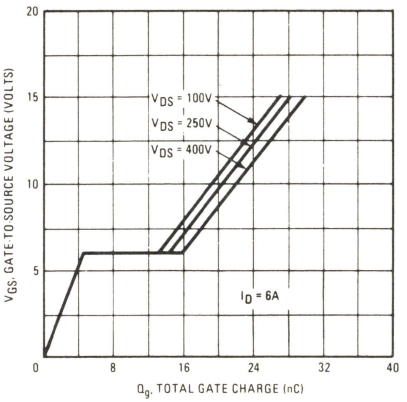


Fig. 11 - Typical gate charge versus gate-to-source voltage.

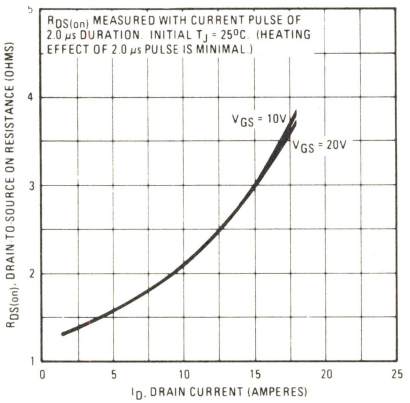


Fig. 12 - Typical on-resistance versus drain current.

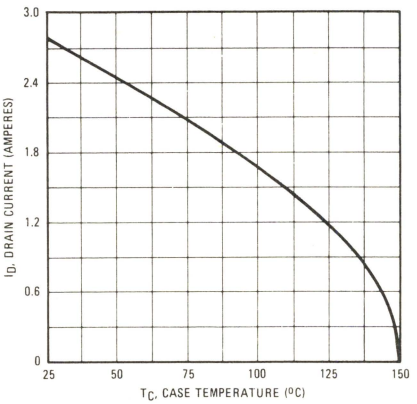


Fig. 13 - Maximum drain current versus case temperature.

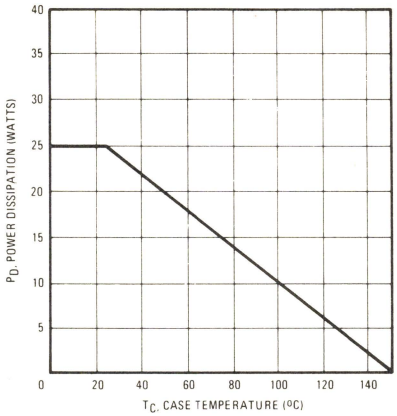
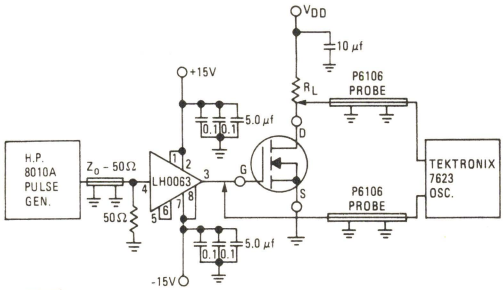
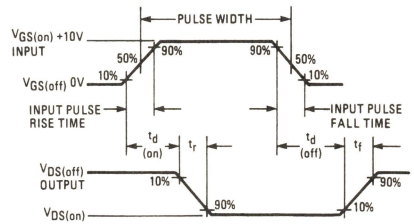


Fig. 14 - Power versus temperature derating curve.

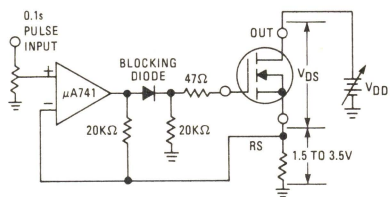


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 - Switching time test circuit.



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \bullet R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 - Safe operating test circuit.

HARRIS

BUZ11

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 30A, 50V
- $r_{DS(on)} = 0.04\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

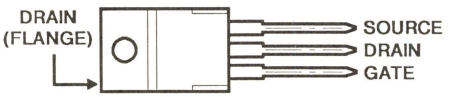
Description

The BUZ11 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ11 is supplied in the JEDEC TO-220AB plastic package.

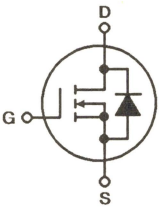
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ11	UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	50	V
Continuous Drain Current T_C = +30°C	I_D	30	A
Pulsed Drain Current T_C = +25°C	I_{DM}	120	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2253

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	50	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 50 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 15 A	—	0.03	0.04	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 15 A	4.0	8.0	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	750	1100	
Reverse Transfer Capacitance	C_{rss}		—	250	400	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 3 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	30 70	45 110	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	180 130	230 170	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	30	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	120	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.7	2.6	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, $I_F = I_{DR}$ dI_F/dt = 100 A/μs, V_R = 30 V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	0.25	—	μC

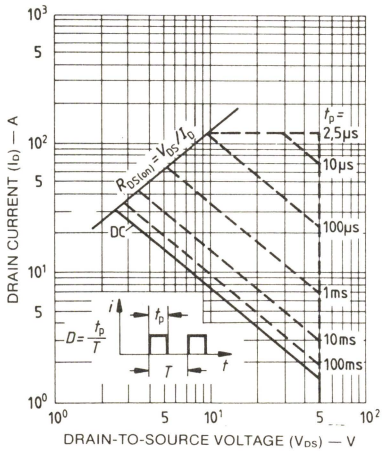


Fig. 1 - Maximum safe operating areas for all types.

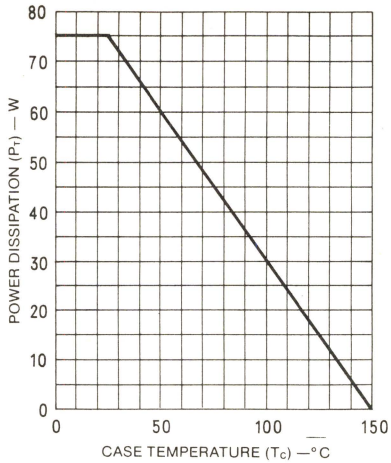


Fig. 2 - Power vs. temperature derating curve for all types.

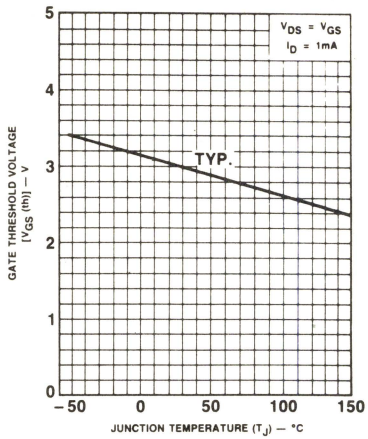


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

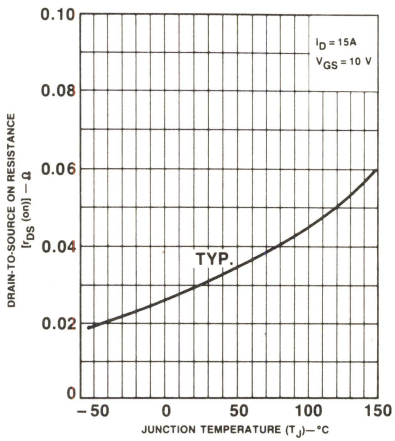


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

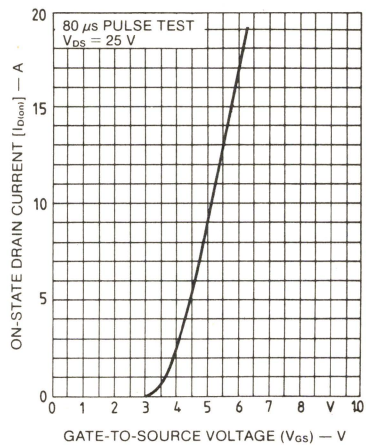


Fig. 5 - Typical transfer characteristics for all types.

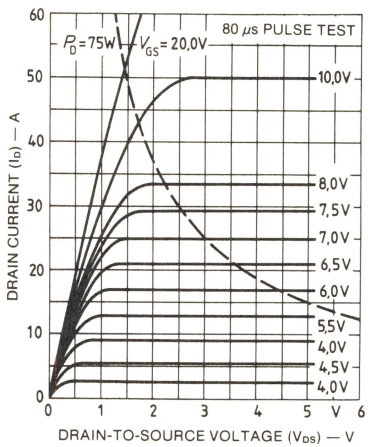


Fig. 6 - Typical output characteristics.

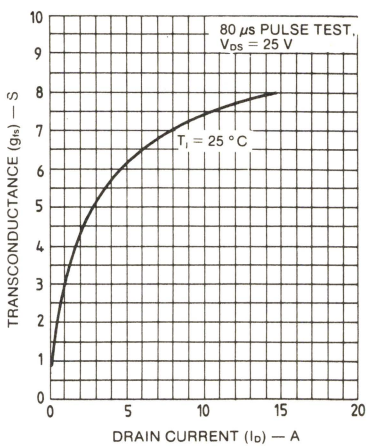


Fig. 7 - Typical transconductance vs. drain current.

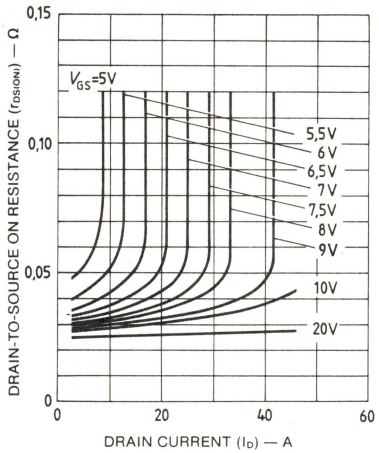


Fig. 8 - Typical on-resistance vs. drain current.

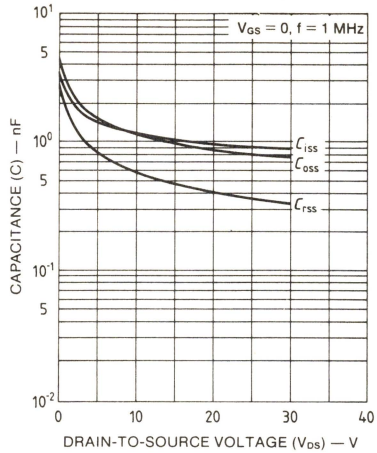


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

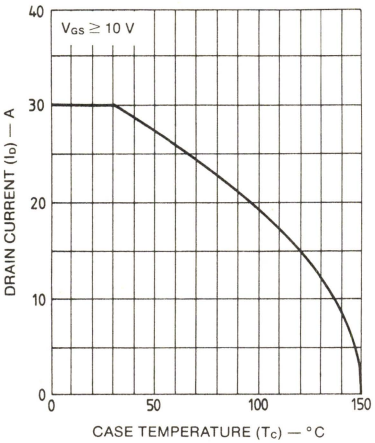


Fig. 10 - Maximum drain current vs. case temperature.

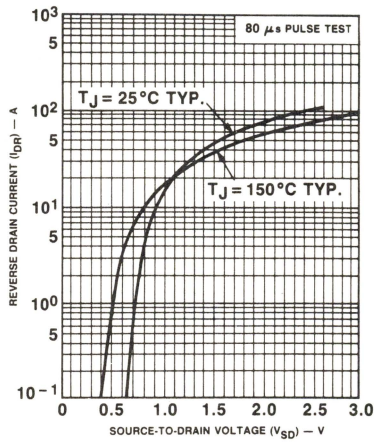


Fig. 11 - Typical source-drain diode forward voltage.

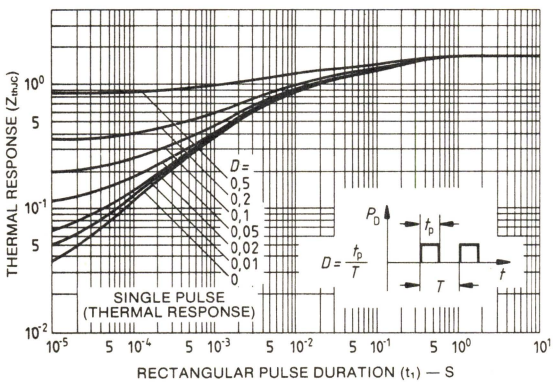


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

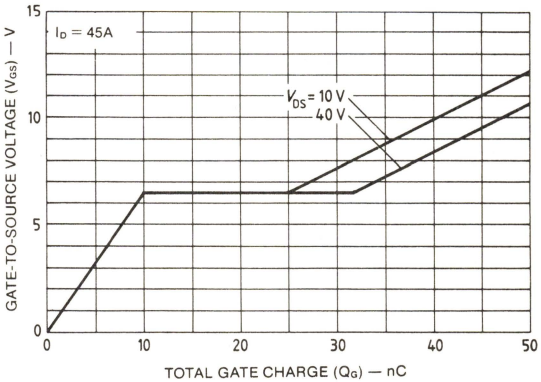


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ20

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 12A, 100V
- $r_{DS(on)} = 0.2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

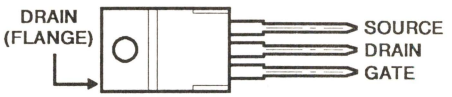
Description

The BUZ20 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ20 is supplied in the JEDEC TO-220AB plastic package.

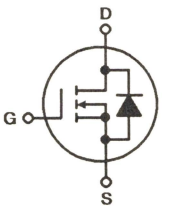
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ20	UNITS
Drain-Source Voltage	V_{DS}	100	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	100	V
Continuous Drain Current T_C = +30°C	I_D	12	A
Pulsed Drain Current T_C = +25°C	I_{DM}	48	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2254**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 100$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 6$ A	—	0.15	0.2	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 6$ A	2.7	4.0	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V f = 1 MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	300	500	
Reverse Transfer Capacitance	C_{rss}		—	80	140	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.9$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	30 50	45 75	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	110 60	140 80	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	—	12	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	48	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.4	1.8	V
Reverse Recovery Time	t_{rr}	$T_j = 25$° C, $I_F = I_{DR}$ $dI_F/dt = 100$ A/μs, $V_R = 30$ V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	1.6	—	μC

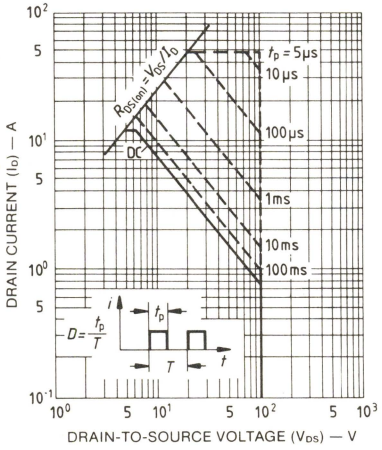


Fig. 1 - Maximum safe operating areas for all types.

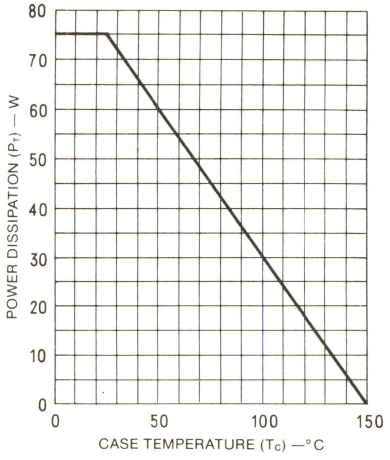


Fig. 2 - Power vs. temperature derating curve for all types.

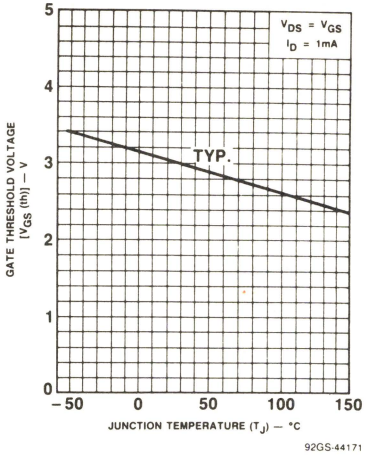


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

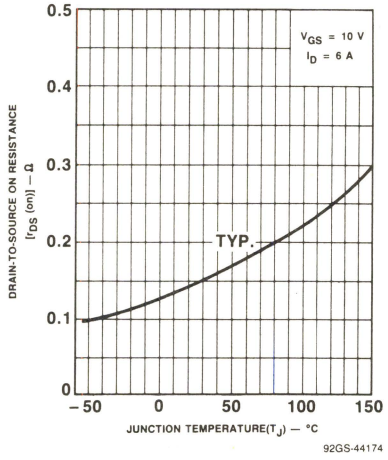


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

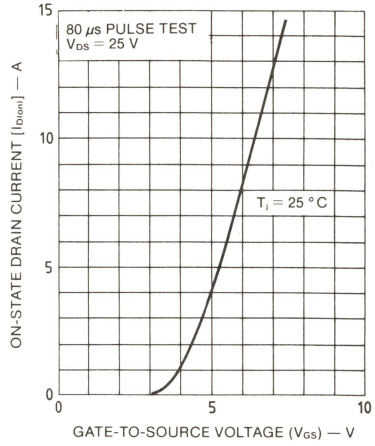


Fig. 5 - Typical transfer characteristics for all types.

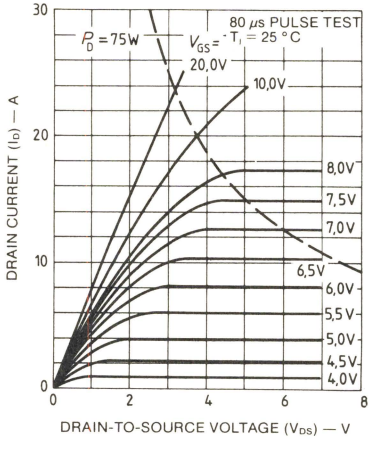


Fig. 6 - Typical output characteristics.

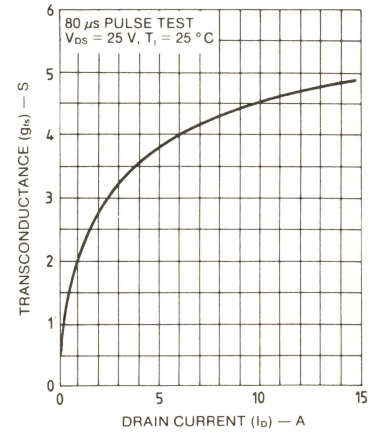


Fig. 7 - Typical transconductance vs. drain current.

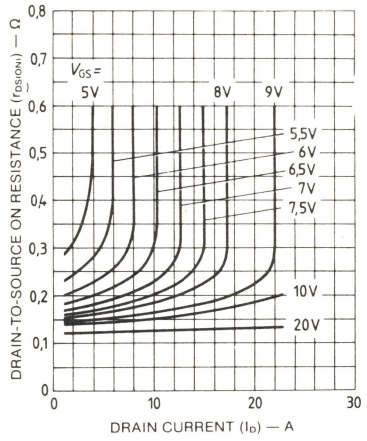


Fig. 8 - Typical on-resistance vs. drain current.

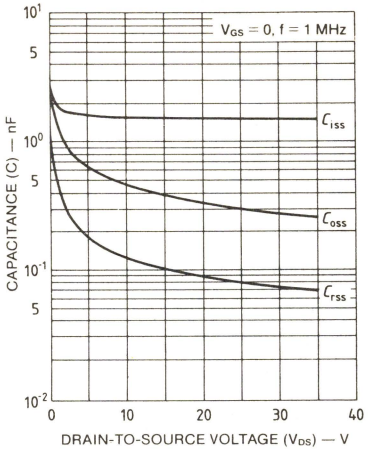


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

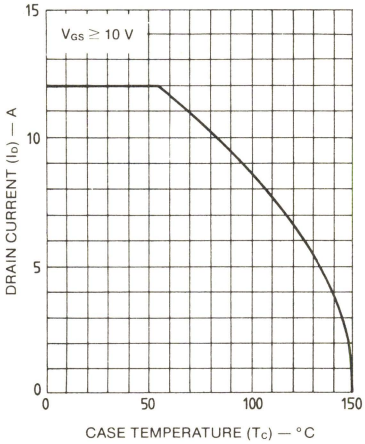


Fig. 10 - Maximum drain current vs. case temperature.

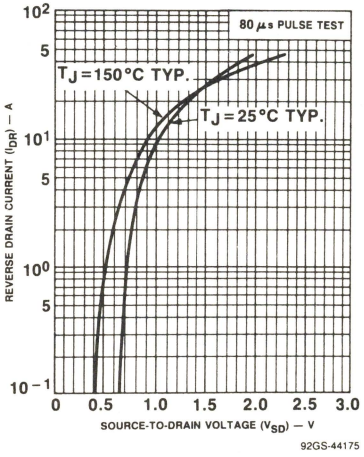


Fig. 11 - Typical source-drain diode forward voltage.

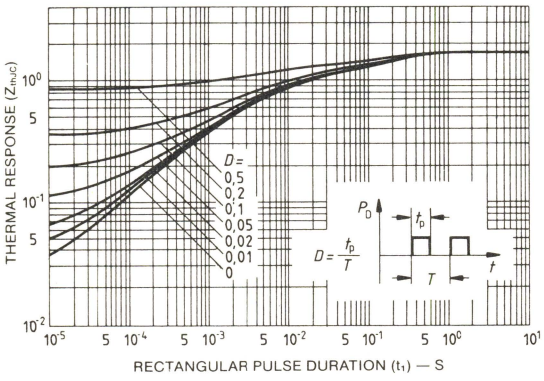


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

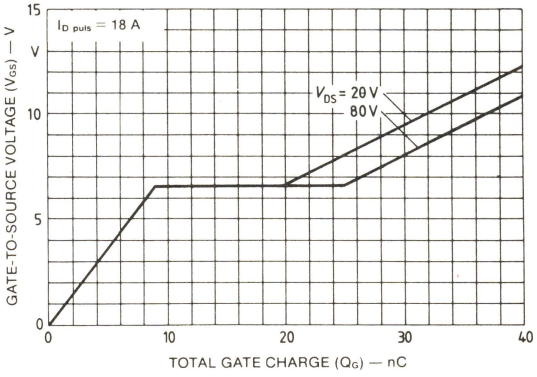


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ21

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 19A, 100V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

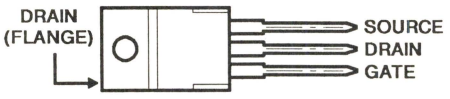
Description

The BUZ21 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ21 is supplied in the JEDEC TO-220AB plastic package.

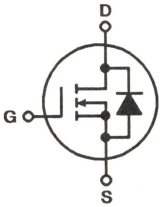
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	BUZ21	UNITS
Drain-Source Voltage ..... V_{DS}	100	V
Drain-Gate Voltage (R_{GS} = 20kΩ) ..... V_{DGR}	100	V
Continuous Drain Current		
T_C = +55°C ..... I_D	19	A
Pulsed Drain Current		
T_C = +25°C ..... I_{DM}	75	A
Single Pulse Avalanche Energy*, EAS	230	mj
Gate-Source Voltage ..... V_{GS}	±20	V
Maximum Power Dissipation		
T_C = +25°C ..... P_D	75	W
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040	E	
IEC Climatic Category - DIN IEC 68-1	55/150/56	

*V_{DD} = 25V, starting T_j = 25°C, L = 440μHy, R_{gs} = 50Ω, Ipeak = 28A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2420**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	100	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 100 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9 A	–	0.09	0.1	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	4	8	–	S
Input Capacitance	Ciss	VGS = 0 V	–	1500	2000	pF
Output Capacitance	Coss	VDS = 25 V	–	450	700	
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	150	240	
Turn-On Time ton	td(on)	Vcc = 30 V	–	30	45	ns
(ton = td(on) + tr)	tr	ID = 3 A	–	50	75	
Turn-Off Time toff	td(off)	VGS = 10 V	–	170	220	
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	80	110	
Thermal Resistance, Junction-to-Case	RθJC		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	RθJA		≤ 75			

*VDD = 25 V, starting Tj = 25°C, L = 440 µHy, Rgs = 50 Ω, Ipeak = 28 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	19	A
Pulsed Reverse Drain Current	IDRM		–	–	75	
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.5	2.1	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	200	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 30 V	–	0.25	–	µC

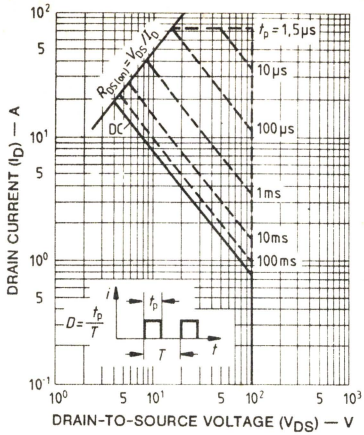


Figure 1 – Maximum safe operating areas for all types.

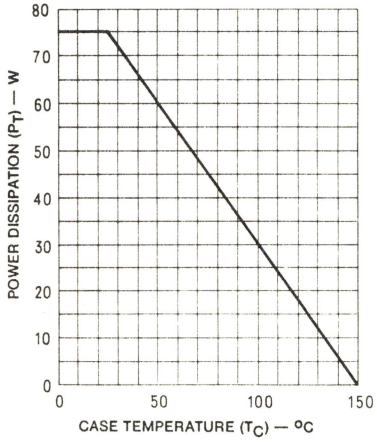


Figure 2 – Power vs temperature derating curve for all types.

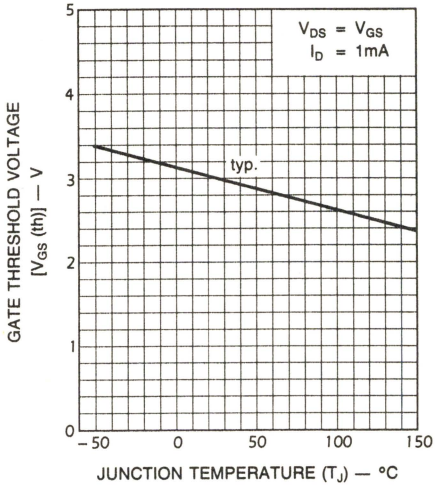


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

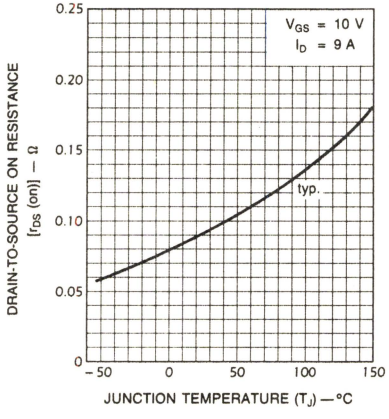


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

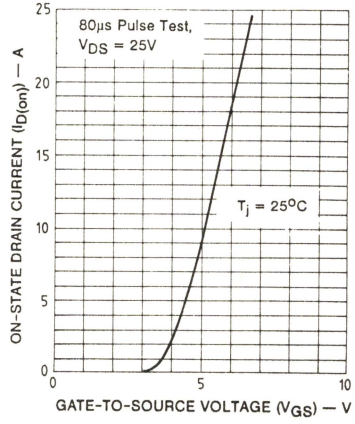


Figure 5 – Typical transfer characteristics for all types.

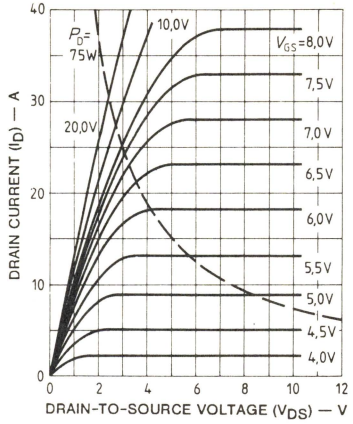


Figure 6 - Typical output characteristics.

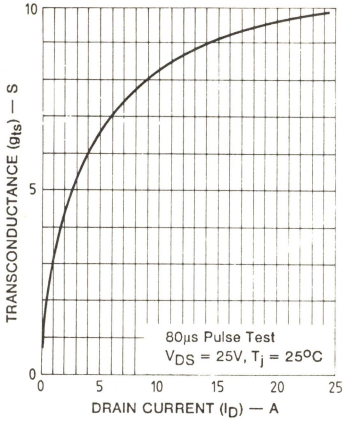


Figure 7 - Typical transconductance vs drain current.

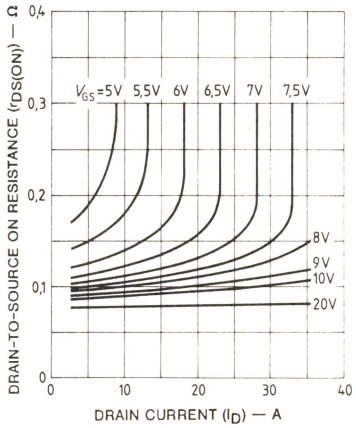


Figure 8 - Typical on-resistance vs drain current.

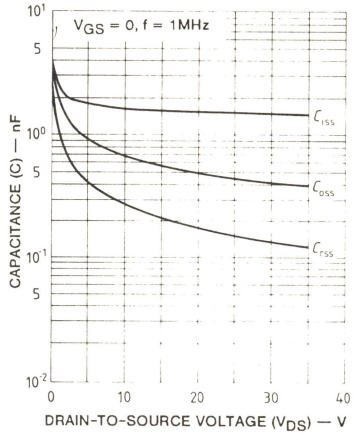


Figure 9 - Typical capacitance vs drain-to-source voltage.

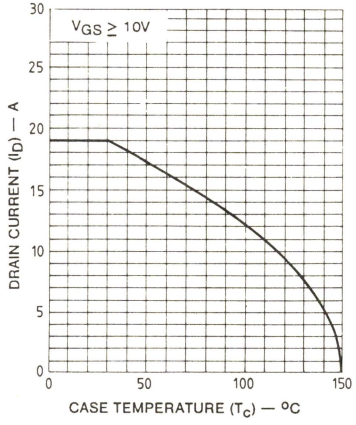


Figure 10 - Maximum drain current vs case temperature.

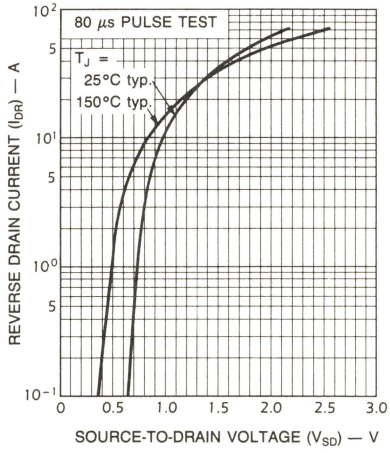


Figure 11 - Typical source-drain diode forward voltage.

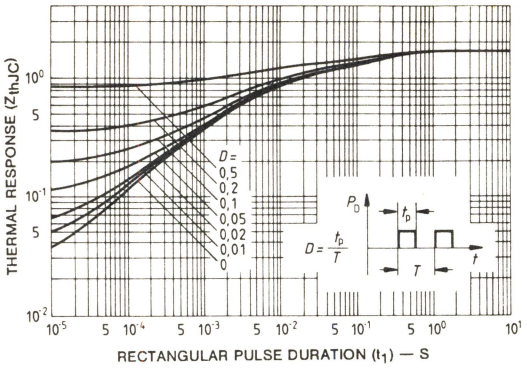


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

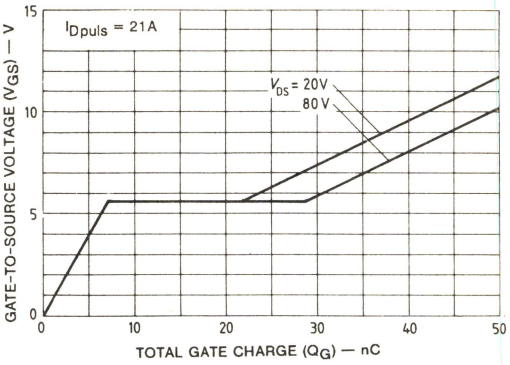


Figure 13 – Typical gate charge vs gate-to-source voltage.

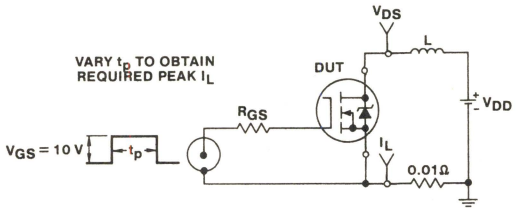


Figure 14 – Unclamped energy test circuit.

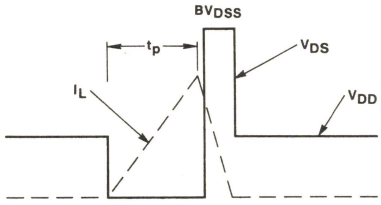


Figure 15 – Unclamped energy test waveforms.

HARRIS

BUZ32

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 9.5A, 200V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

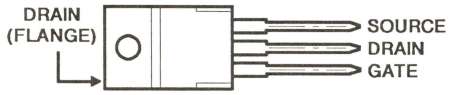
Description

The BUZ32 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ32 is supplied in the JEDEC TO-220AB plastic package.

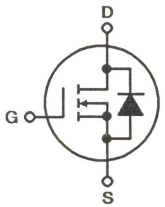
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ32	UNITS
Drain-Source Voltage	V_{DS}	200	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200	V
Continuous Drain Current T_C = +55°C	I_D	9.5	A
Pulsed Drain Current T_C = +25°C	I_{DM}	38	A
Single Pulse Avalanche Energy*, EAS		150	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 20V, starting T_j = 25°C, L = 3.3(μHy, R_{gs} = 50Ω, I_{peak} = 9A, see Figures 14 and 15.

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2416

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	200	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 200 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 4.5 A	–	0.35	0.4	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 4.5 A	2.2	5.0	–	S
Input Capacitance	Ciss	VGS = 0 V	–	1500	2000	pF
Output Capacitance	Coss	VDS = 25 V	–	250	400	
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	70	120	
Turn-On Time ton	td(on)	Vcc = 30 V	–	30	45	ns
(ton = td(on) + tr)	tr	ID = 2.9 A	–	40	60	
Turn-Off Time toff	td(off)	VGS = 10 V	–	110	140	
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	60	80	
Thermal Resistance, Junction-to-Case	RθJC		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	RθJA		≤ 75			

*VDD = 20 V, starting Tj = 25°C, L = 3.37 µHy, Rgs = 50 Ω, Ipeak = 9 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	9.5	A
Pulsed Reverse Drain Current	IDRM		–	–	38	
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.3	1.7	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	400	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 100 V	–	6.0	–	µC

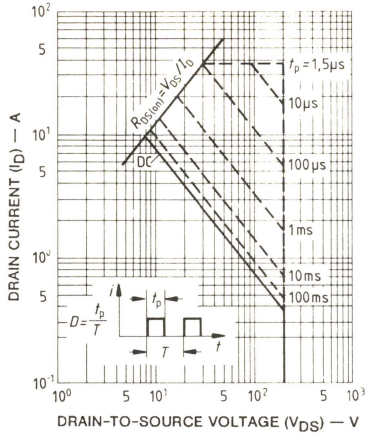


Figure 1 – Maximum safe operating areas for all types.

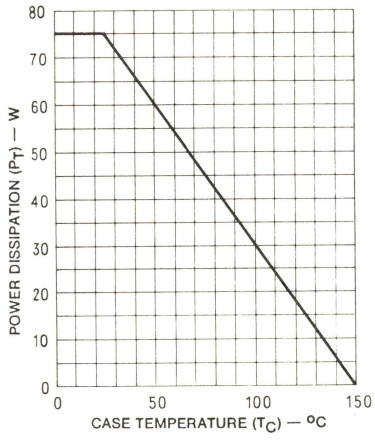


Figure 2 – Power vs temperature derating curve for all types.

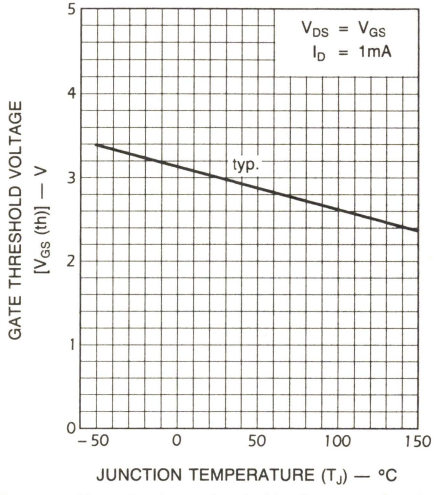


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

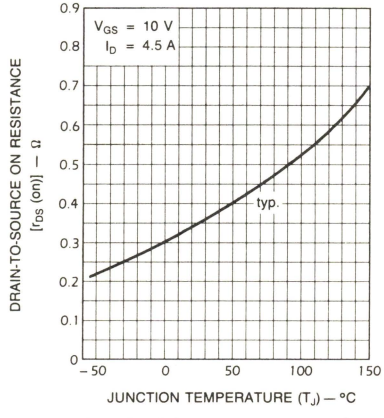


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

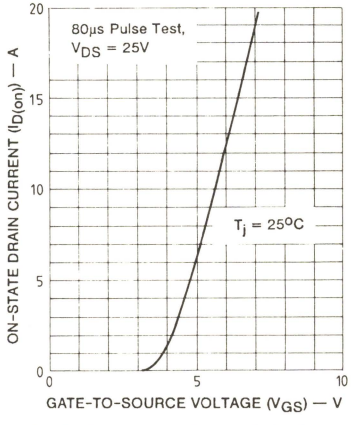


Figure 5 – Typical transfer characteristics for all types.

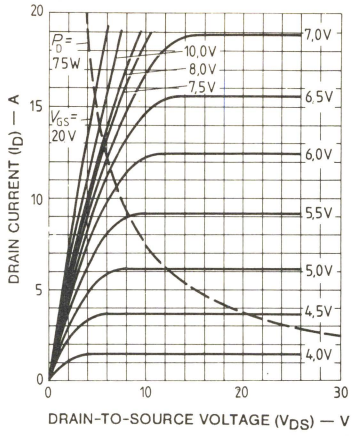


Figure 6 - Typical output characteristics.

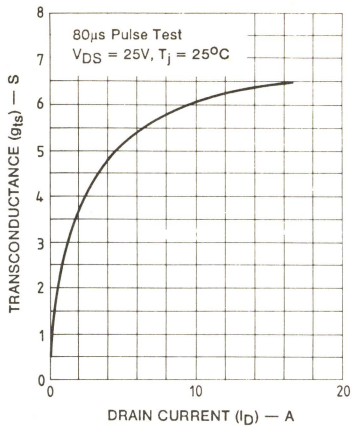


Figure 7 - Typical transconductance vs drain current.

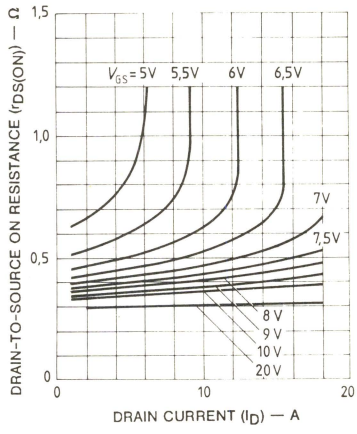


Figure 8 - Typical on-resistance vs drain current.

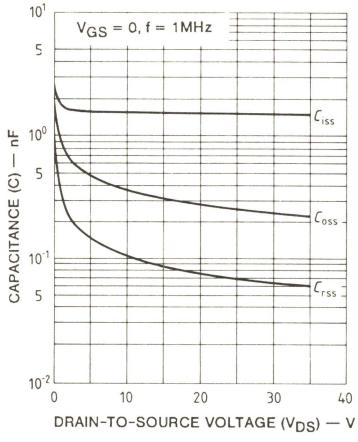


Figure 9 - Typical capacitance vs drain-to-source voltage.

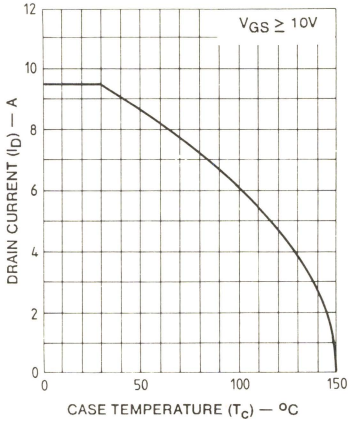


Figure 10 - Maximum drain current vs case temperature.

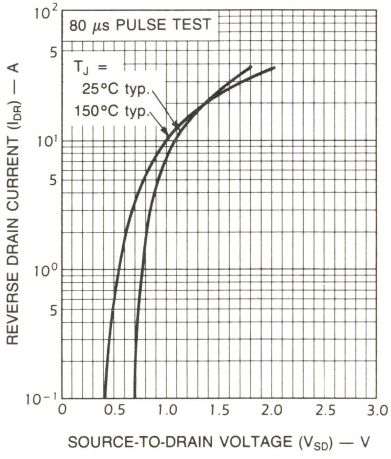


Figure 11 - Typical source-drain diode forward voltage.

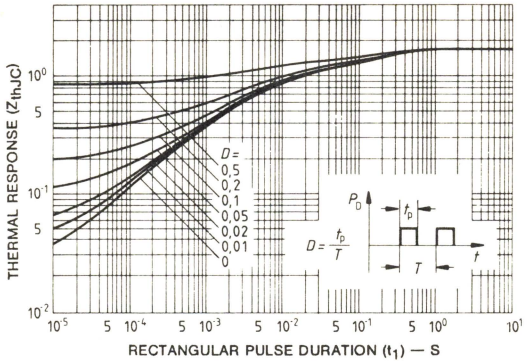


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

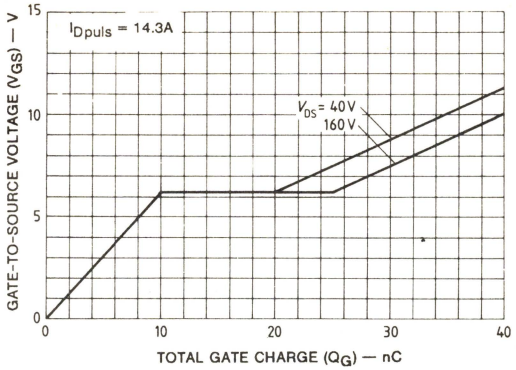


Figure 13 – Typical gate charge vs gate-to-source voltage.

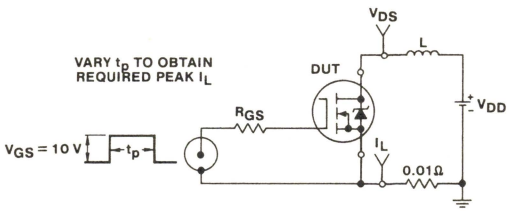


Figure 14 – Unclamped energy test circuit.

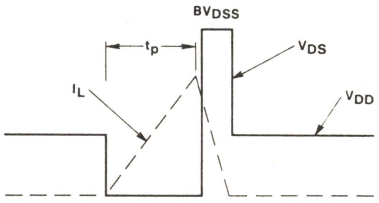


Figure 15 – Unclamped energy test waveforms.

HARRIS

BUZ351

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 11.5A, 400V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

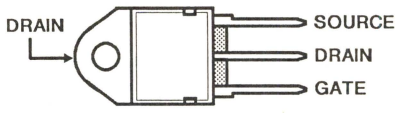
Description

The BUZ351 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ351 is supplied in the JEDEC TO-218AC plastic package.

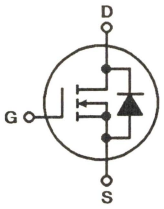
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ351	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current T_C = +30°C	I_D	11.5	A
Pulsed Drain Current T_C = +25°C	I_{DM}	46	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2266**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 400 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 5.5 A	—	0.35	0.4	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 5.5 A	3.3	4.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	3.8	4.9	nF
Output Capacitance	C_{oss}		—	300	500	pF
Reverse Transfer Capacitance	C_{rss}		—	120	200	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.9 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	50 80	75 120	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_f)	$t_{d(off)}$ t_f		— —	330 110	430 140	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 45			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	11.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	46	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR} dI_F/dt = 100 A/μs, V_R = 100 V	—	1	—	ns
Reverse Recovered Charge	Q_{RR}		—	10	—	μC

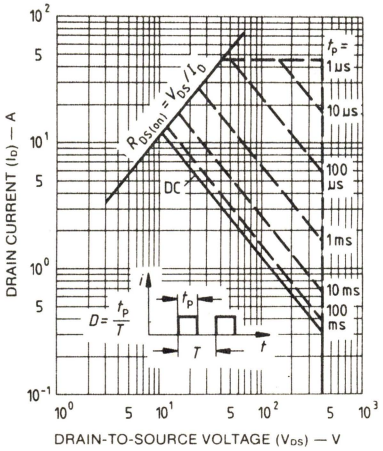


Fig. 1 - Maximum safe operating areas for all types.

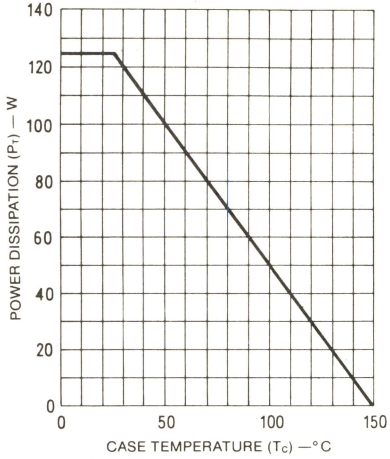


Fig. 2 - Power vs. temperature derating curve for all types.

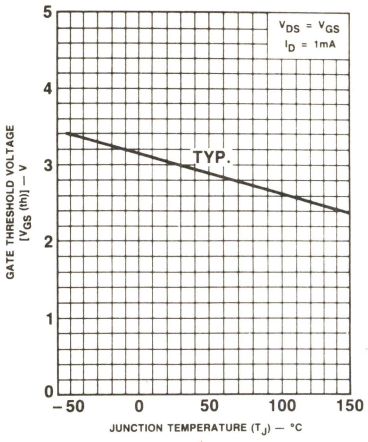


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

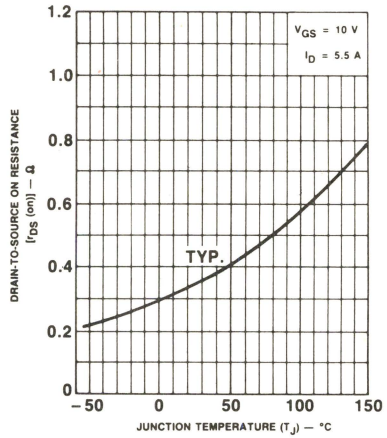


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

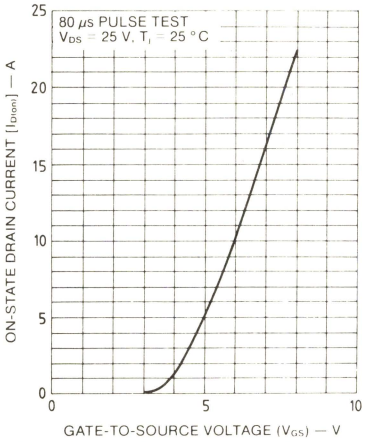


Fig. 5 - Typical transfer characteristics for all types.

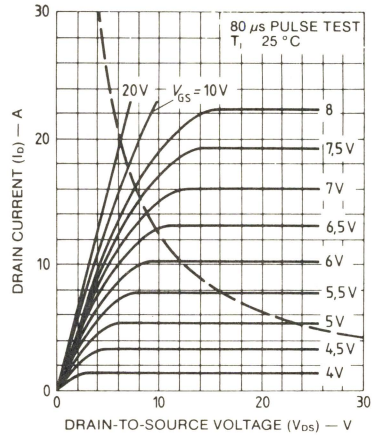


Fig. 6 - Typical output characteristics.

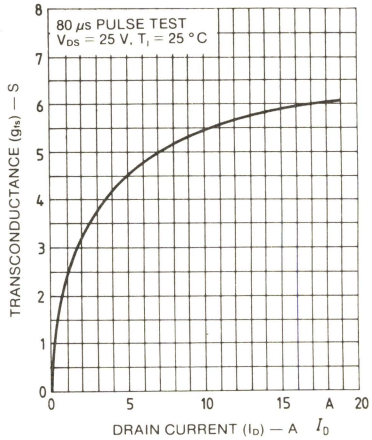


Fig. 7 - Typical transconductance vs. drain current.

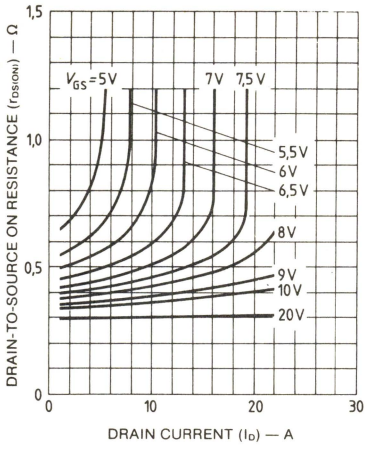


Fig. 8 - Typical on-resistance vs. drain current.

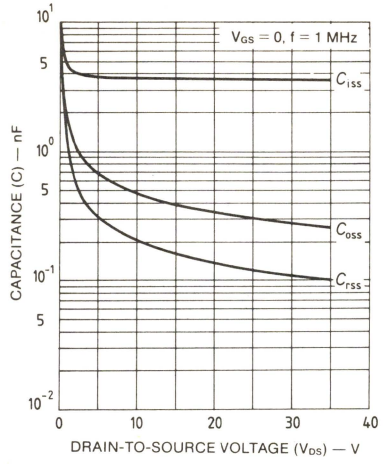


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

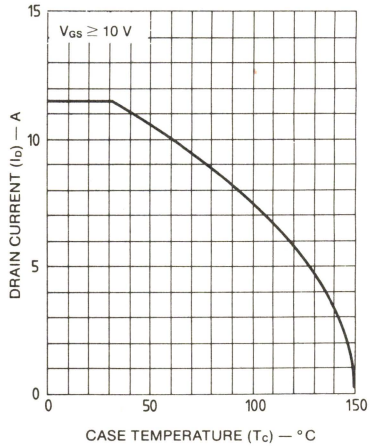


Fig. 10 - Maximum drain current vs. case temperature.

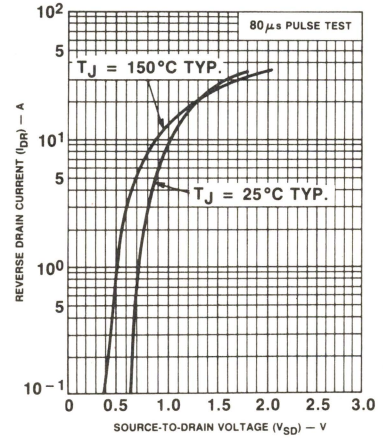


Fig. 11 - Typical source-drain diode forward voltage.

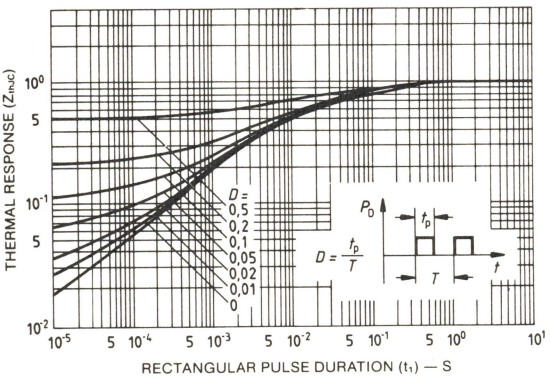


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

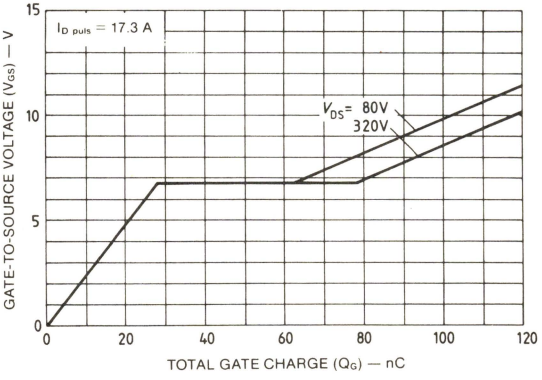


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ41A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 4.5A, 500V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

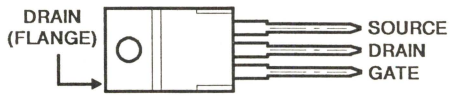
Description

The BUZ41A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ41A is supplied in the JEDEC TO-220AB plastic package.

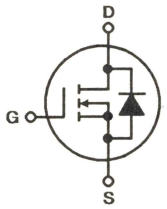
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ41A	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current			
T_C = +35°C	I_D	4.5	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	18	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2256**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 500 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 2.5 A	—	1.4	1.5	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 2.5 A	1.5	2.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	1500	2000	pF
Output Capacitance	C_{oss}		—	110	170	
Reverse Transfer Capacitance	C_{rss}		—	40	70	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.6 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	30 40	45 60	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_r)	$t_{d(off)}$ t_r		— —	110 50	140 65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 75		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	4.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	18	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.1	1.5	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, I_F = I_{DR}	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}	dI_F/dt = 100 A/μs, V_R = 100 V	—	6	—	μC

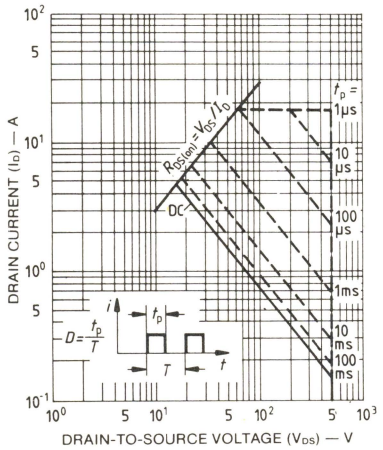


Fig. 1 - Maximum safe operating areas for all types.

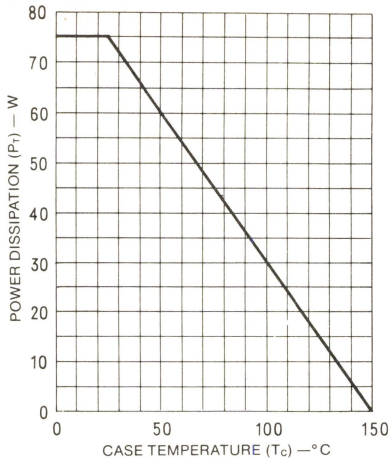


Fig. 2 - Power vs. temperature derating curve for all types.

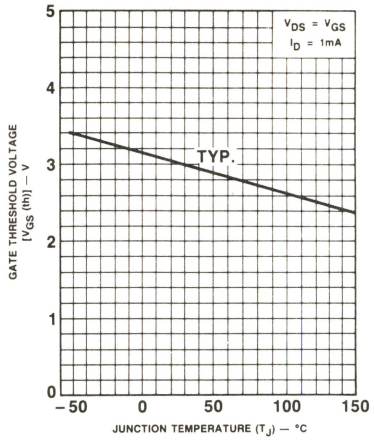


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

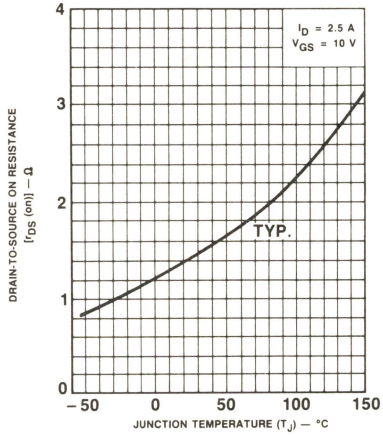


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

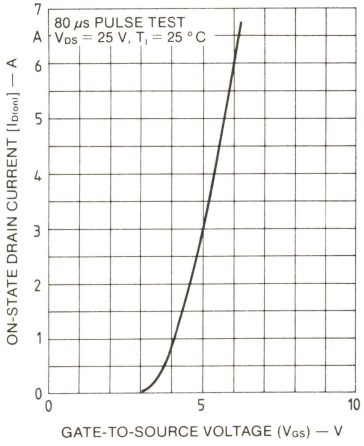


Fig. 5 - Typical transfer characteristics for all types.

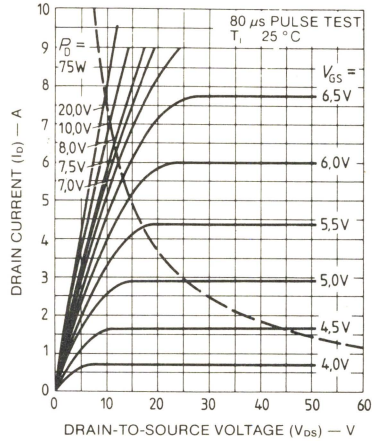


Fig. 6 - Typical output characteristics.

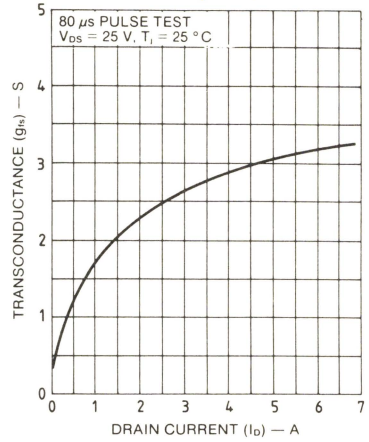


Fig. 7 - Typical transconductance vs. drain current.

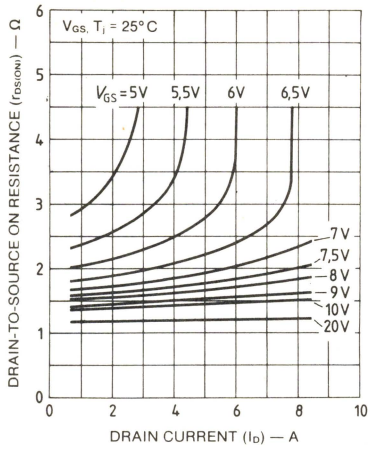


Fig. 8 - Typical on-resistance vs. drain current.

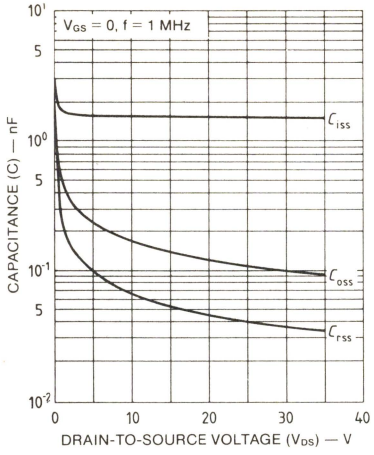


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

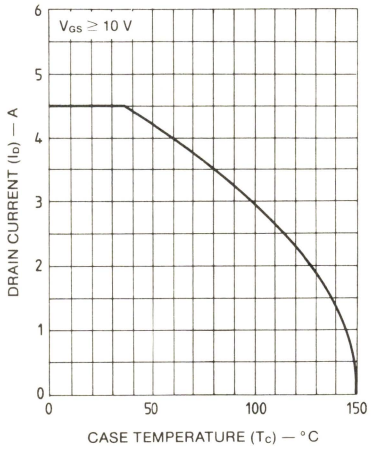


Fig. 10 - Maximum drain current vs. case temperature.

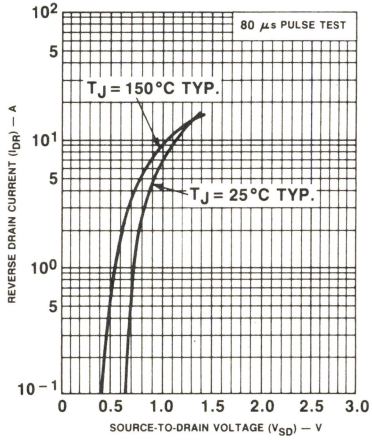


Fig. 11 - Typical source-drain diode forward voltage.

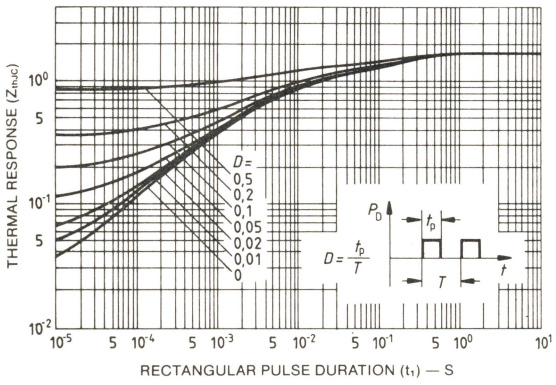


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

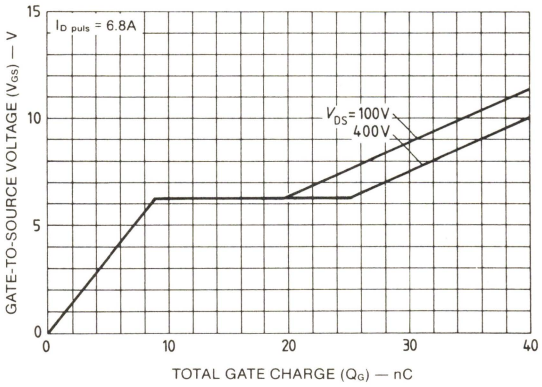


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ42

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 4.0A, 500V
- $r_{DS(on)} = 2.0\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

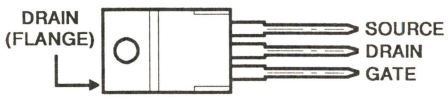
Description

The BUZ42 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ42 is supplied in the JEDEC TO-220AB plastic package.

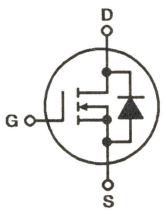
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ42	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current T_C = +55°C	I_D	40	A
Pulsed Drain Current T_C = +25°C	I_{DM}	16	A
Single Pulse Avalanche Energy*, EAS		300	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 50V, starting T_j = 25°C, L = 25μHy, R_{gs} = 25Ω, I_{peak} = 4.5A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2417**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	500	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 500 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 2.5 A	–	1.6	2.0	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 2.5 A	1.5	2.5	–	S
Input Capacitance	Ciss	VGS = 0 V	–	1500	2000	pF
Output Capacitance	Coss	VDS = 25 V	–	110	170	pF
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	40	70	pF
Turn-On Time ton	td(on)	Vcc = 30 V	–	30	45	ns
(ton = td(on) + tr)	tr	ID = 2.5 A	–	40	60	ns
Turn-Off Time toff	td(off)	VGS = 10 V	–	110	140	ns
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	50	65	ns
Thermal Resistance, Junction-to-Case	RθJC			≤ 1.67		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤ 75		°C/W

*VDD = 50 V, starting Tj = 25°C, L = 25 µHy, Rgs = 25Ω, Ipeak = 4.5 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	4.0	A
Pulsed Reverse Drain Current	IDRM		–	–	16	A
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.1	1.5	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	1200	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 100 V	–	6.0	–	µC

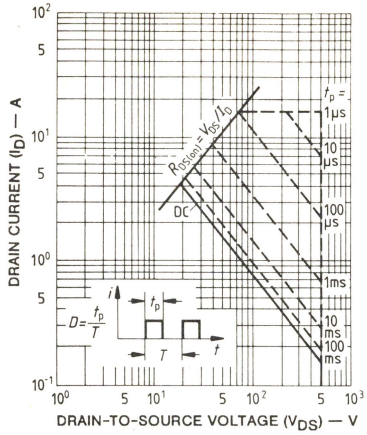


Figure 1 – Maximum safe operating areas for all types.

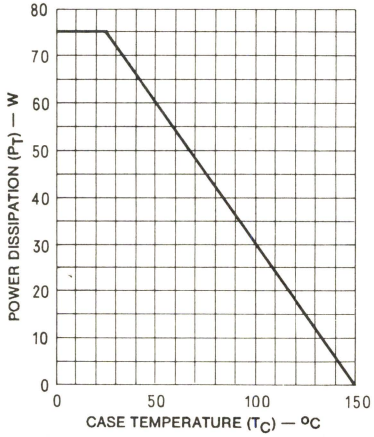


Figure 2 – Power vs temperature derating curve for all types.

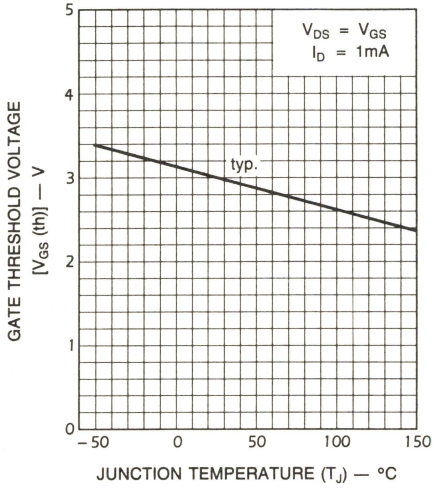


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

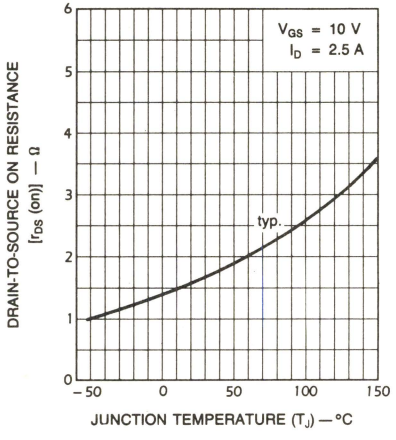


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

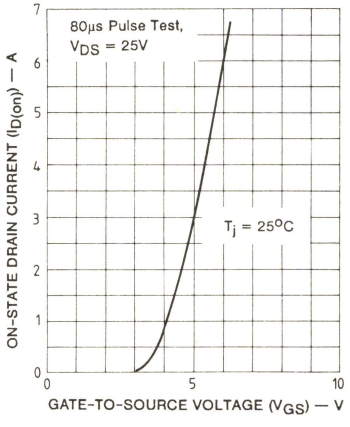


Figure 5 – Typical transfer characteristics for all types.

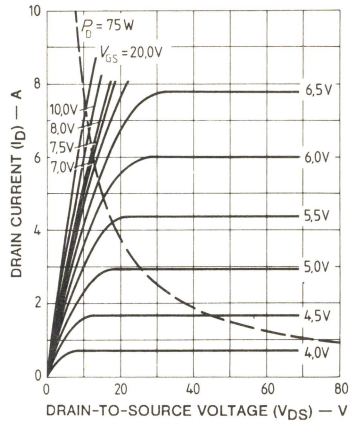


Figure 6 - Typical output characteristics.

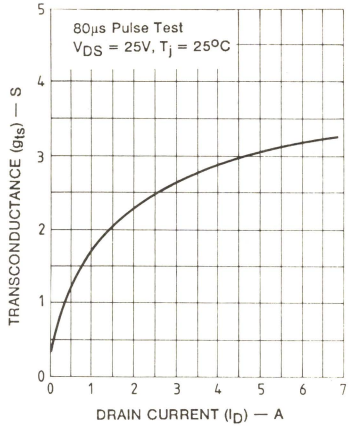


Figure 7 - Typical transconductance vs drain current.

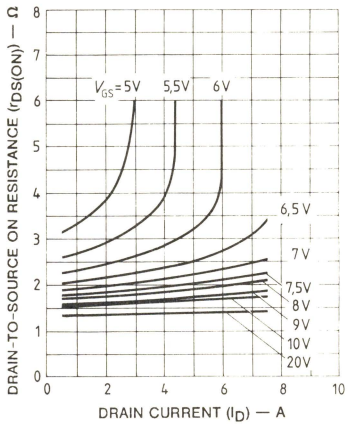


Figure 8 - Typical on-resistance vs drain current.

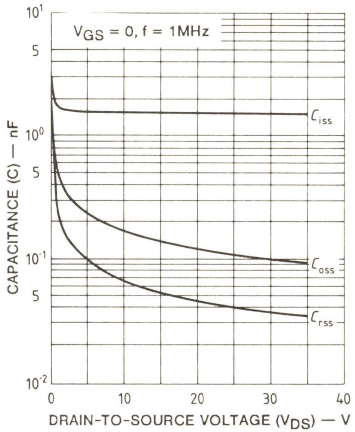


Figure 9 - Typical capacitance vs drain-to-source voltage.

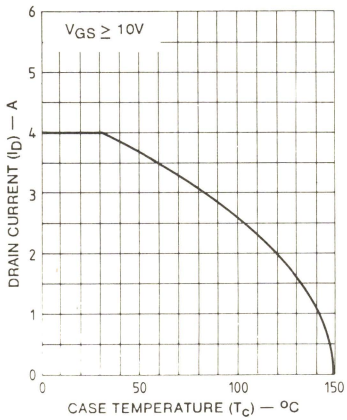


Figure 10 - Maximum drain current vs case temperature.

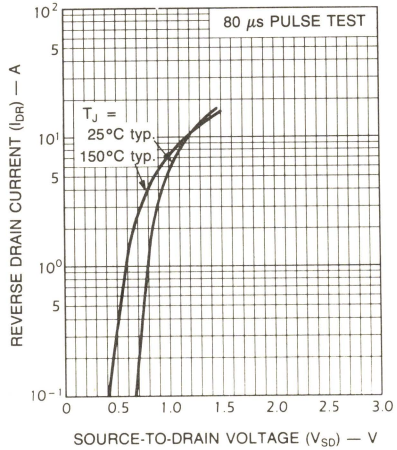


Figure 11 - Typical source-drain diode forward voltage.

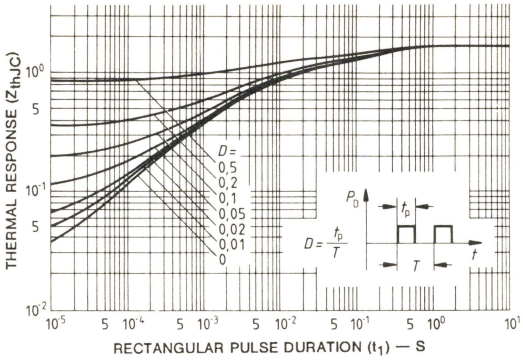


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

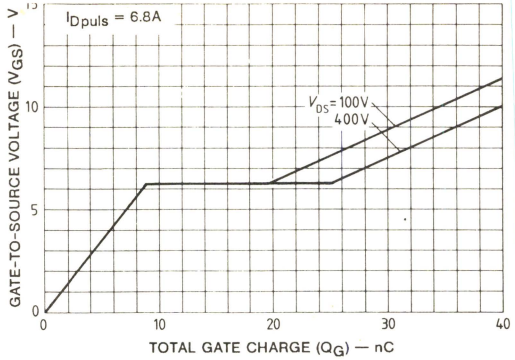


Figure 13 – Typical gate charge vs gate-to-source voltage.

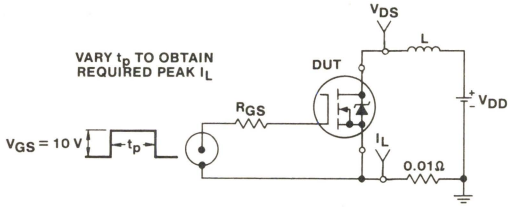


Figure 14 – Unclamped energy test circuit.

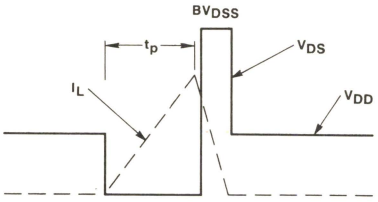


Figure 15 – Unclamped energy test waveforms.

HARRIS

BUZ45

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 9.6A, 500V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

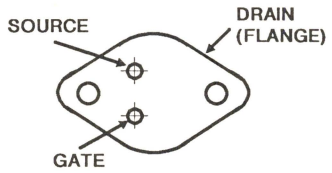
Description

The BUZ45 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ45 is supplied in the JEDEC TO-204AA plastic package.

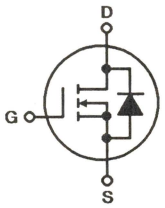
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ45	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current T_C = +25°C	I_D	9.6	A
Pulsed Drain Current T_C = +25°C	I_{DM}	38	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2257

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 500 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 5 A	—	0.55	0.6	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	
Reverse Transfer Capacitance	C_{rss}		—	100	170	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.8 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	50 80	75 120	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_f)	$t_{d(off)}$ t_f		— —	330 110	430 140	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 35			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	9.6	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	38	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR} dI_F/dt = 100 A/μs, V_R = 100 V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	12	—	μC

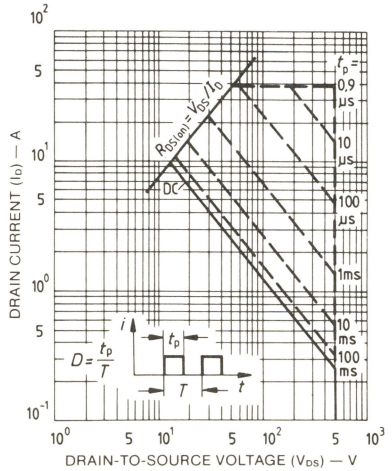


Fig. 1 - Maximum safe operating areas for all types.

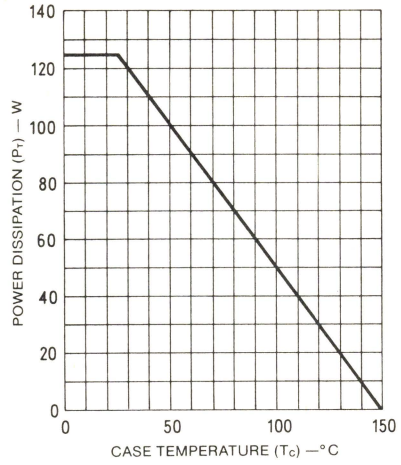


Fig. 2 - Power vs. temperature derating curve for all types.

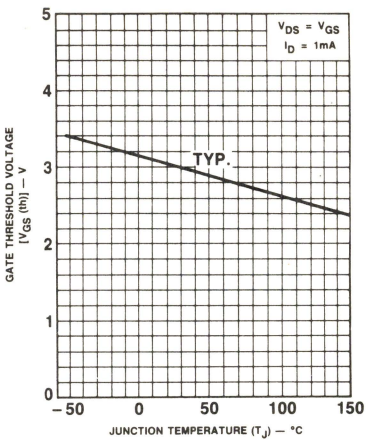


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

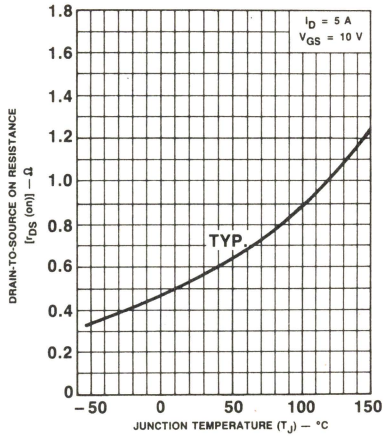


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

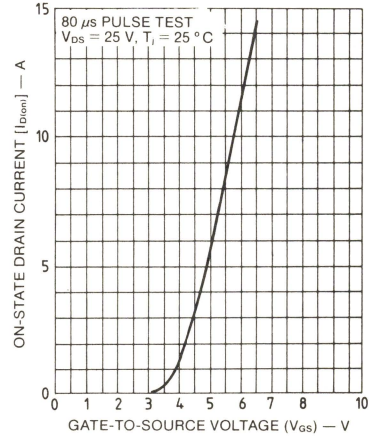


Fig. 5 - Typical transfer characteristics for all types.

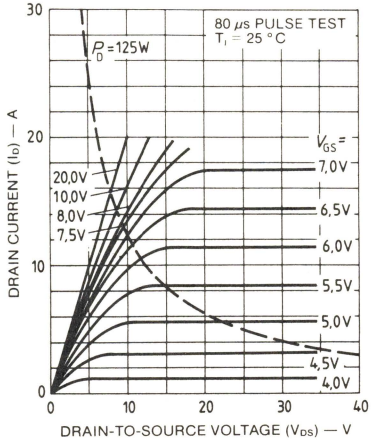


Fig. 6 - Typical output characteristics.

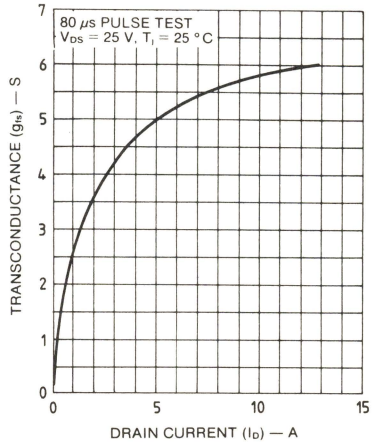


Fig. 7 - Typical transconductance vs. drain current.

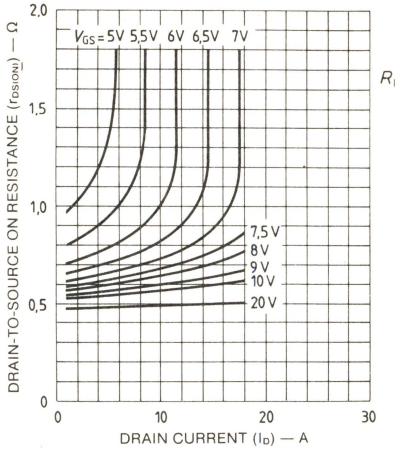


Fig. 8 - Typical on-resistance vs. drain current.

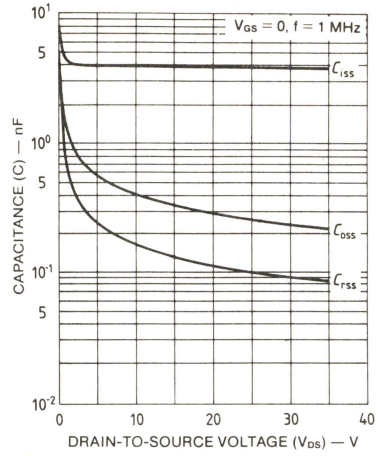


Fig. 9 - Typical capacitance vs. drain-to-source voltage

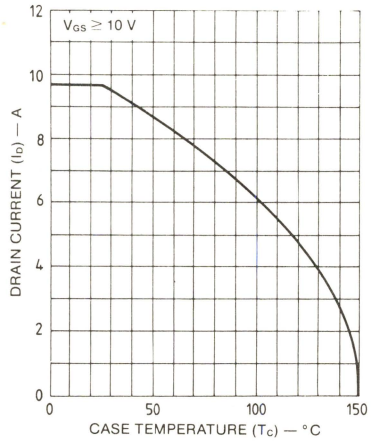


Fig. 10 - Maximum drain current vs. case temperature.

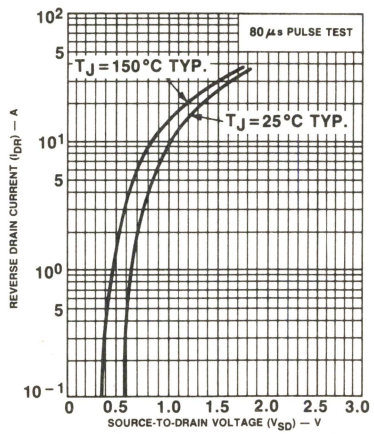


Fig. 11 - Typical source-drain diode forward voltage.

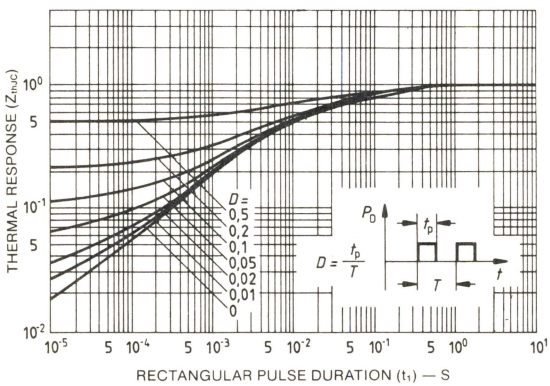


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

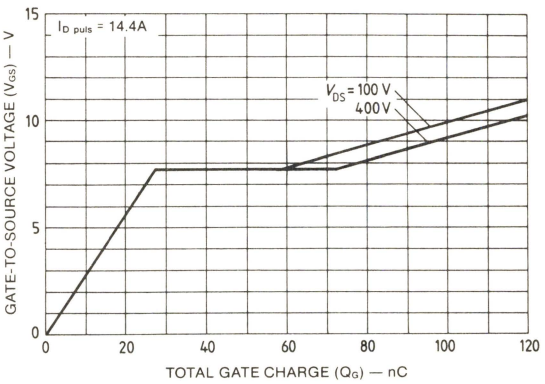


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ45A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 8.3A, 500V
- $r_{DS(on)} = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

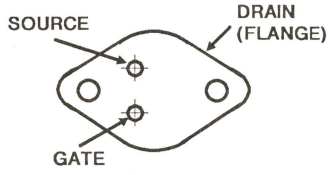
Description

The BUZ45A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ45A is supplied in the JEDEC TO-204AA plastic package.

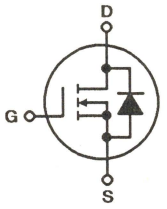
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ45A	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current T_C = +25°C	I_D	8.3	A
Pulsed Drain Current T_C = +25°C	I_{DM}	33	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2258

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1 mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	20	250	μA
		T_j = 125 °C, V_{DS} = 500 V, V_{GS} = 0 V	—	100	1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A	—	0.7	0.8	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	pF
Reverse Transfer Capacitance	C_{rss}		—	100	170	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	V_{CC} = 30 V, I_D = 2.8 A, V_{GS} = 10 V, R_{GS} = 50 Ω	—	50	75	ns
	t_r		—	80	120	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$		—	330	430	ns
	t_f		—	110	140	ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			≤ 1		°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			≤ 35		°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	8.3	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	33	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$, V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.6	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, $I_F = I_{DR}$, dI_F/dt = 100 A/μs, V_R = 100 V	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}		—	12	—	μC

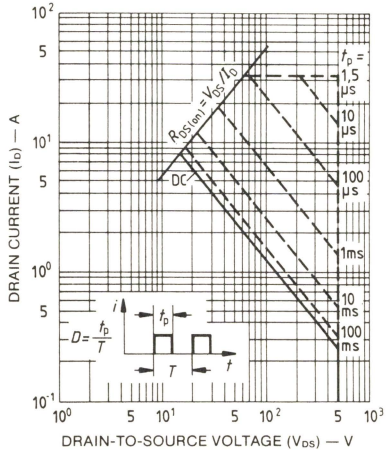


Fig. 1 - Maximum safe operating areas for all types.

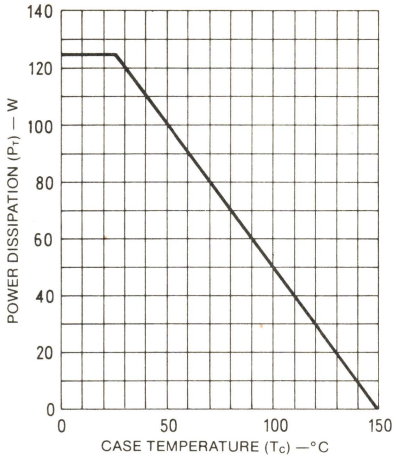


Fig. 2 - Power vs. temperature derating curve for all types.

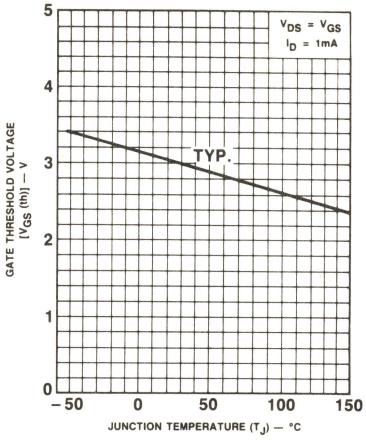


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

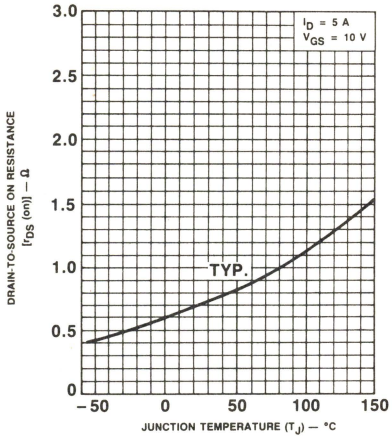


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

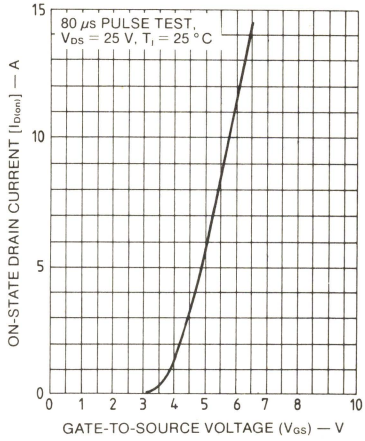


Fig. 5 - Typical transfer characteristics for all types.

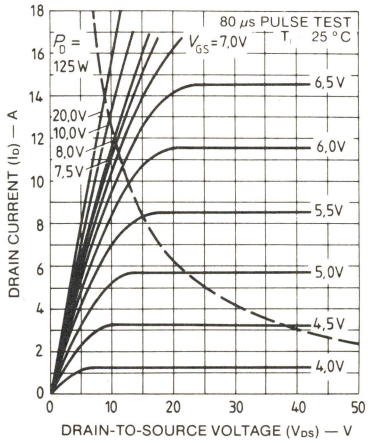


Fig. 6 - Typical output characteristics.

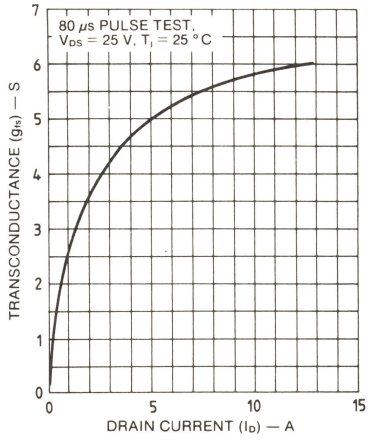


Fig. 7 - Typical transconductance vs. drain current.

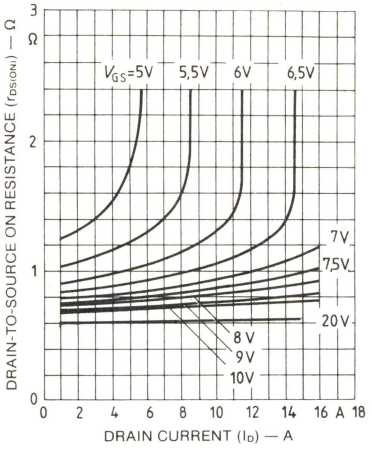


Fig. 8 - Typical on-resistance vs. drain current.

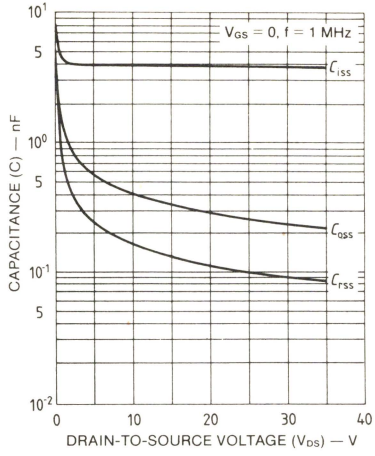


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

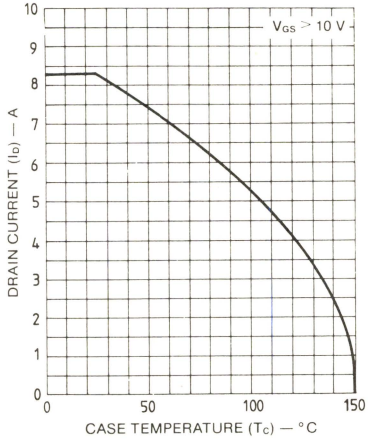


Fig. 10 - Maximum drain current vs. case temperature.

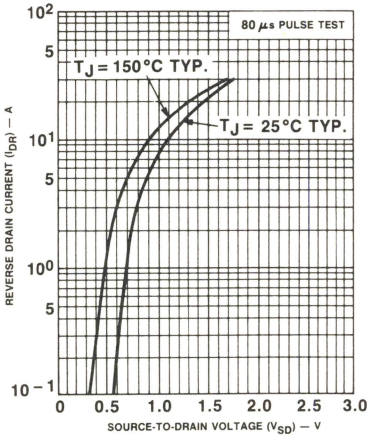


Fig. 11 - Typical source-drain diode forward voltage.

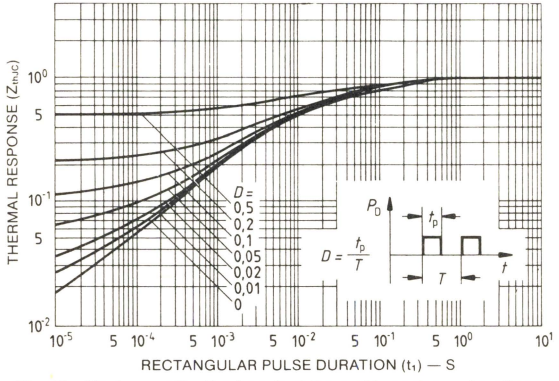


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

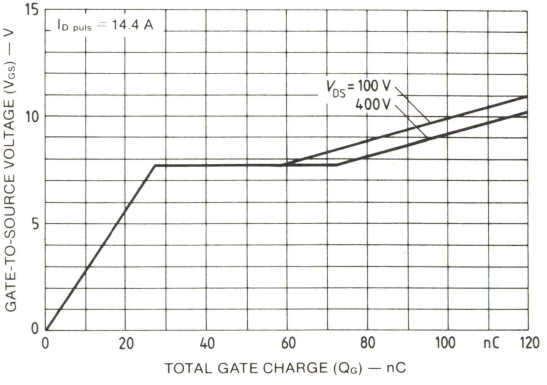


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ45B

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 10A, 500V
- $r_{DS(on)} = 0.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

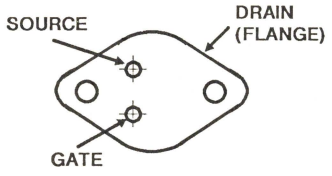
Description

The BUZ45B is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ45B is supplied in the JEDEC TO-204AA plastic package.

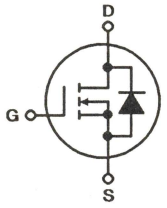
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ45B	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current T_C = +35°C	I_D	10	A
Pulsed Drain Current T_C = +25°C	I_{DM}	40	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2259

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 500 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 5 A	—	0.49	0.50	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	
Reverse Transfer Capacitance	C_{rss}		—	100	170	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.9 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	50 80	75 120	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_r)	$t_{d(off)}$ t_r		— —	330 110	430 140	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 35			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	10	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	40	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, I_F = I_{DR}	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}	dI_F/dt = 100 A/μs, V_R = 100 V	—	12	—	μC

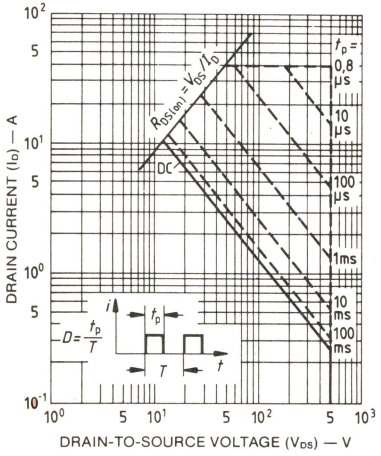


Fig. 1 - Maximum safe operating areas for all types.

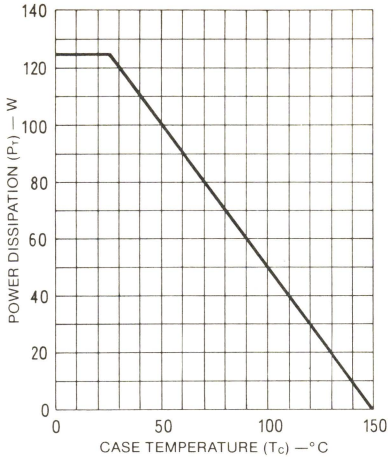


Fig. 2 - Power vs. temperature derating curve for all types.

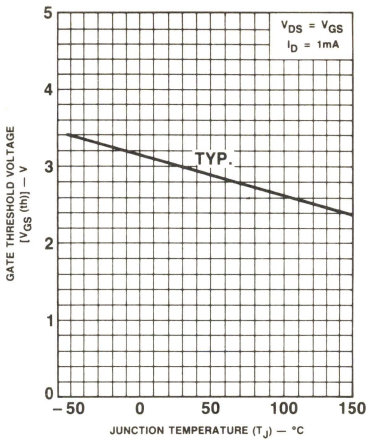


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

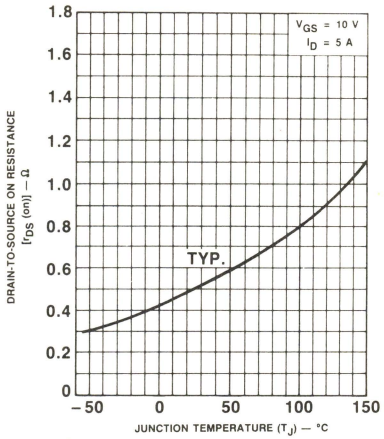


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

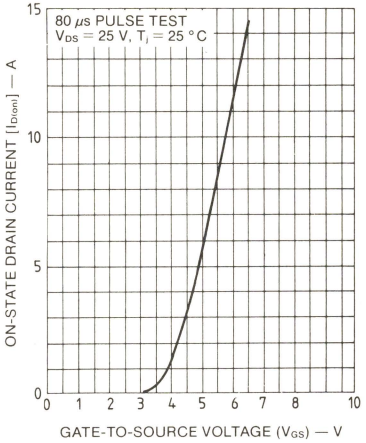


Fig. 5 - Typical transfer characteristics for all types.

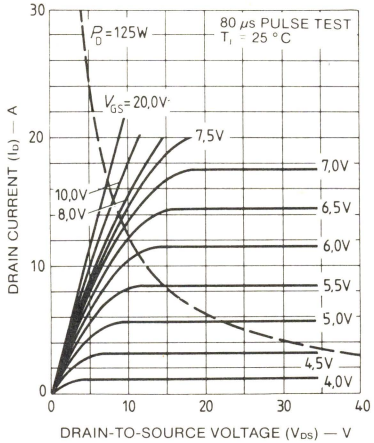


Fig. 6 - Typical output characteristics.

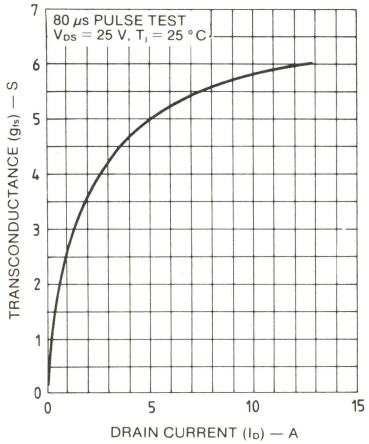


Fig. 7 - Typical transconductance vs. drain current.

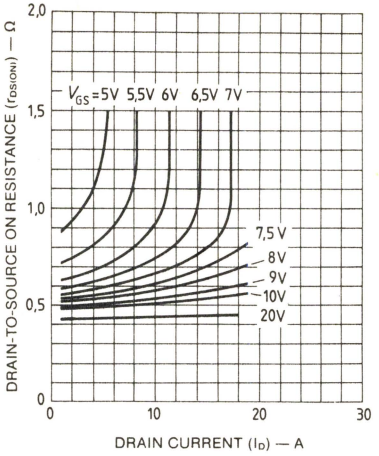


Fig. 8 - Typical on-resistance vs. drain current.

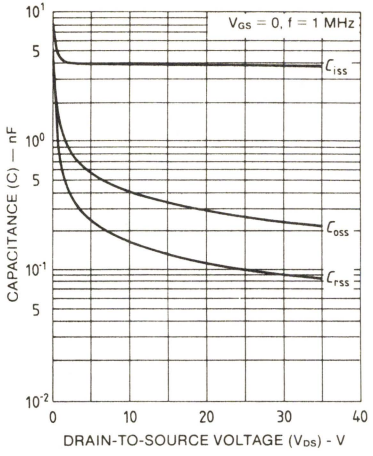


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

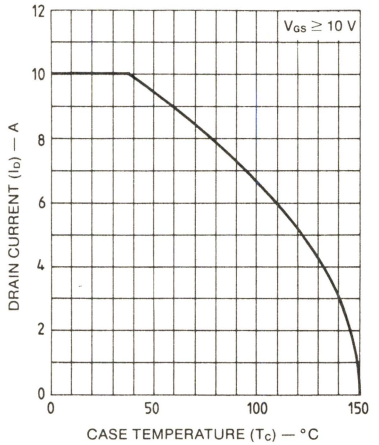


Fig. 10 - Maximum drain current vs. case temperature.

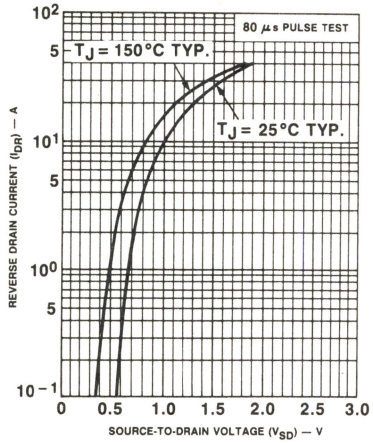


Fig. 11 - Typical source-drain diode forward voltage.

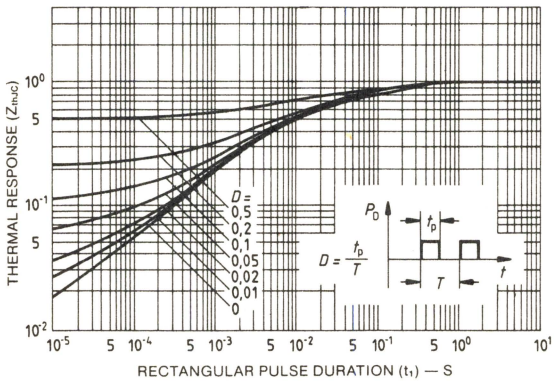


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

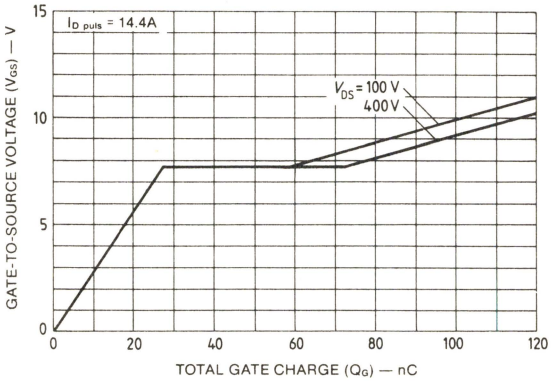


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ60

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 5.5A, 400V
- $r_{DS(on)} = 1.0\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

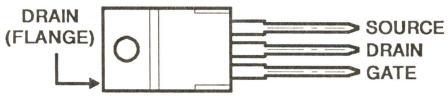
Description

The BUZ60 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ60 is supplied in the JEDEC TO-220AB plastic package.

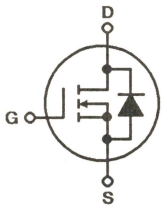
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ60	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current T_C = +35°C	I_D	5.5	A
Pulsed Drain Current T_C = +25°C	I_{DM}	22	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2260

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 400 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 2.5 A	—	0.9	1	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 2.5 A	1.7	2.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	1.5	2	pF
Output Capacitance	C_{oss}		—	120	180	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.7 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	30 40	45 60	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_r)	$t_{d(off)}$ t_r		— —	110 50	140 65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	5.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	22	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.15	1.6	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}	—	1000	—	ns
Reverse Recovered Charge	Q_{RR}	dI_F/dt = 100 A/μs, V_R = 100 V	—	5	—	μC

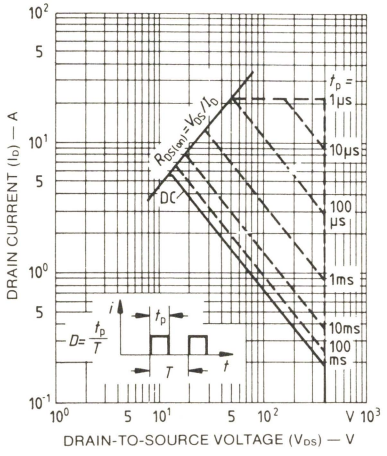


Fig. 1 - Maximum safe operating areas for all types.

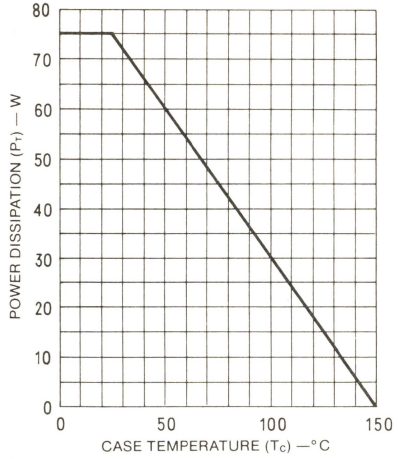


Fig. 2 - Power vs. temperature derating curve for all types.

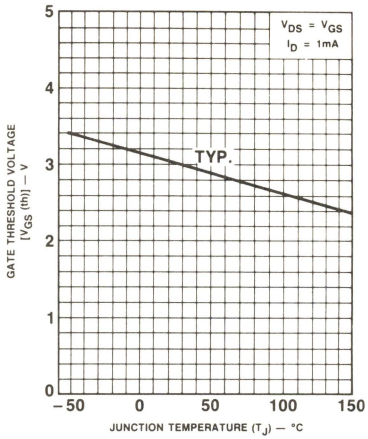


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

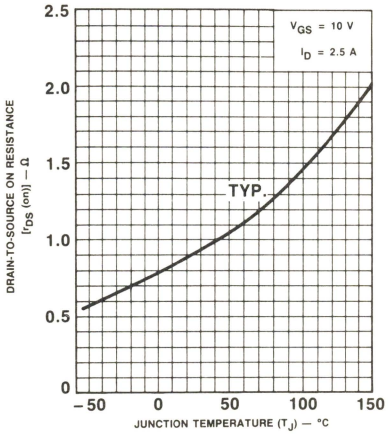


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

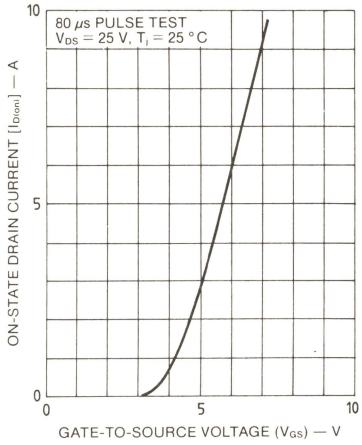


Fig. 5 - Typical transfer characteristics for all types.

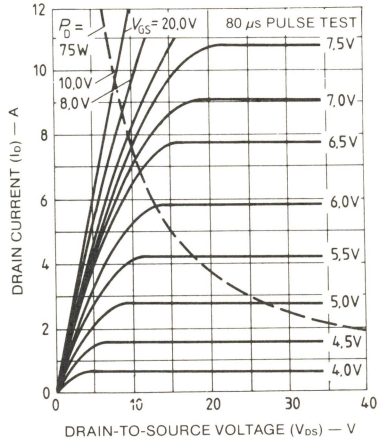


Fig. 6 - Typical output characteristics.

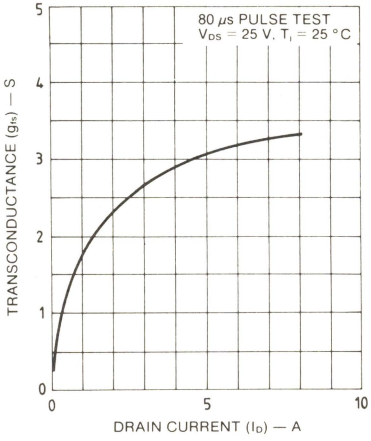


Fig. 7 - Typical transconductance vs. drain current.

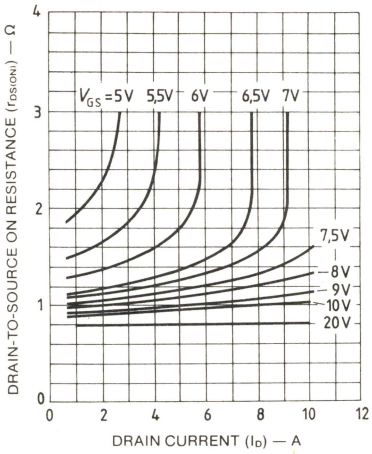


Fig. 8 - Typical on-resistance vs. drain current.

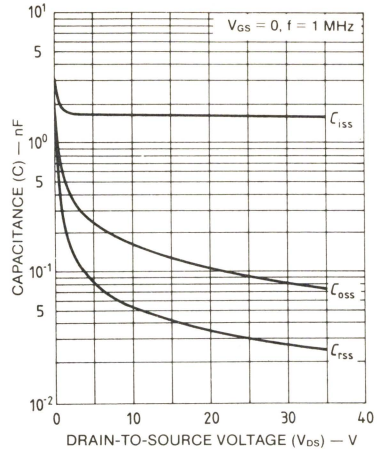


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

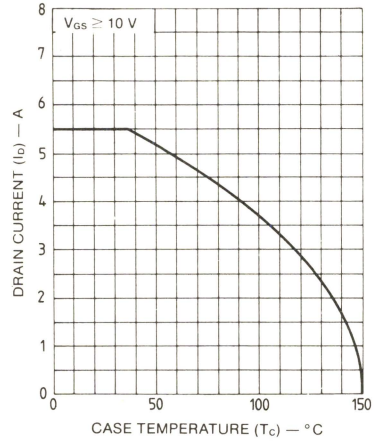


Fig. 10 - Maximum drain current vs. case temperature.

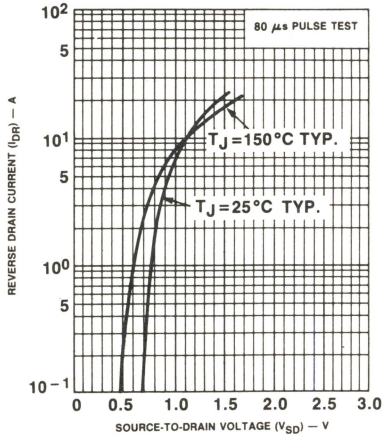


Fig. 11 - Typical source-drain diode forward voltage.

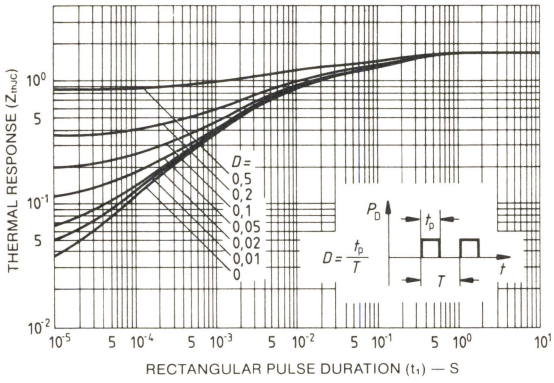


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

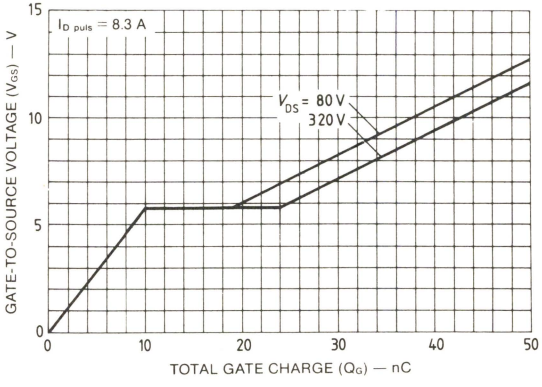


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ60B

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 4.5A, 400V
- $r_{DS(on)} = 1.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

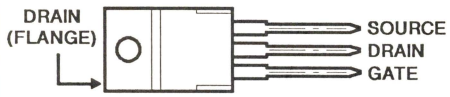
Description

The BUZ60B is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ60B is supplied in the JEDEC TO-220AB plastic package.

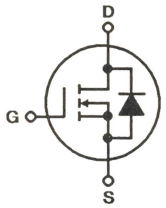
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ60B	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current T_C = +35°C	I_D	4.5	A
Pulsed Drain Current T_C = +25°C	I_{DM}	18	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	75	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2261

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V $I_D = 0.25$ mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ $I_D = 1$ mA	2.1	3	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$T_j = 25$ °C $T_j = 125$ °C $V_{DS} = 400$ V, $V_{GS} = 0$ V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 20$ V $V_{DS} = 0$ V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	$V_{GS} = 10$ V $I_D = 2.5$ A	—	1.2	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25$ V $I_D = 2.5$ A	1.7	2.5	—	S
Input Capacitance	C_{iss}	$V_{GS} = 0$ V $V_{DS} = 25$ V f = 1 MHz	—	1.5	2	pF
Output Capacitance	C_{oss}		—	120	180	pF
Reverse Transfer Capacitance	C_{rss}		—	35	60	pF
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	$V_{CC} = 30$ V $I_D = 2.6$ A $V_{GS} = 10$ V $R_{GS} = 50$ Ω	— —	30 40	45 60	ns ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	110 50	140 65	ns ns
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1.67			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	$T_C = 25$ °C	—	1.7	4.5	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	18	A
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ $V_{GS} = 0$ V, $T_j = 25$ °C	—	1.15	1.50	V
Reverse Recovery Time	t_{rr}	$T_j = 25$°C, $I_F = I_{DR}$	—	1000	—	ns
Reverse Recovered Charge	Q_{RR}	$dI_F/dt = 100$ A/μs, $V_R = 100$ V	—	5	—	μC

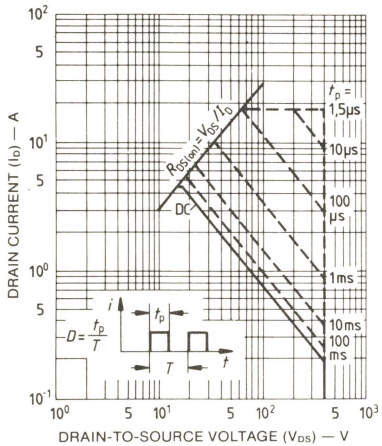


Fig. 1 - Maximum safe operating areas for all types.

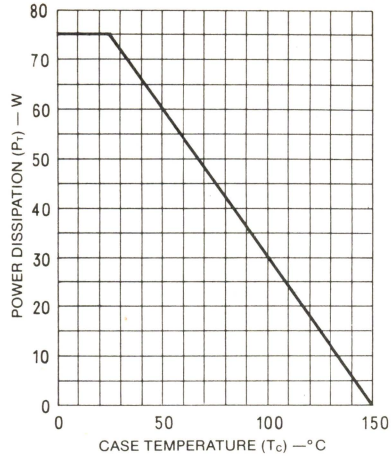


Fig. 2 - Power vs. temperature derating curve for all types.

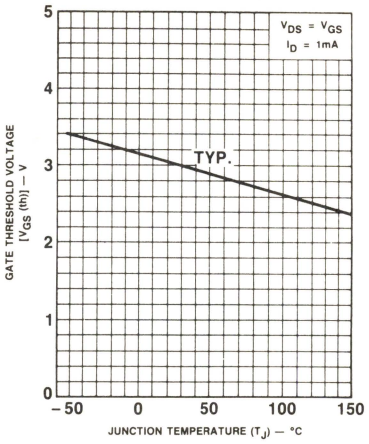


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

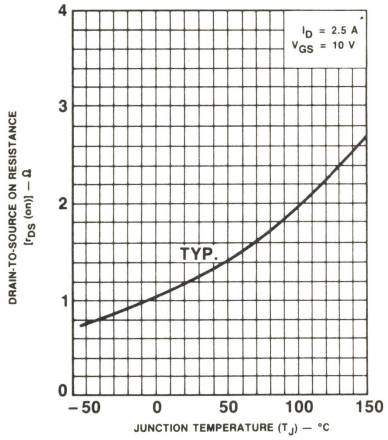


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

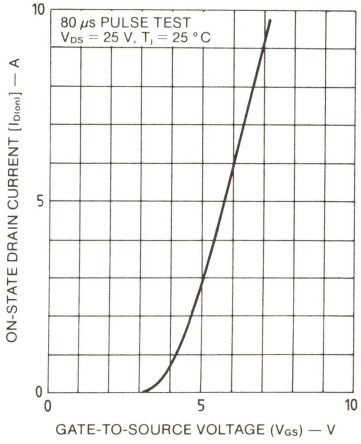


Fig. 5 - Typical transfer characteristics for all types.

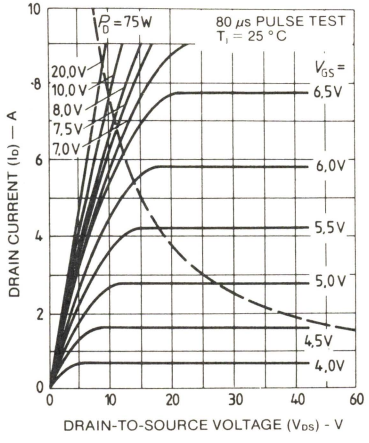


Fig. 6 - Typical output characteristics.

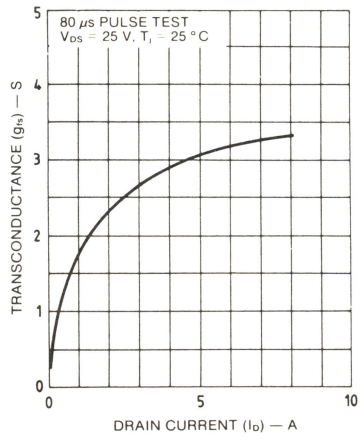


Fig. 7 - Typical transconductance vs. drain current.

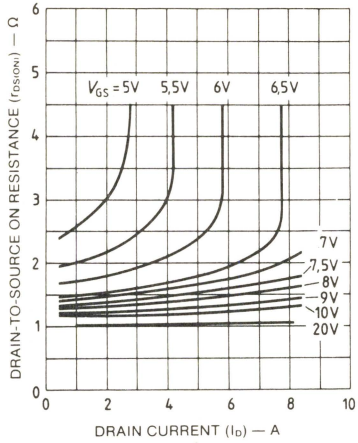


Fig. 8 - Typical on-resistance vs. drain current.

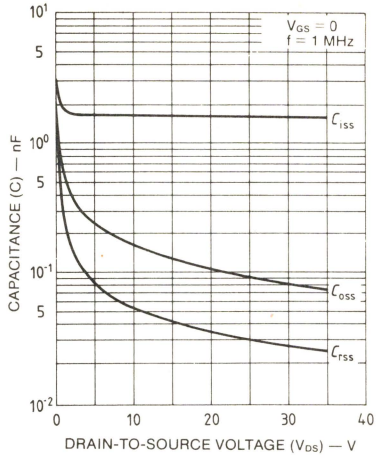


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

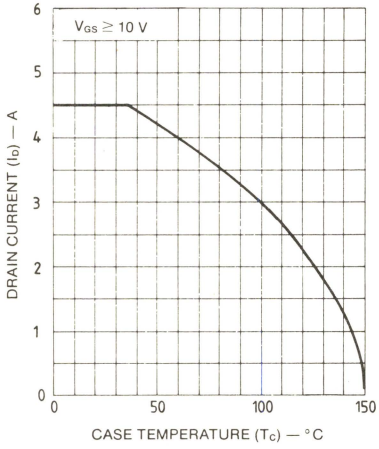


Fig. 10 - Maximum drain current vs. case temperature.

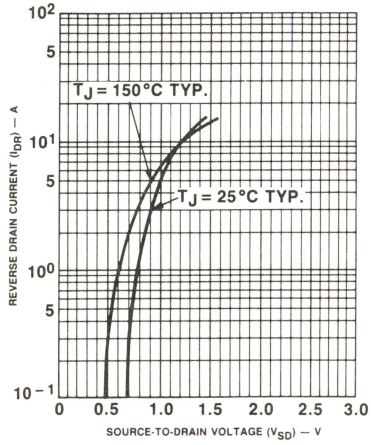


Fig. 11 - Typical source-drain diode forward voltage.

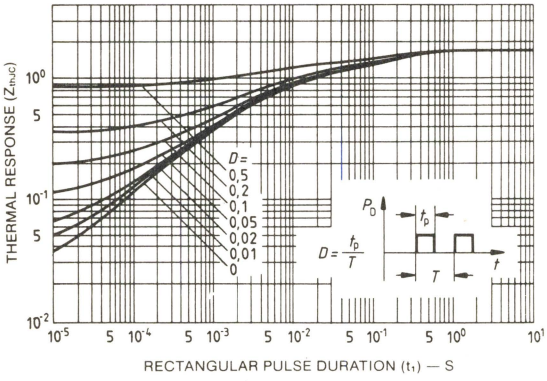


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

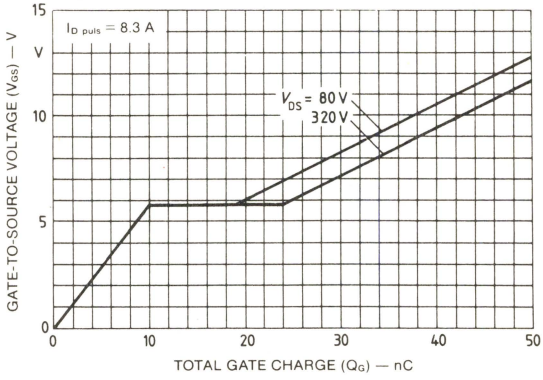


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ71

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 14A, 50V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

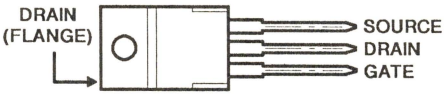
Description

The BUZ71 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ71 is supplied in the JEDEC TO-220AB plastic package.

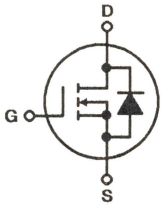
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ71	UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	50	V
Continuous Drain Current T_C = +55°C	I_D	14	A
Pulsed Drain Current T_C = +25°C	I_{DM}	56	A
Single Pulse Avalanche Energy*, EAS		100	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 10V, starting T_j = 25°C, L = 820μHy, I_{peak} = 14A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2418**

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = +25°C Unless Otherwise Specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	50	–	–	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 50 V, VGS = 0 V	– –	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	–	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9A	–	0.09	0.1	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	3.0	5.2	–	S
Input Capacitance	Ciss	VGS = 0 V	–	480	650	pF
Output Capacitance	Coss	VDS = 25 V	–	280	450	
Reverse Transfer Capacitance	Crss	f = 1 MHZ	–	160	280	
Turn-On Time ton	td(on)	Vcc = 30 V	–	20	30	ns
(ton = td(on) + tr)	tr	ID = 3 A	–	55	85	
Turn-Off Time toff	td(off)	VGS = 10 V	–	70	90	
(toff = td(off) = tr)	tr	RGS = 50 Ω	–	80	110	
Thermal Resistance, Junction-to-Case	RθJC			≤ 3.1		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤ 75		

*VDD = 10 V, starting Tj = 25°C, L = 820 µHy, Ipeak = 14 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	–	–	14	A
Pulsed Reverse Drain Current	IDRM		–	–	56	
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	–	1.6	1.8	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	–	120	–	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 30 V	–	0.15	–	µC

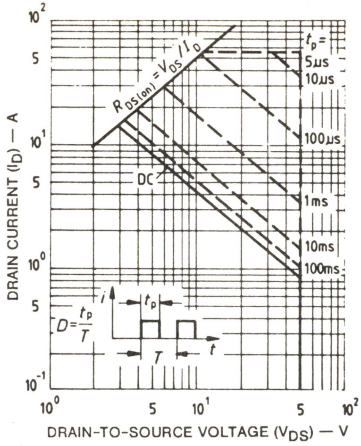


Figure 1 – Maximum safe operating areas for all types.

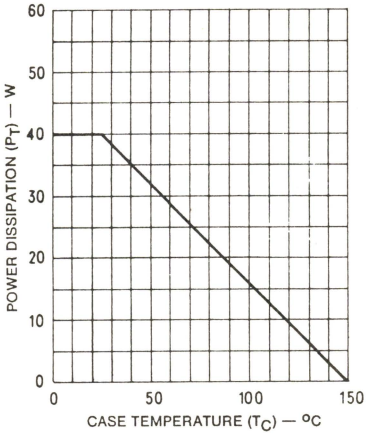


Figure 2 – Power vs temperature derating curve for all types.

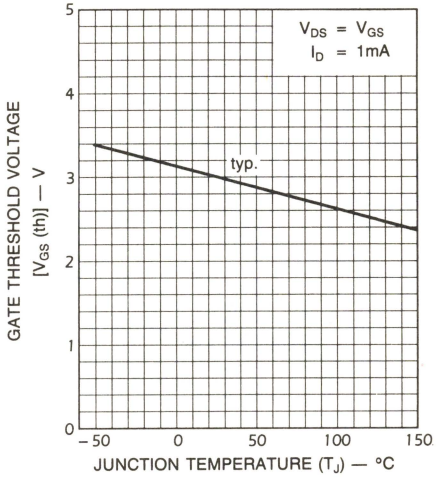


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

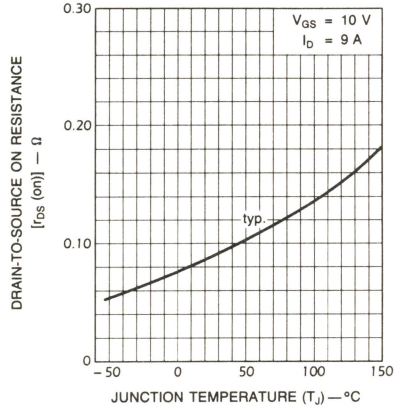


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

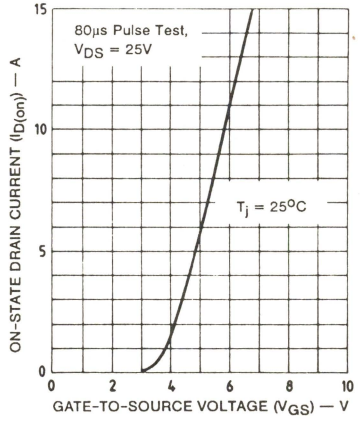


Figure 5 – Typical transfer characteristics for all types.

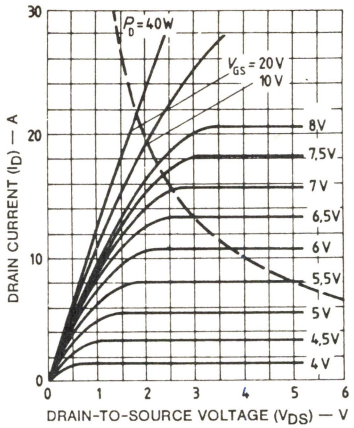


Figure 6 – Typical output characteristics.

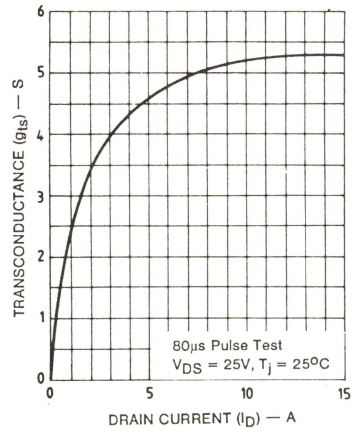


Figure 7 – Typical transconductance vs drain current.

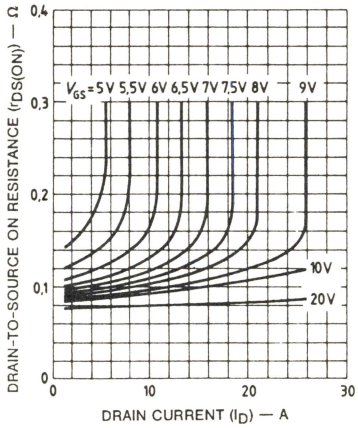


Figure 8 – Typical on-resistance vs drain current.

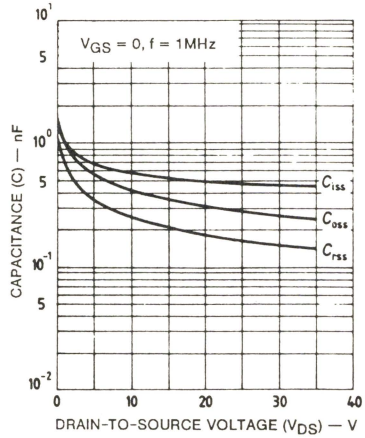


Figure 9 – Typical capacitance vs drain-to-source voltage.

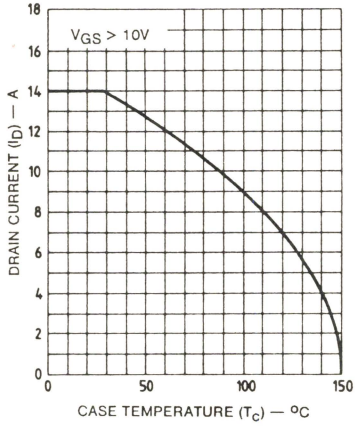


Figure 10 – Maximum drain current vs case temperature.

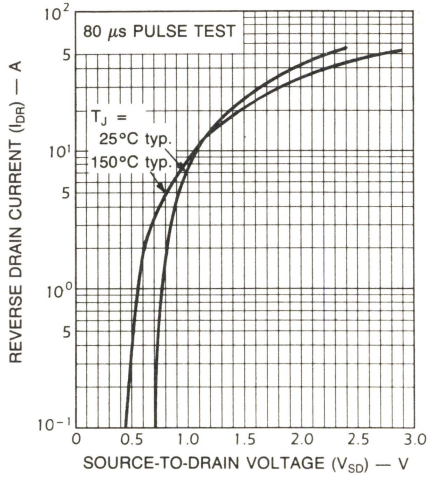


Figure 11 – Typical source-drain diode forward voltage.

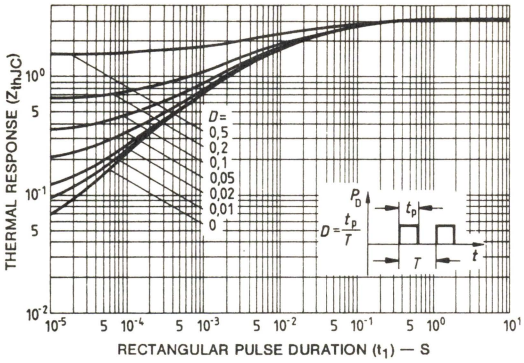


Figure 12 – Maximum effective transient thermal impedance, junction-to-case vs pulse duration

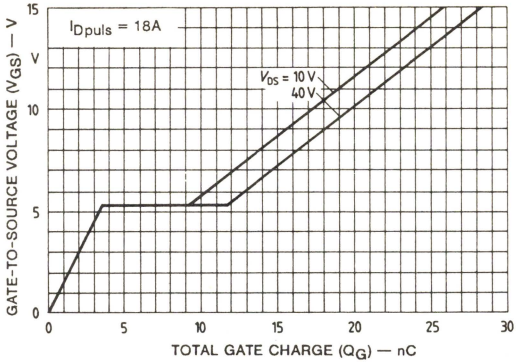


Figure 13 – Typical gate charge vs gate-to-source voltage.

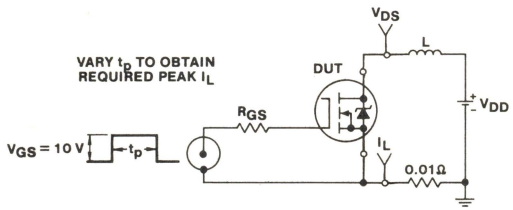


Figure 14 – Unclamped energy test circuit.

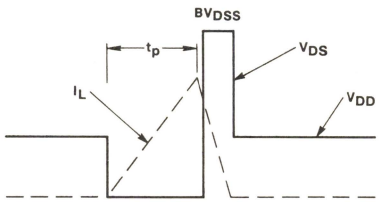


Figure 15 – Unclamped energy test waveforms.

HARRIS

BUZ71A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 13A, 50V
- $r_{DS(on)} = 0.12\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

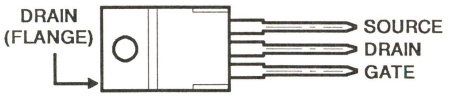
Description

The BUZ71A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ71A is supplied in the JEDEC TO-220AB plastic package.

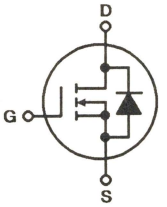
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ71A	UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	50	V
Continuous Drain Current			
T_C = +55°C	I_D	13	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	48	A
Single Pulse Avalanche Energy*, EAS		100	mj
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

*V_{DD} = 10V, starting T_j = +25°C, L = 820μHy, I_{peak} = 14A, see Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2419

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = +25°C Unless Otherwise Specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	50	-	-	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 50 V, VGS = 0 V	- -	20 100	250 1000	µA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	-	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9A	-	0.11	0.12	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	3.0	5.2	-	S
Input Capacitance	Ciss	VGS = 0 V	-	480	650	pF
Output Capacitance	Coss	VDS = 25 V	-	280	450	
Reverse Transfer Capacitance	Crss	f = 1 MHZ	-	160	280	
Turn-On Time ton	td(on)	Vcc = 30 V	-	20	30	ns
(ton = td(on) + tr)	tr	ID = 3 A	-	55	85	
Turn-Off Time toff	td(off)	VGS = 10 V	-	70	90	
(toff = td(off) = tr)	tr	RGS = 50 Ω	-	80	110	
Thermal Resistance, Junction-to-Case	RθJC			≤3.1		°C/W
Thermal Resistance, Junction-to-Ambient	RθJA			≤75		

*VDD = 10 V, starting Tj = 25°C, L = 820 µHy, Ipeak = 14 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Continuous Reverse Drain Current	IDR	Tc = 25°C	-	-	13	A
Pulsed Reverse Drain Current	IDRM		-	-	52	
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	-	1.6	2.2	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	-	120	-	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/µs, VR = 30 V	-	0.15	-	µC

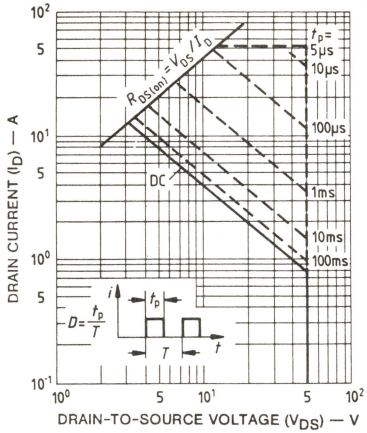


Figure 1 – Maximum safe operating areas for all types.

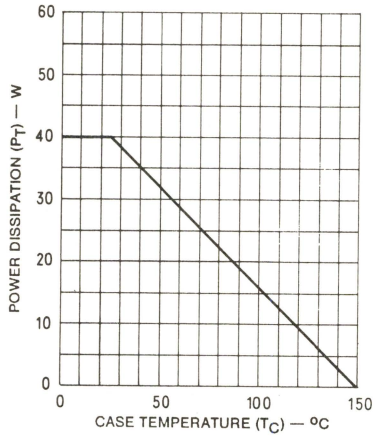


Figure 2 – Power vs temperature derating curve for all types.

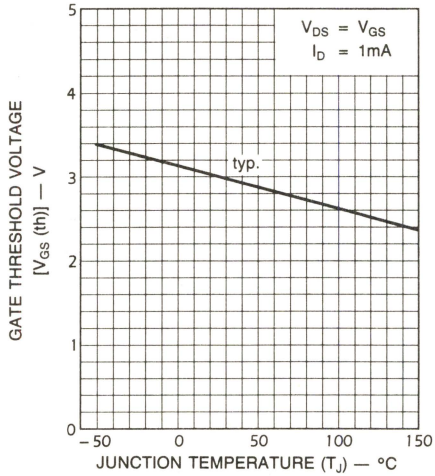


Figure 3 – Normalized gate threshold voltage as a function of junction temperature for all types.

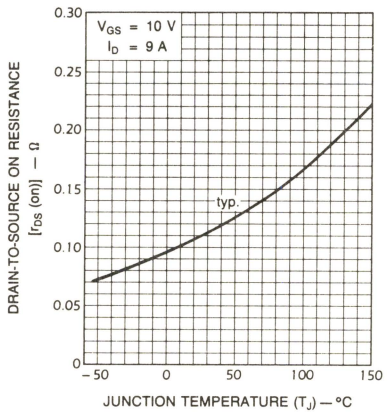


Figure 4 – Normalized drain-to-source on resistance to junction temperature for all types.

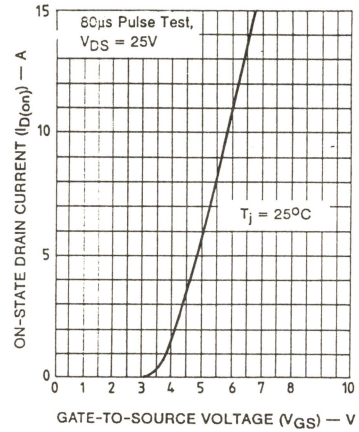


Figure 5 – Typical transfer characteristics for all types.

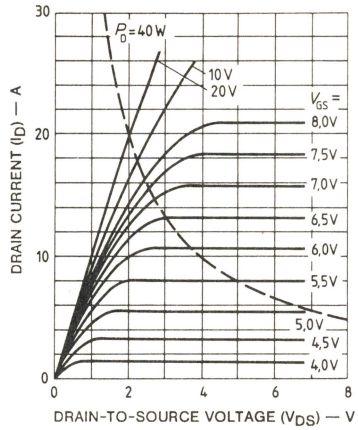


Figure 6 - Typical output characteristics.

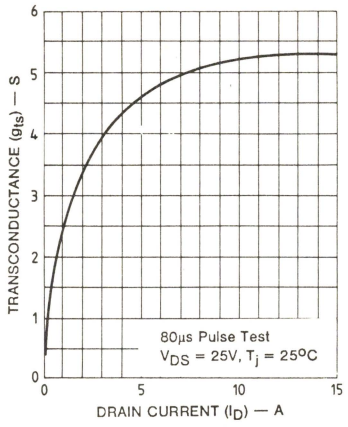


Figure 7 - Typical transconductance vs drain current.

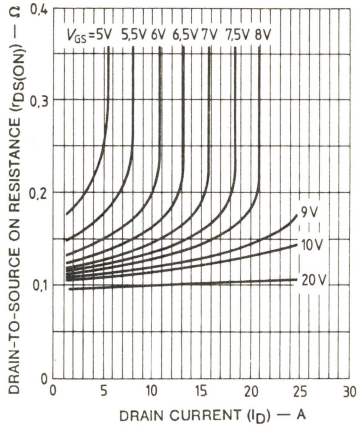


Figure 8 - Typical on-resistance vs drain current.

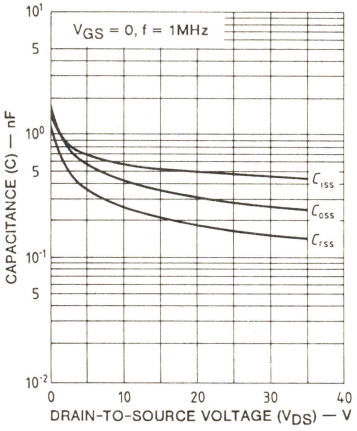


Figure 9 - Typical capacitance vs drain-to-source voltage.

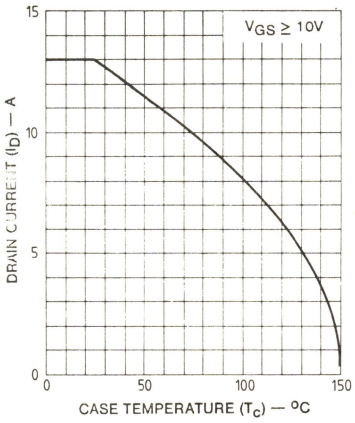


Figure 10 - Maximum drain current vs case temperature.

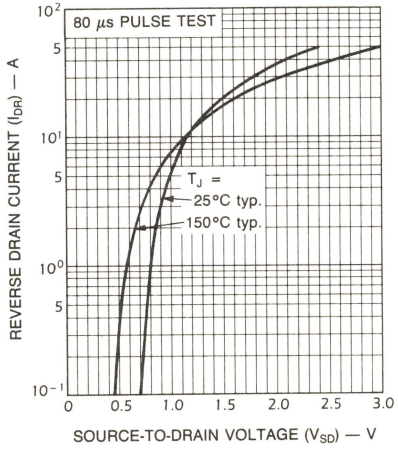


Figure 11 - Typical source-drain diode forward voltage.

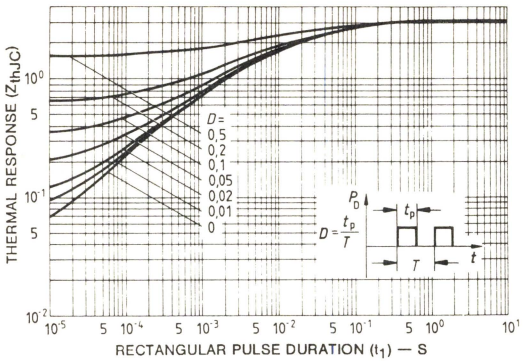


Figure 12 - Maximum effective transient thermal impedance, junction-to-case vs pulse duration

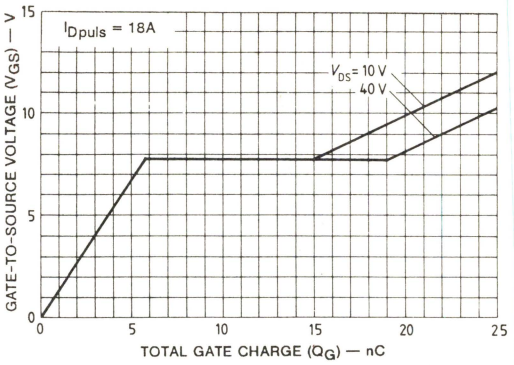


Figure 13 - Typical gate charge vs gate-to-source voltage.

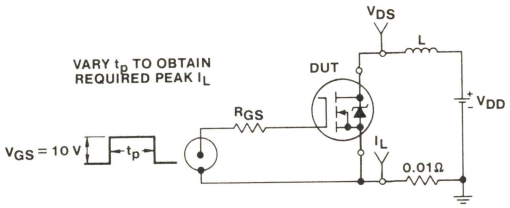


Figure 14 - Unclamped energy test circuit.

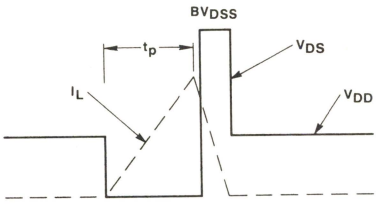


Figure 15 - Unclamped energy test waveforms.

HARRIS

BUZ72A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 9A, 100V
- $r_{DS(on)} = 0.25\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

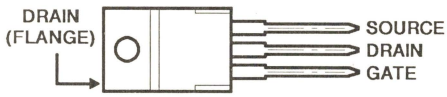
Description

The BUZ72A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ72A is supplied in the JEDEC TO-220AB plastic package.

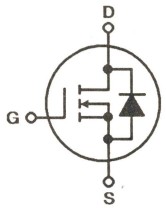
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ72A	UNITS
Drain-Source Voltage	V_{DS}	100	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	100	V
Continuous Drain Current			
T_C = +25°C	I_D	9	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	36	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2262

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	100	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 100 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 5 A	—	0.23	0.25	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 5 A	2.7	3.8	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	450	600	pF
Output Capacitance	C_{oss}		—	150	240	
Reverse Transfer Capacitance	C_{rss}		—	80	130	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.9 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	20 45	30 70	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_f)	$t_{d(off)}$ t_f		— —	70 55	90 70	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 3.1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	9	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	36	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.5	2	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, I_F = I_{DR} dI_F/dt = 100 A/μs, V_R = 30 V	—	170	—	ns
Reverse Recovered Charge	Q_{RR}		—	0.30	—	μC

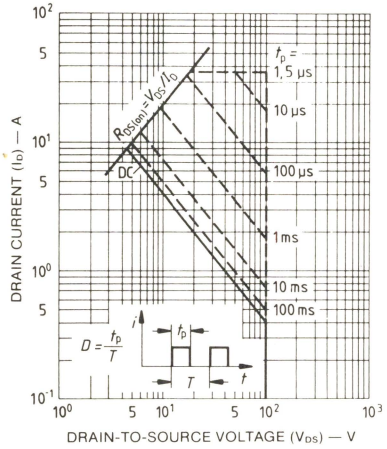


Fig. 1 - Maximum safe operating areas for all types.

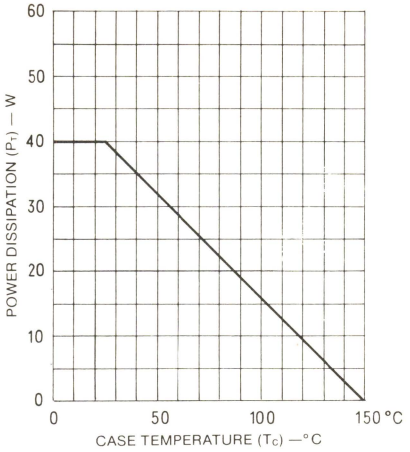


Fig. 2 - Power vs. temperature derating curve for all types.

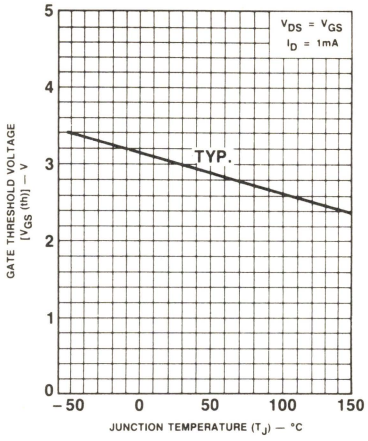


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

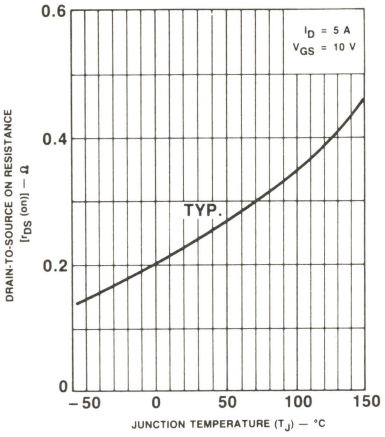


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

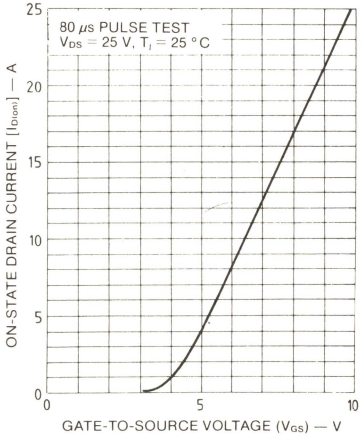


Fig. 5 - Typical transfer characteristics for all types.

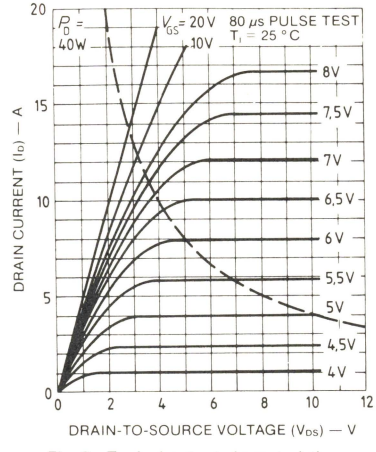


Fig. 6 - Typical output characteristics.

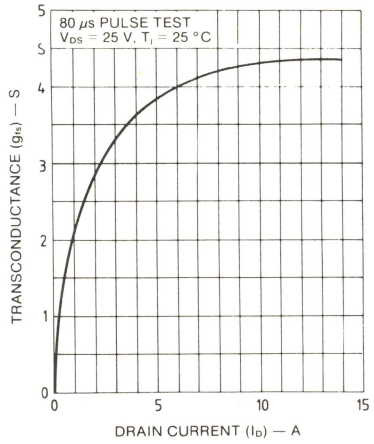


Fig. 7 - Typical transconductance vs. drain current.

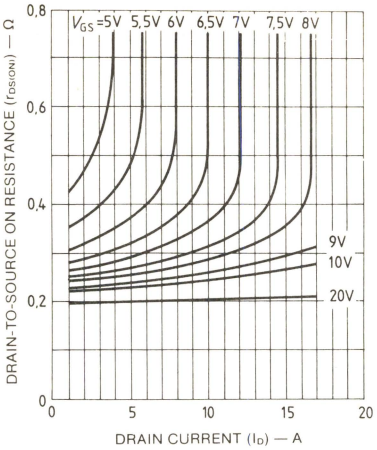


Fig. 8 - Typical on-resistance vs. drain current.

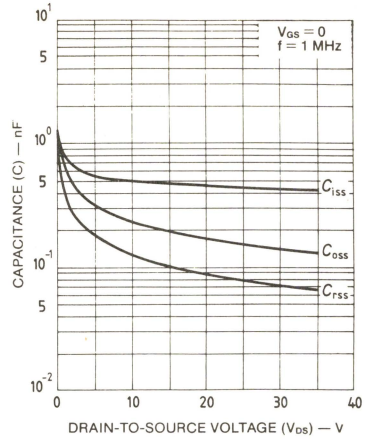


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

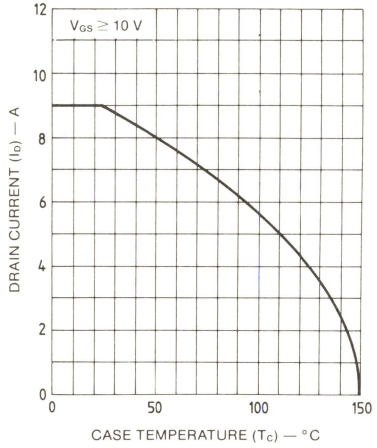


Fig. 10 - Maximum drain current vs. case temperature.

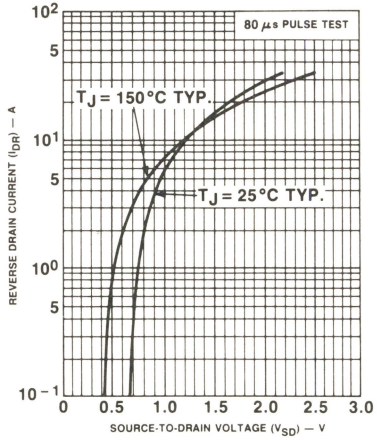


Fig. 11 - Typical source-drain diode forward voltage.

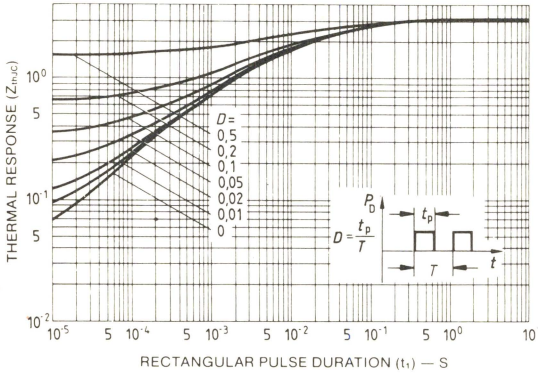


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

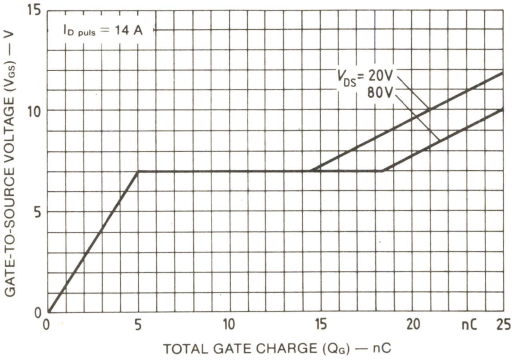


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ73A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 5.8A, 200V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

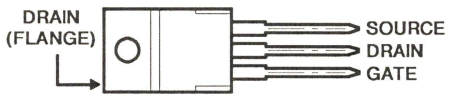
Description

The BUZ73A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ73A is supplied in the JEDEC TO-220AB plastic package.

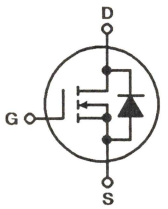
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		BUZ73A	UNITS
Drain-Source Voltage	V_{DS}	200	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	200	V
Continuous Drain Current, T_C = +25°C	I_D	5.8	A
Pulsed Drain Current, T_C = +25°C	I_{DM}	23	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation, T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2263

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	200	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 200 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 3.5 A	—	0.5	0.6	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 3.5 A	2.2	3.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	450	600	pF
Output Capacitance	C_{oss}		—	100	160	
Reverse Transfer Capacitance	C_{rss}		—	50	80	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.8 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	15 40	20 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	70 40	90 55	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 3.1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	5.8	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	23	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ V_{GS} = 0 V, T_j = 25 °C	—	1.4	1.7	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, $I_F = I_{DR}$ dI_F/dt = 100 A/μs, V_R = 100 V	—	200	—	ns
Reverse Recovered Charge	Q_{RR}		—	0.6	—	μC

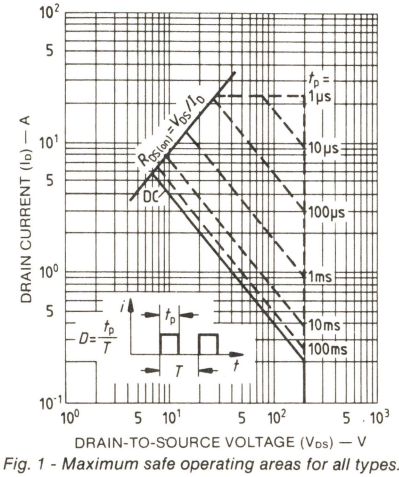


Fig. 1 - Maximum safe operating areas for all types.

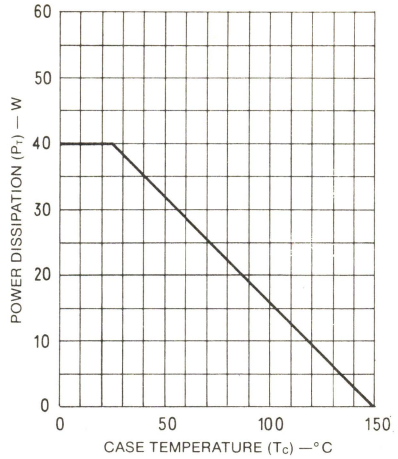


Fig. 2 - Power vs. temperature derating curve for all types.

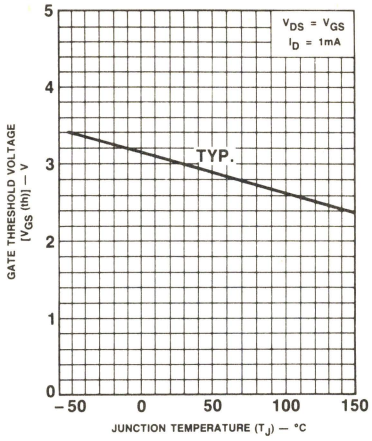


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

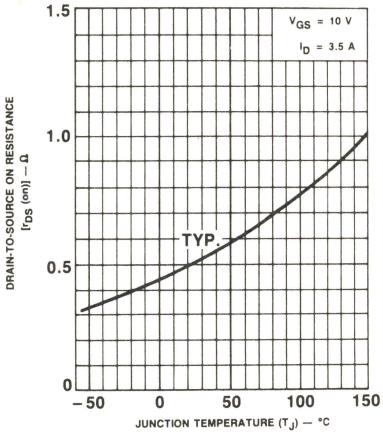


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

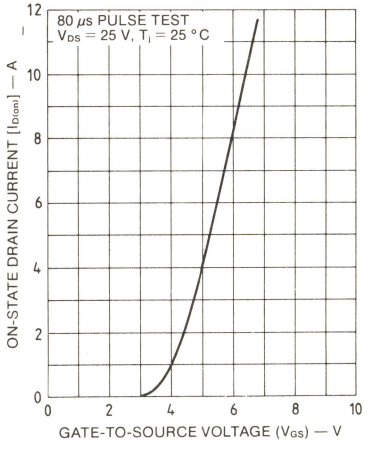


Fig. 5 - Typical transfer characteristics for all types.

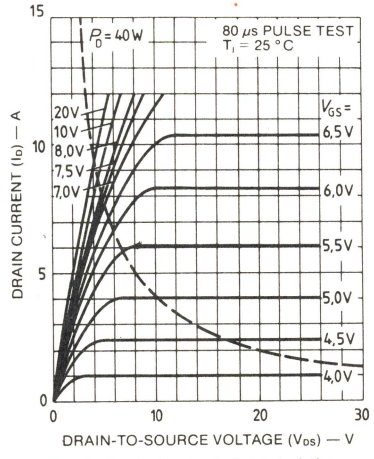


Fig. 6 - Typical output characteristics.

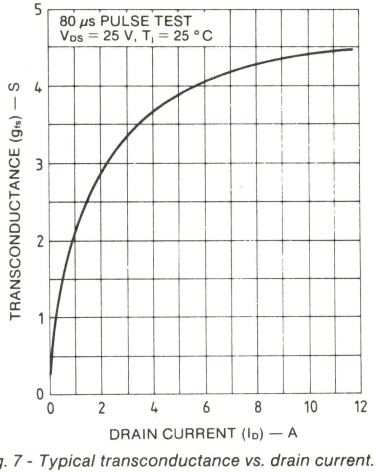


Fig. 7 - Typical transconductance vs. drain current.

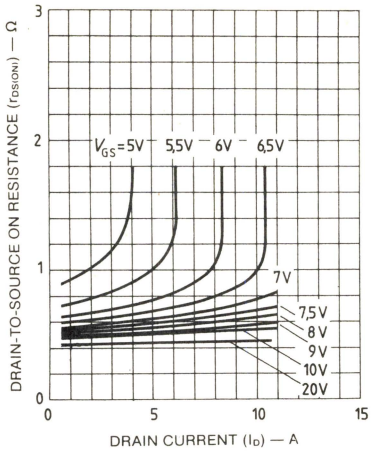


Fig. 8 - Typical on-resistance vs. drain current.

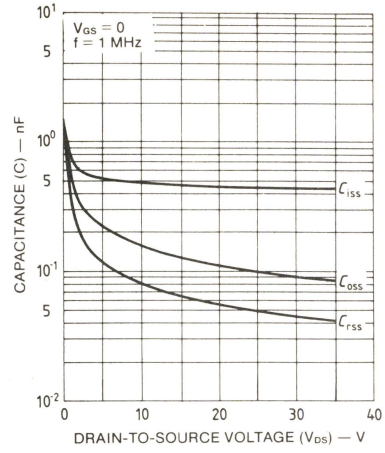


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

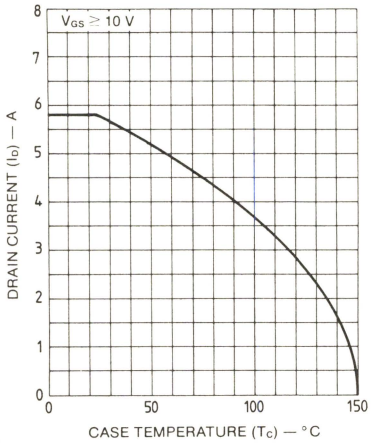


Fig. 10 - Maximum drain current vs. case temperature.

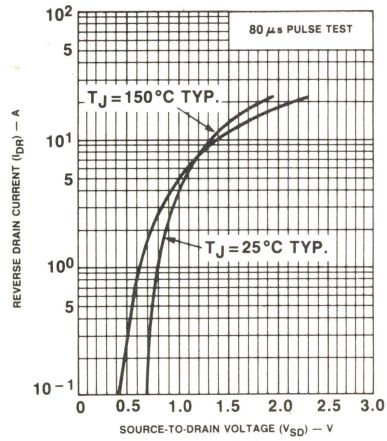


Fig. 11 - Typical source-drain diode forward voltage.

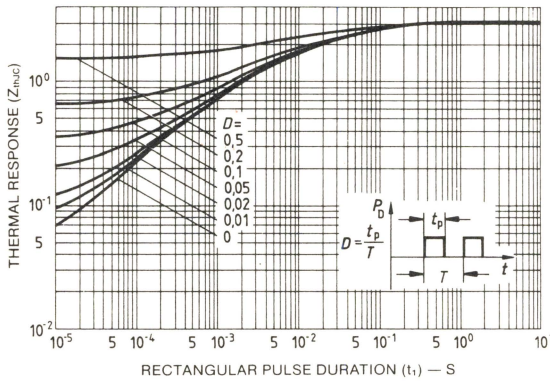


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

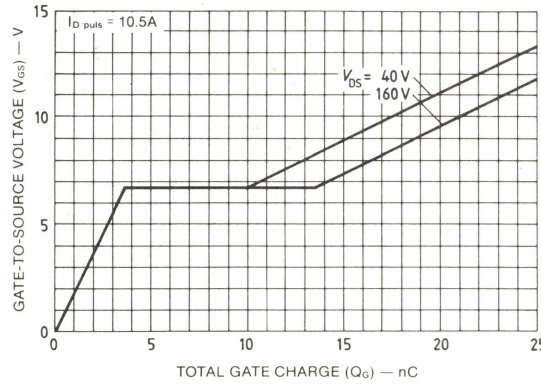


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ76

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 3A, 400V
- $r_{DS(on)} = 1.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

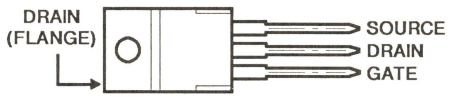
Description

The BUZ76 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ76 is supplied in the JEDEC TO-220AB plastic package.

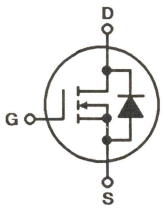
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ76	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current			
T_C = +35°C	I_D	3	A
Pulsed Drain Current			
T_C = +25°C	I_{DM}	12	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2264

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 400 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 1.5 A	—	1.65	1.8	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 3 A	2.1	2.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	300	500	pF
Output Capacitance	C_{oss}		—	50	80	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.5 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	15 40	20 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	50 30	65 40	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 3.1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	3	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	12	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.1	1.4	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR} dI_F/dt = 100 A/μs, V_R = 100 V	—	300	—	ns
Reverse Recovered Charge	Q_{RR}		—	2.5	—	μC

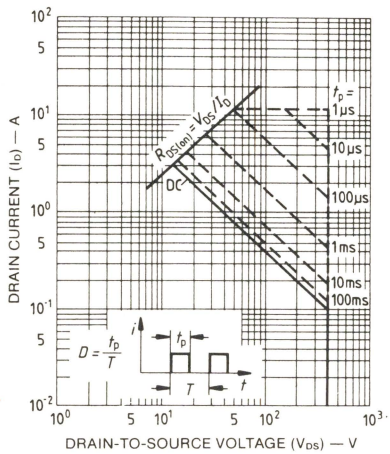


Fig. 1 - Maximum safe operating areas for all types.

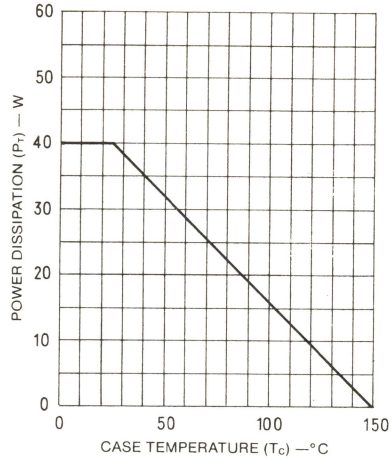


Fig. 2 - Power vs. temperature derating curve for all types.

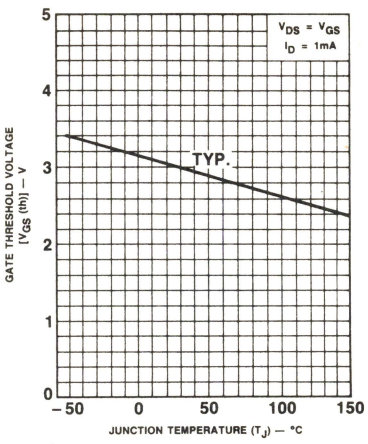


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

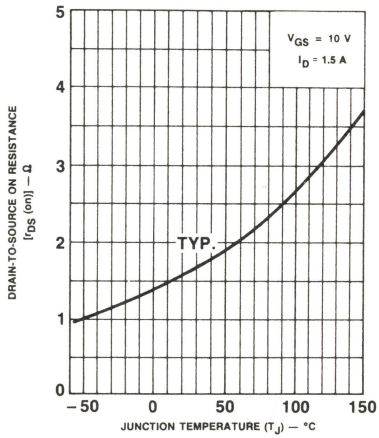


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

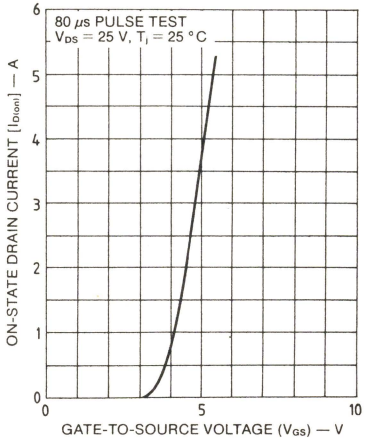


Fig. 5 - Typical transfer characteristics for all types.

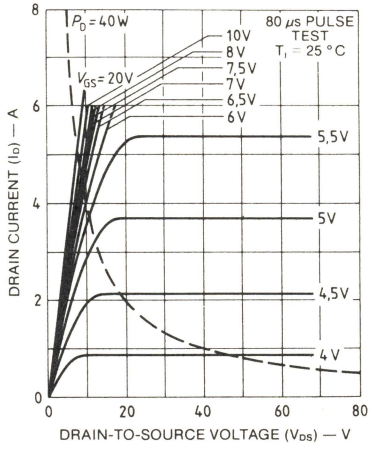


Fig. 6 - Typical output characteristics.

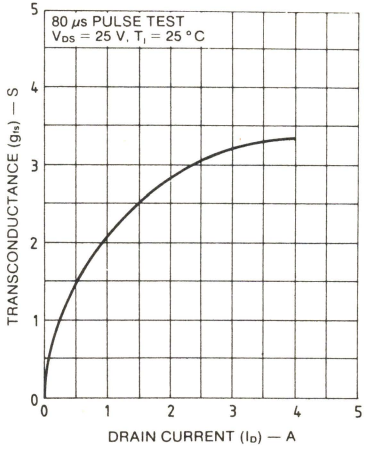


Fig. 7 - Typical transconductance vs. drain current.

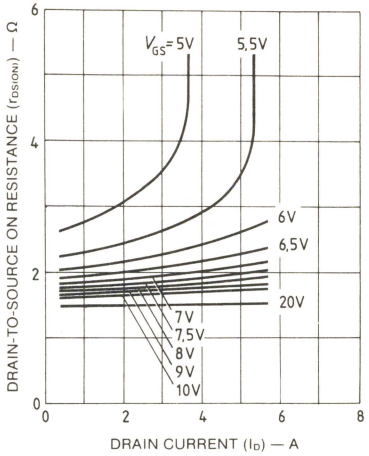


Fig. 8 - Typical on-resistance vs. drain current.

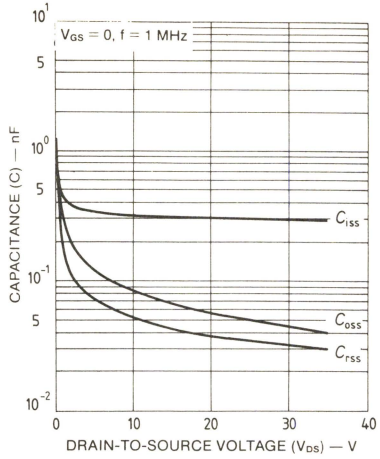


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

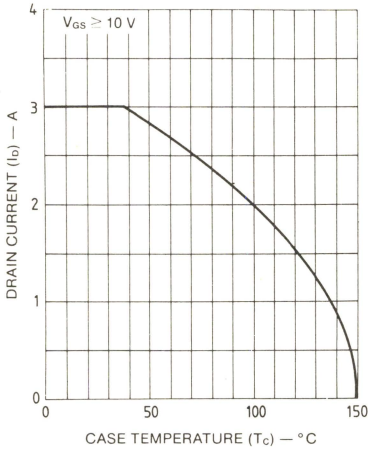


Fig. 10 - Maximum drain current vs. case temperature.

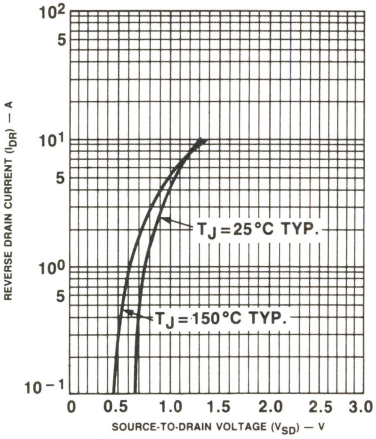


Fig. 11 - Typical source-drain diode forward voltage.

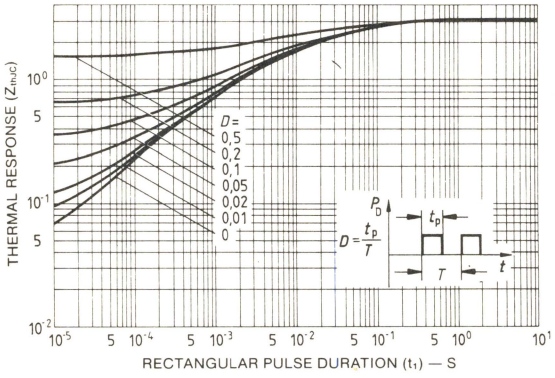


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

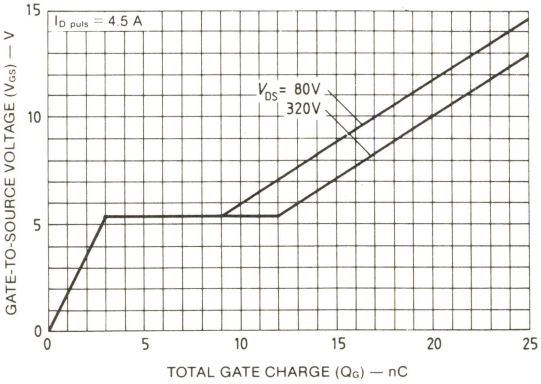


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

BUZ76A

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 2.6A, 400V
- $r_{DS(on)} = 2.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

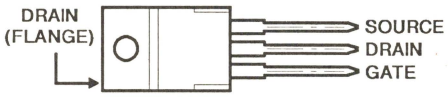
Description

The BUZ76A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ76A is supplied in the JEDEC TO-220AB plastic package.

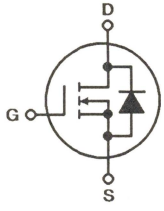
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ76A	UNITS
Drain-Source Voltage	V_{DS}	400	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	400	V
Continuous Drain Current, T_C = +30°C	I_D	2.6	A
Pulsed Drain Current, T_C = +25°C	I_{DM}	10	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation, T_C = +25°C	P_D	40	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2265

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	400	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 400 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 1.5 A	—	2.2	2.5	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 1.5 A	2.1	2.5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	300	500	pF
Output Capacitance	C_{oss}		—	50	80	
Reverse Transfer Capacitance	C_{rss}		—	35	60	
Turn-On Time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.4 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	15 40	20 60	ns
Turn-Off Time t_{off} ($t_{off} = t_{d(off)} + t_r$)	$t_{d(off)}$ t_r		— —	50 30	65 40	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 3.1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 75			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	2.6	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	10	
Diode Forward Voltage	V_{SD}	$I_F = 2 \times I_{DR}$ V_{GS} = 0 V, T_j = 25 °C	—	1.1	1.4	V
Reverse Recovery Time	t_{rr}	T_j = 25° C, $I_F = I_{DR}$ dI_F/dt = 100 A/μs, V_R = 100 V	—	300	—	ns
Reverse Recovered Charge	Q_{RR}		—	2.5	—	μC

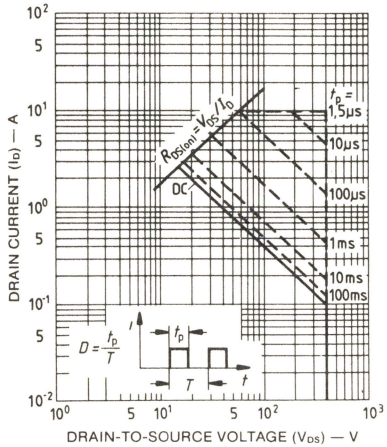


Fig. 1 - Maximum safe operating areas for all types.

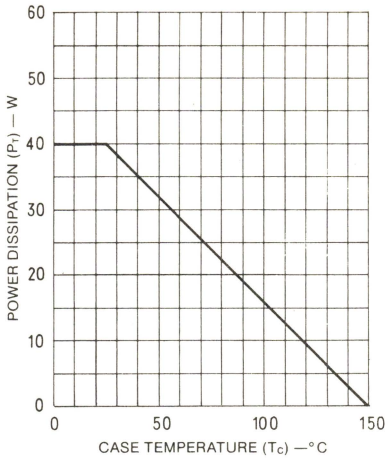


Fig. 2 - Power vs. temperature derating curve for all types.

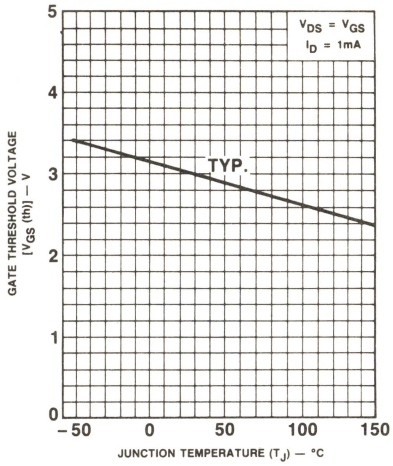


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

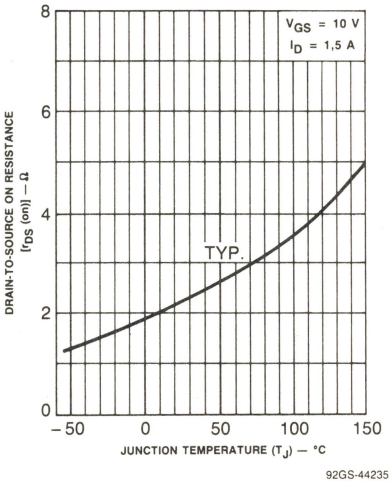


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

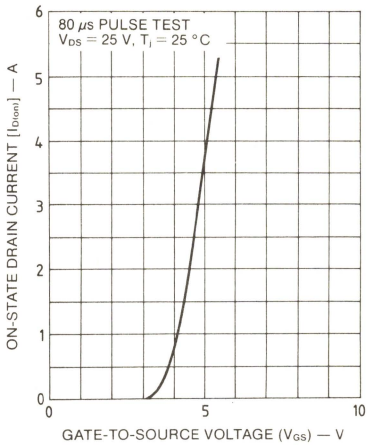


Fig. 5 - Typical transfer characteristics for all types.

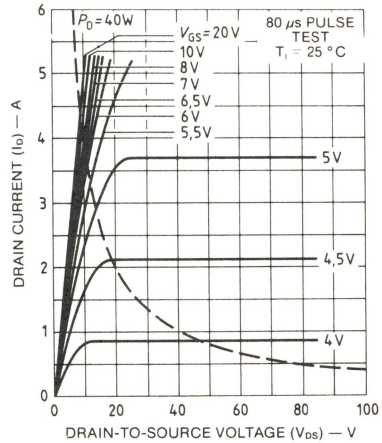


Fig. 6 - Typical output characteristics.

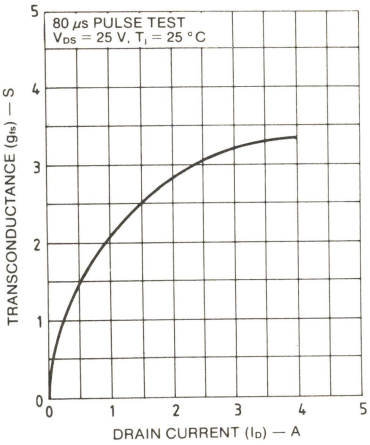


Fig. 7 - Typical transconductance vs. drain current.

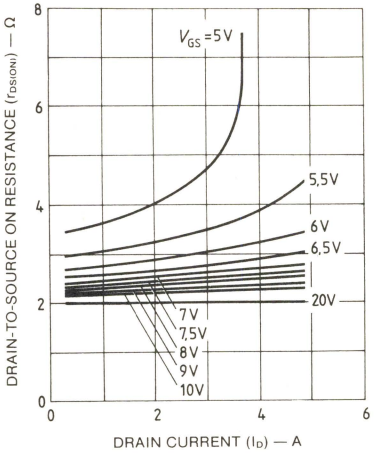


Fig. 8 - Typical on-resistance vs. drain current.

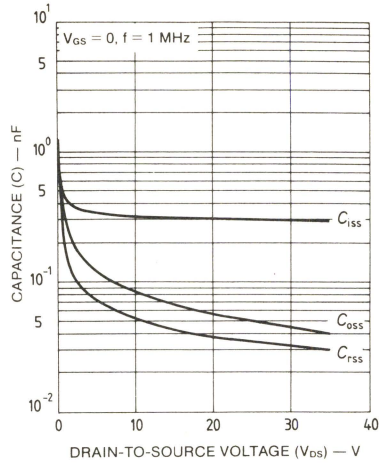


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

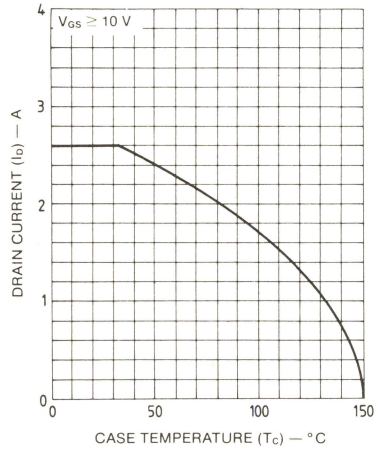


Fig. 10 - Maximum drain current vs. case temperature.

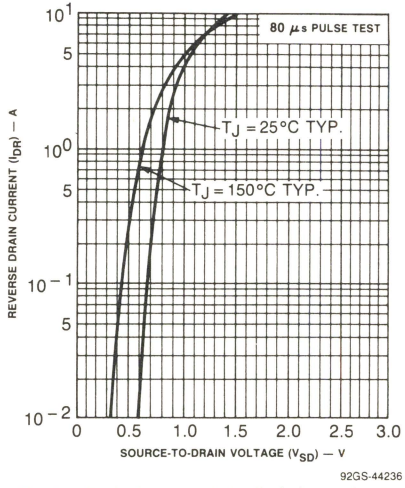


Fig. 11 - Typical source-drain diode forward voltage.

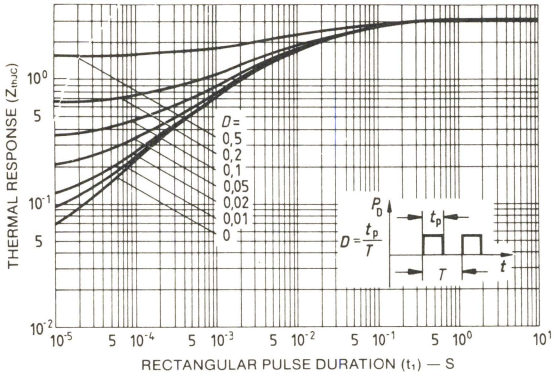


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

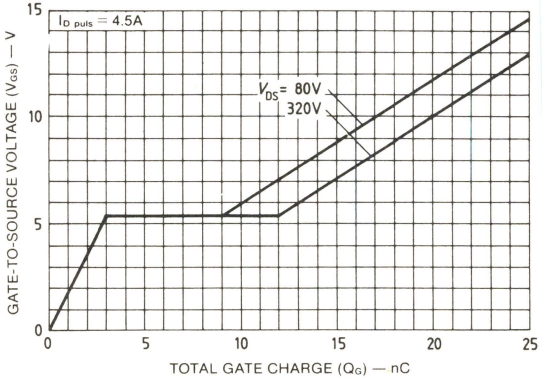


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

HARRIS

IRF120, IRF121 IRF122, IRF123

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 8.0A and 9.2A, 80V - 100V
- $r_{DS(on)}$ = 0.27Ω and 0.36Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

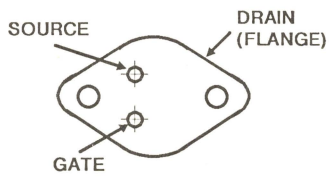
Description

The IRF120, IRF121, IRF122, and IRF123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF120	IRF121	IRF122	IRF123	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	9.2	9.2	8.0	8.0	A
T_C = +100°C ..... I_D	6.5	6.5	5.6	5.6	A
Pulsed Drain Current (3) ..... I_{DM}	37	37	32	32	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	60	60	60	60	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figures 14 and 15, L = 100μH)	32	32	28	28	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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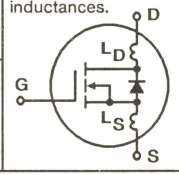
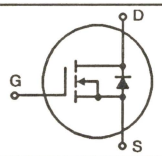
File Number 1565.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF120, IRF122	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	100	-	-	V
IRF121, IRF123			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +150°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF120, IRF121	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	9.2	-	-	A
IRF122, IRF123			8.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF120, IRF121	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.6A	-	0.25	0.27	Ω
IRF122. IRF123			-	0.27	0.36	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 5.6A	2.9	4.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	350	-	pF
Output Capacitance	C_{OSS}		-	130	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	36	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 9.2A, rd = 5.1Ω, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	8.8	13	ns
Rise Time	t_r		-	30	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	19	29	ns
Fall Time	t_f		-	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	9.7	15	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	2.3	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = 9.2A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	55	110	240	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	0.25	0.53	1.10	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5)

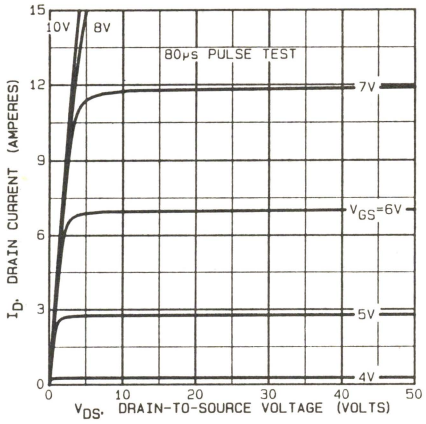


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

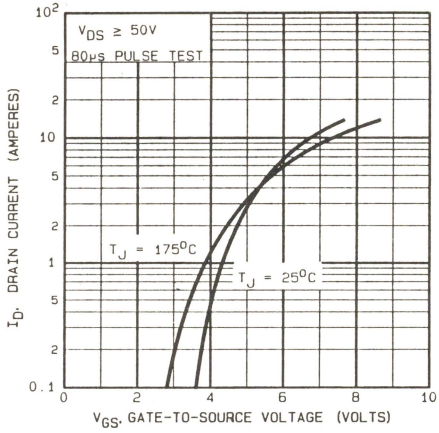


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

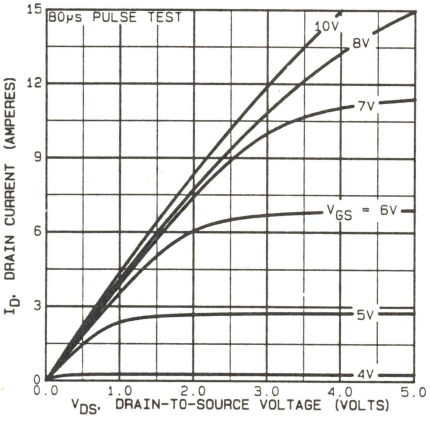


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

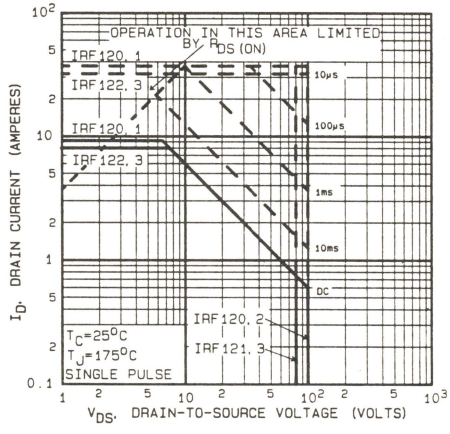


FIGURE 4. MAXIMUM SAFE OPERATING AREA

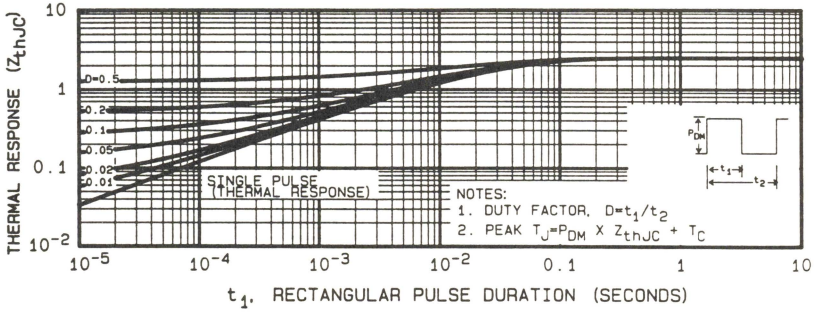


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE vs PULSE DURATION

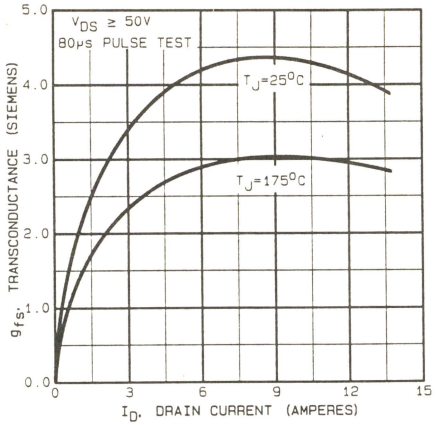


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

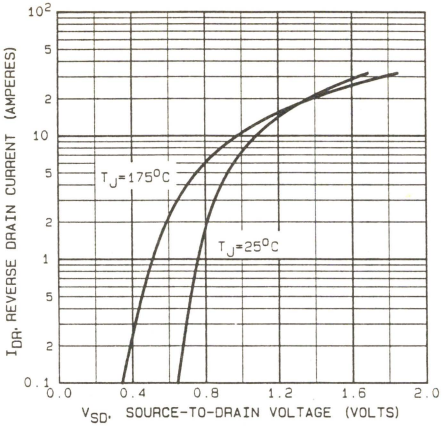


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

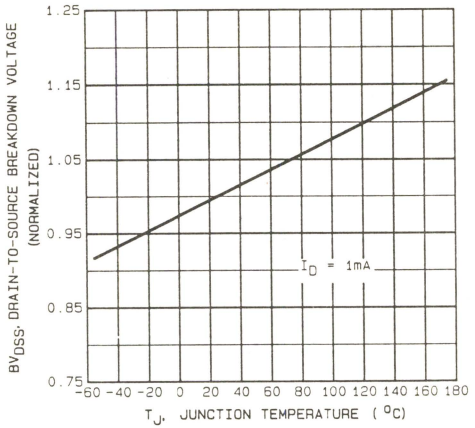


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

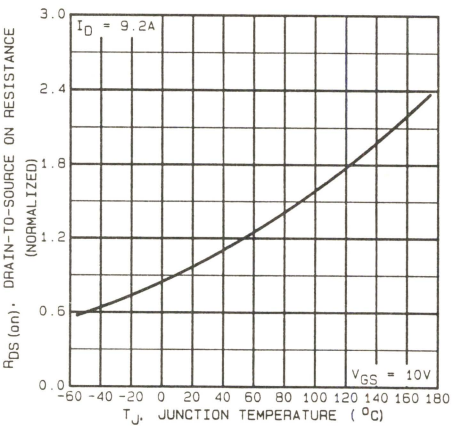


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

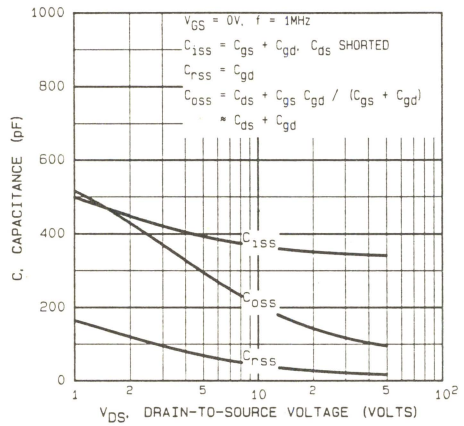


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

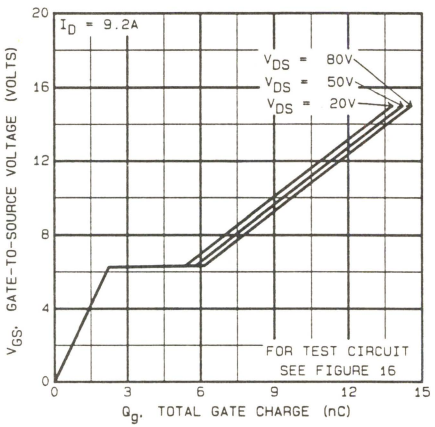


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

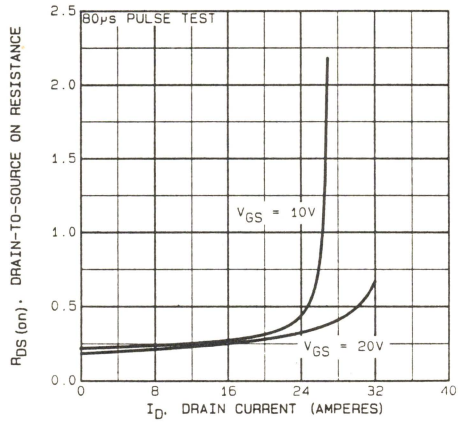


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

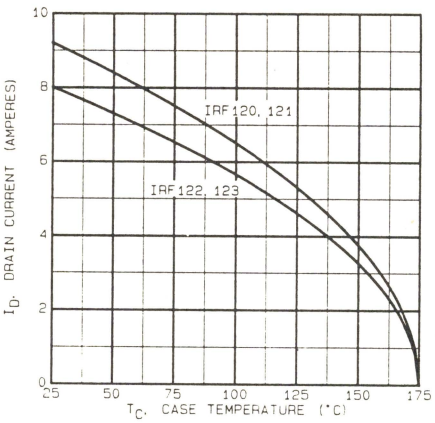


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

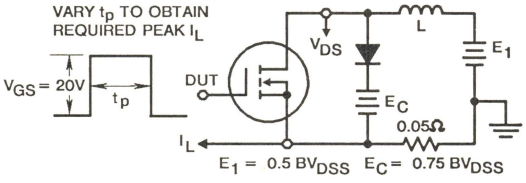


FIGURE 14. CLAMPED INDUCTIVE TEST CIRCUIT

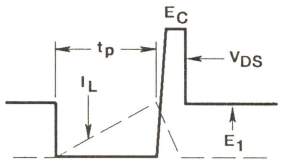


FIGURE 15. CLAMPED INDUCTIVE WAVEFORMS

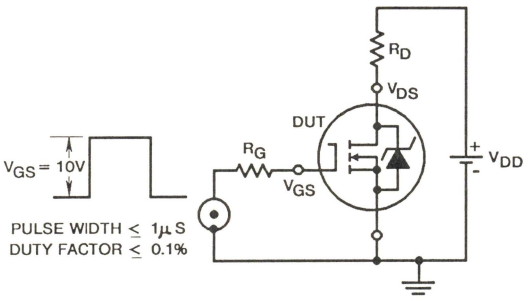


FIGURE 16. SWITCHING TIME TEST CIRCUIT

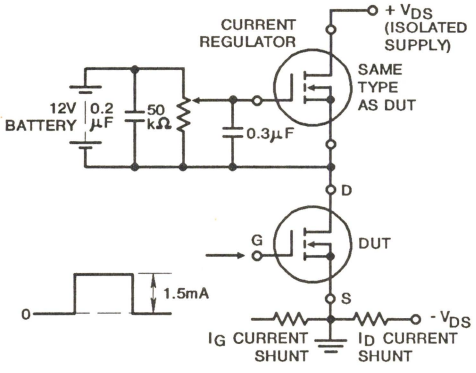


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF130/131/132/133
IRF130R/131R/132R/133R

N-Channel Power MOSFETs
Avalanche Energy Rated*

May 1992

Features

- 12A and 14A, 80V - 100V
- $r_{DS(on)}$ = 0.16Ω and 0.23Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

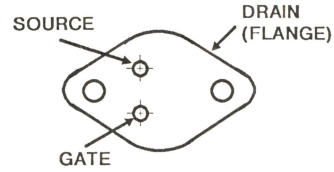
Description

The IRF130, IRF131, IRF132, and IRF133 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF130R, IRF131R, IRF132R, and IRF133R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

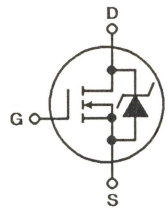
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF130 IRF130R	IRF131 IRF131R	IRF132 IRF132R	IRF133 IRF133R	UNITS
Drain-Source Voltage (1)	V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	100	80	10	80	V
Continuous Drain Current						
T_C = +25°C	I_D	14	14	12	12	A
T_C = +100°C	I_D	9.9	9.9	8.3	8.3	A
Pulsed Drain Current (3)	I_{DM}	56	56	48	48	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation	P_D	79	79	79	79	W
Linear Derating Factor		0.53	0.53	0.53	0.53	W/°C
Inductive Current, Clamped (See Figure 14, L = 100μH)	I_{LM}	56	56	48	48	A
Single Pulse Avalanche Energy Rating (4)	E_{as}*	50	50	50	50	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 380μH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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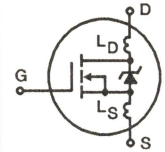
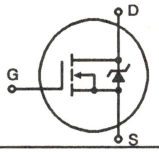
File Number **1566.2**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF130/132, IRF130R/132R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	-	-	V
IRF131/133, IRF131R/133R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF130/131, IRF130R/131R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	14	-	-	A
IRF132/133, IRF132R/133R			12	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF130/131, IRF130R/131R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.3A	-	0.12	0.16	Ω
IRF132/133, IRF132R/133R			-	0.16	0.23	Ω
Forward Transconductance (Note 2)	g_{ts}	$V_{DS} \geq 50V$, I_D = 8.3A	4.6	6.9	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 14A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	-	30	ns
Rise Time	t_r		-	-	75	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	40	ns
Fall Time	t_f		-	-	45	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	18	26	nC
Gate-Source Charge	Q_{gs}		-	5.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	11	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.9	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	55	120	250	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	0.26	0.58	1.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 380µH, R_{GS} = 25Ω, I_{PEAK} = 145A (See Figure 15)

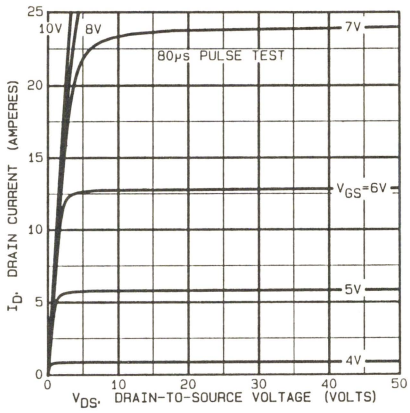


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

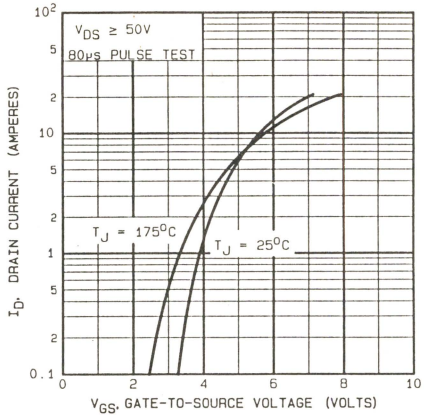


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

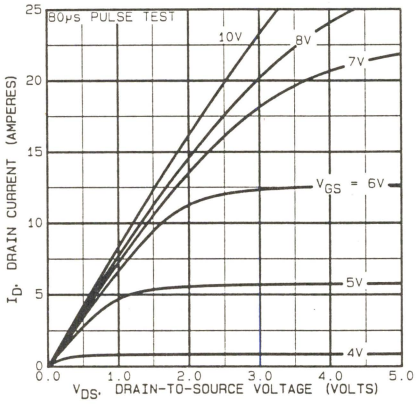


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

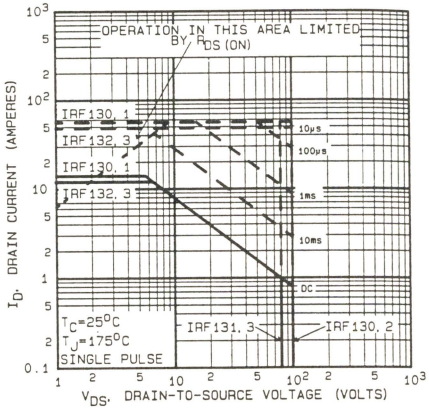


FIGURE 4. MAXIMUM SAFE OPERATING AREA

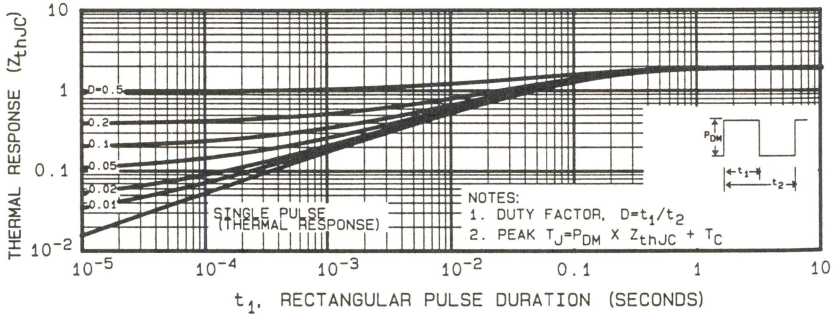


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

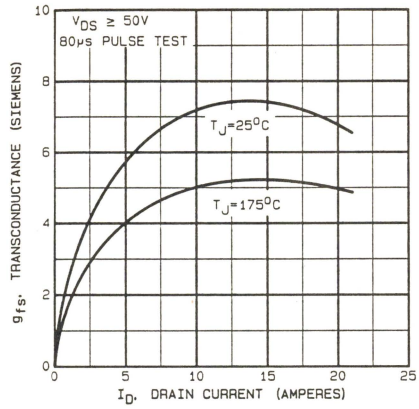


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

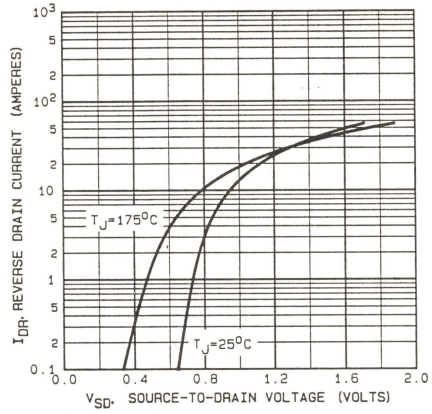


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

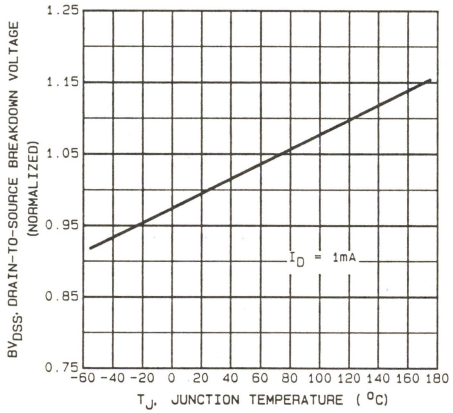


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

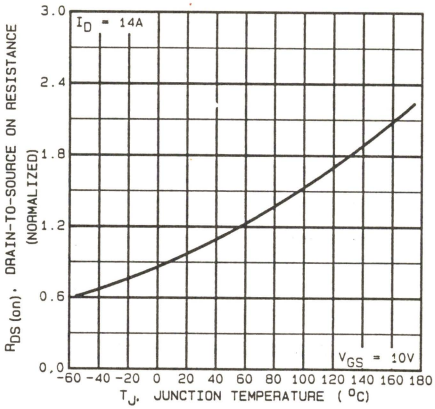


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

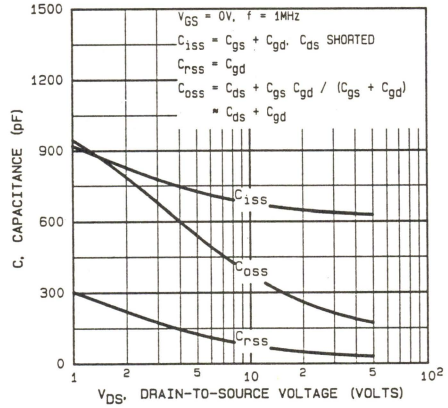


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

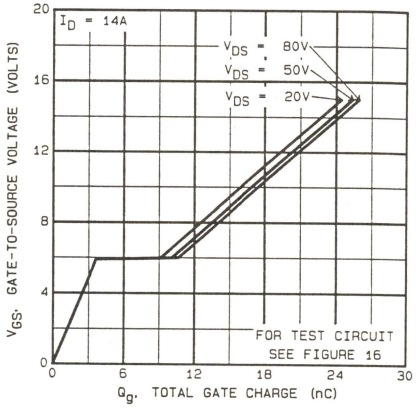


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

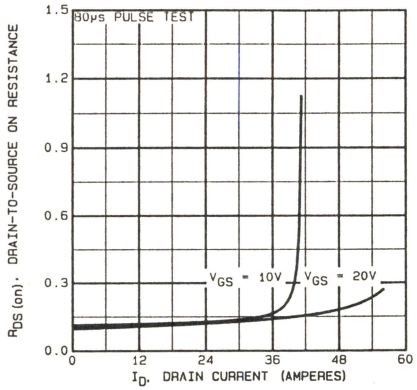


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

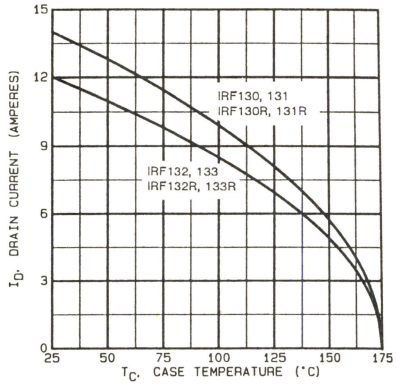


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

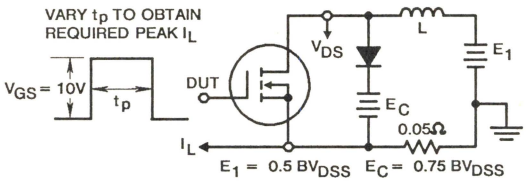


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

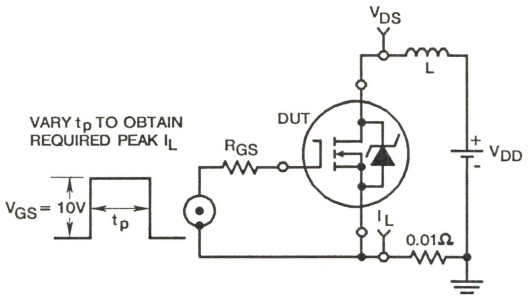


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

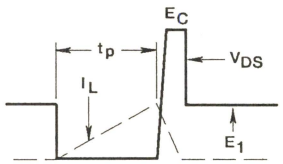


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

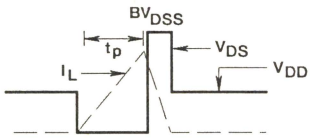


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

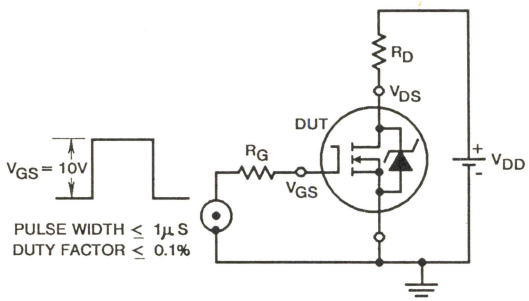


FIGURE 16. SWITCHING TIME TEST CIRCUIT

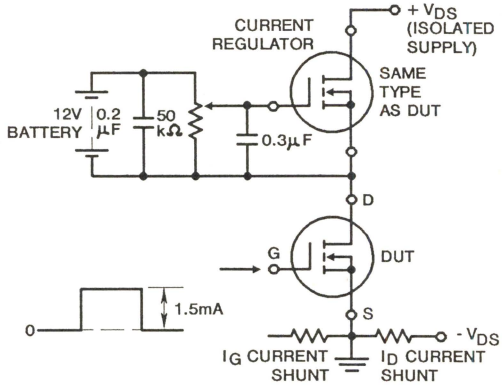


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF140/141/142/143
IRF140R/141R/142R/143R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 28A and 25A, 80V - 100V
- $r_{DS(on)}$ = 0.077Ω and 0.10Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

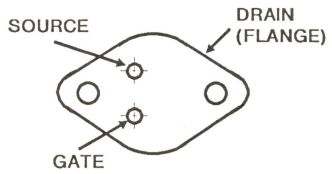
Description

The IRF140, IRF141, IRF142, and IRF143 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF140R, IRF141R, IRF142R, and IRF143R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

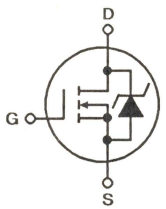
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF140 IRF140R	IRF141 IRF141R	IRF142 IRF142R	IRF143 IRF143R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	28	28	25	25	A
T_C = +100°C ..... I_D	20	20	17	17	A
Pulsed Drain Current (3) ..... I_{DM}	110	110	100	100	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	150	150	150	150	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	108	108	96	96	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	100	100	100	100	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 190μH, R_{GS} = 25Ω, I_{PEAK} = 28A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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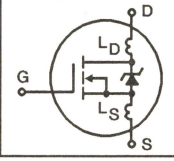
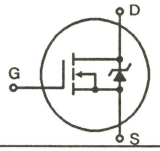
File Number **2306.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF140/142, IRF140R/142R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF141/143, IRF141R/143R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF140/141, IRF140R/141R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	28	–	–	A
IRF142/143, IRF142R/143R			25	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF140/141, IRF140R/141R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 17A	–	0.07	0.077	Ω
IRF142/143, IRF142R/143R			–	0.09	0.100	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 17A	8.7	13	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1275	–	pF
Output Capacitance	C_{OSS}		–	550	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	160	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 28A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	23	ns
Rise Time	t_r		–	27	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	38	60	ns
Fall Time	t_f		–	14	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 28A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	38	59	nC
Gate-Source Charge	Q_{gs}		–	9	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	21	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	28	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	110	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 28A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/µs	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	0.44	0.9	1.9	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 190µH, R_{GS} = 25Ω, I_{PEAK} = 28A (See Figure 15)

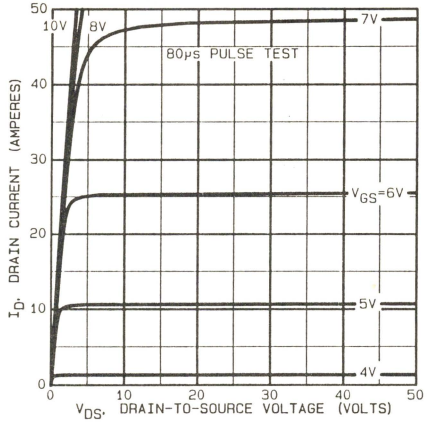


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

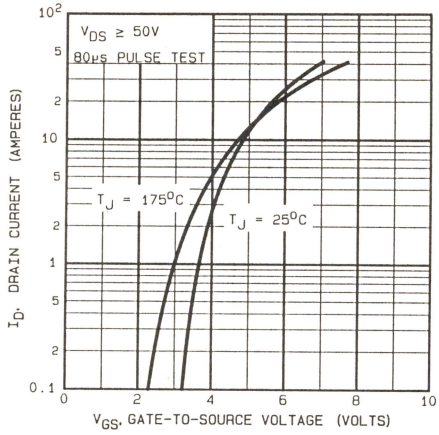


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

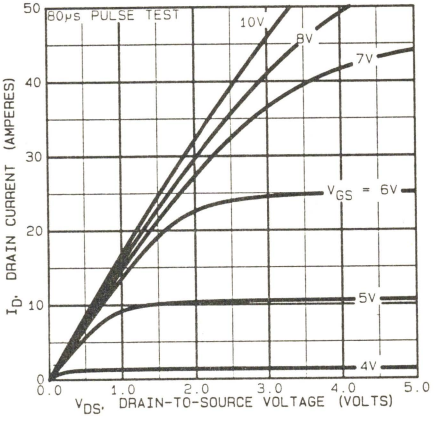


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

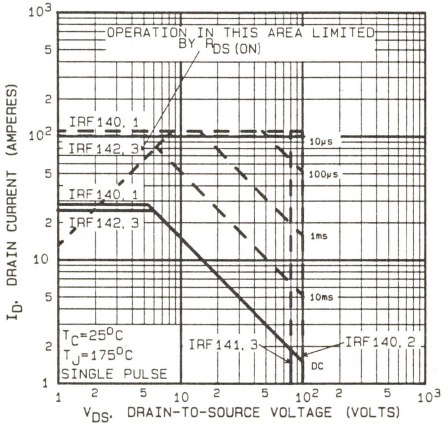


FIGURE 4. MAXIMUM SAFE OPERATING AREA

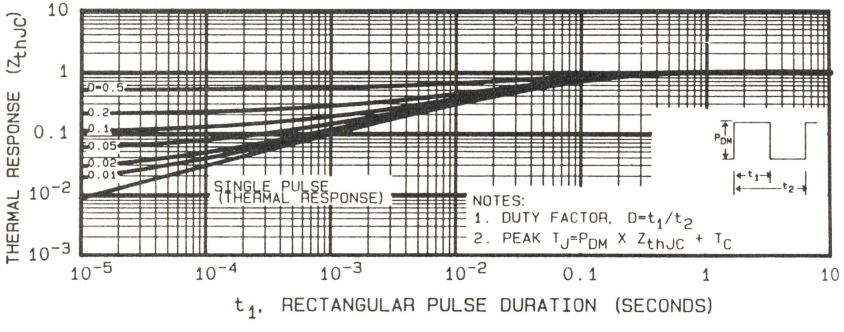


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

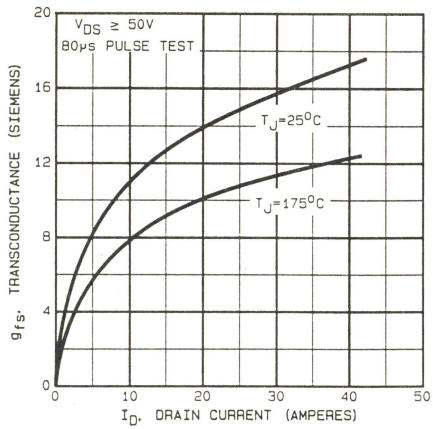


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

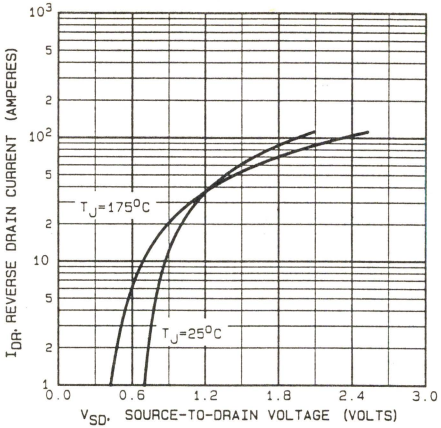


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

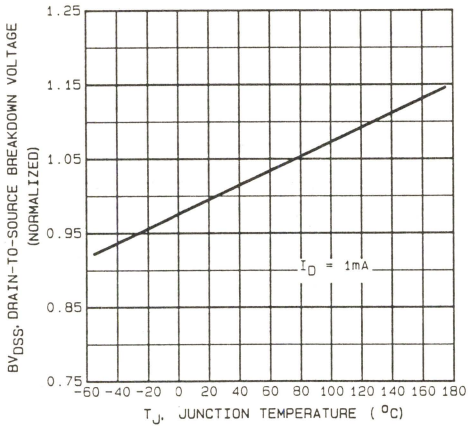


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

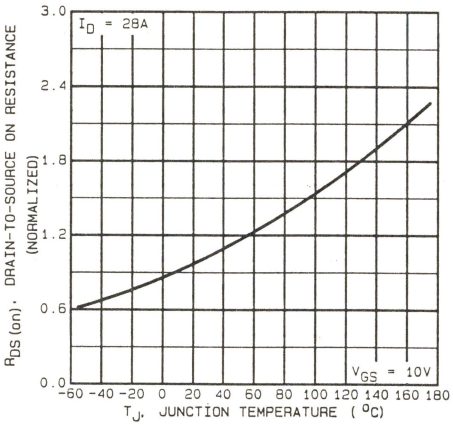


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

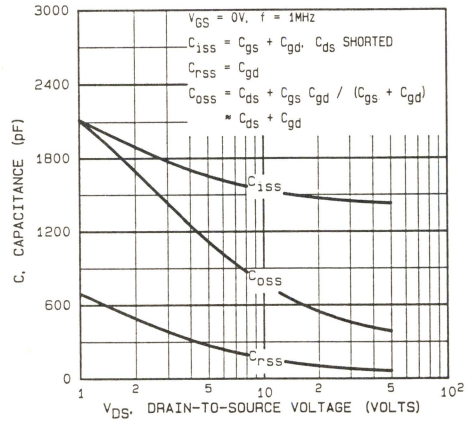


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

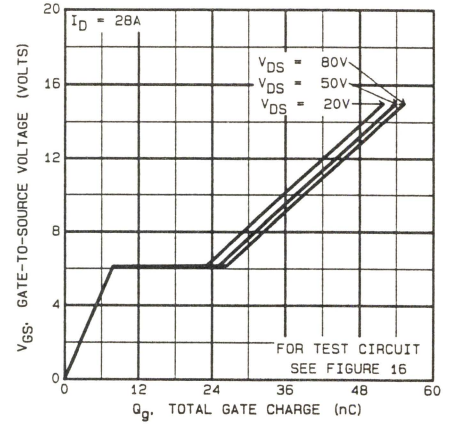


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

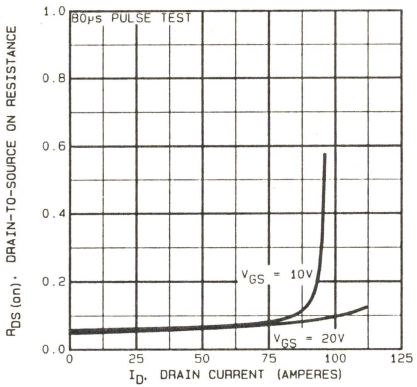


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

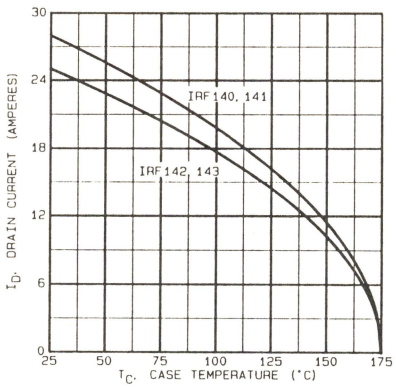


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

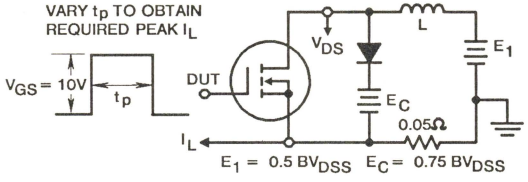


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

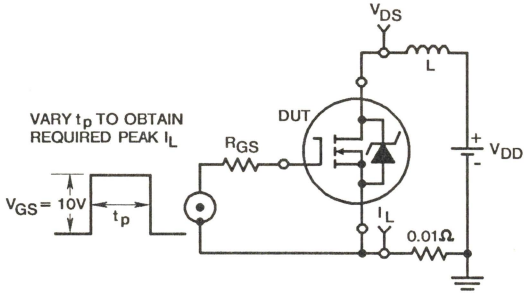


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

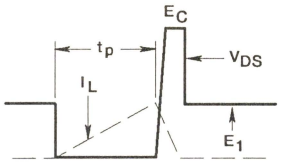


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

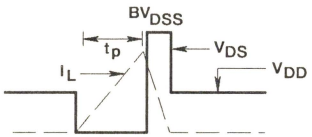


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

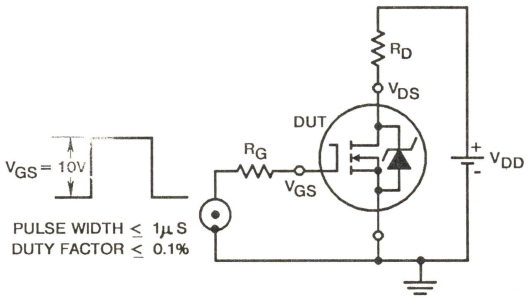


FIGURE 16. SWITCHING TIME TEST CIRCUIT

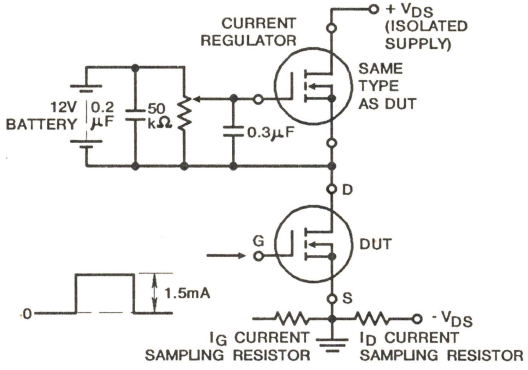


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF150/151/152/153
IRF150R/151R/152R/153R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 33A and 40A, 60V - 100V
- $r_{DS(on)}$ = 0.055Ω and 0.08Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

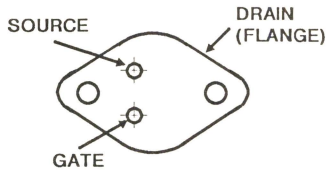
Description

The IRF150, IRF151, IRF152, and IRF153 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF150R, IRF151R, IRF152R, and IRF153R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

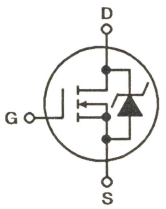
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF150 IRF150R	IRF151 IRF151R	IRF152 IRF152R	IRF153 IRF153R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	60	100	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	60	10	60	V
Continuous Drain Current					
T_C = +25°C ..... I_D	40	40	33	33	A
T_C = +100°C ..... I_D	25	25	20	20	A
Pulsed Drain Current (3) ..... I_{DM}	160	160	132	132	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Fig. 14) ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	160	160	132	132	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	150	150	150	150	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 10V, starting T_J = +25°C, L = 170μH, R_{GS} = 50Ω, I_{PEAK} = 40A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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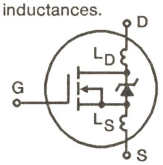
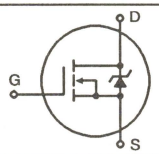
File Number **1824.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF150/152, IRF150R/152R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF151/153, IRF151R/153R			60	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF150/151, IRF150R/151R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	40	–	–	A
IRF152/153, IRF152R/153R			33	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF150/151, IRF150R/151R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 20A	–	0.045	0.055	Ω
IRF152/153, IRF152R/153R			–	0.06	0.08	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 20A	9.0	11	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	1000	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	350	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 24V, I_D = 20A, Z_0 = 4.7Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	35	ns
Rise Time	t_r		–	–	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	125	ns
Fall Time	t_f		–	–	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	63	120	nC
Gate-Source Charge	Q_{gs}		–	27	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	36	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.8	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	40	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	160	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 40A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 40A, dI_F/dt = 100A/µs	–	600	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	–	3.3	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 10V, Start T_J = +25°C, L = 170µH, R_{GS} = 50Ω, I_{PEAK} = 40A (See Figure 15)

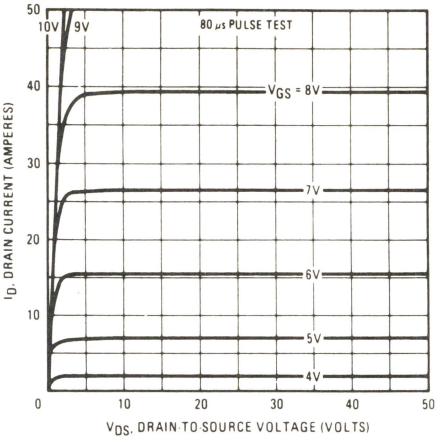


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

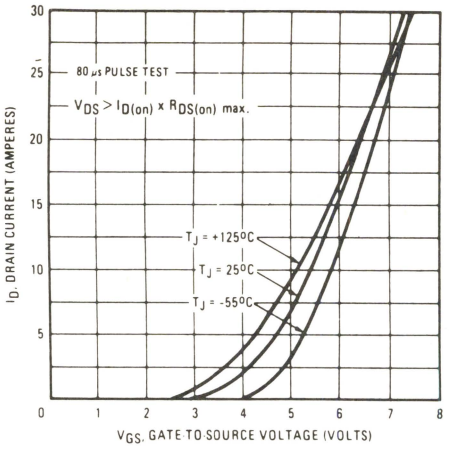


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

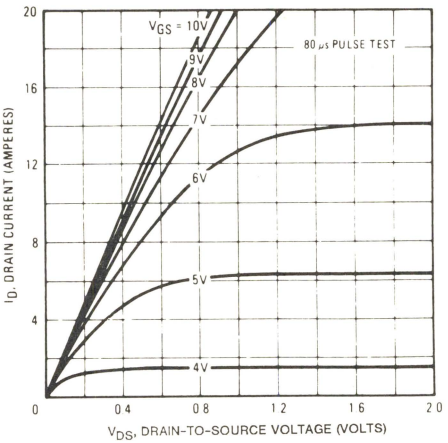


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

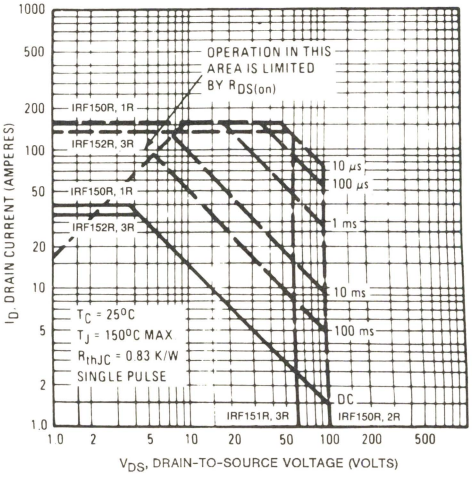


FIGURE 4. MAXIMUM SAFE OPERATING AREA

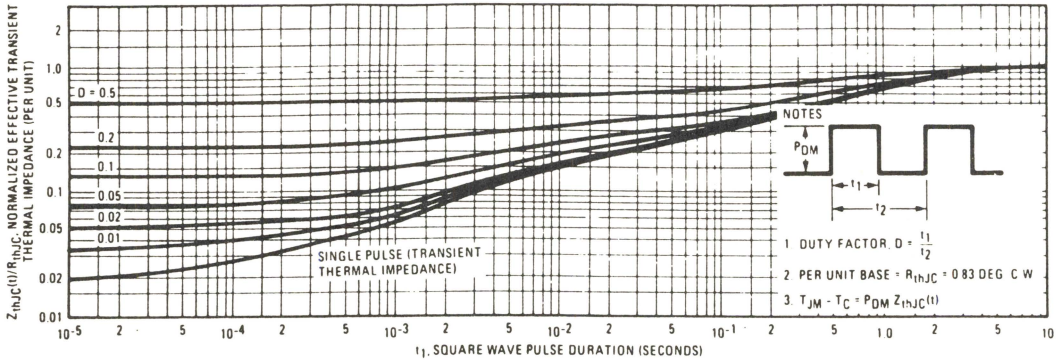


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

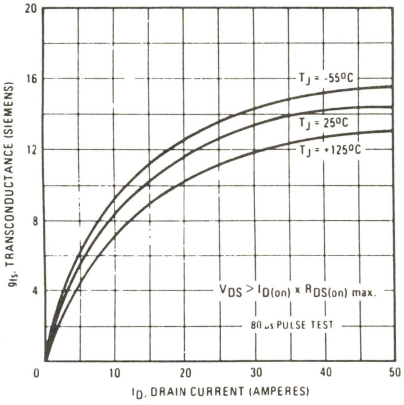


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

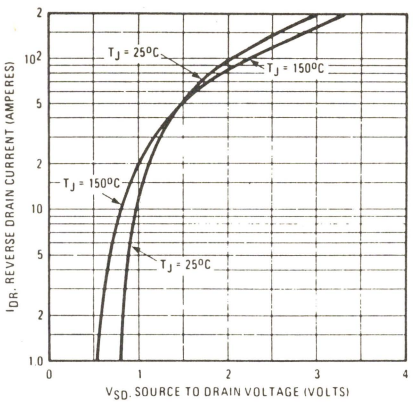


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

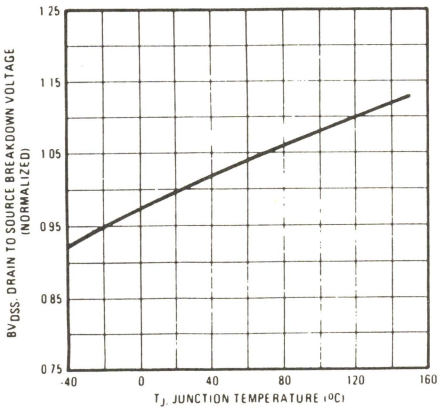


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

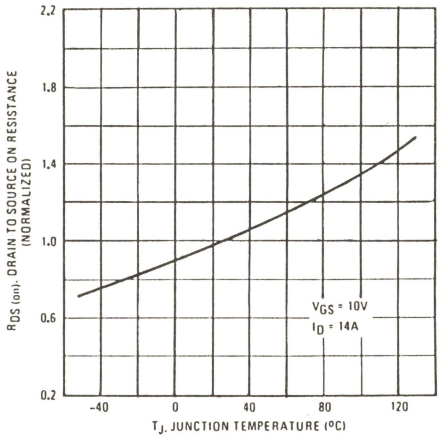


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

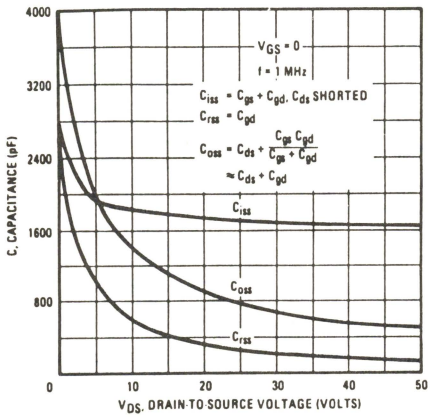


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

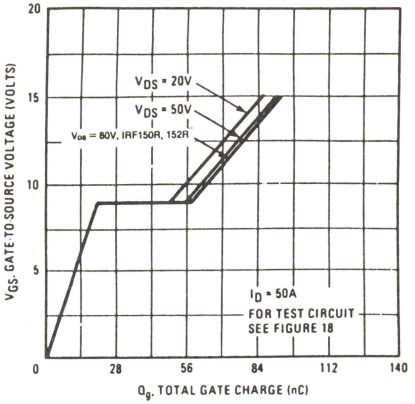


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

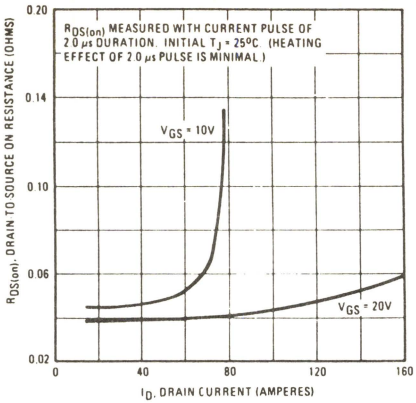


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

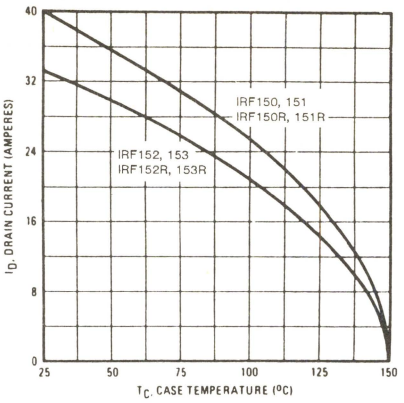


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

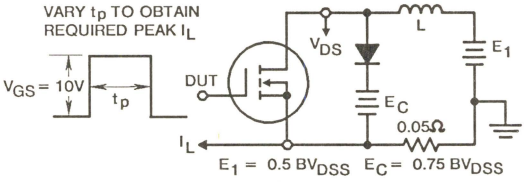


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

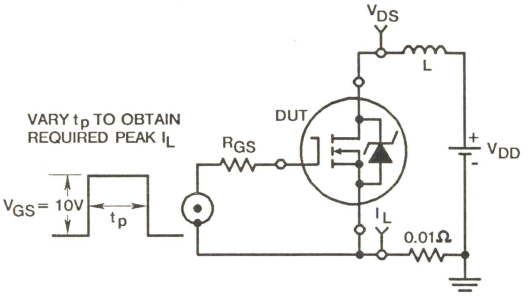


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

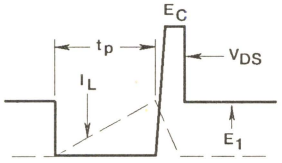


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

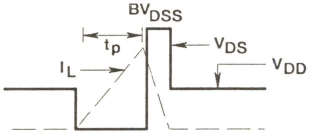


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

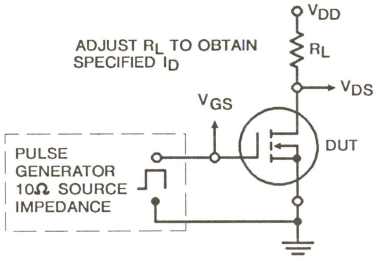


FIGURE 16. SWITCHING TIME TEST CIRCUIT

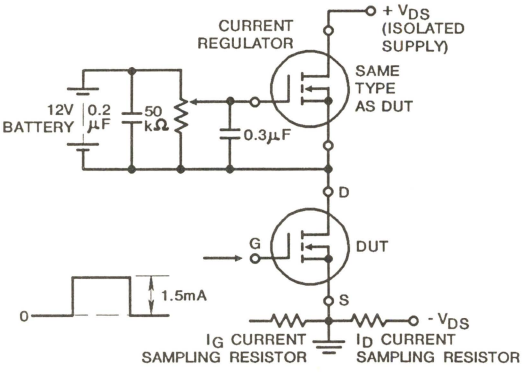


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF220, IRF221 IRF222, IRF223

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.0A and 5.0A, 150V - 200V
- $r_{DS(on)}$ = 0.8Ω and 1.2Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

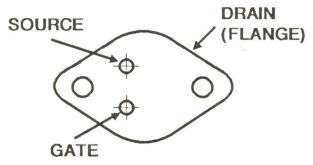
Description

The IRF220, IRF221, IRF222, and IRF223 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

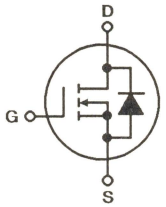
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		IRF220	IRF221	IRF222	IRF223	UNITS
Drain-Source Voltage (1)	V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	200	150	200	150	V
Continuous Drain Current						
T_C = +25°C	I_D	5.0	5.0	4.0	4.0	A
T_C = +100°C	I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3)	I_{DM}	20	20	16	16	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C (See Figure 14)	P_D	40	40	40	40	W
Linear Derating Factor (See Figure 14)		0.32	0.32	0.32	0.32	W/°C
Inductive Current, Clamped (See Figures 14 and 15, L = 100μH)	I_{LM}	20	20	16	16	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-50 to +150	-50 to +150	-50 to +150	-50 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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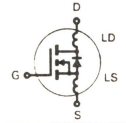
File Number **1567.1**

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF220 IRF222	200	–	–	V	V_{GS} = 0V
		IRF221 IRF223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF220 IRF221	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF222 IRF223	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF220 IRF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF222 IRF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	—	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	—	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF220 IRF221	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF222 IRF223	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF220 IRF221	–	–	20	A	
		IRF222 IRF223	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF220 IRF221	–	–	2.0	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF222 IRF223	–	–	1.8	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

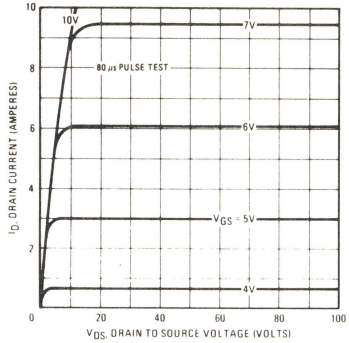


Fig. 1 — Typical Output Characteristics

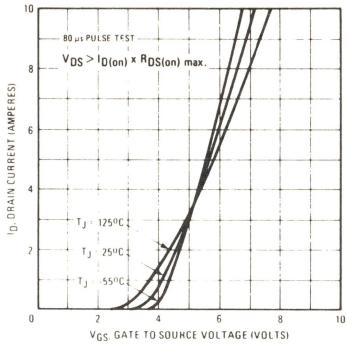


Fig. 2 — Typical Transfer Characteristics

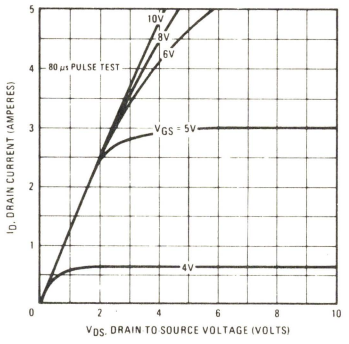


Fig. 3 — Typical Saturation Characteristics

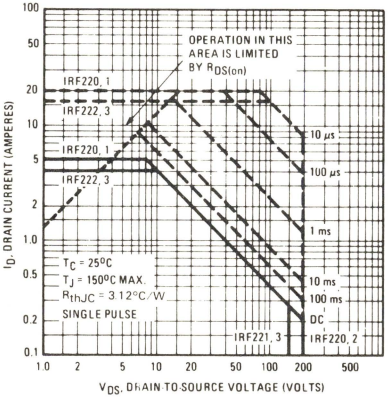


Fig. 4 — Maximum Safe Operating Area

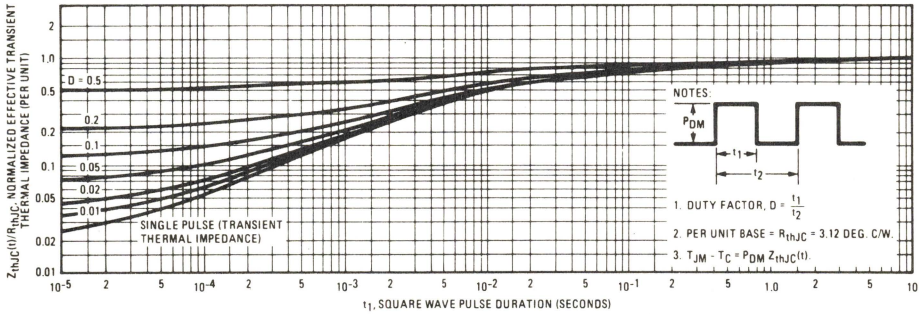


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

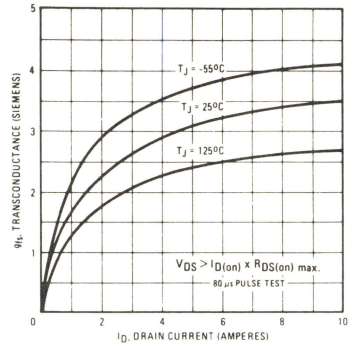


Fig. 6 — Typical Transconductance Vs. Drain Current

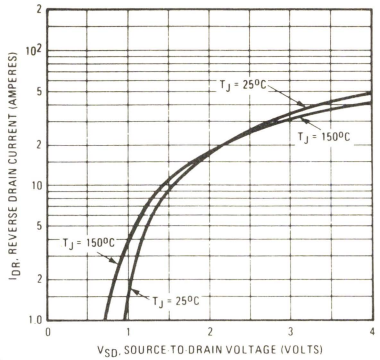


Fig. 7 — Typical Source-Drain Diode Forward Voltage

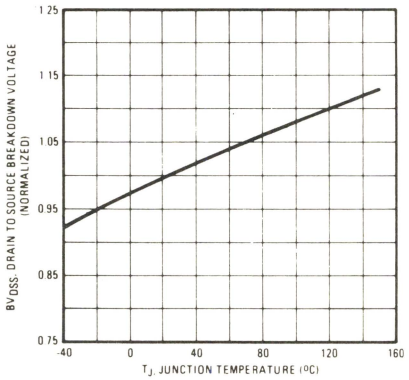


Fig. 8 — Breakdown Voltage Vs. Temperature

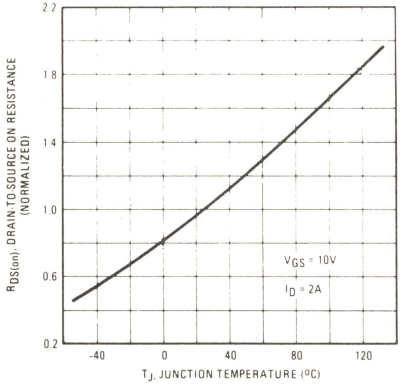


Fig. 9 — Normalized On-Resistance Vs. Temperature

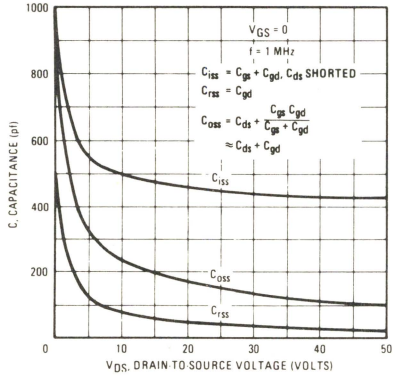


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

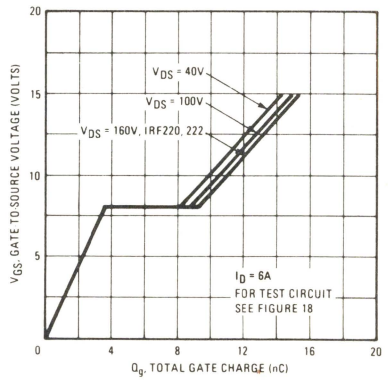


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

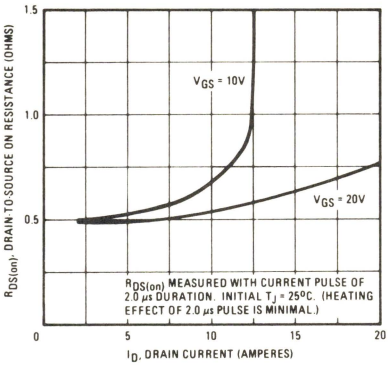


Fig. 12 – Typical On-Resistance Vs. Drain Current

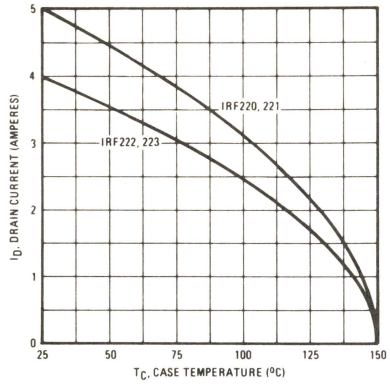


Fig. 13 – Maximum Drain Current Vs. Case Temperature

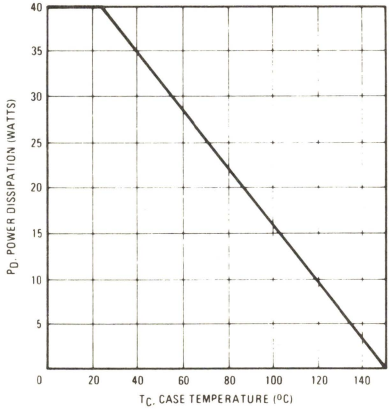


Fig. 14 – Power Vs. Temperature Derating Curve

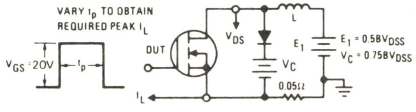


Fig. 15 – Clamped Inductive Test Circuit

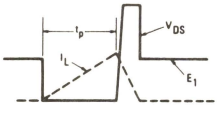


Fig. 16 – Clamped Inductive Waveforms

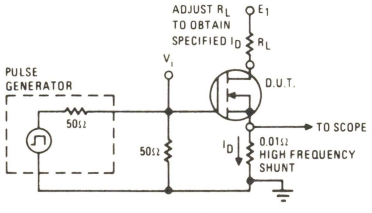


Fig. 17 – Switching Time Test Circuit

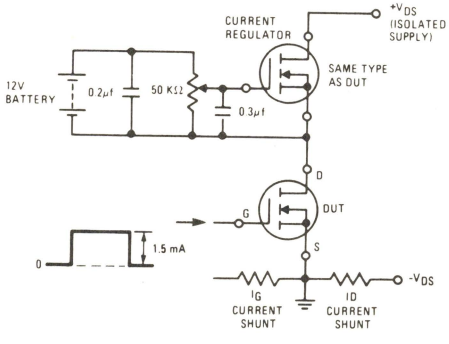


Fig. 18 – Gate Charge Test Circuit

HARRIS

IRF230/231/232/233
IRF230R/231R/232R/233R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 8.0A and 9.0A, 150V - 200V
- $r_{DS}(on)$ = 0.4Ω and 0.6Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

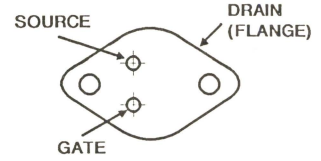
Description

The IRF230, IRF231, IRF232, and IRF233 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF230R, IRF231R, IRF232R and IRF233R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

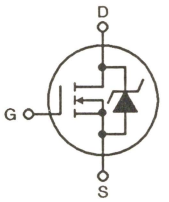
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	IRF230 IRF230R	IRF231 IRF231R	IRF232 IRF232R	IRF233 IRF233R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	9.0	9.0	8.0	8.0	A
T_C = +100°C ..... I_D	6.0	6.0	5.0	5.0	A
Pulsed Drain Current (3) ..... I_{DM}	36	36	32	32	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	36	36	32	32	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	150	150	150	150	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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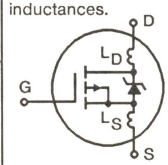
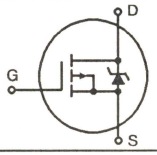
File Number **1568.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF230/232, IRF230R/232R	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	200	–	–	V
IRF231/233, IRF231R/233R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF230/231, IRF230R/231R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	9.0	–	–	A
IRF232/233, IRF232R/233R			8.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF230/231, IRF230R/231R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.0A	–	0.25	0.4	Ω
IRF232/233, IRF232R/233R			–	0.4	0.6	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} > 50V, I_D = 5.0A	3.0	4.8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	250	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq$ 90V, I_D = 5.0A, Zo = 15Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature)	–	–	30	ns
Rise Time	t_r		–	–	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	50	ns
Fall Time	t_f		–	–	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8V Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	19	30	nC
Gate-Source Charge	Q_{gs}		–	10	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	9.0	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.6	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	9.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	36	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 9A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/μs	–	450	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/μs	–	3.0	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, Start T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A (See Figure 15)

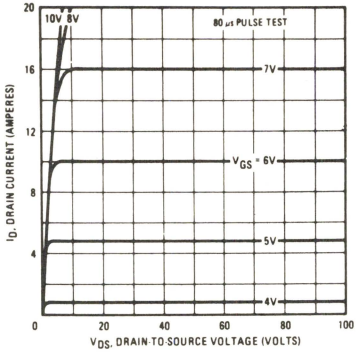


Fig. 1 – Typical Output Characteristics

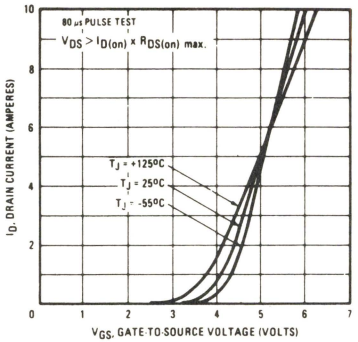


Fig. 2 – Typical Transfer Characteristics

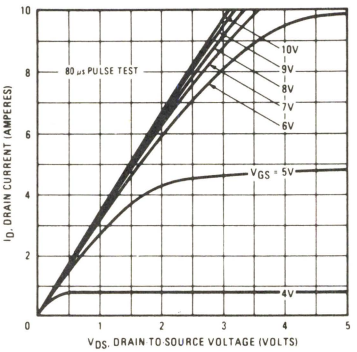


Fig. 3 – Typical Saturation Characteristics

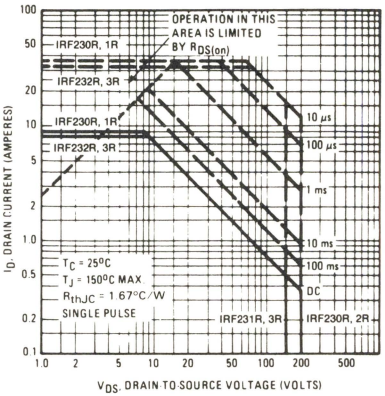


Fig. 4 – Maximum Safe Operating Area

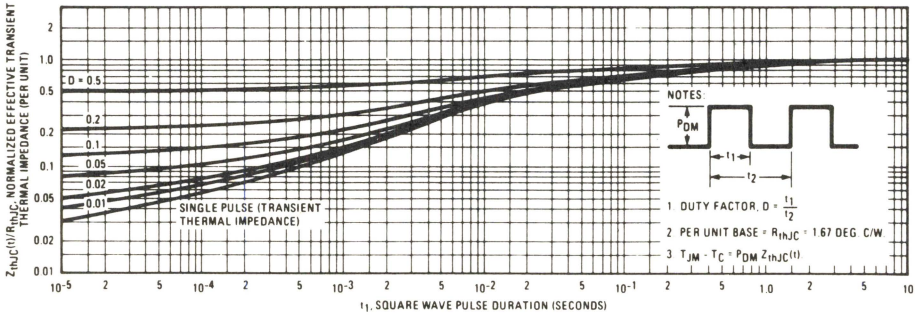


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

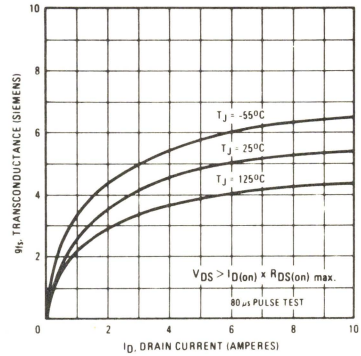


Fig. 6 – Typical Transconductance Vs. Drain Current

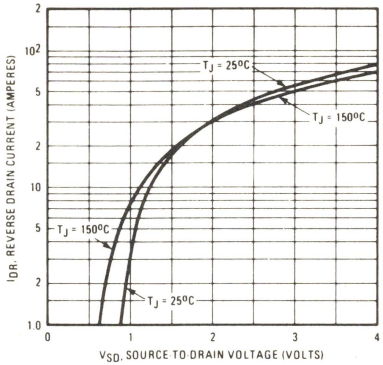


Fig. 7 – Typical Source-Drain Diode Forward Voltage

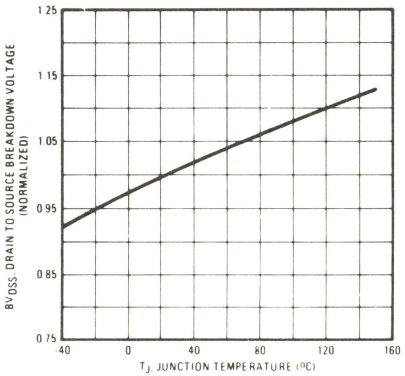


Fig. 8 – Breakdown Voltage Vs. Temperature

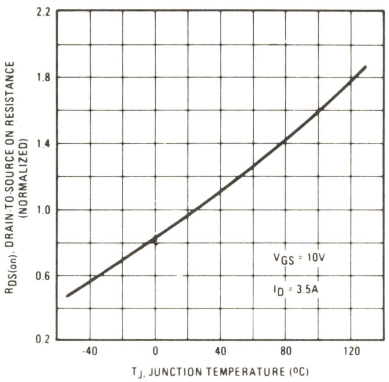


Fig. 9 – Normalized On-Resistance Vs. Temperature

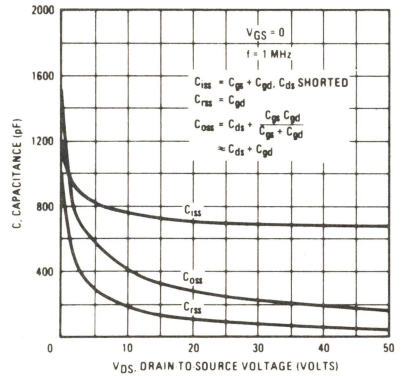


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

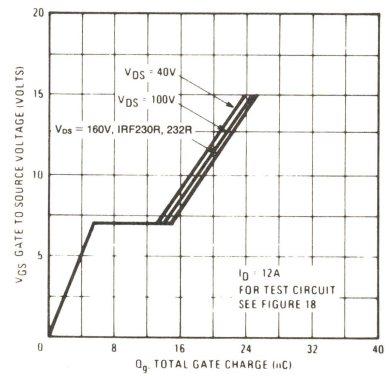


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

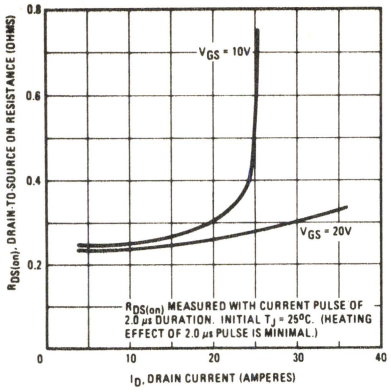


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

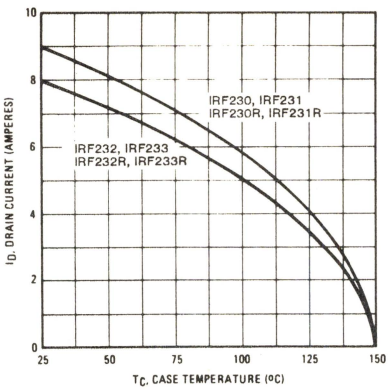


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

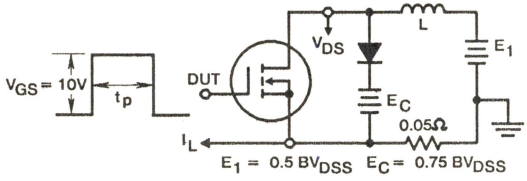


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

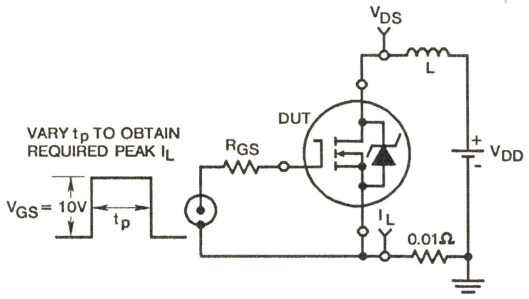


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

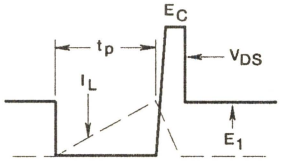


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

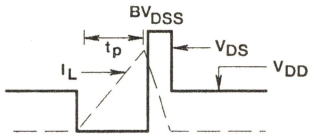


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

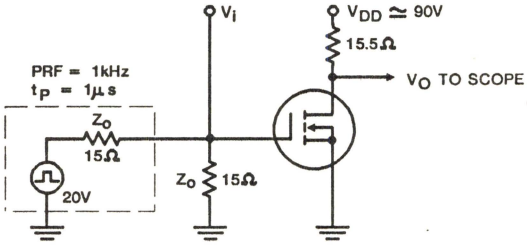


FIGURE 16. SWITCHING TIME TEST CIRCUIT

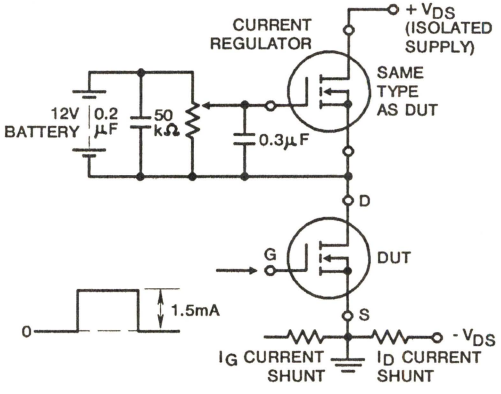


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF234, IRF235
IRF236, IRF237

N-Channel Power MOSFETs
Avalanche-Energy Rated

May 1992

Features

- 8.1A and 6.5A, 275V - 250V
- $r_{DS}(on)$ = 0.45Ω and 0.68Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275V, 250V Rating - 120V AC Line System Operation

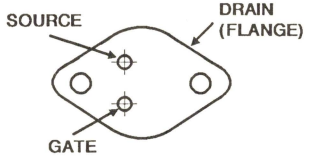
Description

The IRF234, IRF235, IRF236, and IRF237 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

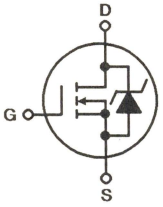
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	IRF234	IRF235	IRF236	IRF237	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.1	6.5	8.1	6.5	A
T_C = +100°C ..... I_D	5.1	4.1	5.1	4.1	A
Pulsed Drain Current (3) ..... I_{DM}	32	26	32	26	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}	180	180	180	180	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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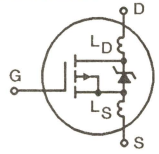
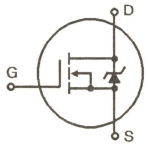
File Number 2208.2

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF236, IRF237	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	275	-	-	V
IRF234, IRF235			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF234, IRF236	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	8.1	-	-	A
IRF235, IRF237			6.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF234, IRF236	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.1A	-	0.32	0.45	Ω
IRF235, IRF237			-	0.48	0.68	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} = 2 X V_{GS}, I_D = 4.1A	2.9	4.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	180	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	52	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 8.1A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	9.1	14	ns
Rise Time	t_r		-	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	47	ns
Fall Time	t_f		-	19	29	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8.1A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	24	35	nC
Gate-Source Charge	Q_{gs}		-	5.1	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.1	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.1A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	92	180	390	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	0.63	1.3	2.7	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A (See Figures 14 & 15)

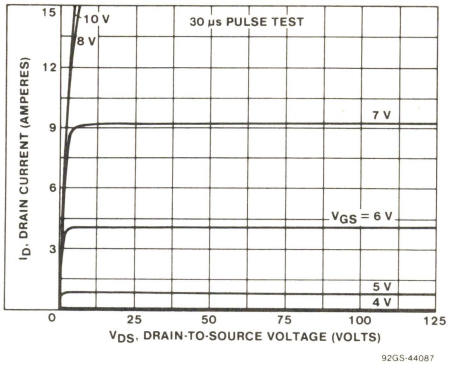


Fig. 1 - Typical output characteristics.

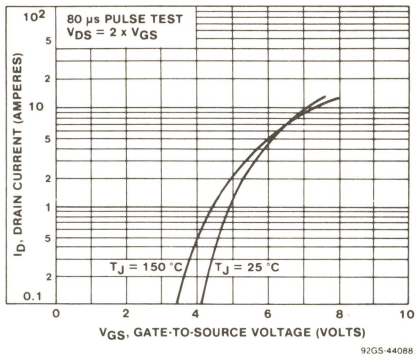


Fig. 2 - Typical transfer characteristics.

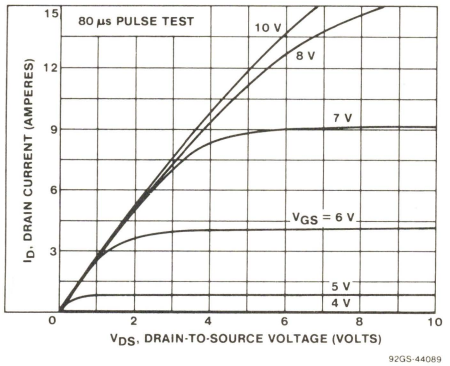


Fig. 3 - Typical saturation characteristics.

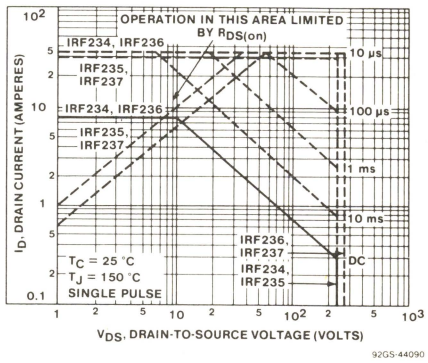


Fig. 4 - Maximum safe operating area.

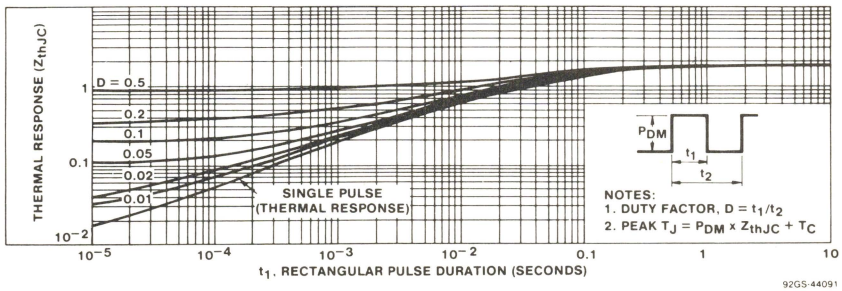


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

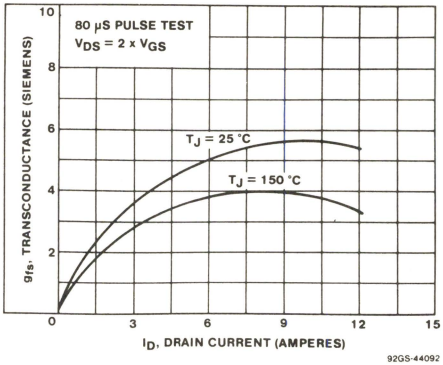


Fig. 6 - Typical transconductance vs. drain current.

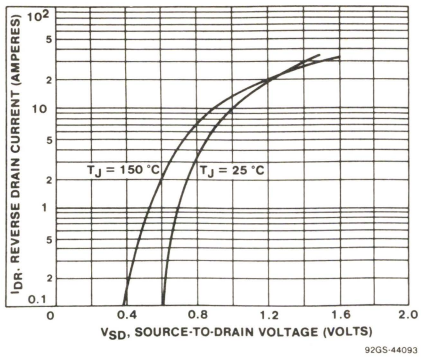


Fig. 7 - Typical source-drain diode forward voltage.

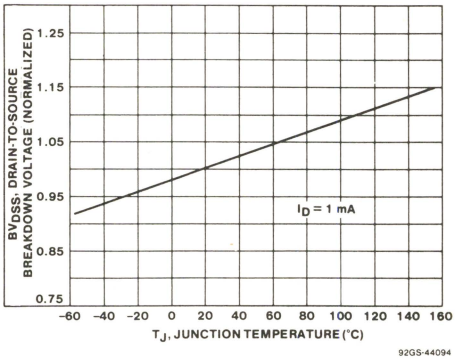


Fig. 8 - Breakdown voltage vs. temperature.

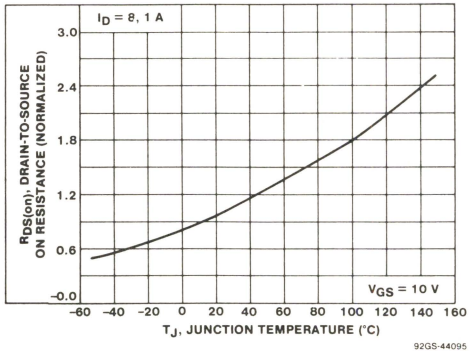


Fig. 9 - Normalized on-resistance vs. temperature.

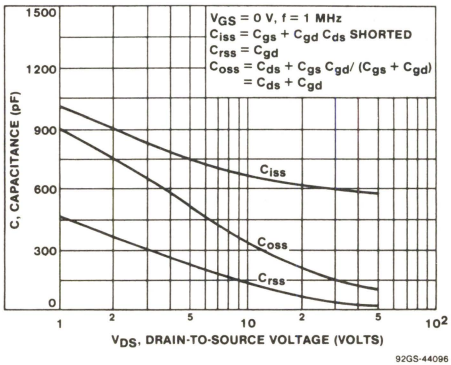


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

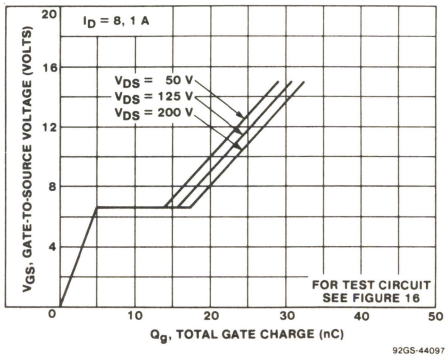


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

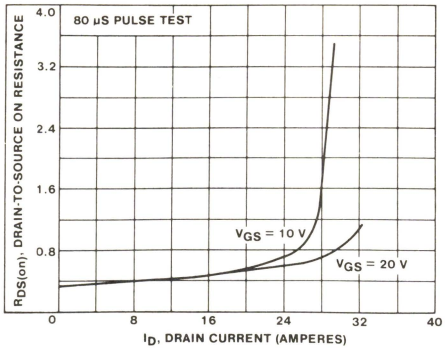


Figure 12. Typical On Resistance vs Drain Current

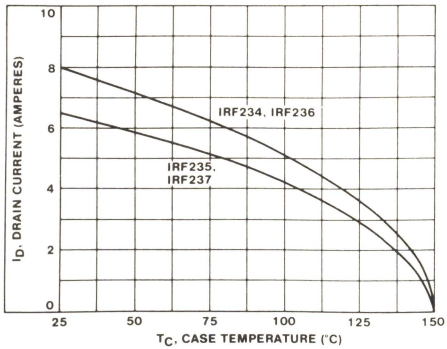


Figure 13. Maximum Drain Current vs Case Temperature

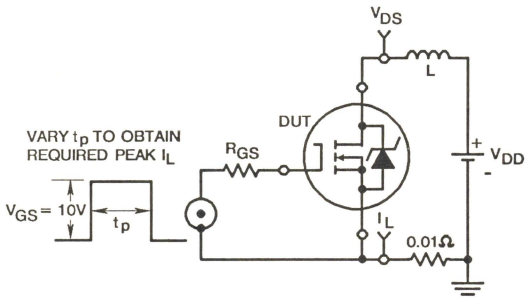


Figure 14. Unclamped Energy Test Circuit

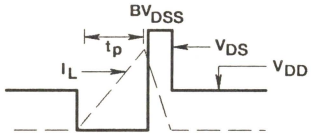


Figure 15. Unclamped Energy Waveforms

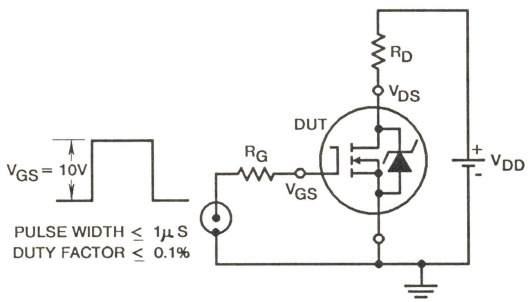


Figure16. Switching Time Test Circuit

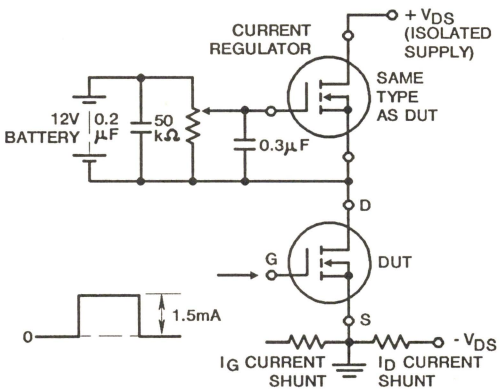


Figure 17. Gate Charge Test Circuit

HARRIS

IRF240/241/242/243
IRF240R/241R/242R/243R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 16A and 18A, 200V, 150V
- $r_{DS}(on)$ = 0.18Ω and 0.22Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

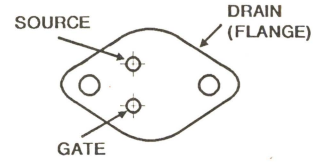
Description

The IRF240, IRF241, IRF242, and IRF243 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF240R, IRF241R, IRF242R and IRF243R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE steel package.

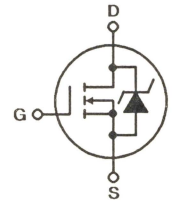
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	IRF240 IRF240R	IRF241 IRF241R	IRF242 IRF242R	IRF243 IRF243R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	18	18	16	16	A
T_C = +100°C ..... I_D	11	11	10	10	A
Pulsed Drain Current (3) ..... I_{DM}	72	72	64	64	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	72	72	64	64	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	580	580	580	580	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 2.7mH, R_{GS} = 25Ω, I_{PEAK} = 9A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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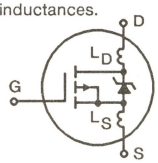
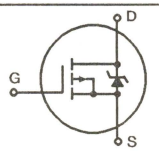
File Number **1584.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF240/242, IRF240R/242R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF241/243, IRF241R/243R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF240/241, IRF240R/241R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	18	–	–	A
IRF242/243, IRF242R/243R			16	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF240/241, IRF240R/241R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	–	0.14	0.18	Ω
IRF242/243, IRF242R/243R			–	0.20	0.22	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} > ID(ON) x $r_{DS(ON)Max}$, I_D = 10A	6.7	9.0	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1275	–	pF
Output Capacitance	C_{OSS}		–	500	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	160	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 18A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	30	ns
Rise Time	t_r		–	27	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	40	80	ns
Fall Time	t_f		–	31	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	43	60	nC
Gate-Source Charge	Q_{gs}		–	8	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	27	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	18	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	72	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 18A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 18A, dI_F/dt = 100A/µs	–	650	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 18A, dI_F/dt = 100A/µs	–	4.1	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 2.7mH, R_{GS} = 25Ω, I_{PEAK} = 18A (See Figure 15)

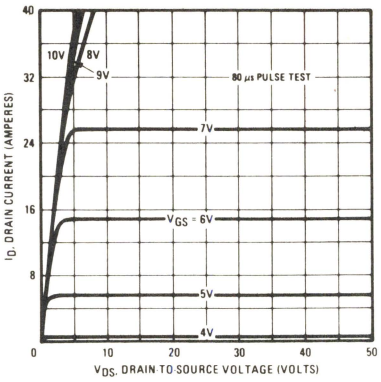


Fig. 1 – Typical Output Characteristics

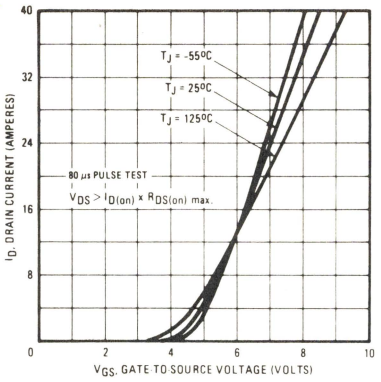


Fig. 2 – Typical Transfer Characteristics

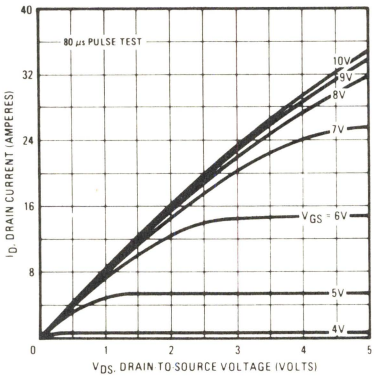


Fig. 3 – Typical Saturation Characteristics

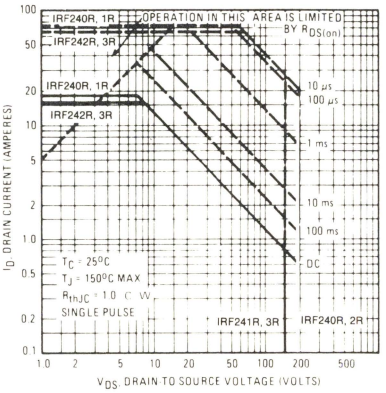


Fig. 4 – Maximum Safe Operating Area

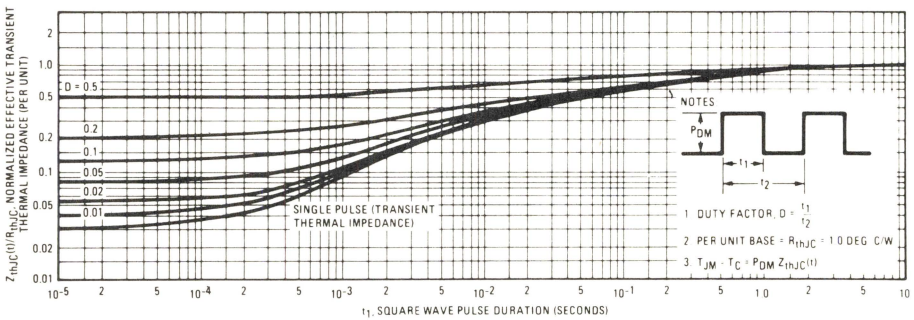


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

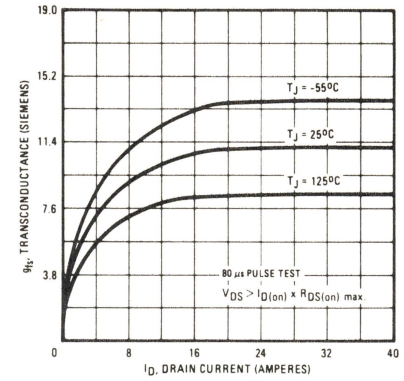


Fig. 6 – Typical Transconductance Vs. Drain Current

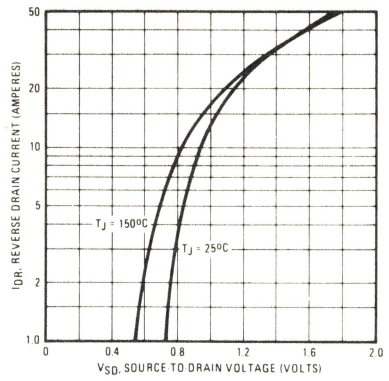


Fig. 7 – Typical Source-Drain Diode Forward Voltage

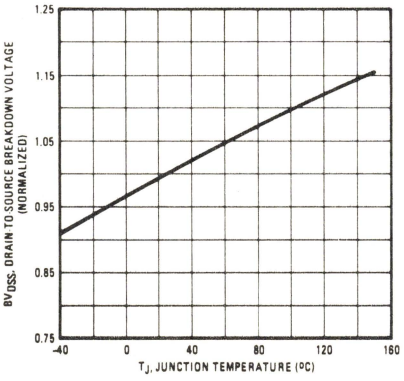


Fig. 8 – Breakdown Voltage Vs. Temperature

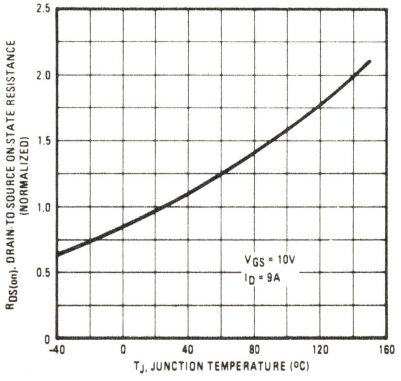


Fig. 9 – Normalized On-Resistance Vs. Temperature

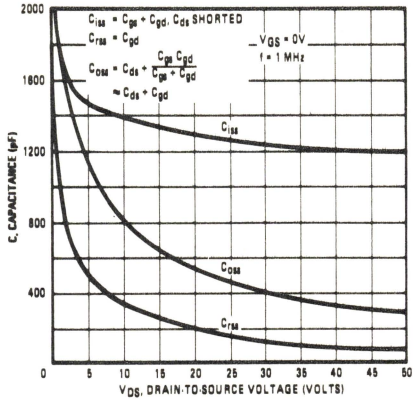


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

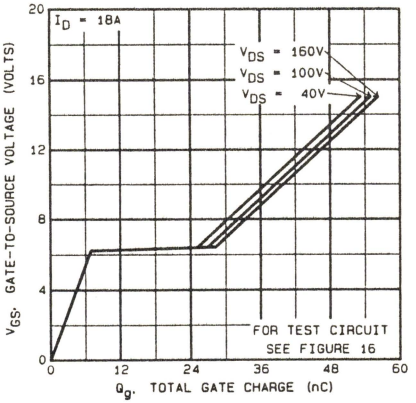


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

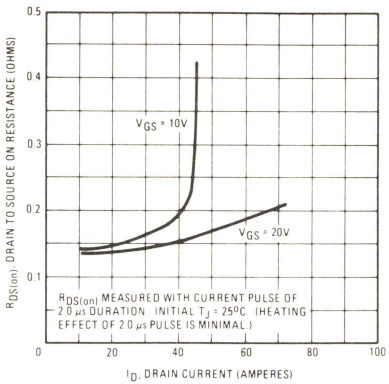


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

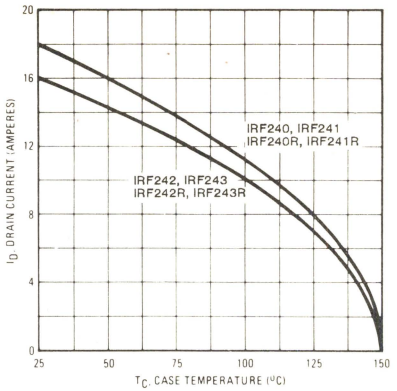


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

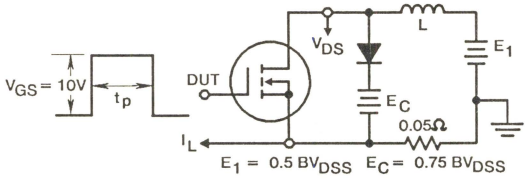


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

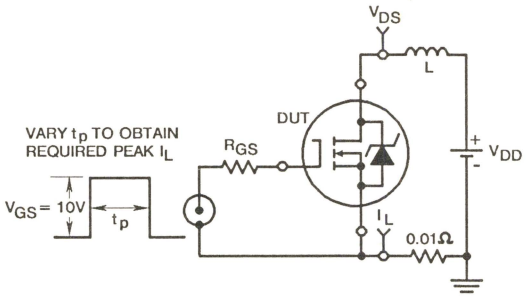


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

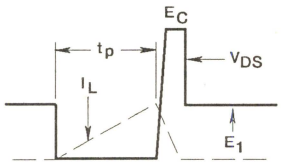


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

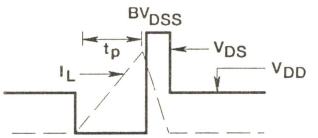


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

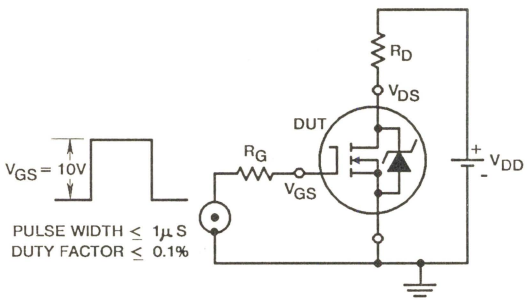


FIGURE 16. SWITCHING TIME TEST CIRCUIT

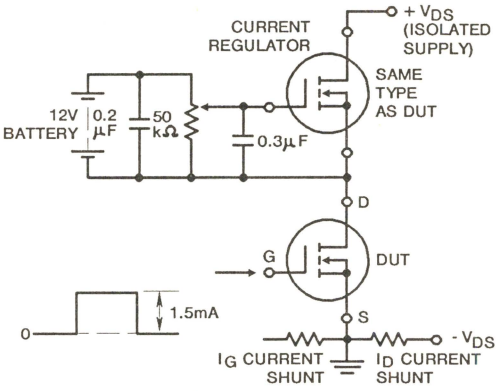


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF244, IRF245
IRF246, IRF247

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 14A and 13A, 275V - 250V
- $r_{DS(on)}$ = 0.28Ω and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275, 250V DC Rated - 120V AC Line System Operation

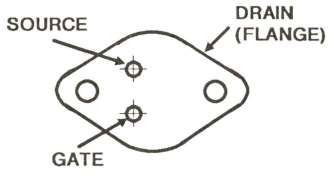
Description

The IRF244, IRF245, IRF246, and IRF247 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

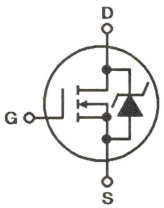
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF244	IRF245	IRF246	IRF247	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	13	14	13	A
T_C = +100°C ..... I_D	8.8	8.0	8.8	8.0	A
Pulsed Drain Current (3) ..... I_{DM}	56	52	56	52	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	550	550	550	550	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 4.5mH, R_G = 25Ω, Peak I_L = 14A (See Figures 14 & 15).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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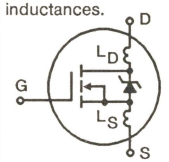
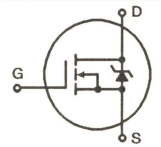
File Number **2209.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF244, 1RF245	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	–	–	V
IRF246, IRF247			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF244, IRF246	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\ Max}$, V_{GS} = 10V	14	–	–	A
1RF245, IRF247			13	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF244, IRF246	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8A	–	0.20	0.28	Ω
1RF245. IRF247			–	0.24	0.34	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 8A	6.7	10	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1300	–	pF
Output Capacitance	C_{OSS}		–	320	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	69	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 14A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	24	ns
Rise Time	t_r		–	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	53	80	ns
Fall Time	t_f		–	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	39	59	nC
Gate-Source Charge	Q_{gs}		–	6.6	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	20	–	nC
Internal Drain Inductance	L_D	Measured from the source lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	1.6	3.4	7.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 4.5mH, R_G = 25Ω, Peak I_L = 14A (See Figures 14 & 15).

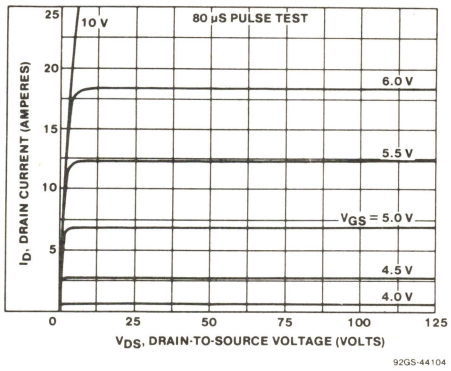


Fig. 1 - Typical output characteristics.

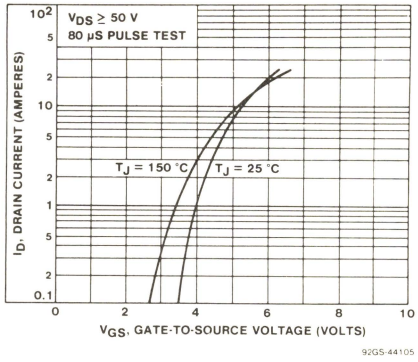


Fig. 2 - Typical transfer characteristics.

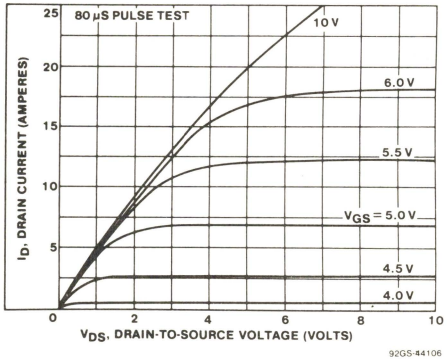


Fig. 3 - Typical saturation characteristics.

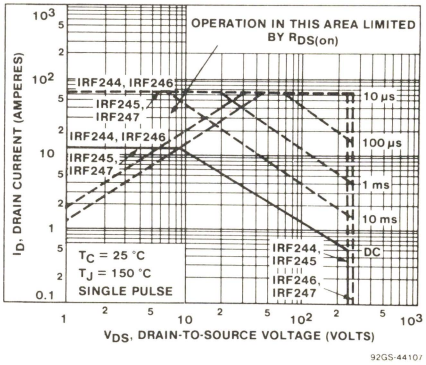


Fig. 4 - Maximum safe operating area.

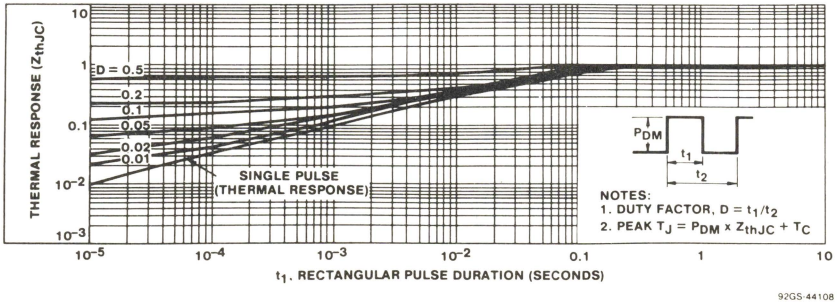


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

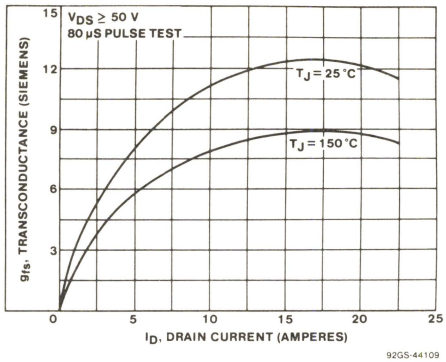


Fig. 6 - Typical transconductance vs. drain current.

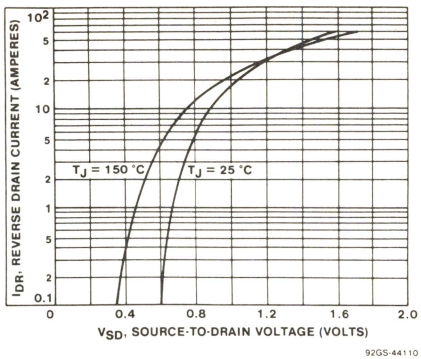


Fig. 7 - Typical source-drain diode forward voltage.

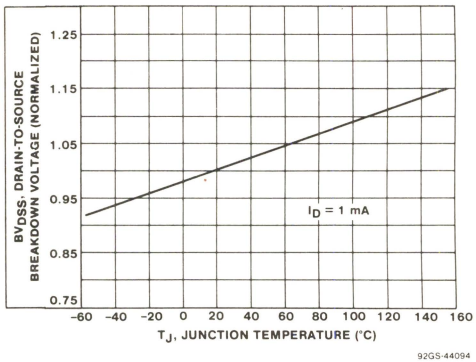


Fig. 8 - Breakdown voltage vs. temperature.

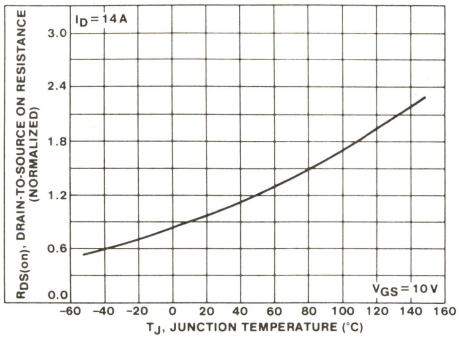


Fig. 9 - Normalized on-resistance vs. temperature.

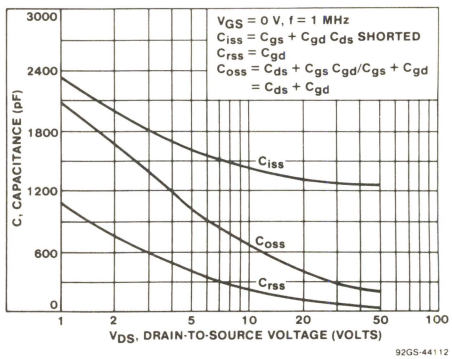


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

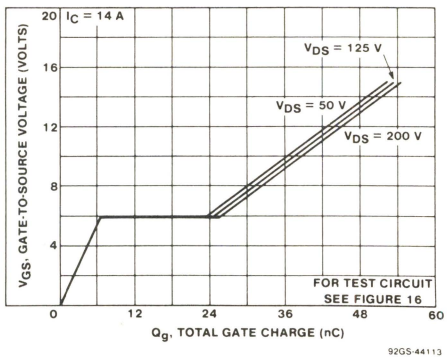


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

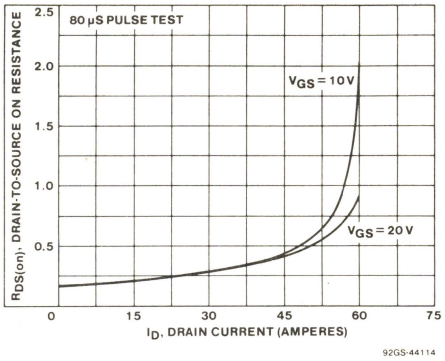


Figure 12. Typical On Resistance vs Drain Current

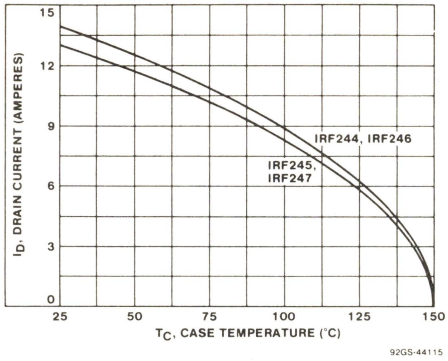


Figure 13. Maximum Drain Current vs Case Temperature

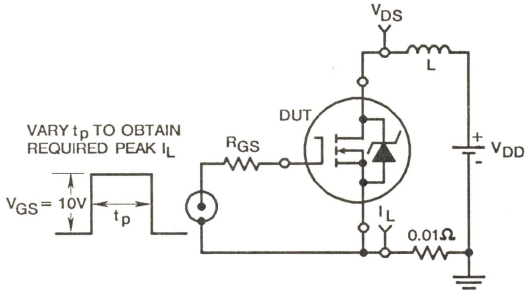


Figure 14. Unclamped Energy Test Circuit

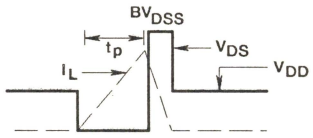


Figure 15. Unclamped Energy Waveforms

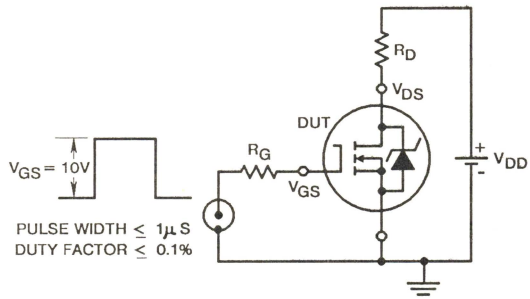


Figure16. Switching Time Test Circuit

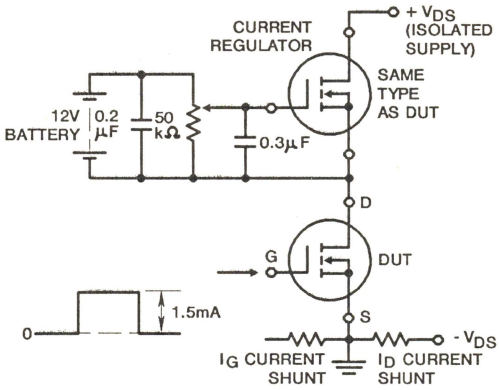


Figure 17. Gate Charge Test Circuit

HARRIS

IRF250/251/252/253
IRF250R/251R/252R/253R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 25A and 30A, 150V - 200V
- $r_{DS(on)}$ = 0.085Ω and 0.120Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

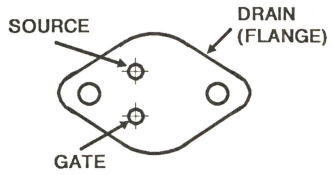
Description

The IRF250, IRF251, IRF252, and IRF253 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF250R, IRF251R, IRF252R, and IRF253R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

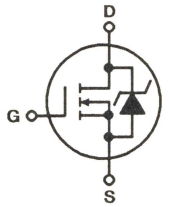
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF250 IRF250R	IRF251 IRF251R	IRF252 IRF252R	IRF253 IRF253R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	30	30	25	25	A
T_C = +100°C ..... I_D	19	19	16	16	A
Pulsed Drain Current (3) ..... I_{DM}	120	120	100	100	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	120	120	100	100	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	910	910	910	910	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 30A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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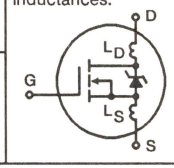
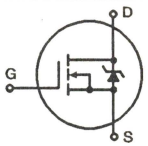
File Number **1825.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF250/252, IRF250R/252R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF251/253, IRF251R/253R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF250/251, IRF250R/251R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	30	–	–	A
IRF252/253, IRF252R/253R			25	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF250/251, IRF250R/251R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 16A	–	0.07	0.085	Ω
IRF252/253, IRF252R/253R			–	0.09	0.120	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 16A	13	19	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	800	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	300	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, $I_D \approx$ 30A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	30	ns
Rise Time	t_r		–	120	180	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	70	100	ns
Fall Time	t_f		–	80	120	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 30A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	79	120	nC
Gate-Source Charge	Q_{gs}		–	13	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	30	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	120	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 30A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/µs	140	350	630	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/µs	1.8	4.7	8.1	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 30A (See Figure 15)

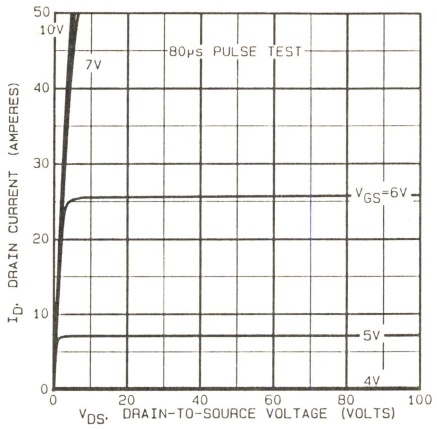


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

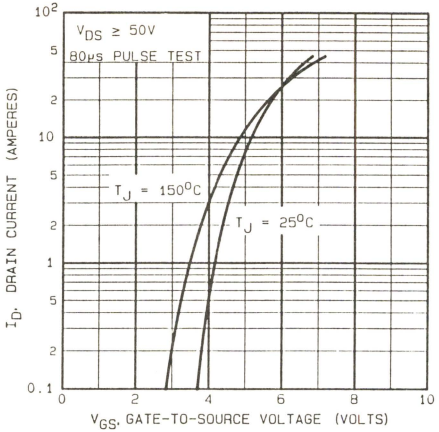


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

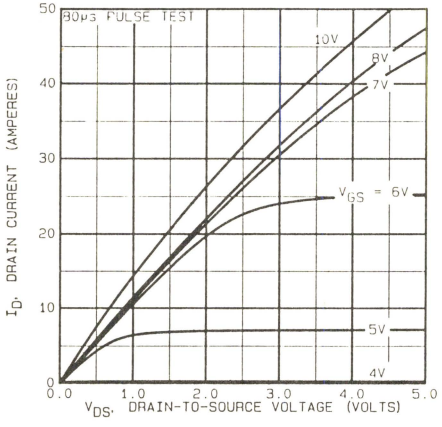


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

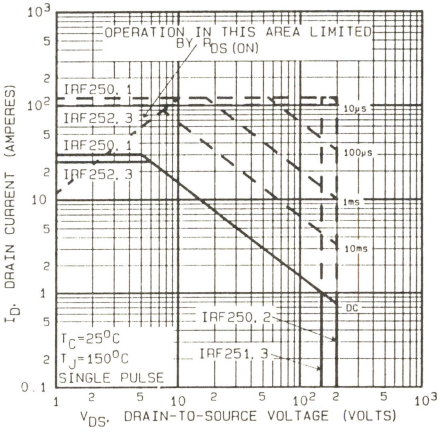


FIGURE 4. MAXIMUM SAFE OPERATING AREA

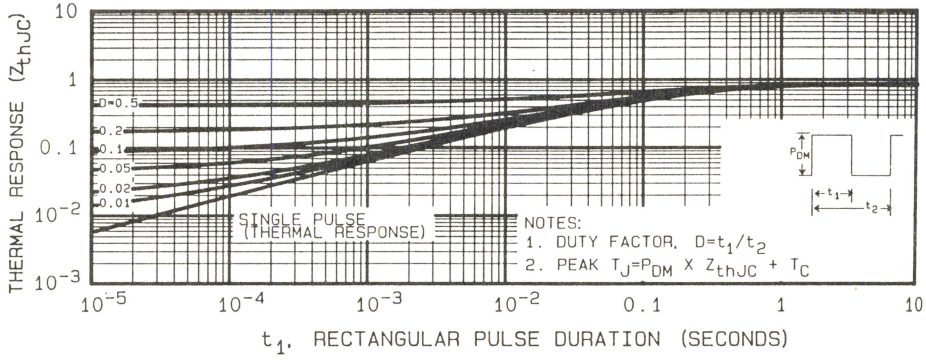


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

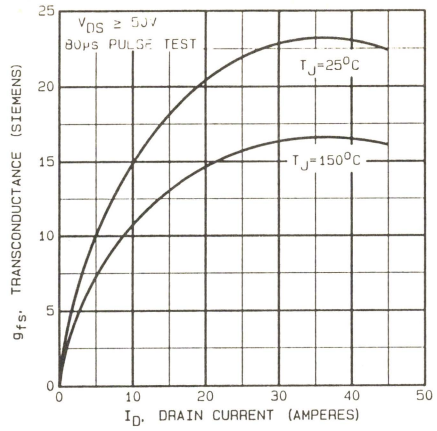


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

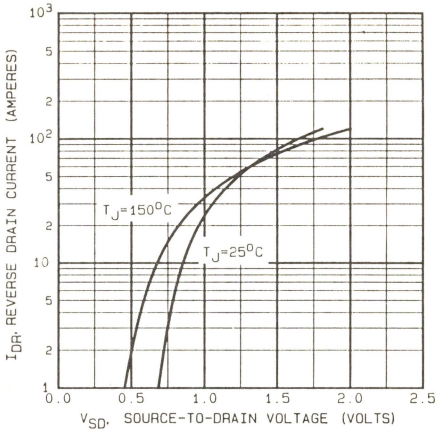


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

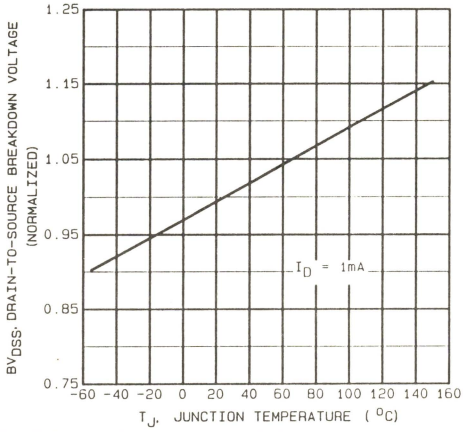


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

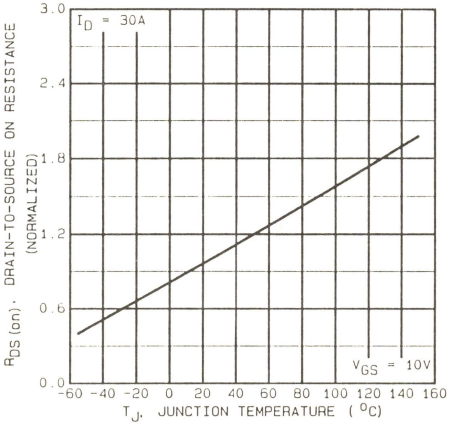


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

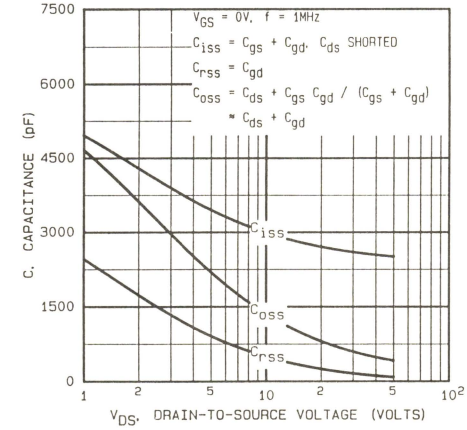


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

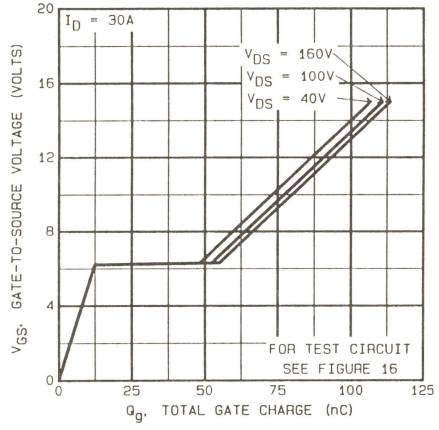


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

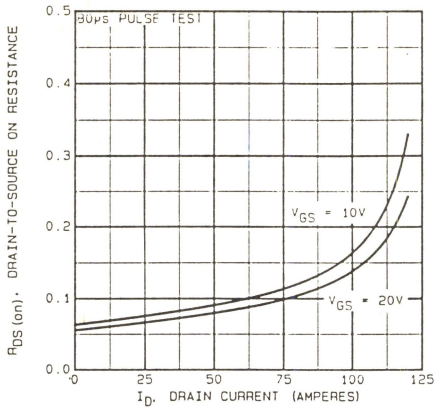


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

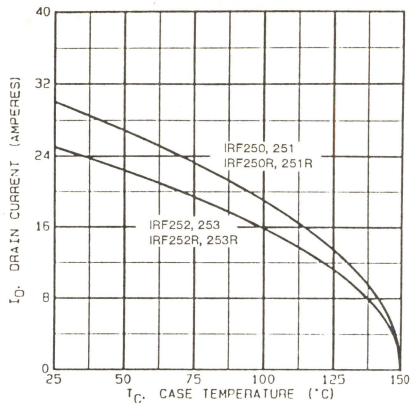


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

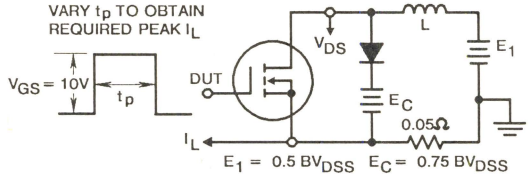


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

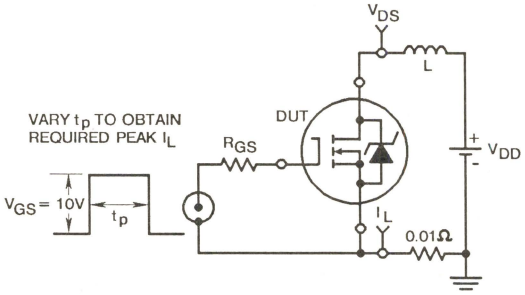


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

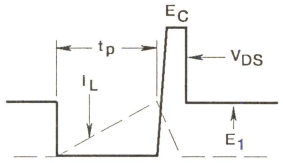


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

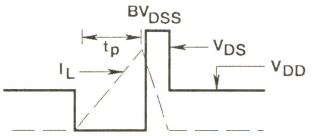


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

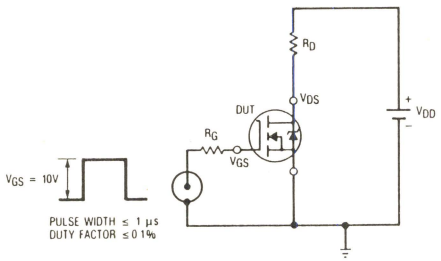


FIGURE 16. SWITCHING TIME TEST CIRCUIT

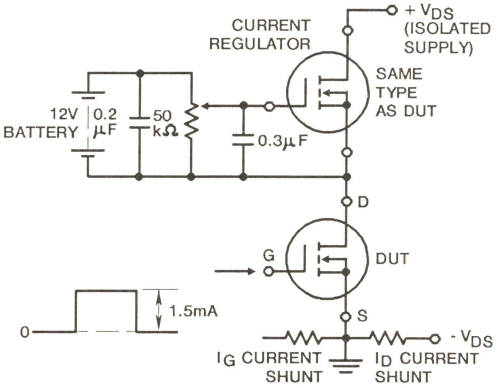


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF254, IRF255
IRF256, IRF257

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 22A and 20A, 275V - 250V
- $r_{DS(on)}$ = 0.14Ω and 0.17Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275, 250V DC Rated - 120V AC Line System Operation

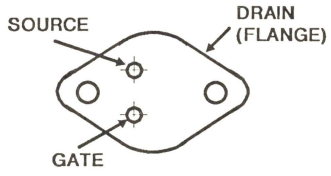
Description

The IRF254, IRF255, IRF256, and IRF257 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AE steel package.

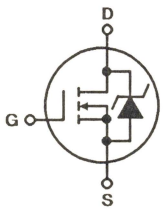
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF254	IRF255	IRF256	IRF257	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	22	20	22	20	A
T_C = +100°C	I_D	14	12	14	12	A
Pulsed Drain Current (3)	I_{DM}	88	80	88	80	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	150	150	150	150	W
Linear Derating Factor		1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	1000	1000	1000	1000	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 3.3mH, R_G = 25Ω, Peak I_L = 22A (See Figures 14 & 15).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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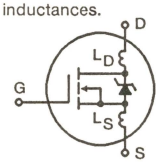
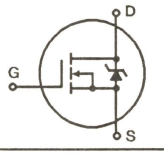
File Number 2300.2

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF254, 1RF255	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	250	–	–	V
IRF256, IRF257			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF254, IRF256	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\ Max}$, V_{GS} = 10V	22	–	–	A
1RF255, IRF257			20	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF254, IRF256	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 12A	–	0.11	0.14	Ω
1RF255. IRF257			–	0.14	0.17	Ω
Forward Transconductance (Note 2)	g_{ts}	$V_{DS} \geq$ 50V, I_D = 12A	11	17	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2700	–	pF
Output Capacitance	C_{OSS}		–	580	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	130	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 22A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	19	29	ns
Rise Time	t_r		–	84	130	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	75	110	ns
Fall Time	t_f		–	65	98	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	87	130	nC
Gate-Source Charge	Q_{gs}		–	14	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	73	–	nC
Internal Drain Inductance	L_D	Measured from the source lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	13	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	22	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	88	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 22A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/µs	150	310	650	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/µs	1.9	4	8.4	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, Starting T_J = +25°C, L = 3.3mH, R_G = 25Ω, Peak I_L = 22A (See Figures 14 & 15).

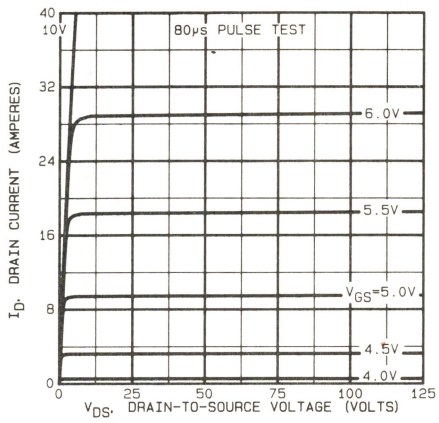


Fig. 1 - Typical output characteristics.

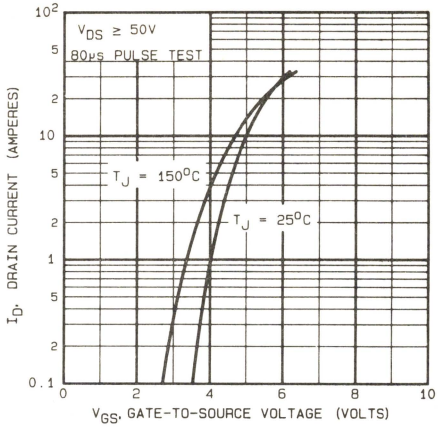


Fig. 2 - Typical transfer characteristics.

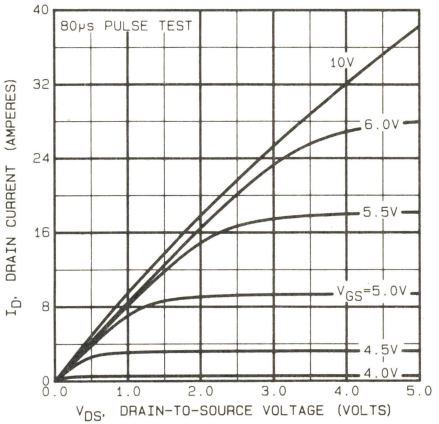


Fig. 3 - Typical saturation characteristics.

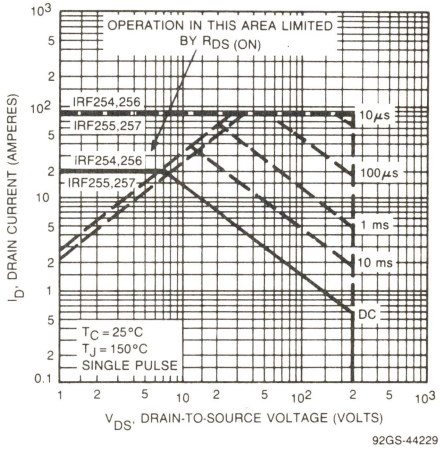


Fig. 4 - Maximum safe operating area.

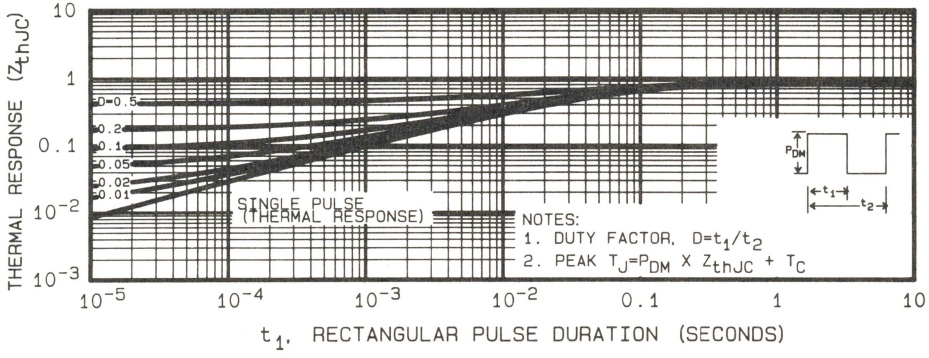


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

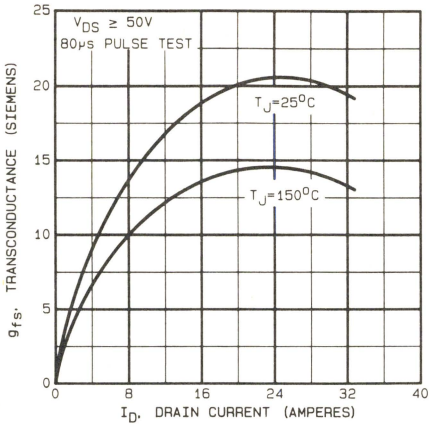


Fig. 6 - Typical transconductance vs. drain current.

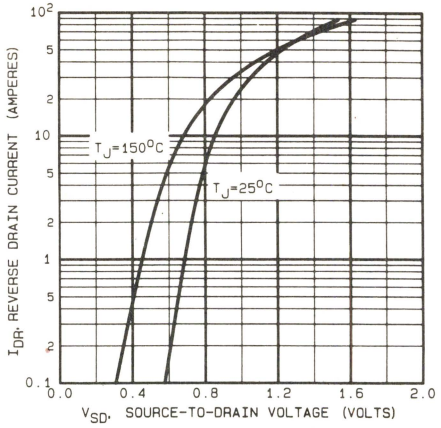


Fig. 7 - Typical source-drain diode forward voltage.

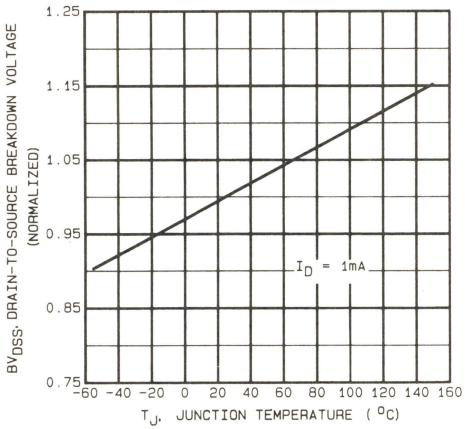


Fig. 8 - Breakdown voltage vs. temperature.

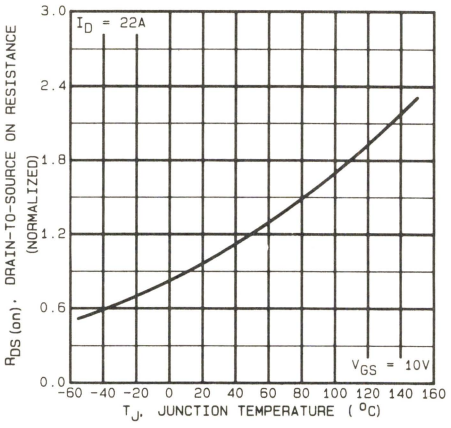


Fig. 9 - Normalized on-resistance vs. temperature.

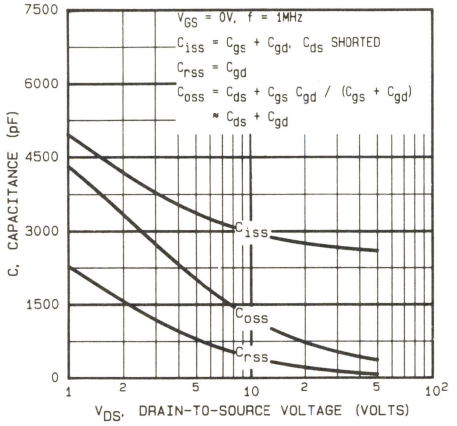


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

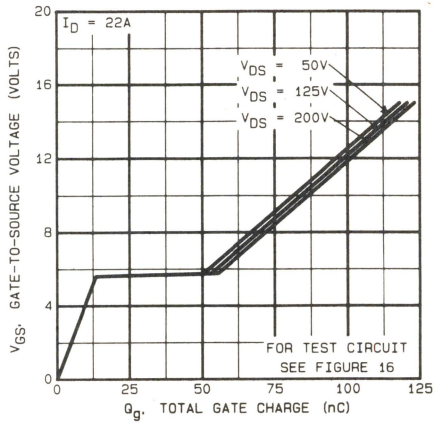


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

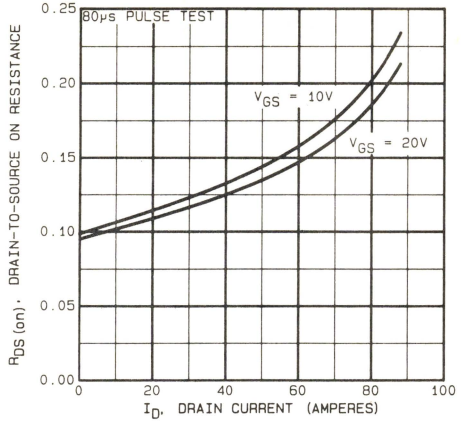


Figure 12. Typical On Resistance vs Drain Current

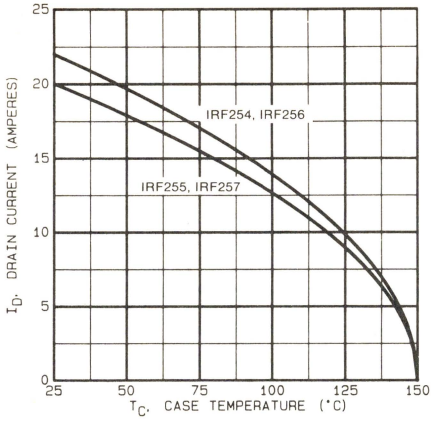


Figure 13. Maximum Drain Current vs Case Temperature

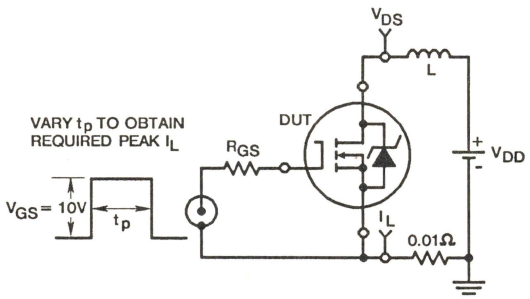


Figure 14. Unclamped Energy Test Circuit

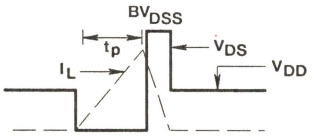


Figure 15. Unclamped Energy Waveforms

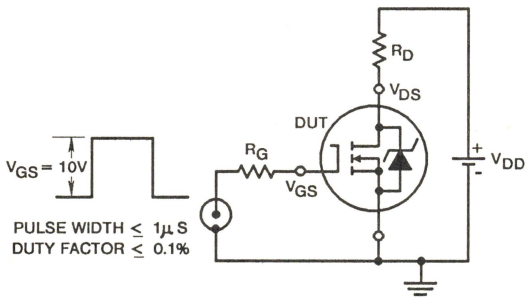


Figure16. Switching Time Test Circuit

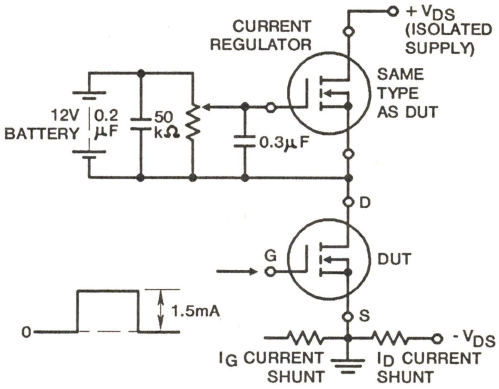


Figure 17. Gate Charge Test Circuit

HARRIS

IRF320, IRF321 IRF322, IRF323

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 2.8A and 3.3A, 350V - 400V
- $r_{DS(on)}$ = 1.8Ω and 2.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

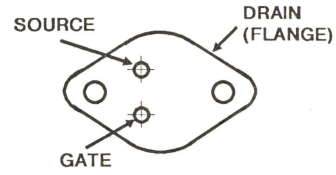
Description

The IRF320, IRF321, IRF322, and IRF323 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

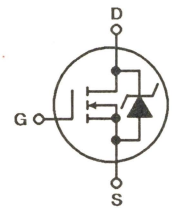
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF320	IRF321	IRF322	IRF323	UNITS
Drain-Source Voltage (1)	V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	400	350	400	350	V
Continuous Drain Current						
T_C = +25°C	I_D	3.3	3.3	2.8	2.8	A
T_C = +100°C	I_D	2.1	2.1	1.8	1.8	A
Pulsed Drain Current (3)	I_{DM}	13	13	11	11	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	50	50	50	50	W
Linear Derating Factor		0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped (See Figures 14 and 15, L = 100μH)	I_{LM}	12	12	10	10	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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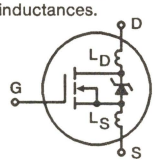
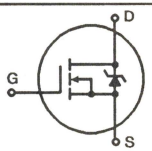
File Number **1569.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF320, IRF322	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRF321, IRF323			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF320, IRF321	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.3	–	–	A
IRF322, IRF323			2.8	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF320, IRF321	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.8A	–	1.5	1.8	Ω
IRF322, IRF323			–	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 1.8A	1.8	2.7	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	450	–	pF
Output Capacitance	C_{OSS}		–	100	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 3.3A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	15	ns
Rise Time	t_r		–	14	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	30	45	ns
Fall Time	t_f		–	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.3A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	12	20	nC
Gate-Source Charge	Q_{gs}		–	3.3	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	11	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	3.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	13	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = 3.3A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	120	270	600	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	0.64	1.4	3.0	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:
1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5)

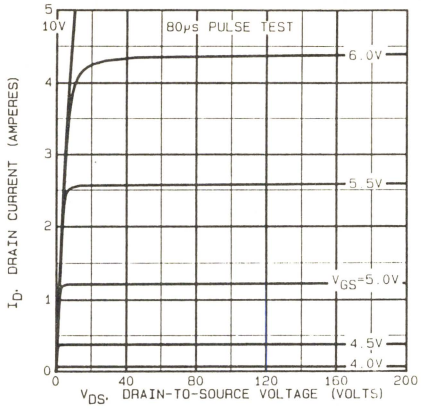


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

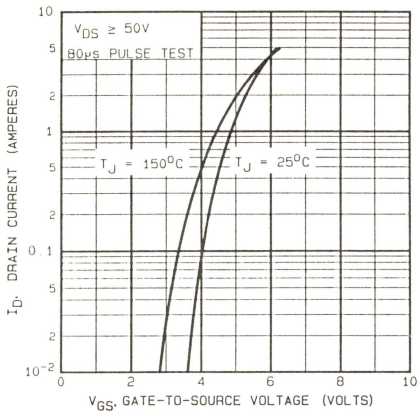


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

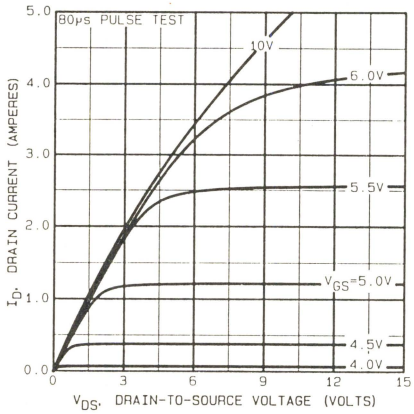


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

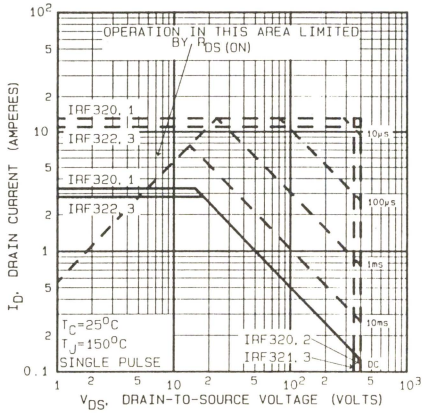


FIGURE 4. MAXIMUM SAFE OPERATING AREA

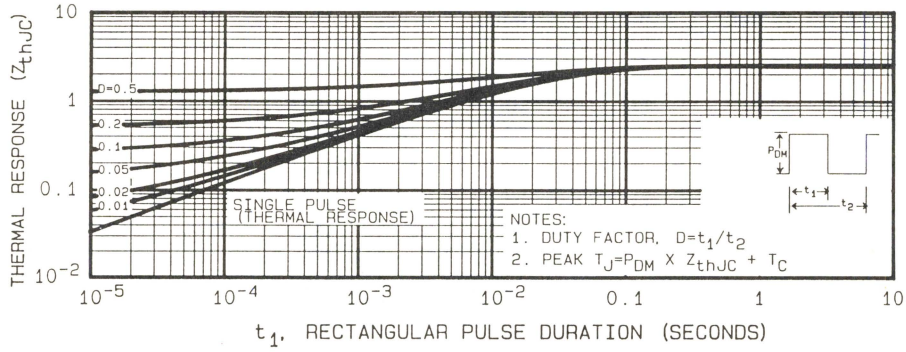


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

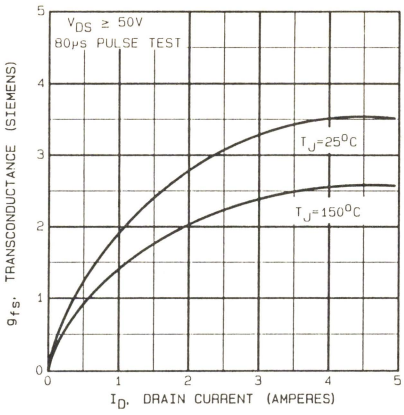


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

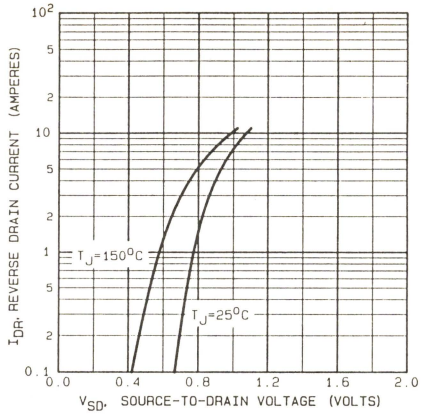


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

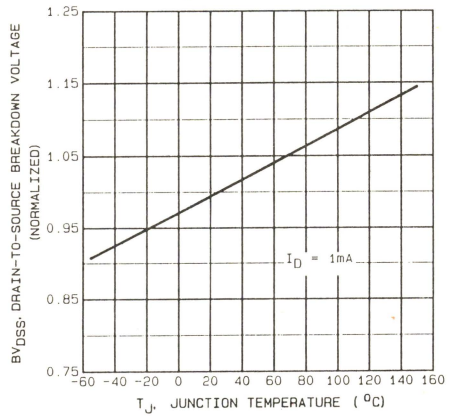


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

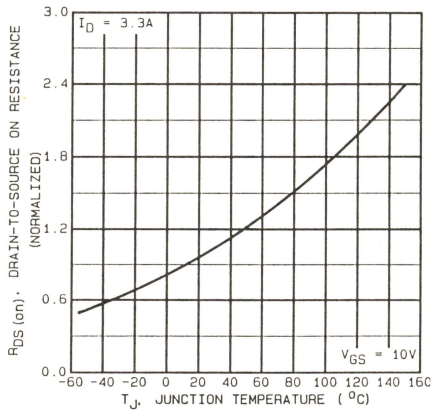


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

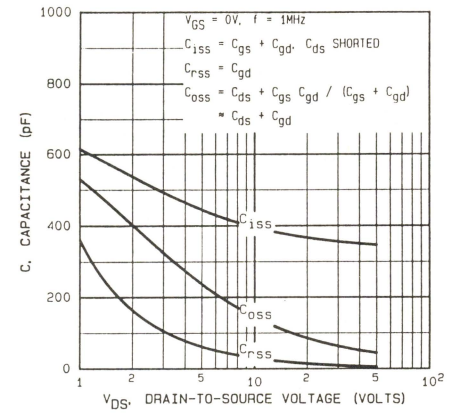


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

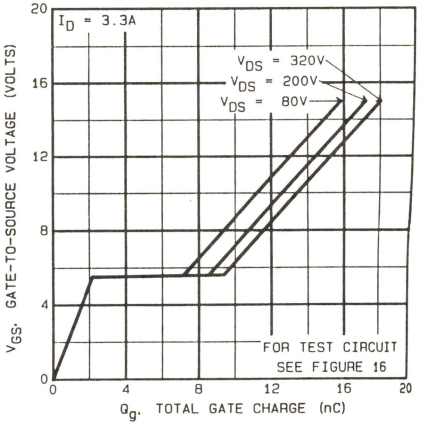


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

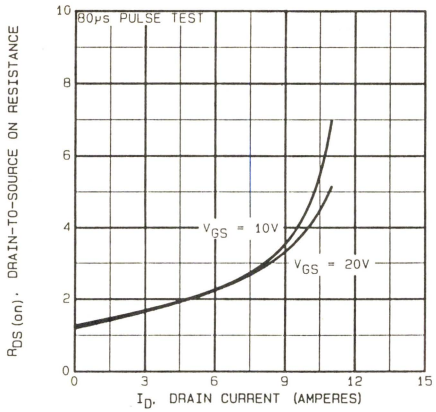


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

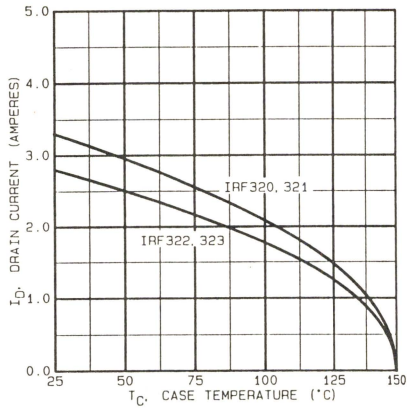


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

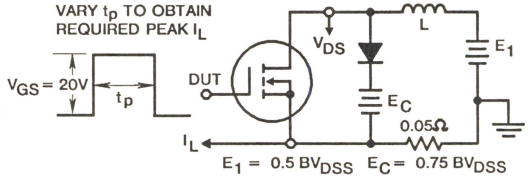


FIGURE 14. CLAMPED INDUCTIVE TEST CIRCUIT

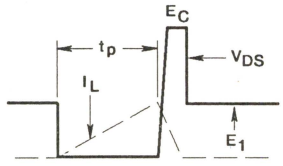


FIGURE 15. CLAMPED INDUCTIVE WAVEFORMS

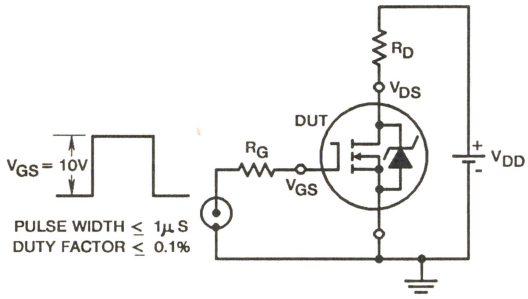


FIGURE 16. SWITCHING TIME TEST CIRCUIT

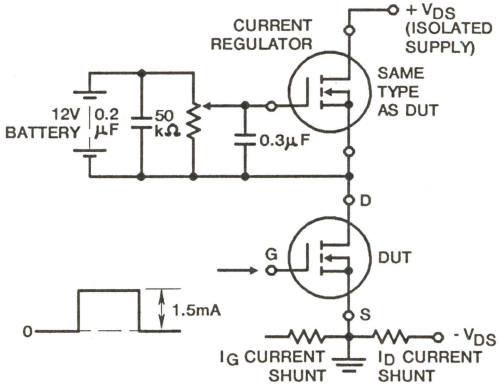


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF330/331/332/333
IRF330R/331R/332R/333R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.5A and 5.5A, 350V - 400V
- $r_{DS(on)}$ = 1.0Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

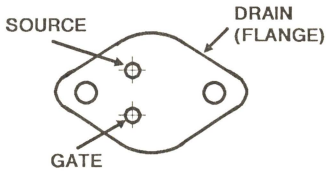
Description

The IRF330, IRF331, IRF332, and IRF333 are n-channel enhancement mode silicon gate power field effect transistors. IRF330R, IRF331R, IRF332R, and IRF333R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of the power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	IRF330 IRF330R	IRF331 IRF331R	IRF332 IRF332R	IRF333 IRF333R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	5.5	5.5	4.5	4.5	A
T_C = +100°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	22	22	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L 100μH)	22	22	18	18	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	300	300	300	300	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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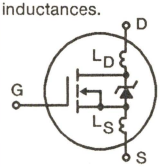
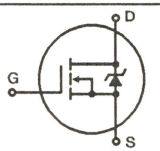
File Number **1570.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF330/332, IRF330R/332R	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	400	-	-	V
IRF331/333, IRF331R/333R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF330/331, IRF330R/331R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	5.5	-	-	A
IRF332/333, IRF332R/333R			4.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF330/331, IRF330R/331R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	-	0.8	1.0	Ω
IRF332/333, IRF332R/333R			-	1.0	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 3.0A	2.9	4.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	700	-	pF
Output Capacitance	C_{OSS}		-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	40	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D ≈ 5.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	11	17	ns
Rise Time	t_r		-	20	29	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	35	56	ns
Fall Time	t_f		-	15	24	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	21	35	nC
Gate-Source Charge	Q_{gs}		-	4	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	17	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	5.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	22	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.5A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/μs	140	400	660	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/μs	0.93	2.4	4.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A (See Figure 15)

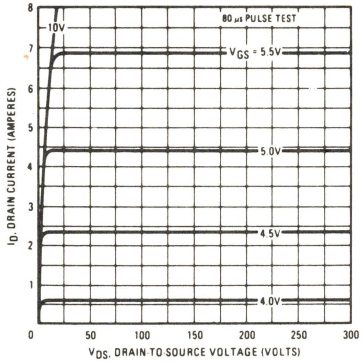


Fig. 1 – Typical Output Characteristics

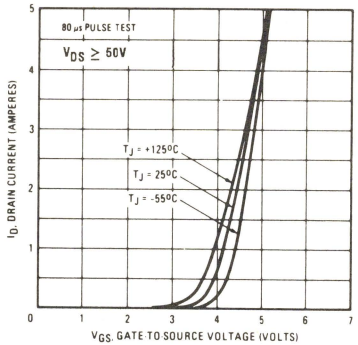


Fig. 2 – Typical Transfer Characteristics

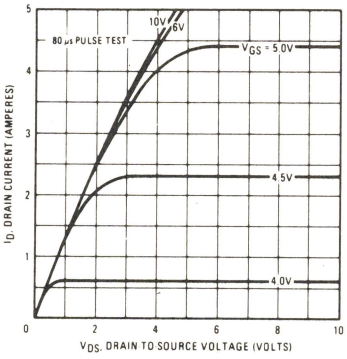


Fig. 3 – Typical Saturation Characteristics

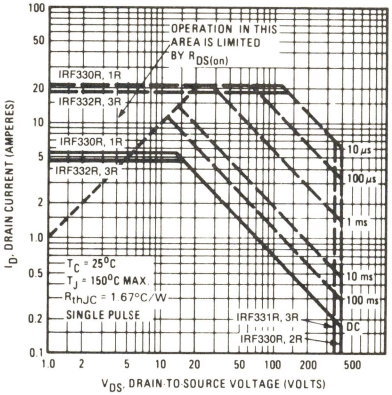


Fig. 4 – Maximum Safe Operating Area

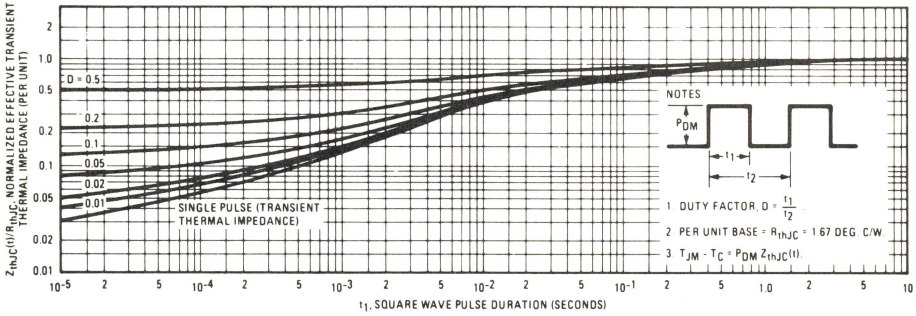


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

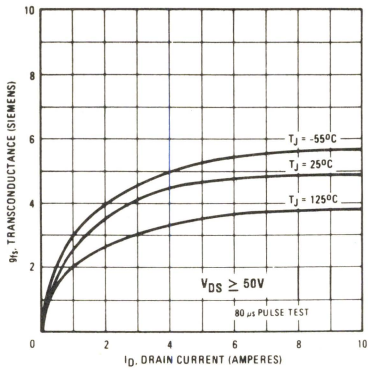


Fig. 6 – Typical Transconductance Vs. Drain Current

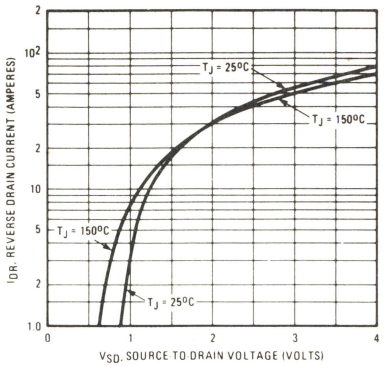


Fig. 7 – Typical Source-Drain Diode Forward Voltage

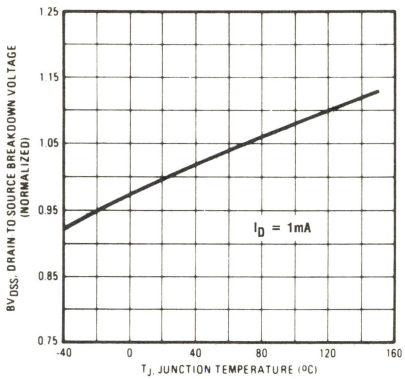


Fig. 8 – Breakdown Voltage Vs. Temperature

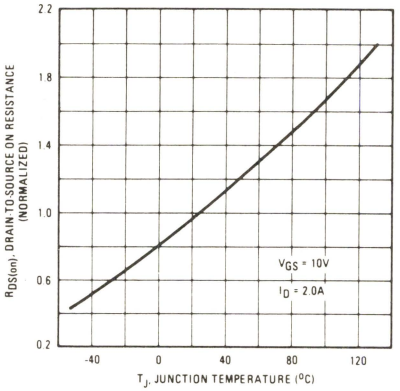


Fig. 9 – Normalized On-Resistance Vs. Temperature

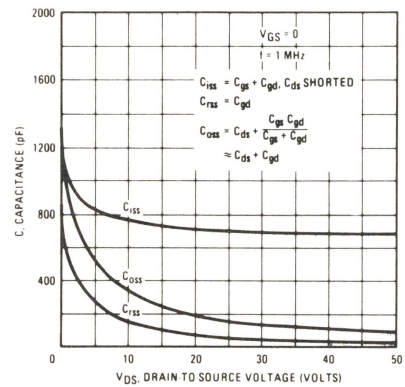


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

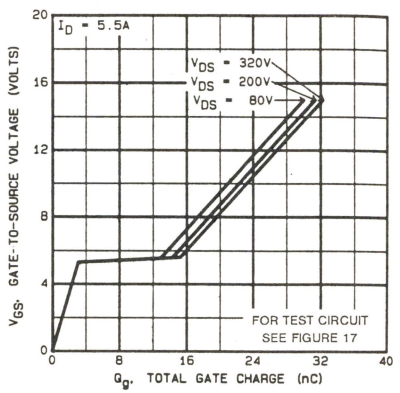


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

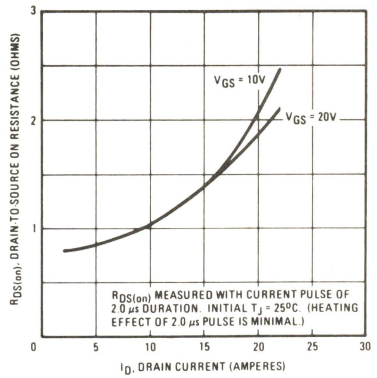


Fig. 12 - Typical On Resistance vs Drain Current

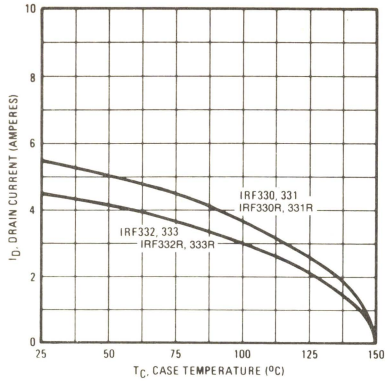


Fig. 13 - Maximum Drain Current vs Case Temperature

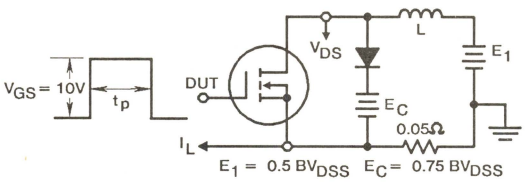


Fig. 14a - Clamped Inductive Test Circuit

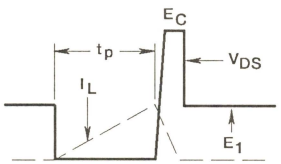


Fig. 14b - Clamped Inductive Waveforms

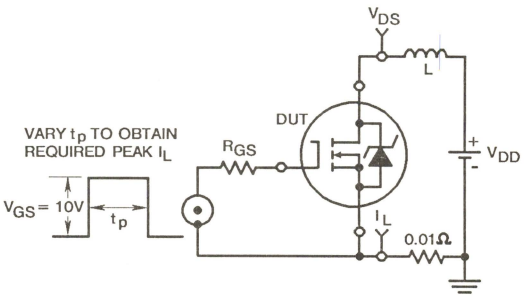


Fig. 15a - Unclamped Energy Test Circuit

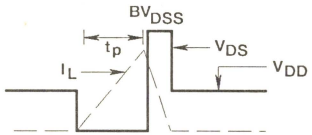


Fig. 15b - Unclamped Energy Waveforms

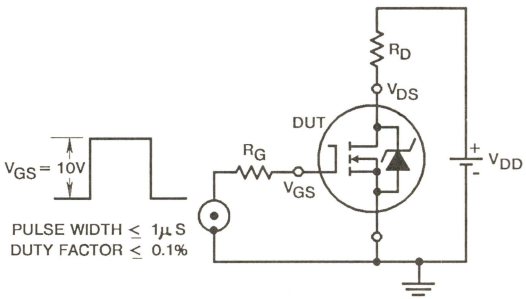


Fig. 16 - Switching Time Test Circuit

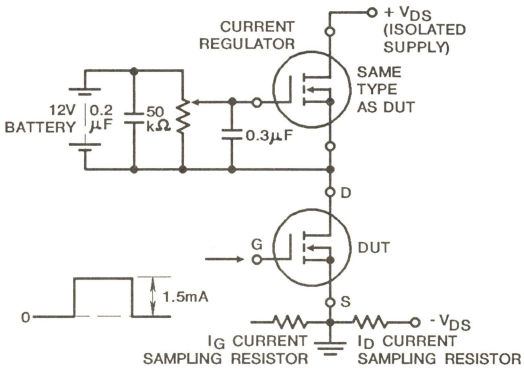


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRF340/341/342/343
IRF340R/341R/342R/343R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 10A and 8.3A, 400V - 350V
- $r_{DS(on)}$ = 0.55Ω and 0.80Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

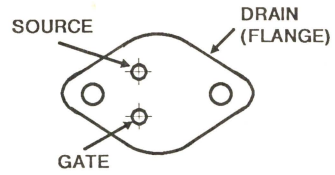
Description

The IRF340, IRF341, IRF342, and IRF343 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF340R, IRF341R, IRF342R, and IRF343R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

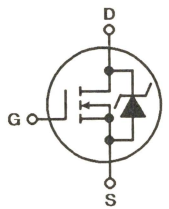
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF340 IRF340R	IRF341 IRF341R	IRF342 IRF342R	IRF343 IRF343R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	10	10	8.3	8.3	A
T_C = +100°C ..... I_D	6.3	6.3	5.2	5.2	A
Pulsed Drain Current (3) ..... I_{DM}	40	40	33	33	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	40	40	32	32	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	520	520	520	520	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max junction temp. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 10A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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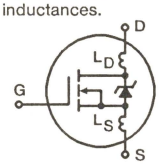
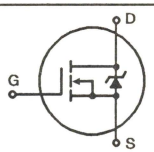
File Number **2307.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF340/342, IRF340R/342R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
IRF341/343, IRF341R/343R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF340/341, IRF340R/341R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	10	–	–	A
IRF342/343, IRF342R/343R			8.3	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF340/341, IRF340R/341R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.2A	–	0.4	0.55	Ω
IRF342/343, IRF342R/343R			–	0.5	0.80	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 5.2A	5.8	8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1250	–	pF
Output Capacitance	C_{OSS}		–	300	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D ≈ 10A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	17	21	ns
Rise Time	t_r		–	27	41	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	45	75	ns
Fall Time	t_f		–	20	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	41	63	nC
Gate-Source Charge	Q_{gs}		–	7	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	23	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	10	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	40	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 10A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	170	350	790	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	1.6	4.0	8.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 10A (See Figure 15)

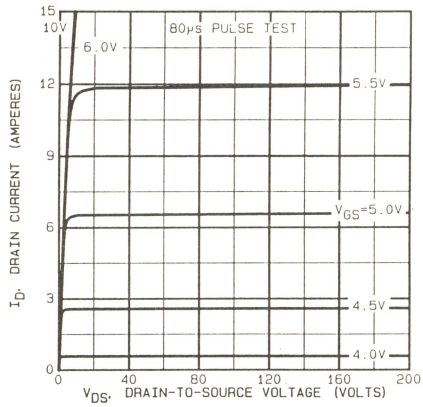


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

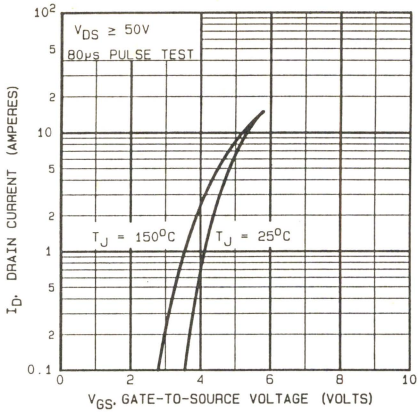


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

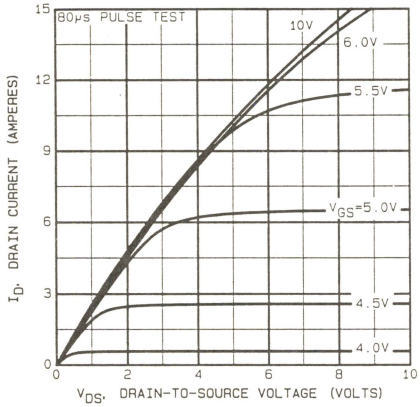


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

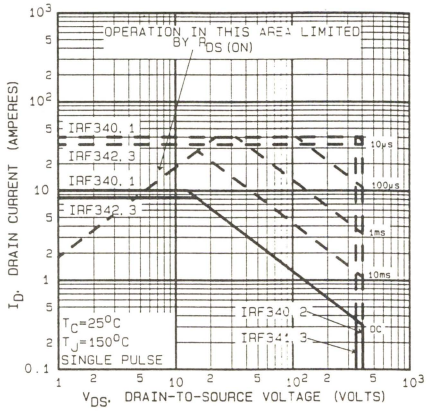


FIGURE 4. MAXIMUM SAFE OPERATING AREA

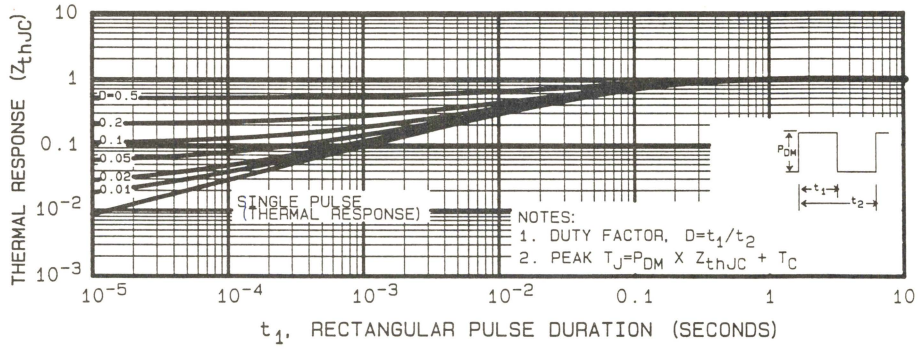


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

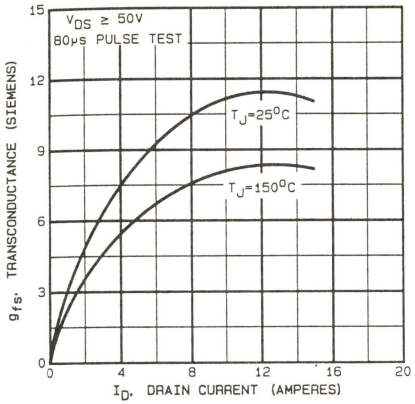


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

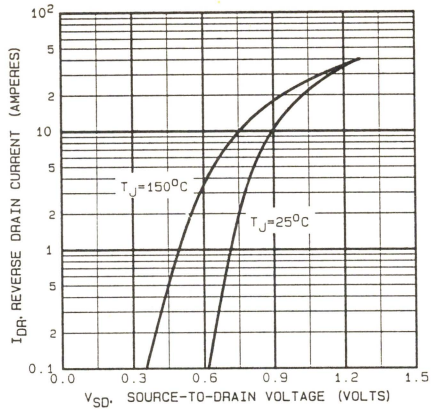


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

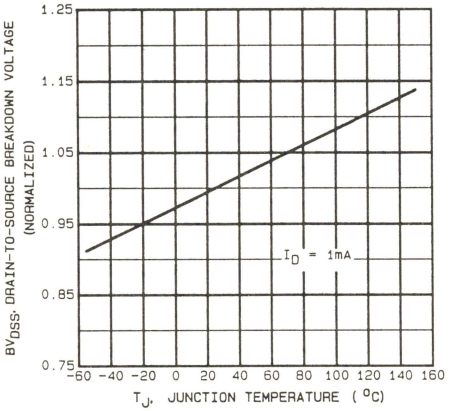


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

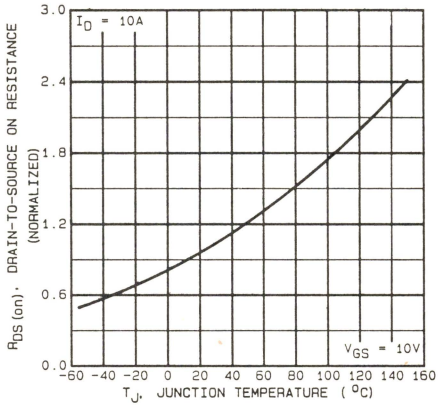


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

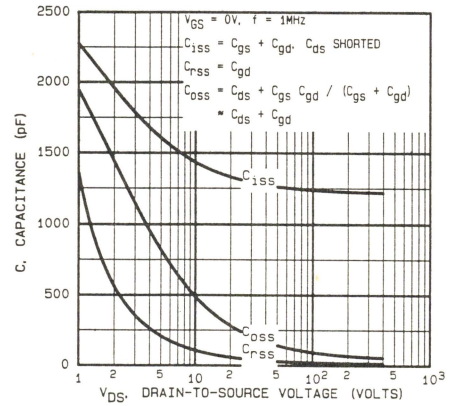


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

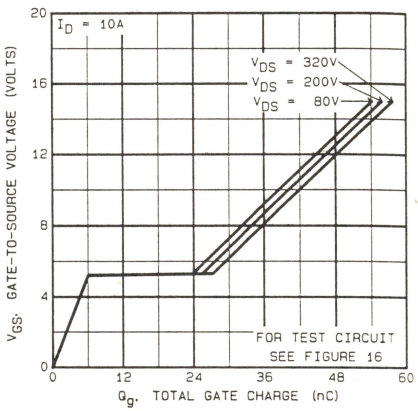


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

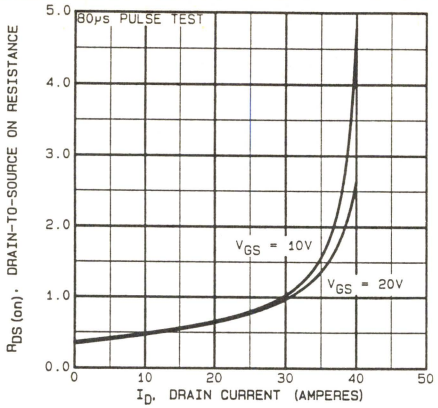


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

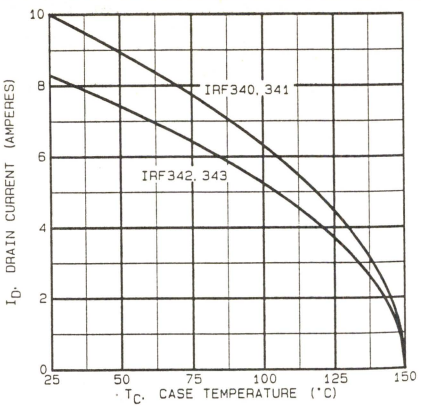


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

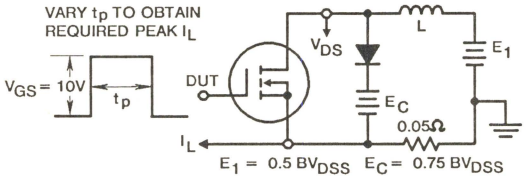


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

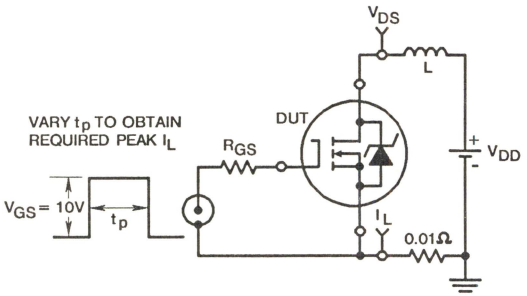


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

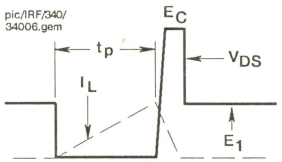


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

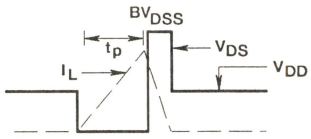


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

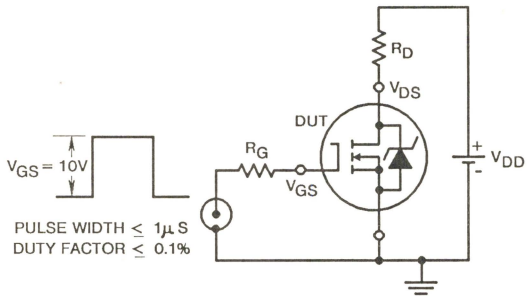


FIGURE 16. SWITCHING TIME TEST CIRCUIT

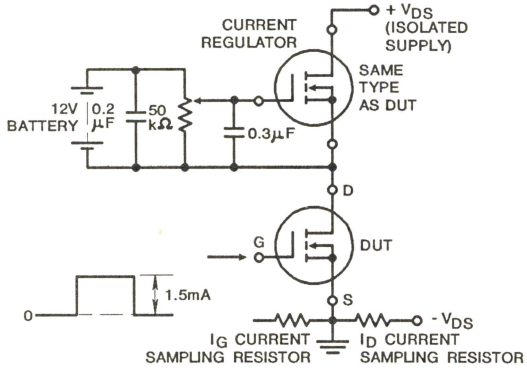


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF350/351/352/353
IRF350R/351R/352R/353R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 13A and 15.0A, 350V - 400V
- $r_{DS}(on)$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

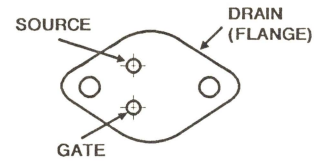
Description

The IRF350, IRF351, IRF352, and IRF353 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF350R, IRF351R, IRF352R and IRF353R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

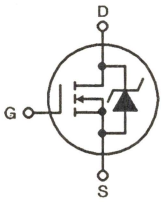
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF350 IRF350R	IRF351 IRF351R	IRF352 IRF352R	IRF353 IRF353R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	15	15	13	13	A
T_C = +100°C ..... I_D	9.0	9.0	8.0	8.0	A
Pulsed Drain Current (3) ..... I_{DM}	60	60	52	52	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	60	60	52	52	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	700	700	700	700	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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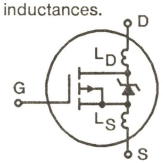
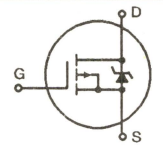
File Number **1826.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF350/352, IRF350R/352R	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	400	–	–	V
IRF351/353, IRF351R/353R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF350/351, IRF350R/351R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	15	–	–	A
IRF352/353, IRF352R/353R			13	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF350/351, IRF350R/351R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.0A	–	0.25	0.3	Ω
IRF352/353, IRF352R/353R			–	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{ts}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)Max}$, I_D = 8.0A	8.0	10	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 180V, I_D = 8.0A, Zo = 4.7Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	35	ns
Rise Time	t_r		–	–	65	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	150	ns
Fall Time	t_f		–	–	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	79	120	nC
Gate-Source Charge	Q_{gs}		–	38	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	41	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	15	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	60	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 15A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/μs	–	1000	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/μs	–	6.6	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 40V, Start T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A (See Figure 15)

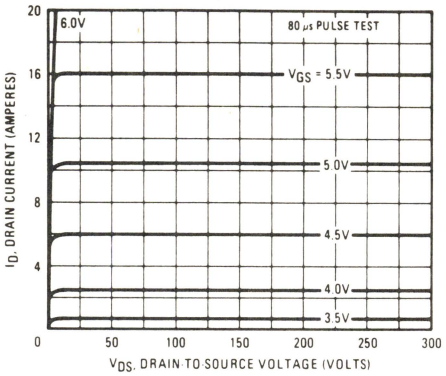


Fig. 1 — Typical Output Characteristics

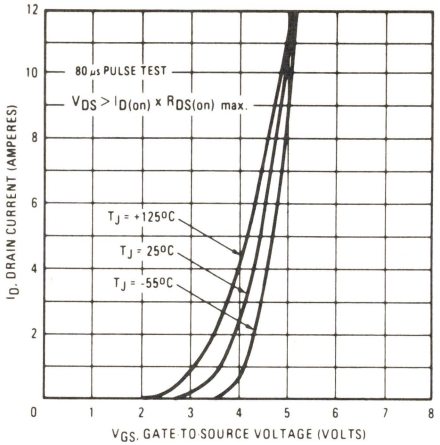


Fig. 2 — Typical Transfer Characteristics

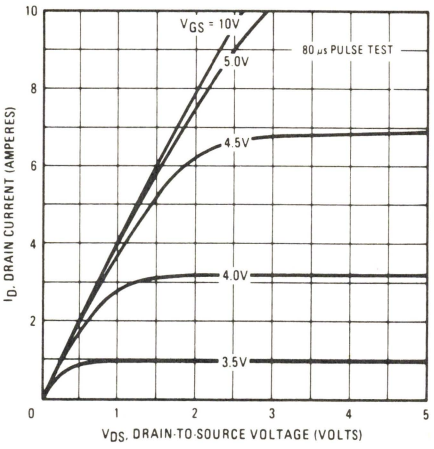


Fig. 3 — Typical Saturation Characteristics

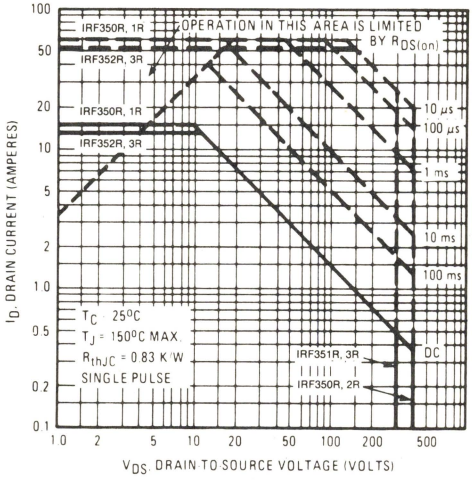


Fig. 4 — Maximum Safe Operating Area

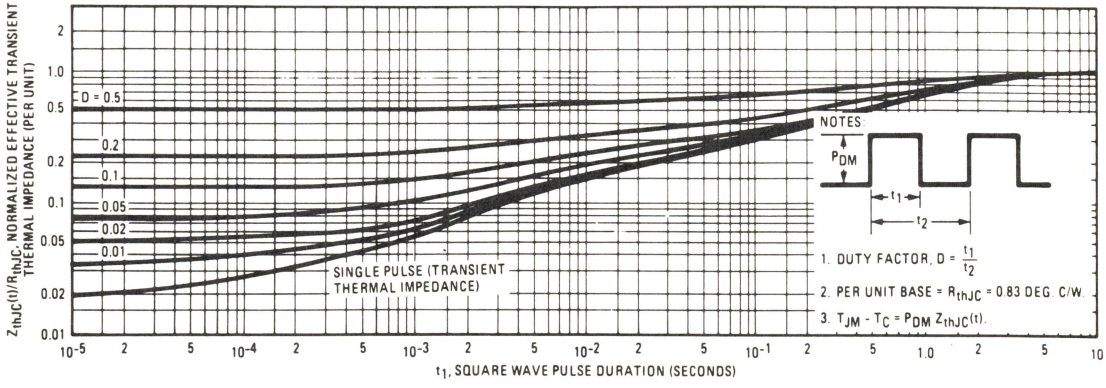


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

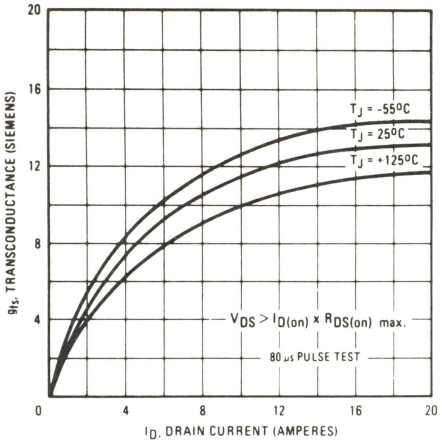


Fig. 6 – Typical Transconductance Vs. Drain Current

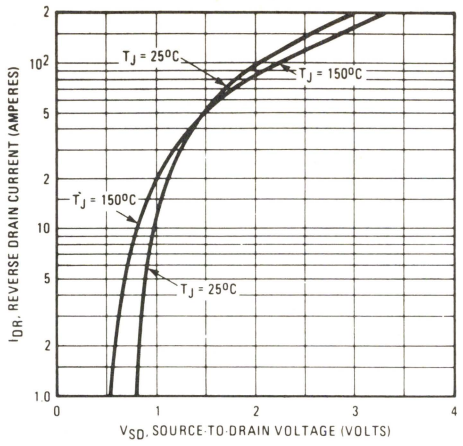


Fig. 7 – Typical Source-Drain Diode Forward Voltage

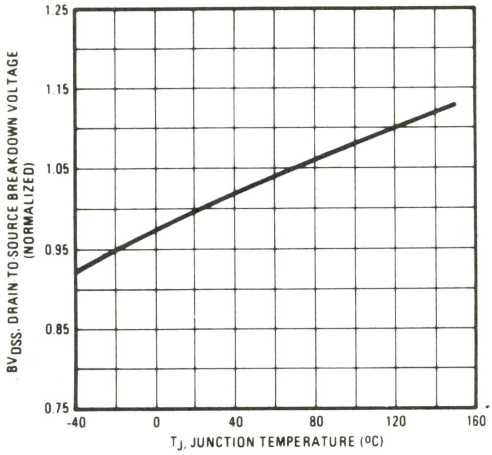


Fig. 8 – Breakdown Voltage Vs. Temperature

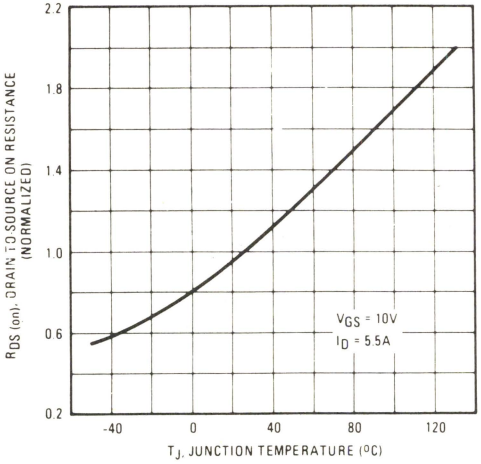


Fig. 9 – Normalized On-Resistance Vs. Temperature

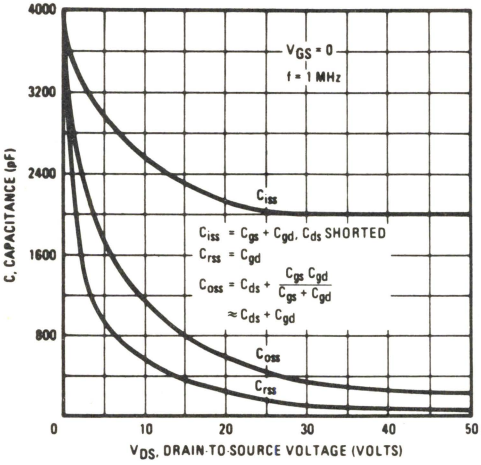


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

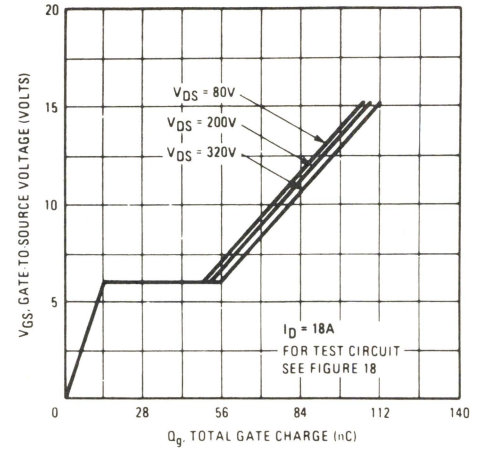


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

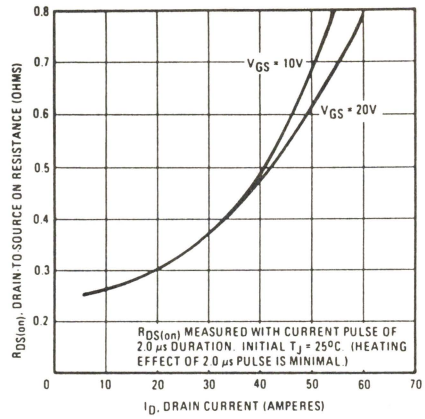


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

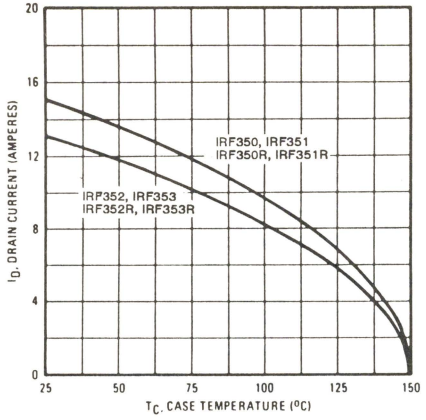


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

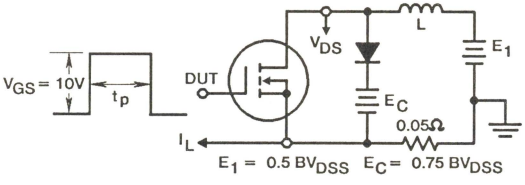


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

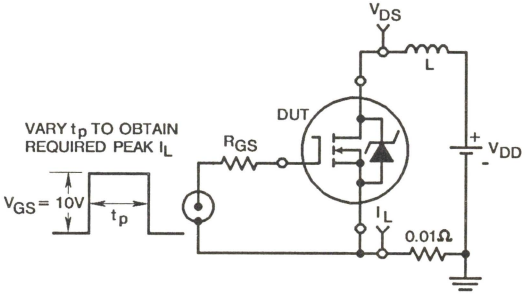


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

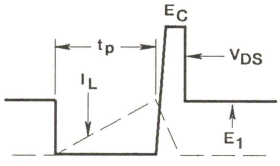


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

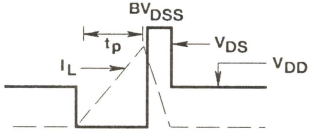


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

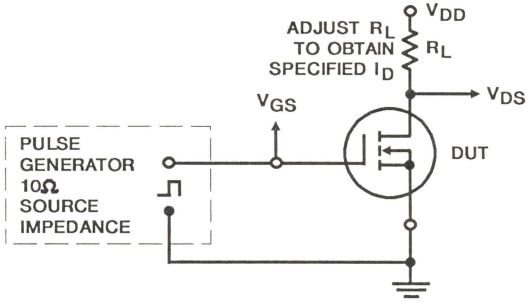


FIGURE 16. SWITCHING TIME TEST CIRCUIT

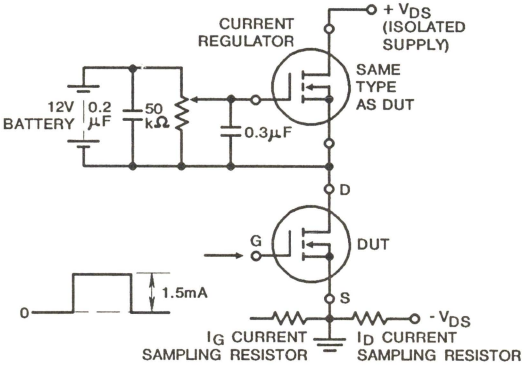


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF360
IRF362

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 25A and 22A, 400V
- $r_{DS}(on)$ = 0.20Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

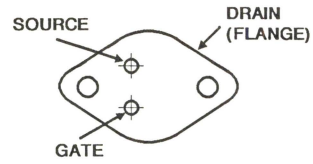
Description

The IRF360 and IRF362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

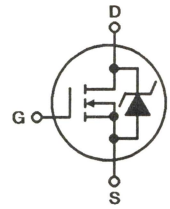
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF360	IRF362	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	25	22	A
T_C = +100°C ..... I_D	16	14	A
Pulsed Drain Current (1) ..... I_{DM}	100	88	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	300	300	W
Linear Derating Factor	2.4	2.4	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS} See Figure 14	980	980	mj
Avalanche Current, Repetitive or Non-repetitive (1) ..... I_{AR}	25	25	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 2.8mH, R_{GS} = 25Ω, Peak I_L = 25A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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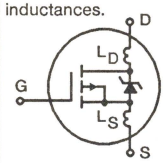
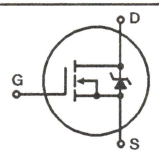
File Number **2276.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 3) IRF360	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	25	–	–	A
IRF362			22	–	–	A
Static Drain-Source On-State Resistance (Note 3) IRF360	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 14A	–	0.18	0.20	Ω
IRF362			–	0.20	0.25	Ω
Forward Transconductance (Note 3)	g_{fs}	I_{DS} = 14A, $V_{DS} \geq$ 50V	14	21	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	4000	–	pF
Output Capacitance	C_{OSS}		–	550	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	97	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 25A, R_G = 4.3Ω R_D = 7.5Ω. (MOSFET switching times are essentially independent of operating temperature)	–	22	33	ns
Rise Time	t_r		–	94	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	80	120	ns
Fall Time	t_f		–	66	99	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 25A, V_{DS} = 0.8V x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	120	170	nC
Gate-Source Charge	Q_{gs}		–	19	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	60	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	13	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.42	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	100	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 25A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	200	460	1000	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	3.1	7.1	16	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:
1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 50V, Starting T_J = +25°C, L = 2.8mH, I_L = 25A
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

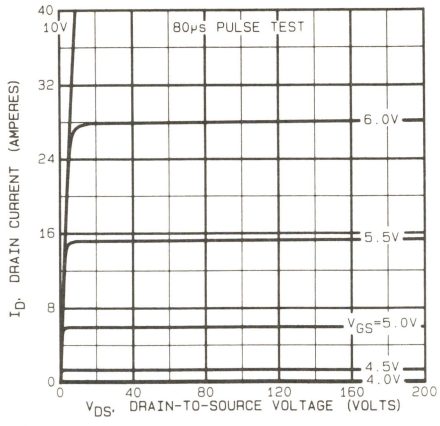


Fig. 1 - Typical output characteristics.

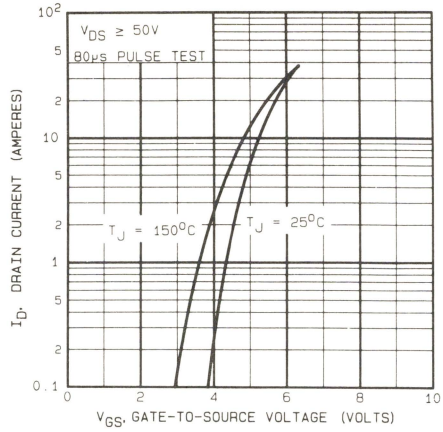


Fig. 2 - Typical transfer characteristics.

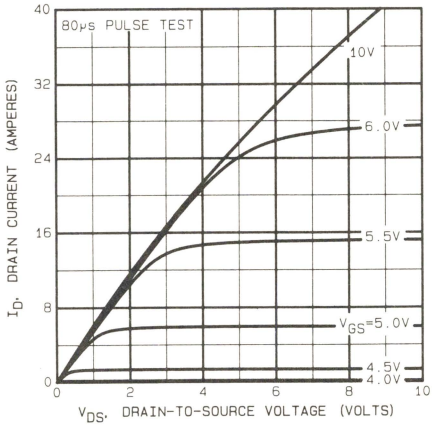


Fig. 3 - Typical saturation characteristics.

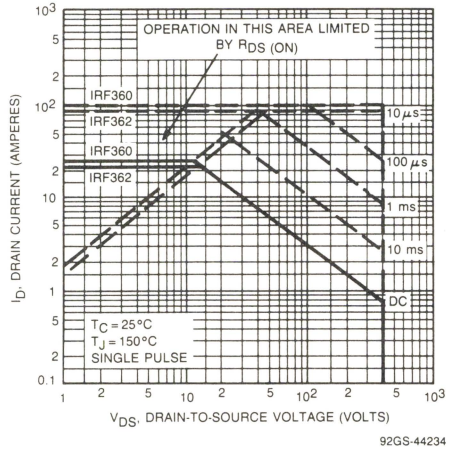
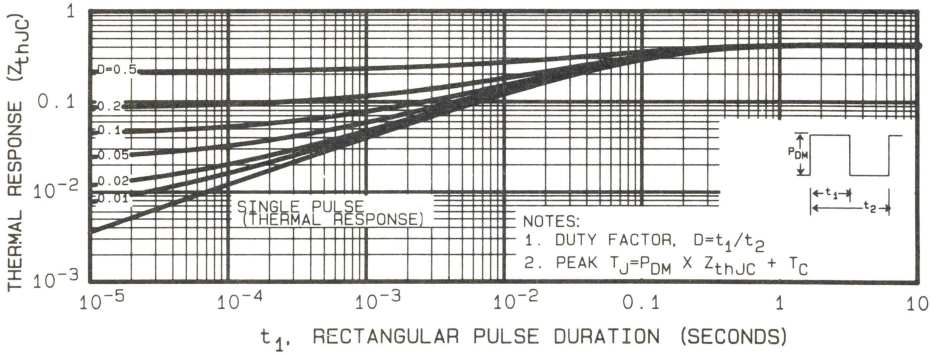


Fig. 4 - Maximum safe operating area.



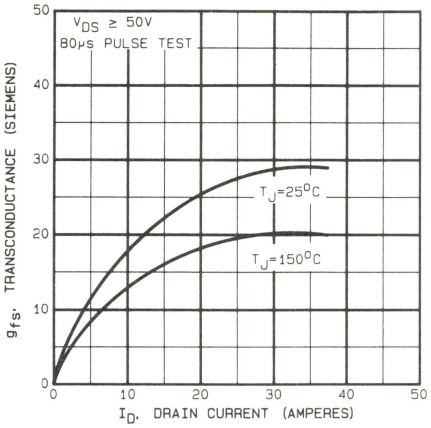


Fig. 6 - Typical transconductance vs. drain current.

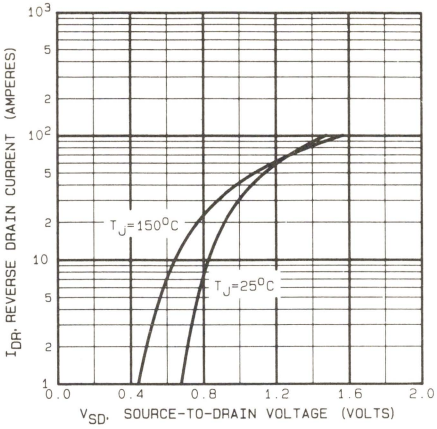


Fig. 7 - Typical source-drain diode forward voltage.

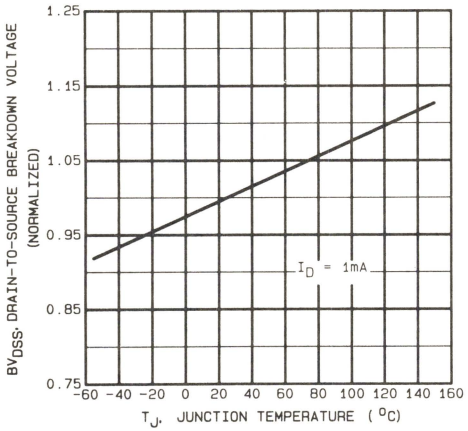


Fig. 8 - Breakdown voltage vs. temperature.

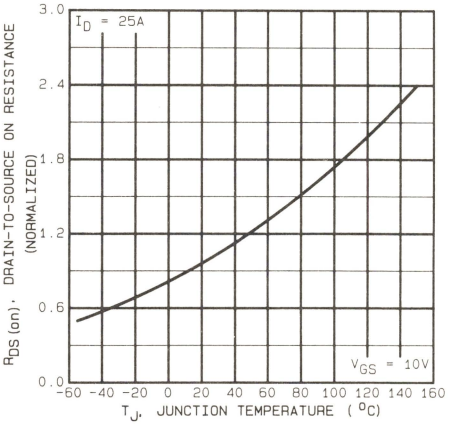


Fig. 9 - Normalized on-resistance vs. temperature.

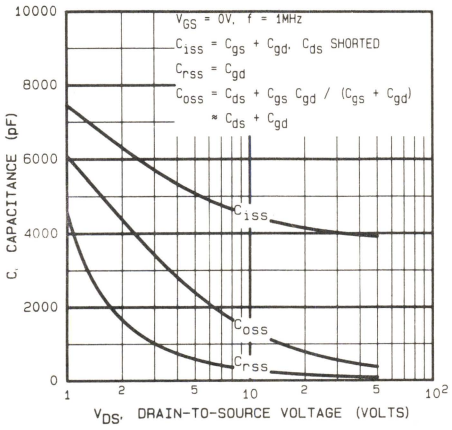


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

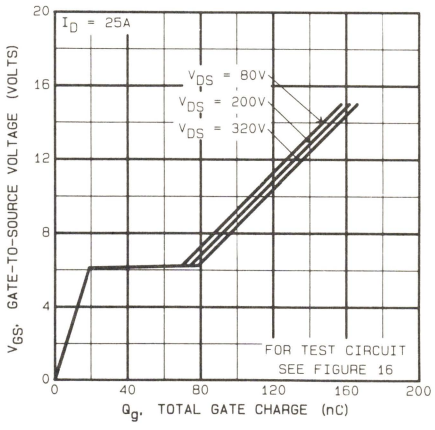


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

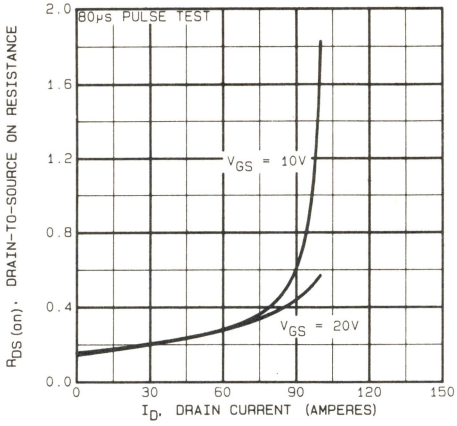


Fig. 12 - Typical on-resistance vs. drain current.

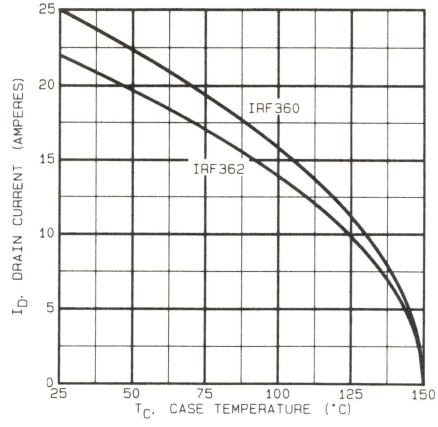


Fig. 13 - Maximum drain current vs. case temperature.

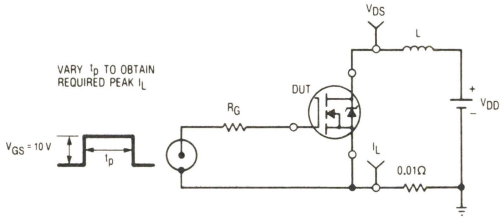


Fig. 14a - Unclamped inductive test circuit.

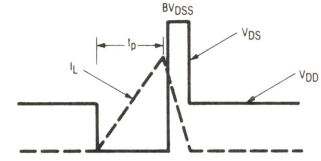


Fig. 14b - Unclamped inductive waveforms.

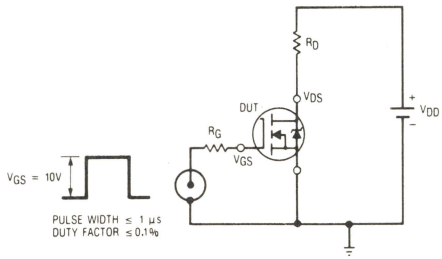


Fig. 15a - Switching time test circuit.

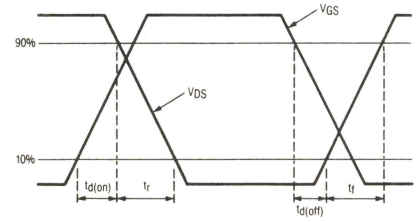


Fig. 15b - Switching time waveforms.

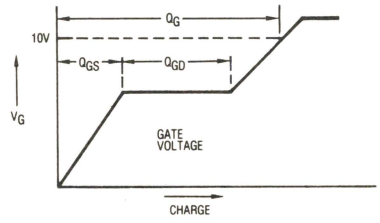


Fig. 16a - Basic gate charge waveform.

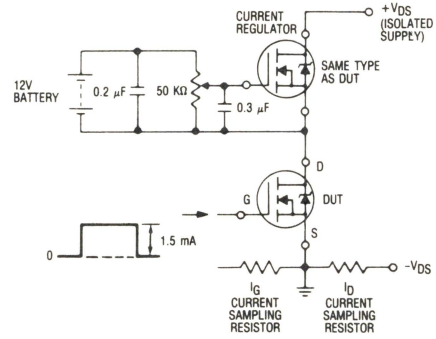


Fig. 16b - Gate charge test circuit.

IRF420, IRF421
IRF422, IRF423

N-Channel Enhnancement Mode Power Field-Effect Transistors

August 1991

Features

- 2.2A and 2.5A, 450V - 500V
- $r_{DS}(on)$ = 3.0Ω and 4.0Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

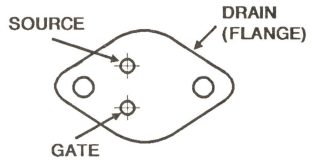
Description

The IRF420, IRF421, IRF422, and IRF423 are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF420	IRF421	IRF422	IRF423	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	2.5	2.5	2.2	2.2	A
T_C = +100°C ..... I_D	1.6	1.6	1.4	1.4	A
Pulsed Drain Current (3) ..... I_{DM}	10	10	8.0	8.0	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	50	50	50	50	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped ..... (See Figures 14 & 15, L = 100μH)	10	10	8.0	8.0	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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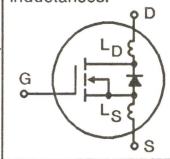
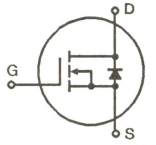
File Number **1571.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF420, IRF422	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	–	–	V
IRF421, IRF423			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF420, IRF241	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	2.5	–	–	A
IRF242, IRF243			2.2	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF420, IRF241	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.4A	–	2.5	3.0	Ω
IRF242, IRF243			–	3.0	4.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 1.4A	1.5	2.3	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	300	–	pF
Output Capacitance	C_{OSS}		–	75	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 2.5A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	15	ns
Rise Time	t_r		–	12	18	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	28	42	ns
Fall Time	t_f		–	12	18	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	19	nC
Gate-Source Charge	Q_{gs}		–	5.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	10	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.5A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	130	270	540	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	0.57	1.2	2.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

Performance Curves

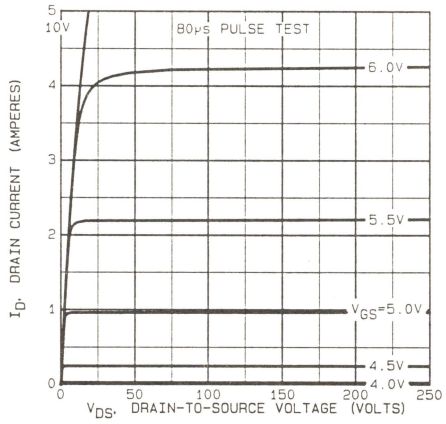


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

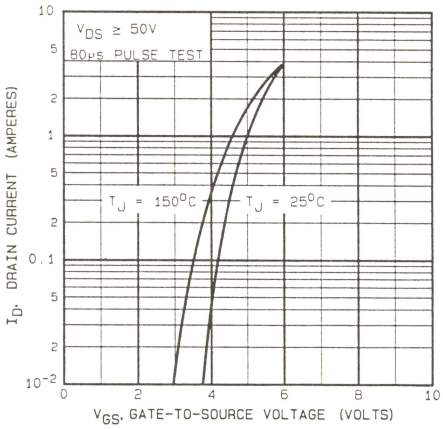


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

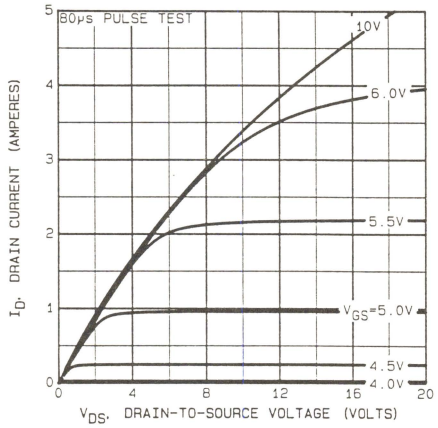


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

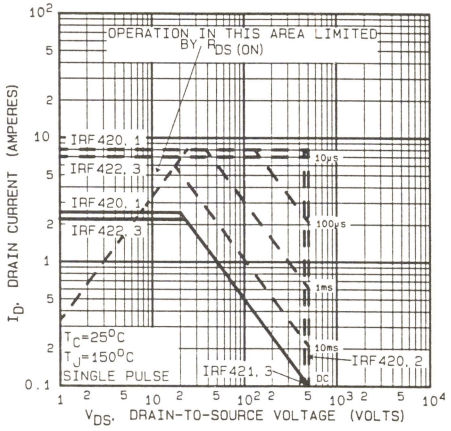


FIGURE 4. MAXIMUM SAFE OPERATING AREA

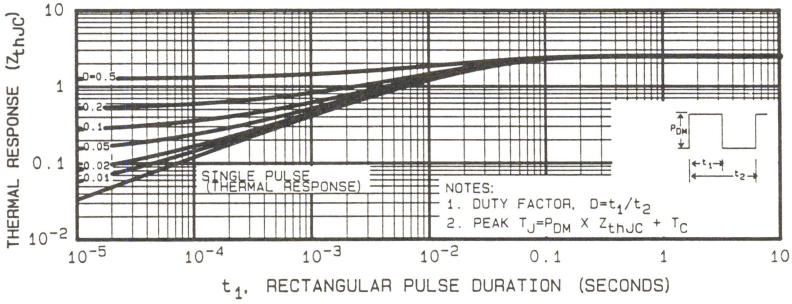


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

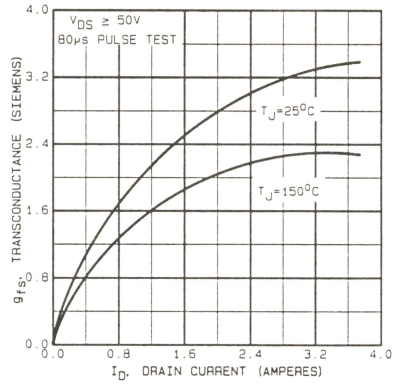


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

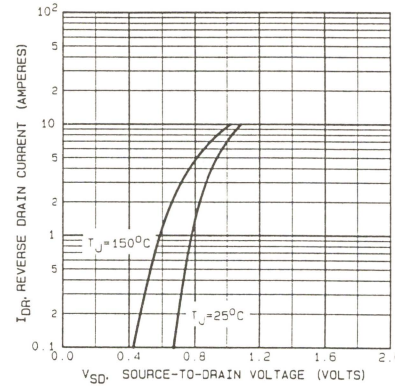


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

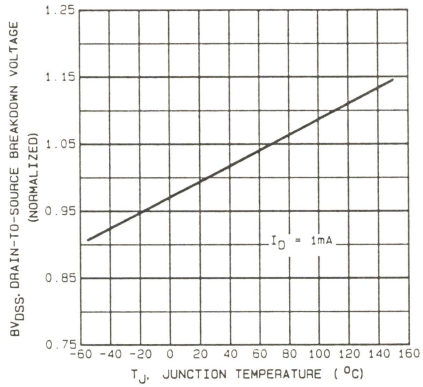


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

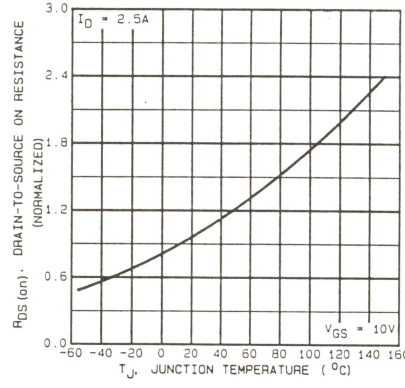


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

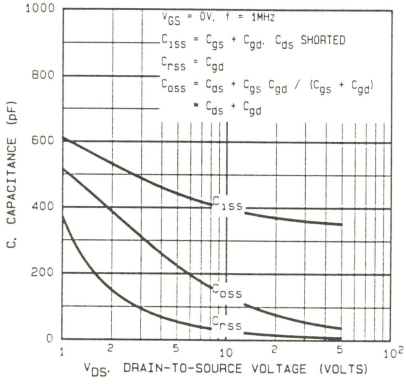


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

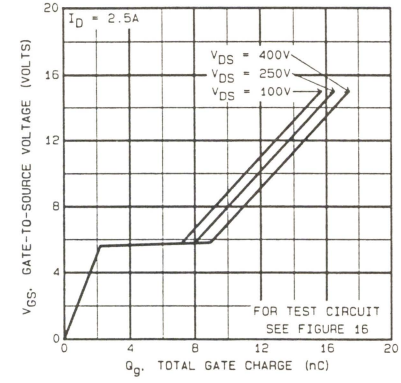


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

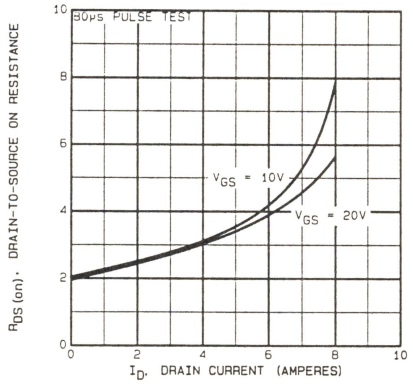


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

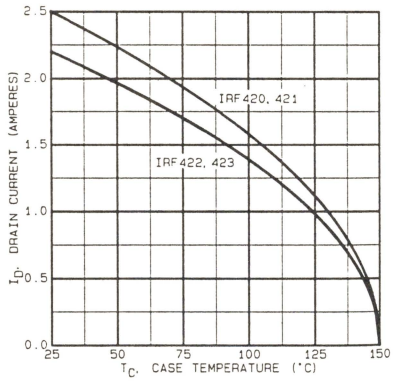


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

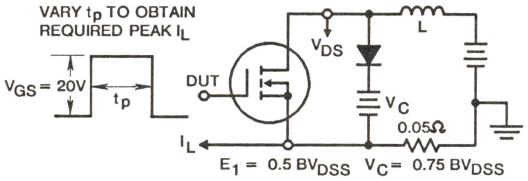


FIGURE 14. CLAMPED INDUCTIVE TEST CIRCUIT

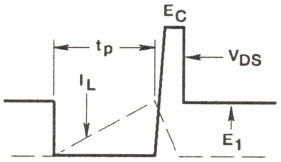


FIGURE 15. CLAMPED INDUCTIVE WAVEFORMES

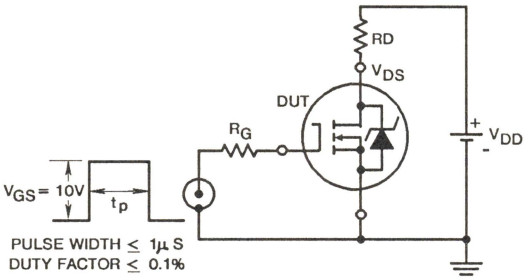


FIGURE 16. SWITCHING TIME TEST CIRCUIT

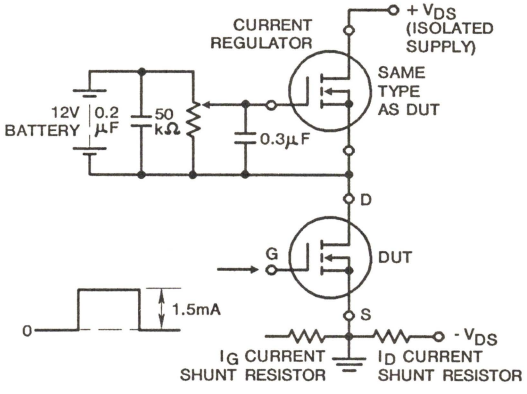


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF430/431/432/433
IRF430R/431R/432R/433R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.0A and 4.5A, 450V - 500V
- $r_{DS}(on)$ = 1.5Ω and 2.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

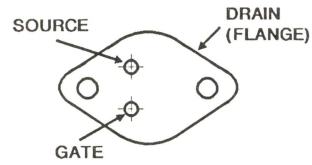
Description

The IRF430, IRF431, IRF432, and IRF433 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF430R, IRF431R, IRF432R and IRF433R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

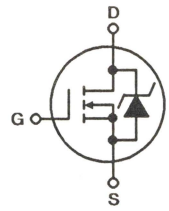
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF430 IRF430R	IRF431 IRF431R	IRF432 IRF432R	IRF433 IRF433R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	4.5	4.5	4.0	4.0	A
T_C = +100°C ..... I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3) ..... I_{DM}	18	18	16	16	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	18	18	16	16	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	300	300	300	300	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 25mH, R_{GS} = 20Ω, I_{PEAK} = 4.5A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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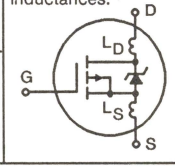
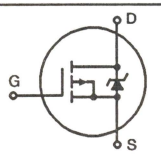
File Number **1572.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF430/432, IRF430R/432R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	-	-	V
IRF431/433, IRF431R/433R			450	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRF430/431, IRF430R/431R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	4.5	-	-	A
IRF432/433, IRF432R/433R			4.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF430/431, IRF430R/431R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	-	1.3	1.5	Ω
IRF432/433, IRF432R/433R			-	1.5	2.0	Ω
Forward Transconductance (Note 2)	g_{ts}	$V_{DS} \geq$ 50V, I_D = 2.5A	2.7	3.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 4.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	11	17	ns
Rise Time	t_r		-	15	23	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	35	53	ns
Fall Time	t_f		-	15	23	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	22	32	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	11	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	4.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	18	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 4.5A, V_{GS} = 0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/µs	180	370	760	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/µs	0.96	2	4.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 25mH, R_{GS} = 25Ω, I_{PEAK} = 4.5A (See Figure 15)

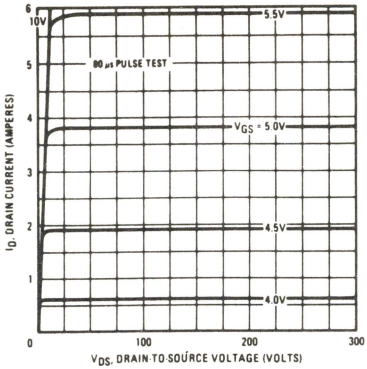


Fig. 1 — Typical Output Characteristics

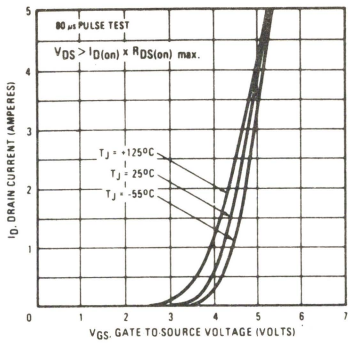


Fig. 2 — Typical Transfer Characteristics

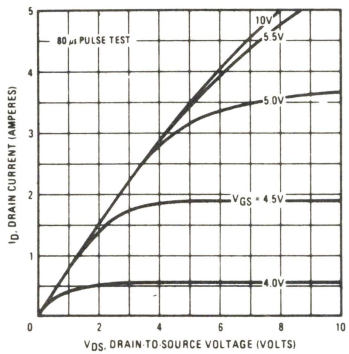


Fig. 3 — Typical Saturation Characteristics

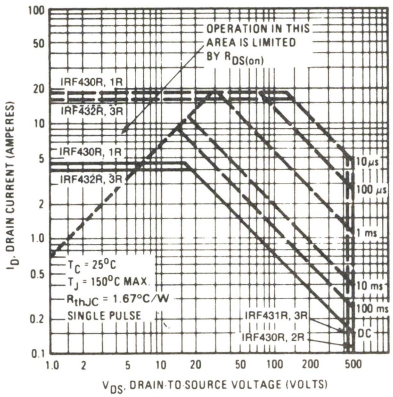


Fig. 4 — Maximum Safe Operating Area

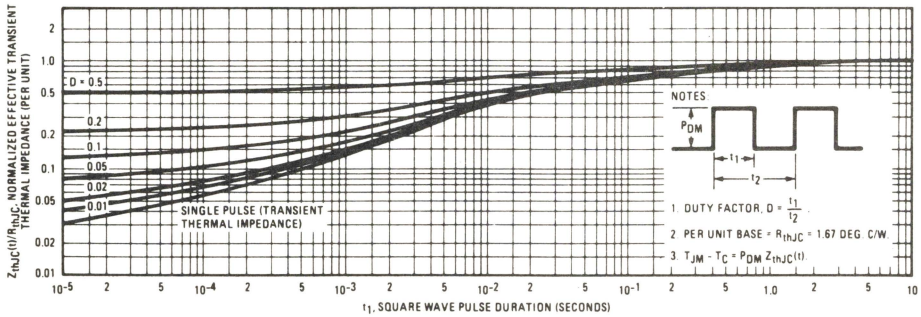


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

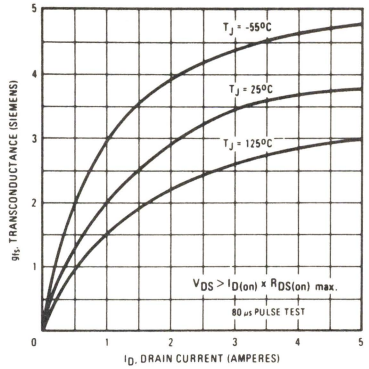


Fig. 6 – Typical Transconductance Vs. Drain Current

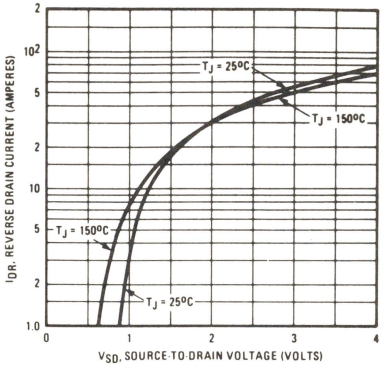


Fig. 7 – Typical Source-Drain Diode Forward Voltage

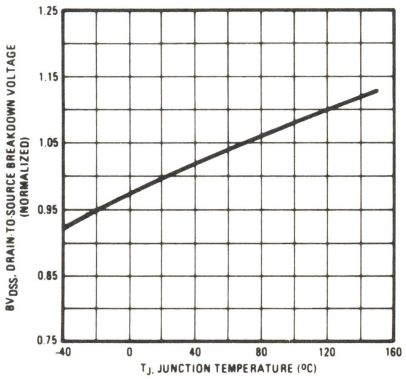


Fig. 8 – Breakdown Voltage Vs. Temperature

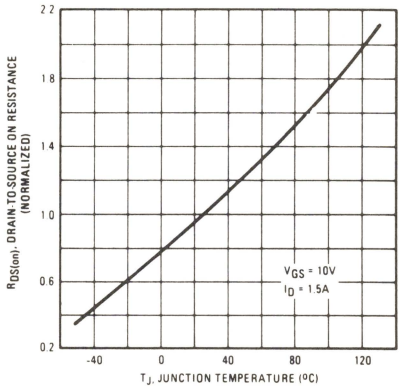


Fig. 9 – Normalized On-Resistance Vs. Temperature

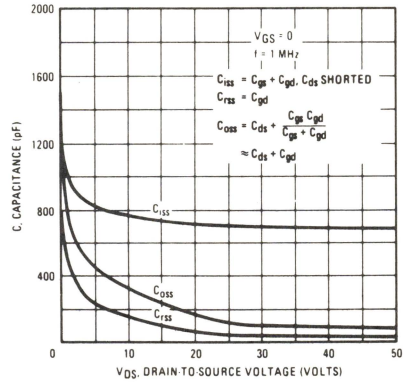


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

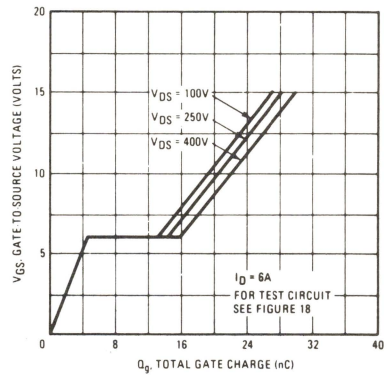


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

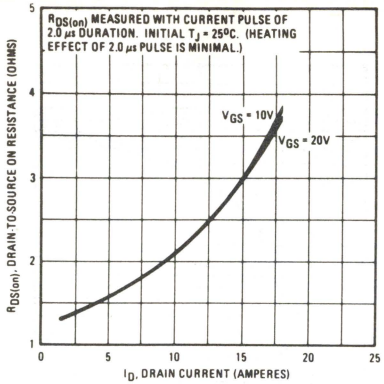


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

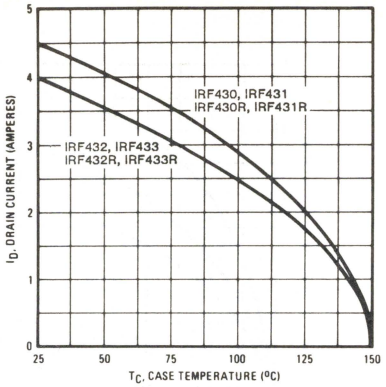


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

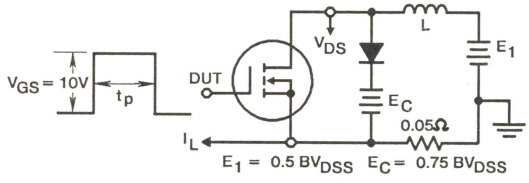


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

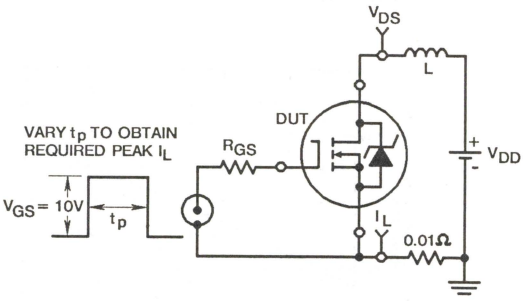


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

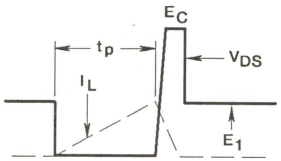


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

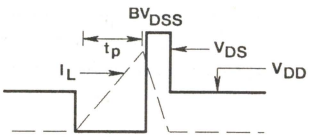


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

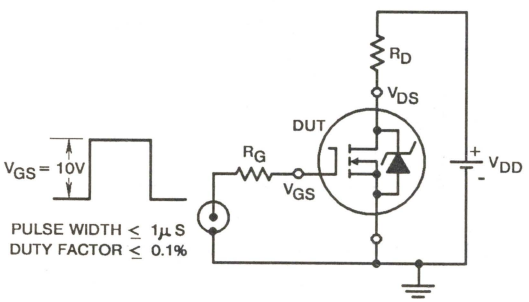


FIGURE 16. SWITCHING TIME TEST CIRCUIT

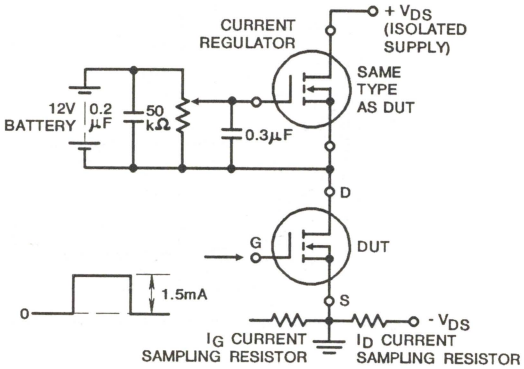


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF440/441/442/443
IRF440R/441R/442R/443R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 7A and 8A, 450V - 500V
- $r_{DS}(on)$ = 0.85Ω and 1.1Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

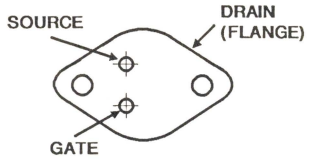
Description

The IRF440, IRF441, IRF442, and IRF443 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF440R, IRF441R, IRF442R and IRF443R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

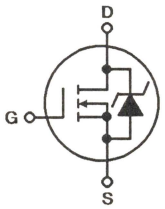
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF440 IRF440R	IRF441 IRF441R	IRF442 IRF442R	IRF443 IRF443R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.0	8.0	7.0	7.0	A
T_C = +100°C ..... I_D	5.0	5.0	4.4	4.4	A
Pulsed Drain Current (3) ..... I_{DM}	32	32	28	28	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	32	32	28	28	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	510	510	510	510	mj
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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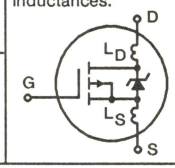
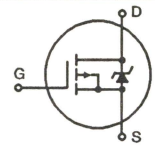
File Number **2308.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF440/442, IRF440R/442R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	-	-	V
IRF441/443, IRF441R/443R			450	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF440/441, IRF440R/441R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	8.0	-	-	A
IRF442/443, IRF442R/443R			7.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF440/441, IRF440R/441R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.4A	-	0.70	0.85	Ω
IRF442/443, IRF442R/443R			-	0.85	1.1	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 4.4A	4.9	7.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1225	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	85	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, $I_D \simeq$ 8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	21	ns
Rise Time	t_r		-	22	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	49	74	ns
Fall Time	t_f		-	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	42	63	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	22	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.0A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/μs	210	460	970	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/μs	2	4	8.9	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A (See Figure 15)

Performance Curves

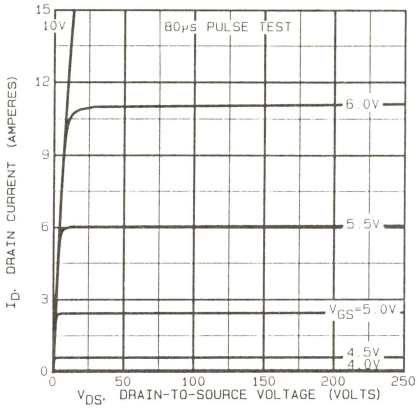


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

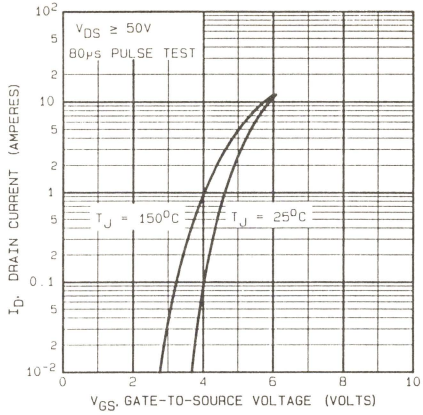


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

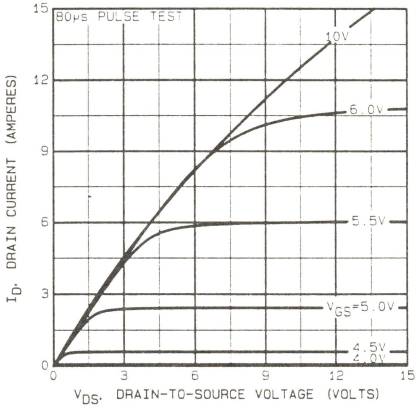


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

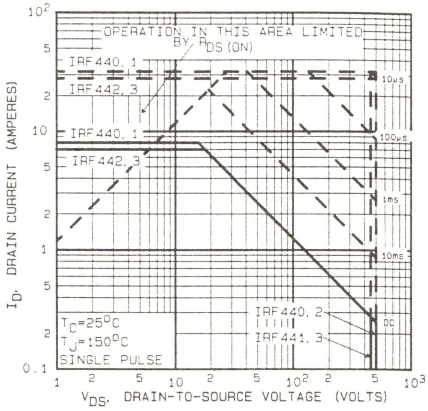


FIGURE 4. MAXIMUM SAFE OPERATING AREA

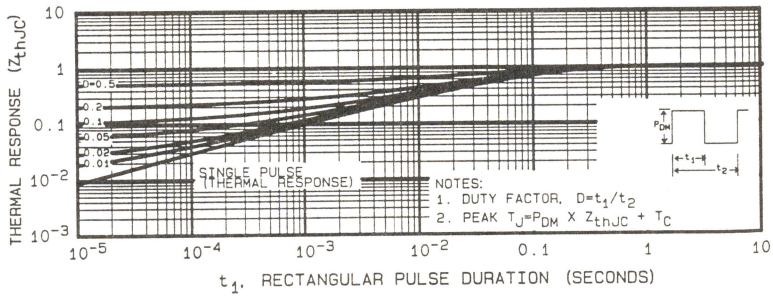


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

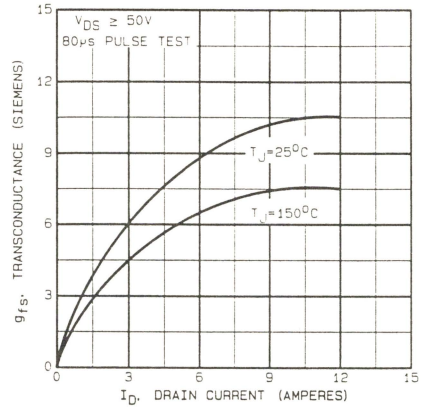


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

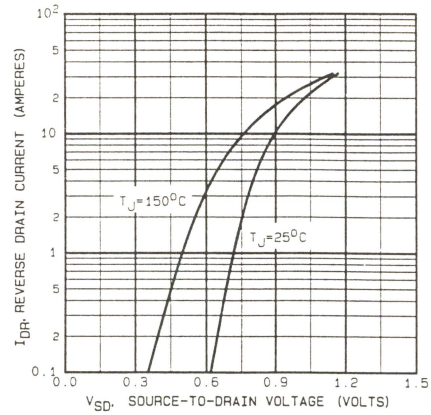


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

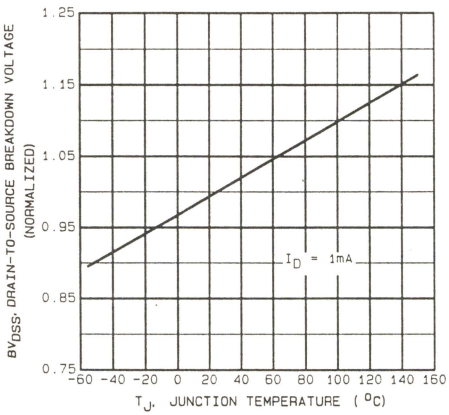


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

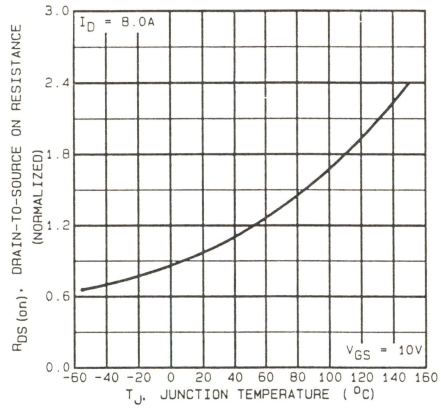


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

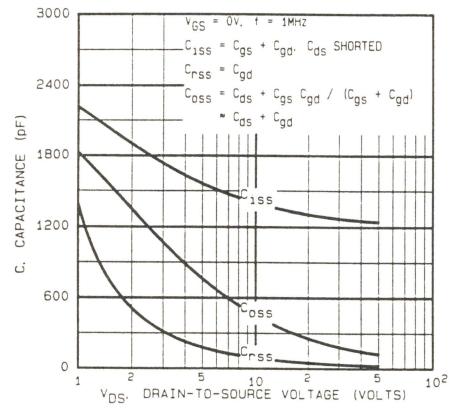


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

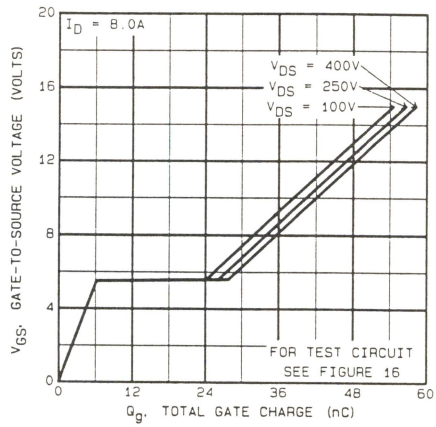


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

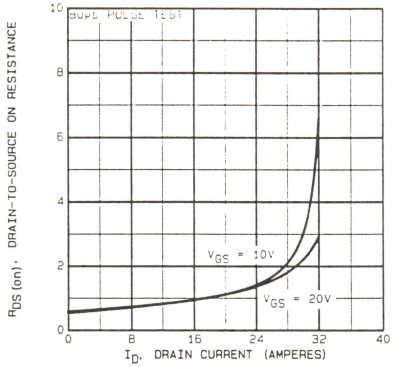


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

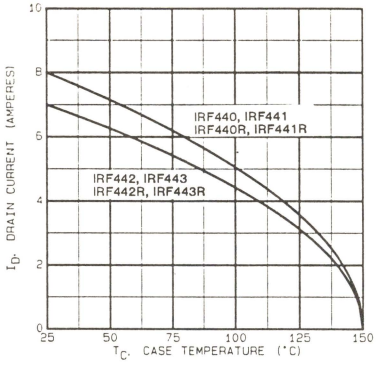


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

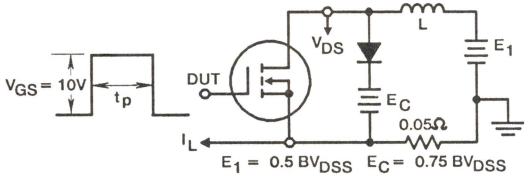


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

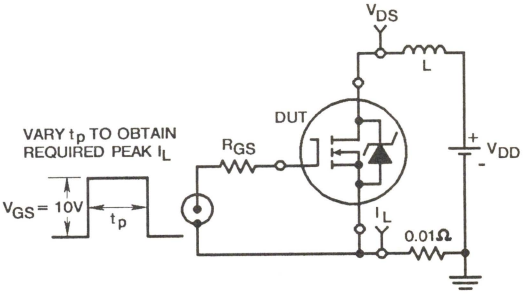


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

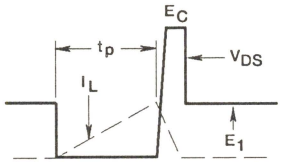


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

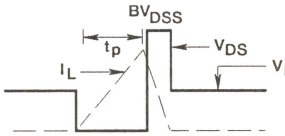


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

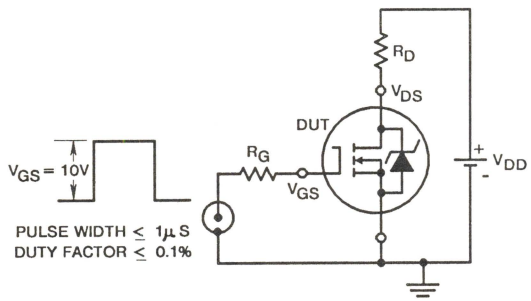


FIGURE 16. SWITCHING TIME TEST CIRCUIT

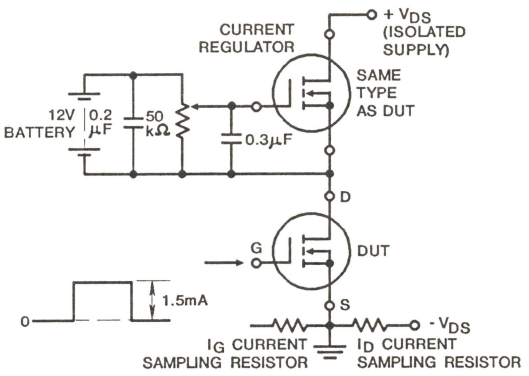


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF450/451/452/453
IRF450R/451R/452R/453R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 11A and 13A, 450V - 500V
- $r_{DS}(on)$ = 0.4Ω and 0.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

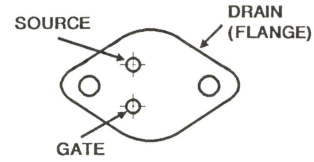
Description

The IRF450, IRF451, IRF452, and IRF453 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF450R, IRF451R, IRF452R and IRF453R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

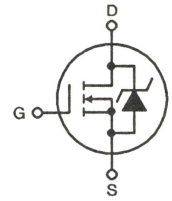
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF450 IRF450R	IRF451 IRF451R	IRF452 IRF452R	IRF453 IRF453R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	13	13	11	11	A
T_C = +100°C ..... I_D	8.1	8.1	7.2	7.2	A
Pulsed Drain Current (3) ..... I_{DM}	52	52	44	44	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	52	52	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	860	860	860	860	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 13A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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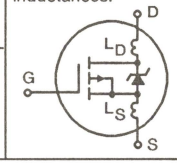
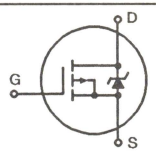
File Number **1827.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF450/452, IRF450R/452R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRF451/453, IRF451R/453R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF450/451, IRF450R/451R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	13	–	–	A
IRF452/453, IRF452R/453R			11	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF450/451, IRF450R/451R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 7.2A	–	0.3	0.4	Ω
IRF452/453, IRF452R/453R			–	0.4	0.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 7.2A	6.0	11	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1800	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D ≃ 13A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	27	ns
Rise Time	t_r		–	40	66	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	72	100	ns
Fall Time	t_f		–	35	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 13A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	85	130	nC
Gate-Source Charge	Q_{gs}		–	12	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	13	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	52	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 13A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 13A, dI_F/dt = 100A/µs	280	600	1200	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 13A, dI_F/dt = 100A/µs	3.2	7.5	14	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 9.2mH, R_{GS} = 25Ω, I_{PEAK} = 13A (See Figure 15)

Performance Curves

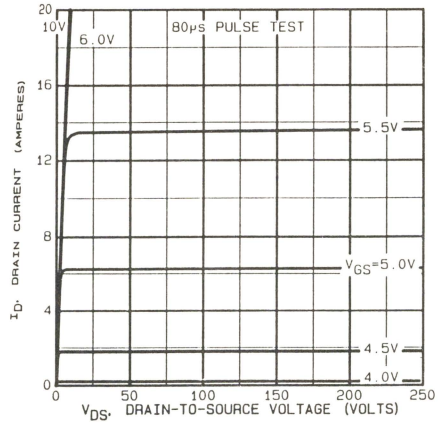


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

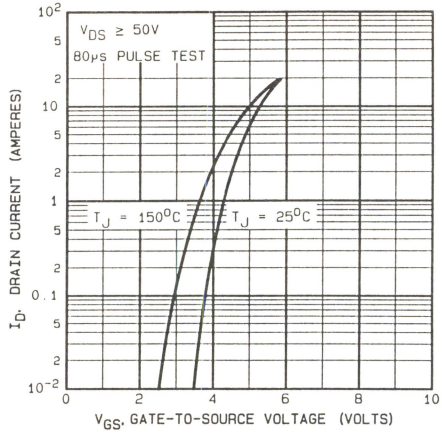


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

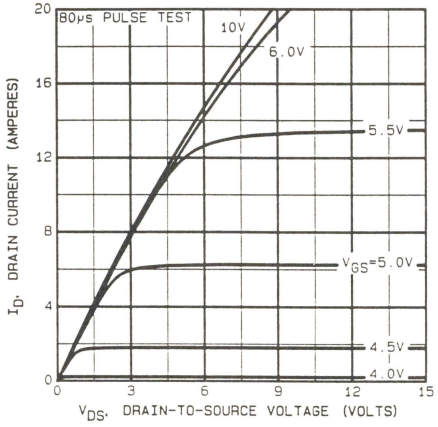


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

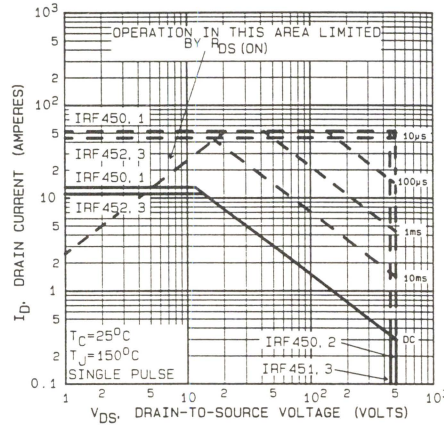


FIGURE 4. MAXIMUM SAFE OPERATING AREA

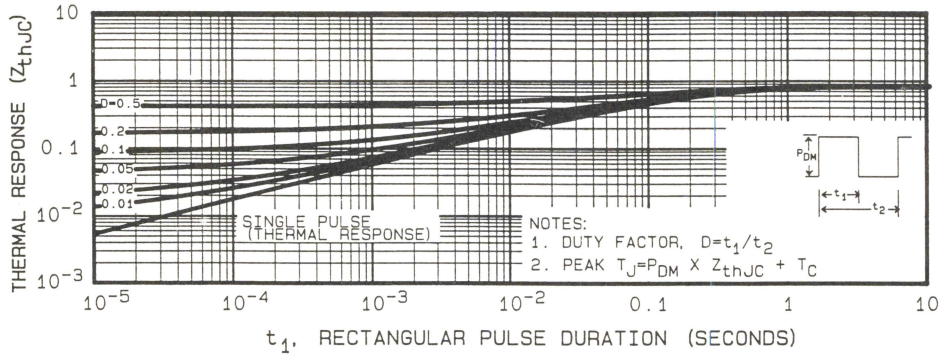


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

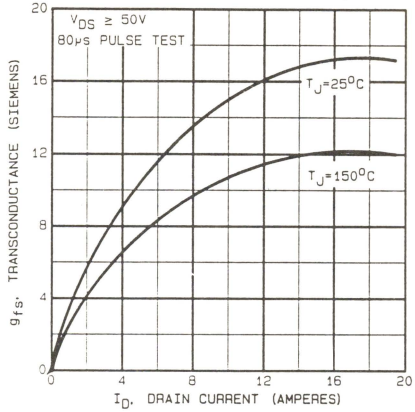


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

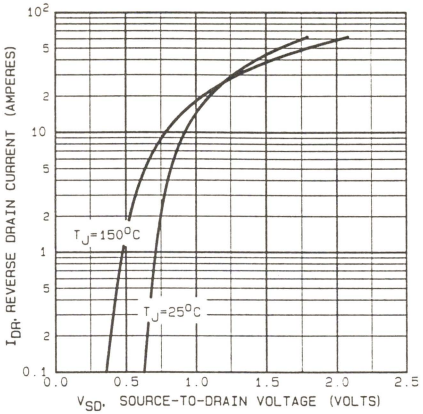


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

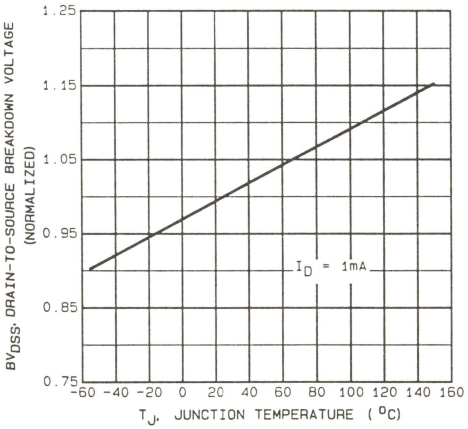


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

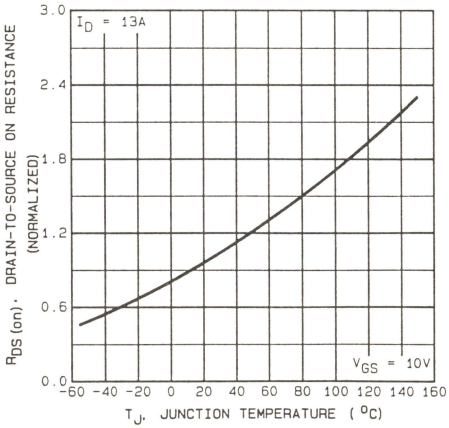


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

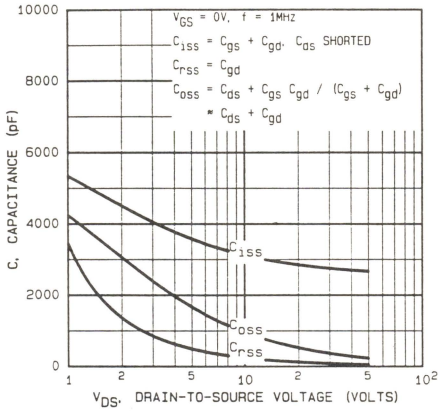


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

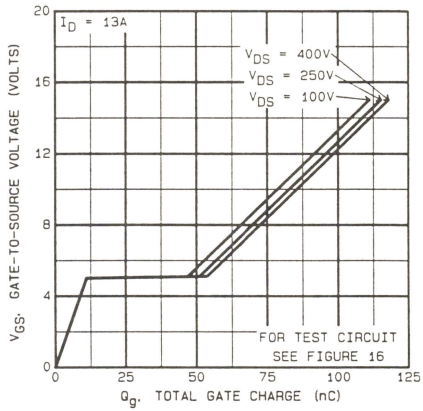


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

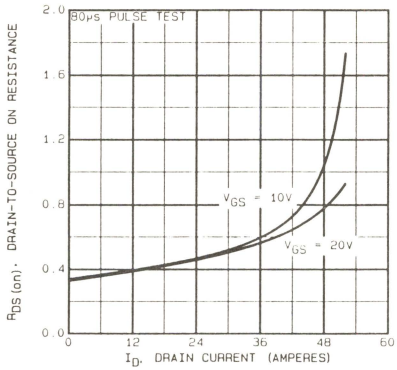


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

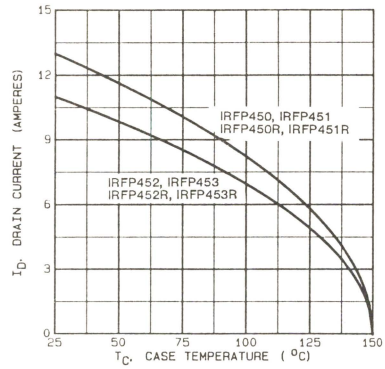


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

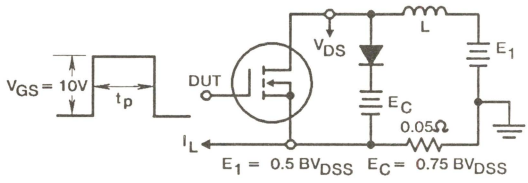


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

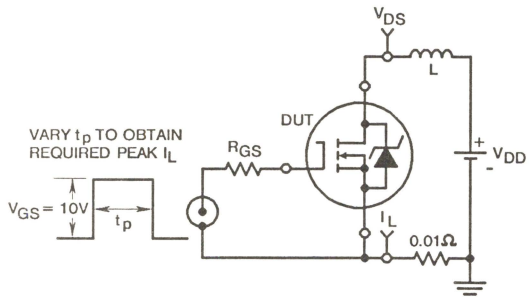


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

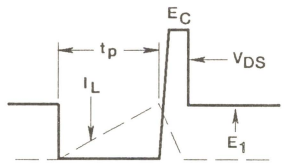


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

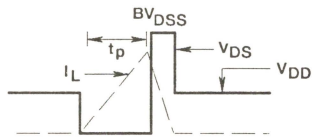


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

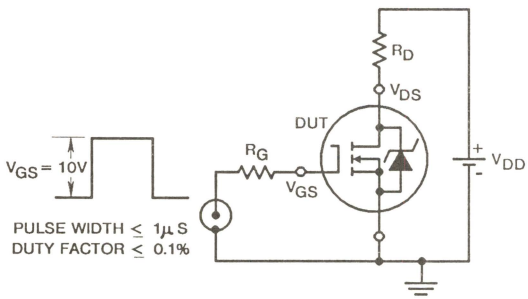


FIGURE 16. SWITCHING TIME TEST CIRCUIT

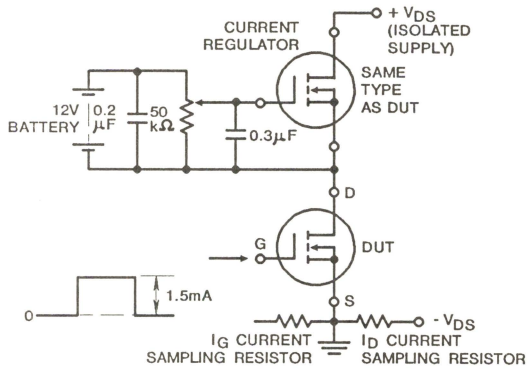


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF460
IRF462

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 21A and 19A, 500V
- $r_{DS}(on)$ = 0.27Ω and 0.35Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

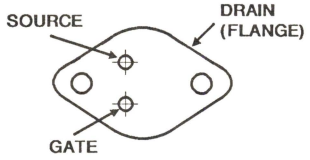
Description

The IRF460 and IRF462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

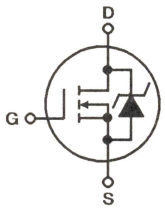
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF460	IRF462	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	21	19	A
T_C = +100°C ..... I_D	14	12	A
Pulsed Drain Current (1) ..... I_{DM}	84	76	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	300	300	W
Linear Derating Factor	2.4	2.4	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS}*	1200	1200	mj
See Figure 14			
Avalanche Current, Repetitive or Non-repetitive (1) ..... I_{AR}	21	21	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.9mH, R_{GS} = 25Ω, Peak I_L = 21A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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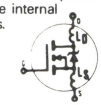
File Number **2277.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25° C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRF460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 12A
		IRF462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRF460	21	–	–	A	V_{DS} > $I_{D(on)}$ X $R_{DS(on)}$ Max.
		IRF462	19	–	–		V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	13	20	–	S (℧)	V_{DS} ≥ 50V, I_{DS} = 12A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	–100	nA	V_{GS} = –20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A
Q_{gs}	Gate-to-Source Charge	ALL	–	18	—	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	—	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D ≈ 21A, R_G = 4.3Ω
t_r	Rise Time	ALL	–	81	120	ns	R_D = 12Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	See Fig. 15
t_f	Fall Time	ALL	–	65	98	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	480	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.42	°C/W	
R_{thJS}	Case-to-Sink	ALL	–	0.10	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Typical socket mount

Modified MOSFET symbol showing the internal inductances.



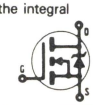
① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.9 μH, R_G = 25Ω, Peak I_L = 21A.

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	21	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	84	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



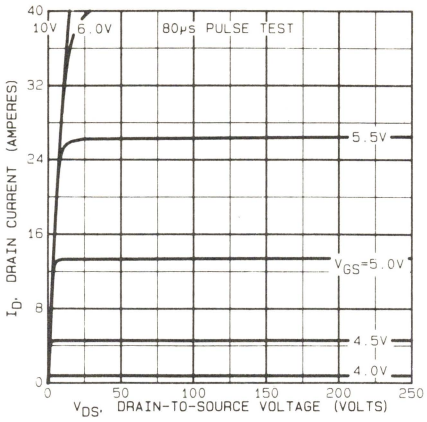


Fig. 1 - Typical output characteristics.

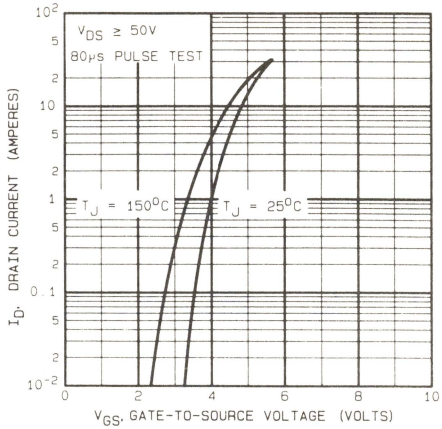


Fig. 2 - Typical transfer characteristics.

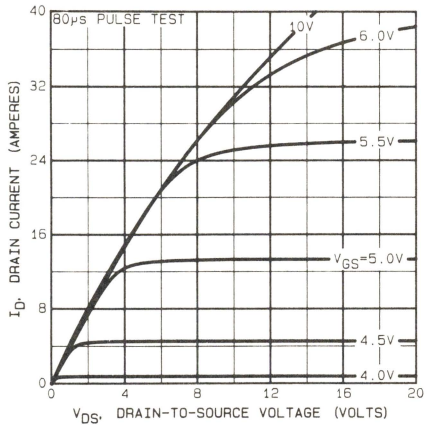


Fig. 3 - Typical saturation characteristics.

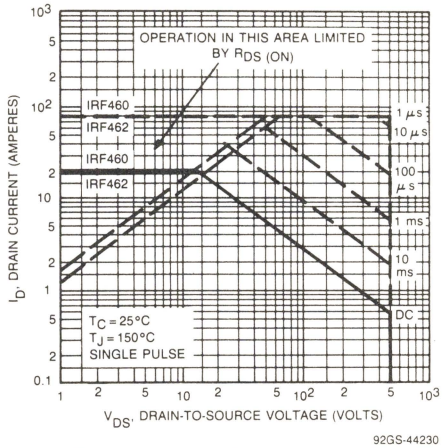


Fig. 4 - Maximum safe operating area.

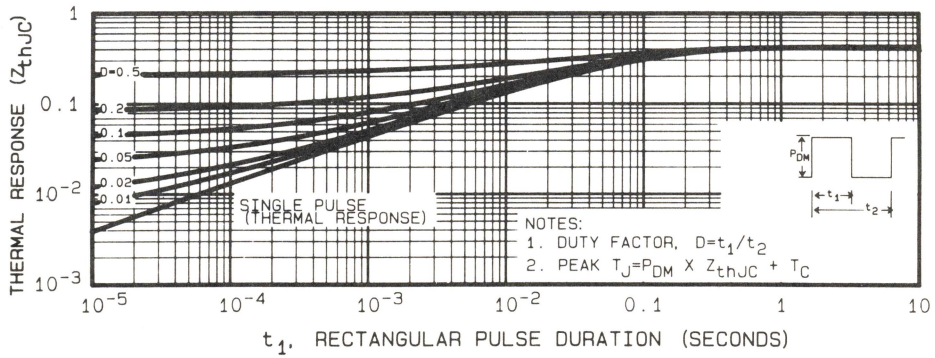


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

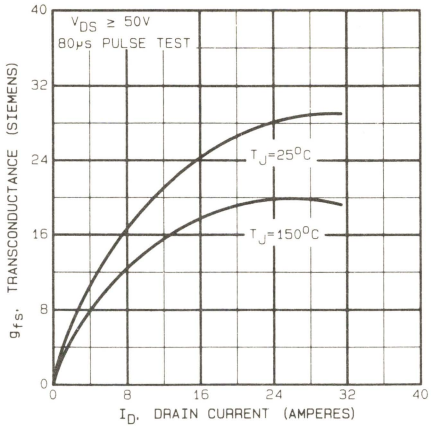


Fig. 6 - Typical transconductance vs. drain current.

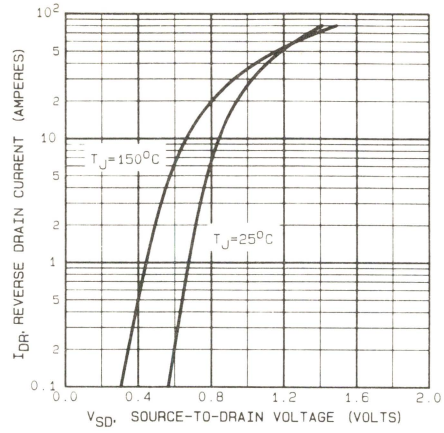


Fig. 7 - Typical source-drain diode forward voltage.

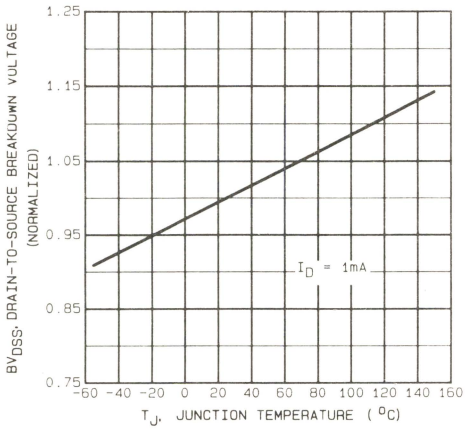


Fig. 8 - Breakdown voltage vs. temperature.

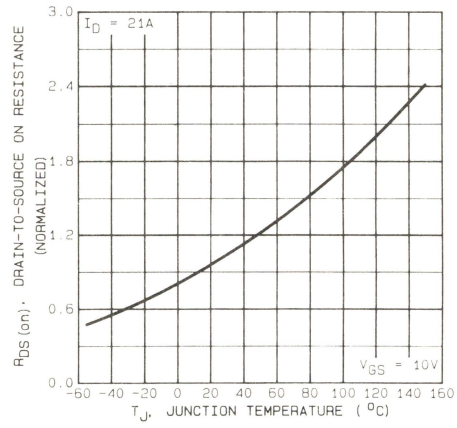


Fig. 9 - Normalized on-resistance vs. temperature.

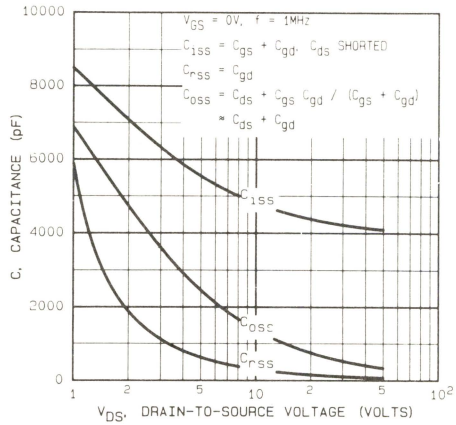


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

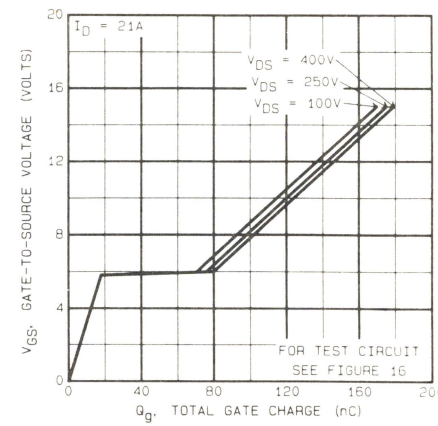


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

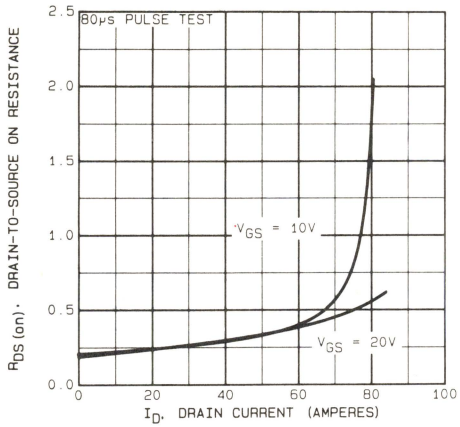


Fig. 12 - Typical on-resistance vs. drain current.

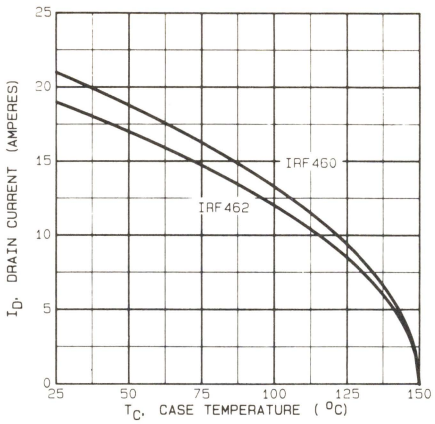


Fig. 13 - Maximum drain current vs. case temperature.

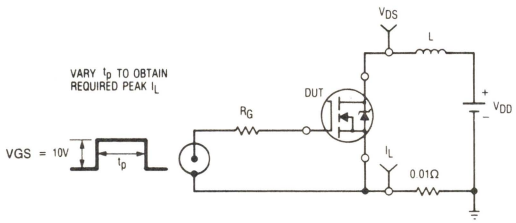


Fig. 14a - Unclamped inductive test circuit.

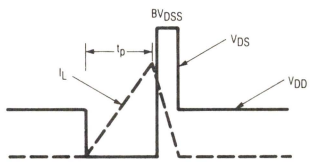


Fig. 14b - Unclamped inductive waveforms.

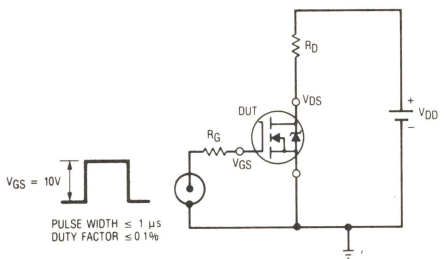


Fig. 15a - Switching time test circuit.

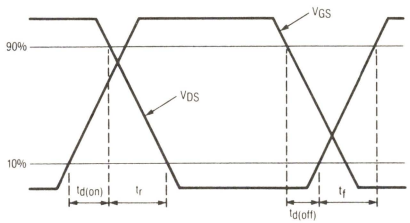


Fig. 15b - Switching time waveforms.

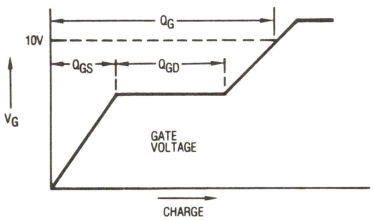


Fig. 16a - Basic gate charge waveform.

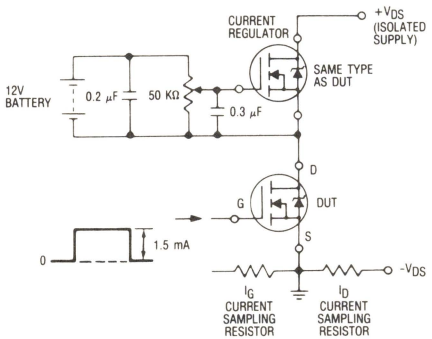


Fig. 16b - Gate charge test circuit.

HARRIS

IRF510/511/512/513
IRF510R/511R/512R/513R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.9A and 5.6A, 80V - 100V
- $r_{DS}(on)$ = 0.54Ω and 0.74Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

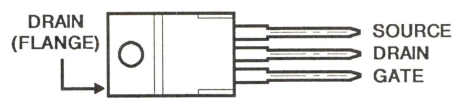
Description

The IRF510, IRF511, IRF512, and IRF513 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF510R, IRF511R, IRF512R and IRF513R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

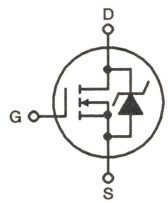
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF510 IRF510R	IRF511 IRF511R	IRF512 IRF512R	IRF513 IRF513R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	5.6	5.6	4.9	4.9	A
T_C = +100°C ..... I_D	4	4	3.4	3.4	A
Pulsed Drain Current (3) ..... I_{DM}	20	20	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	43	43	43	43	W
Linear Derating Factor	0.29	0.29	0.29	0.29	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	16	16	14	14	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	19	19	19	19	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 910μH, R_{GS} = 25Ω, I_{PEAK} = 5.6A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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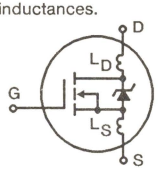
File Number **1573.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

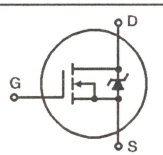
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF510/512, IRF510R/512R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF511/513, IRF511R/513R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +150°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF510/511, IRF510R/511R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\,Max}$, V_{GS} = 10V	5.6	–	–	A
IRF512/513, IRF512R/513R			4.9	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF510/511, IRF510R/511R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.4A	–	0.4	0.54	Ω
IRF512/513, IRF512R/513R			–	0.5	0.74	Ω
Forward Transconductance (Note 2)	g_{ts}	$V_{DS} \geq$ 50V, I_D = 3.4A	1.3	2.0	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	80	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \simeq$ 5.6A, R_G = 24Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8	11	ns
Rise Time	t_r		–	25	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	15	21	ns
Fall Time	t_f		–	12	21	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.0	7.7	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	3.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	5.6	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	20	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.6A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 5.6A, dI_F/dt = 100A/µs	4.6	96	200	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.6A, dI_F/dt = 100A/µs	0.17	0.4	0.83	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 910µH, R_{GS} = 25Ω, I_{PEAK} = 5.6A (See Figure 15)

Performance Curves

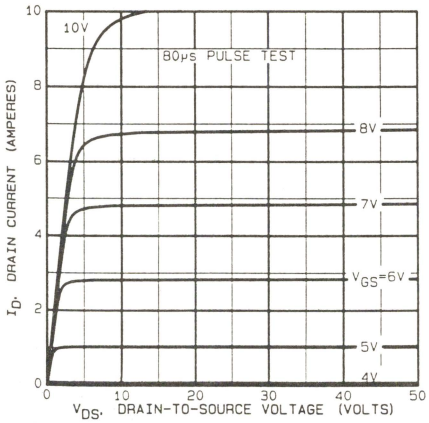


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

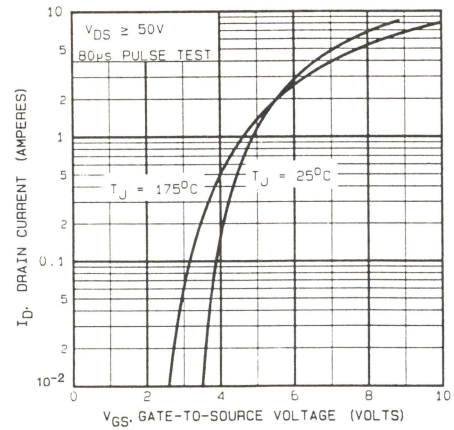


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

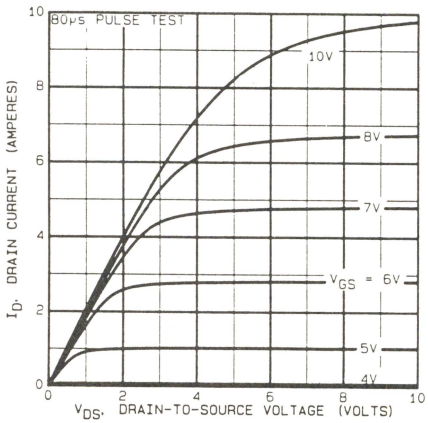


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

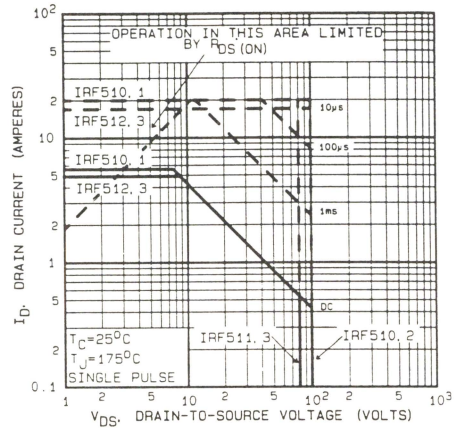


FIGURE 4. MAXIMUM SAFE OPERATING AREA

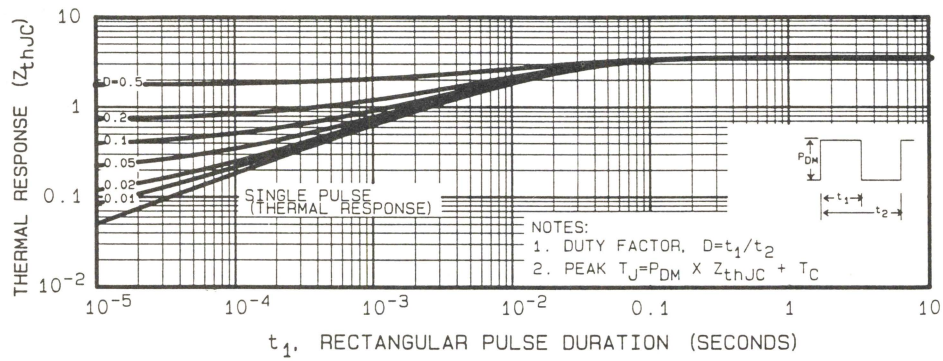


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

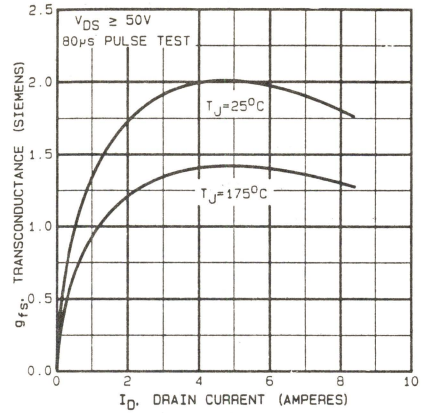


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

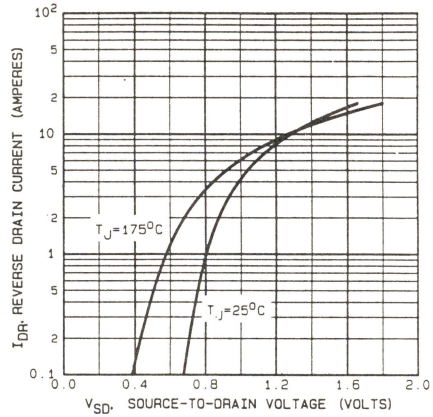


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

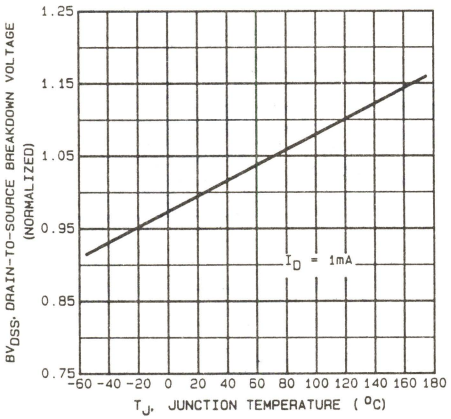


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

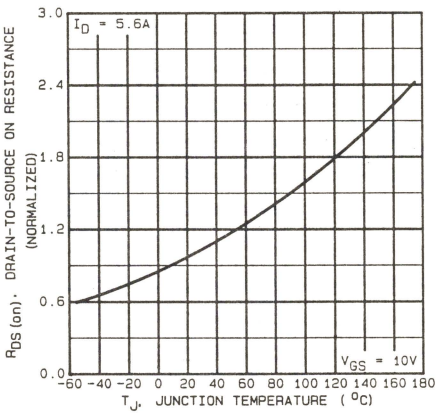


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

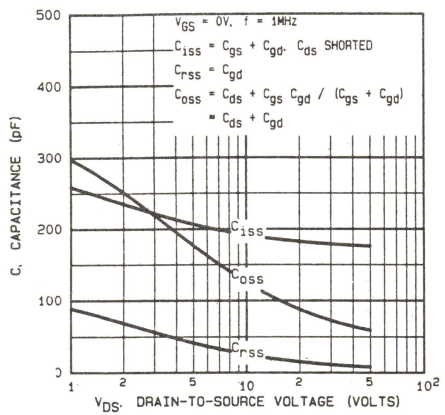


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

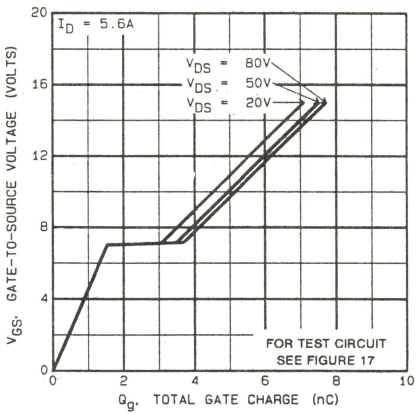


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

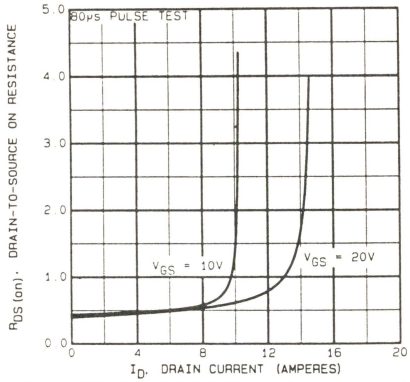


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

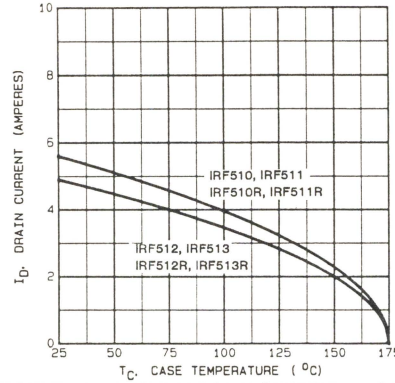


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

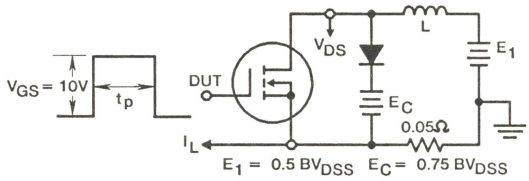


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

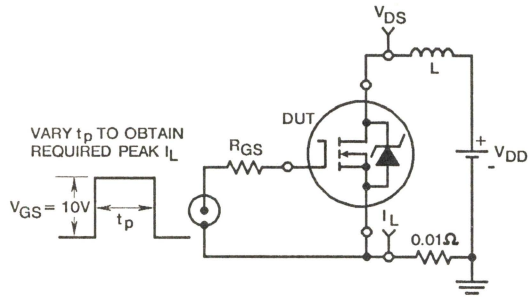


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

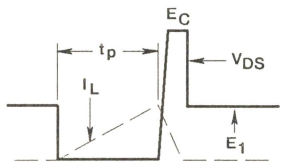


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

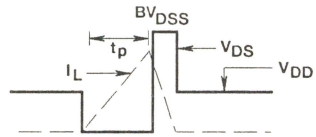


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

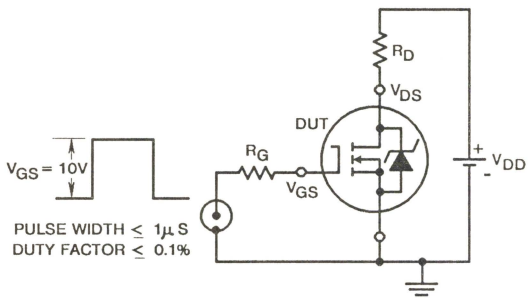


FIGURE 16. SWITCHING TIME TEST CIRCUIT

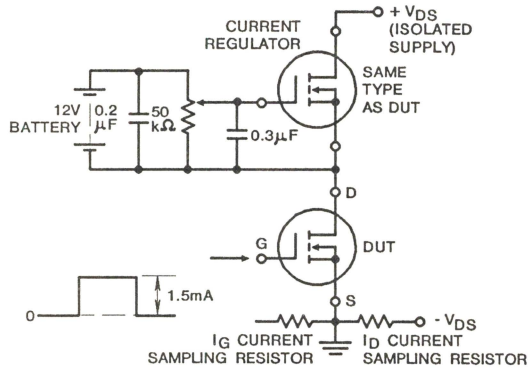


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF520/521/522/523
IRF520R/521R/522R/523R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 8A and 9.2A, 80V - 100V
- $r_{DS}(on)$ = 0.27Ω and 0.36Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

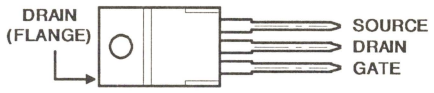
Description

The IRF520, IRF521, IRF522, and IRF523 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF520R, IRF521R, IRF522R and IRF523R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

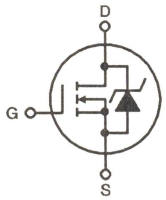
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF520 IRF520R	IRF521 IRF521R	IRF522 IRF522R	IRF523 IRF523R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	9.2	9.2	8	8	A
T_C = +100°C ..... I_D	6.5	6.5	5.6	5.6	A
Pulsed Drain Current (3) ..... I_{DM}	37	37	32	32	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	60	60	60	60	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	32	32	28	28	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	36	36	36	36	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 640μH, R_{GS} = 25Ω, I_{PEAK} = 9.2A. See Figures 15 & 16.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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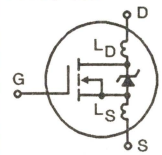
File Number **1574.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

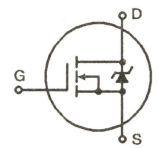
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF520/522, IRF520R/522R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRF521/523, IRF521R/523R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +150°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF520/521, IRF520R/521R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	9.2	–	–	A
IRF522/523, IRF522R/523R			8.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF520/521, IRF520R/521R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.6A	–	0.25	0.27	Ω
IRF522/523, IRF522R/523R			–	0.27	0.36	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 5.6A	2.7	4.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	350	–	pF
Output Capacitance	C_{OSS}		–	130	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	25	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≃ 9.2A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	9	13	ns
Rise Time	t_r		–	30	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	18	29	ns
Fall Time	t_f		–	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 9.2A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	10	15	nC
Gate-Source Charge	Q_{gs}		–	2.5	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	2.5	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	9.2	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	37	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 9.2A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	5.5	100	240	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 9.2A, dI_F/dt = 100A/μs	0.25	0.5	1.1	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 640μH, R_{GS} = 25Ω, I_{PEAK} = 9.2A (See Figures 15 & 16)

Performance Curves

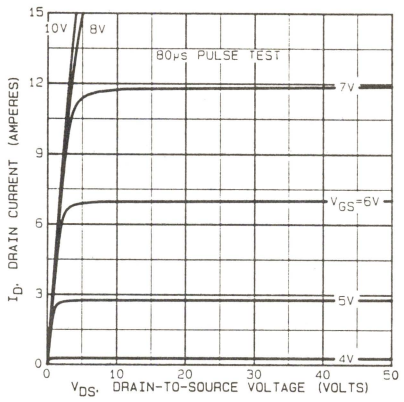


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

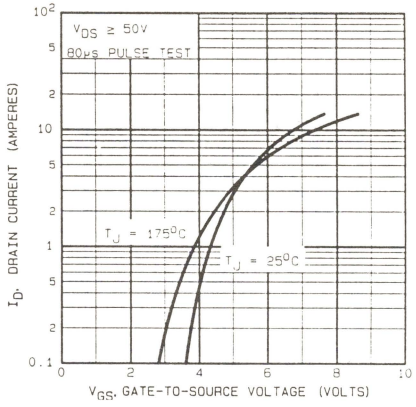


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

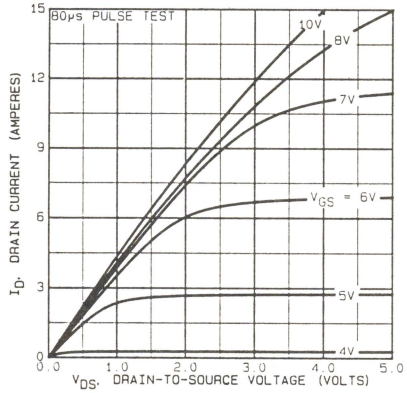


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

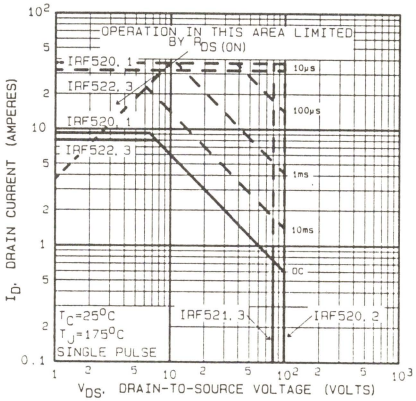


FIGURE 4. MAXIMUM SAFE OPERATING AREA

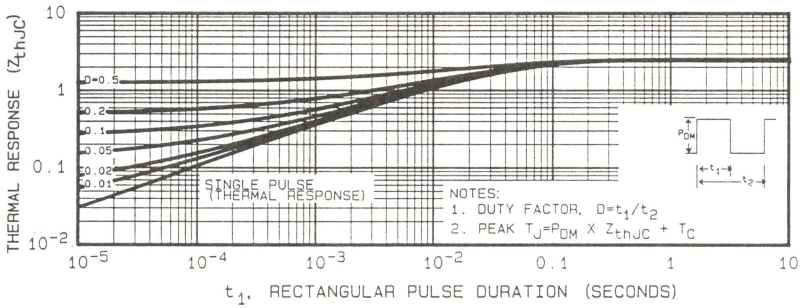


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

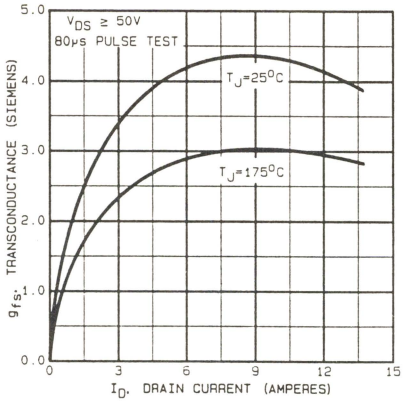


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

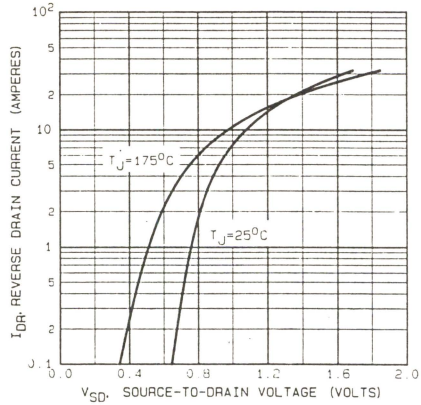


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

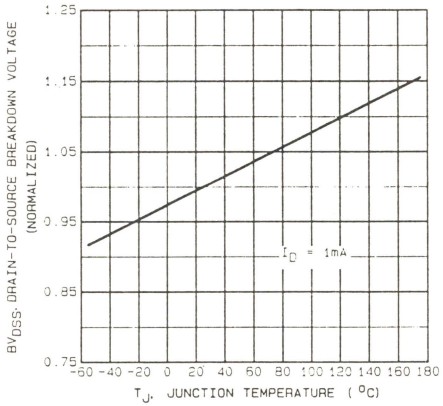


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

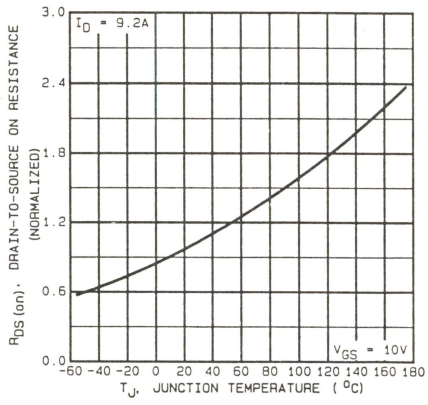


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

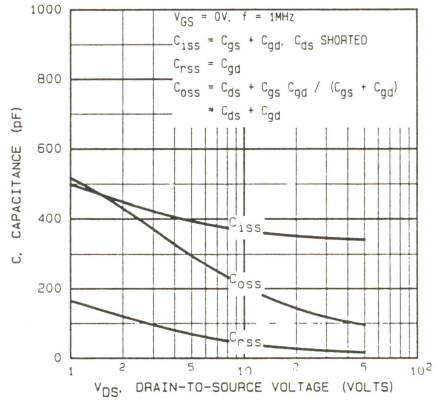


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

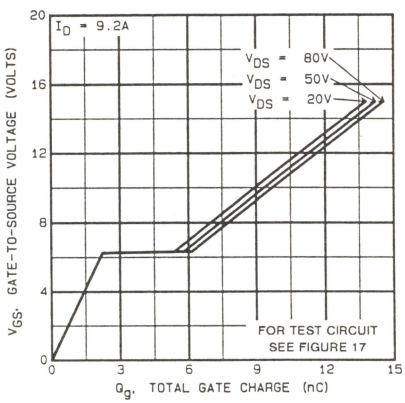


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

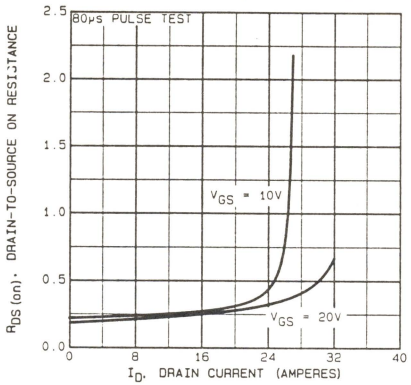


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

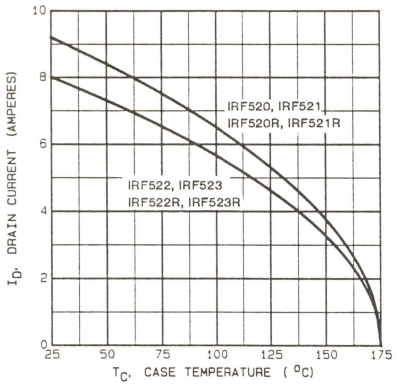


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

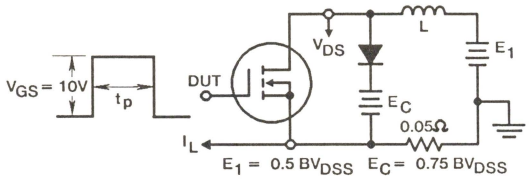


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

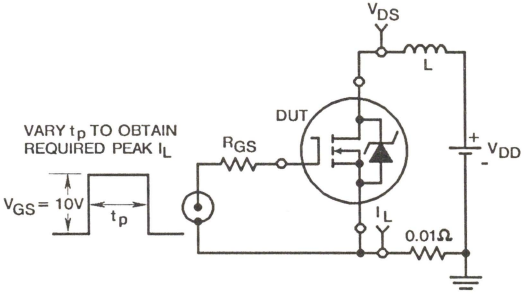


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

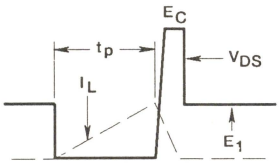


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

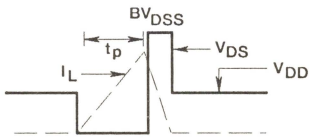


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

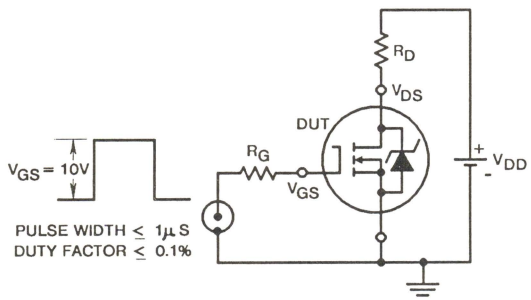


FIGURE 16. SWITCHING TIME TEST CIRCUIT

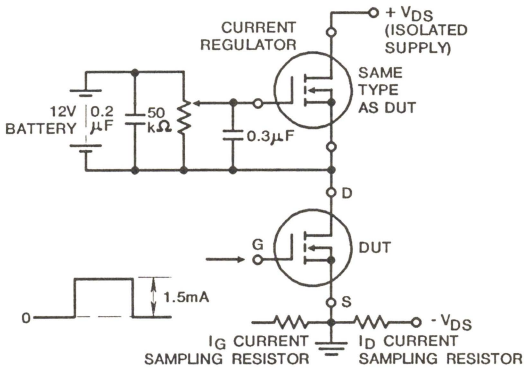


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF530/531/532/533
IRF530R/531R/532R/533R

N-Channel Power MOSFETs
Avalanche Energy Rated*

May 1992

Features

- 12A and 14A, 80V - 100V
- $r_{DS}(on)$ = 0.16Ω and 0.23Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

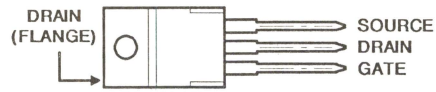
Description

The IRF530, IRF531, IRF532, and IRF533 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF530R, IRF531R, IRF532R and IRF533R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

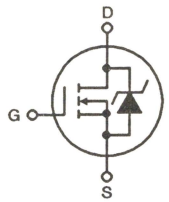
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF530 IRF530R	IRF531 IRF531R	IRF532 IRF532R	IRF533 IRF533R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	14	12	12	A
T_C = +100°C ..... I_D	10	10	8.3	8.3	A
Pulsed Drain Current (3) ..... I_{DM}	56	56	48	48	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	79	79	79	79	W
Linear Derating Factor	0.53	0.53	0.53	0.53	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	56	56	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	69	69	69	69	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 530μH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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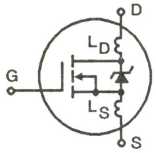
File Number **1575.2**

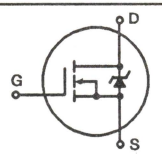
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF530/532, IRF530R/532R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRF531/533, IRF531R/533R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF530/531, IRF530R/531R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	14	–	–	A
IRF532/533, IRF532R/533R			12	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF530/531, IRF530R/531R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.3A	–	0.14	0.16	Ω
IRF532/533, IRF532R/533R			–	0.20	0.23	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 8.3A	5.1	7.6	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	250	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	50	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \simeq$ 14A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	12	15	ns
Rise Time	t_r		–	35	51	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	25	35	ns
Fall Time	t_f		–	25	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	18	26	nC
Gate-Source Charge	Q_{gs}		–	4	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	7	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.9	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	5.5	120	250	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	0.26	0.6	1.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 350µH, R_{GS} = 25Ω, I_{PEAK} = 14A (See Figure 15)

Performance Curves

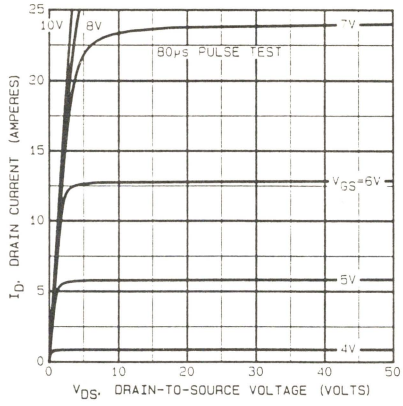


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

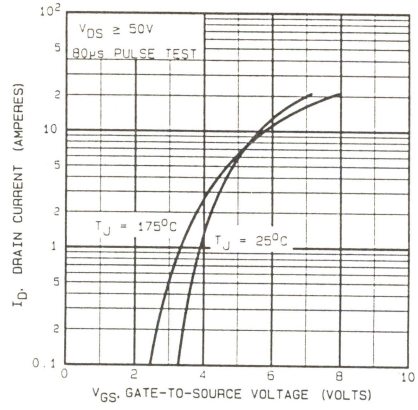


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

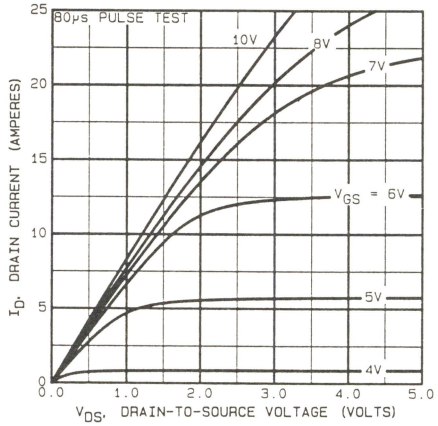


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

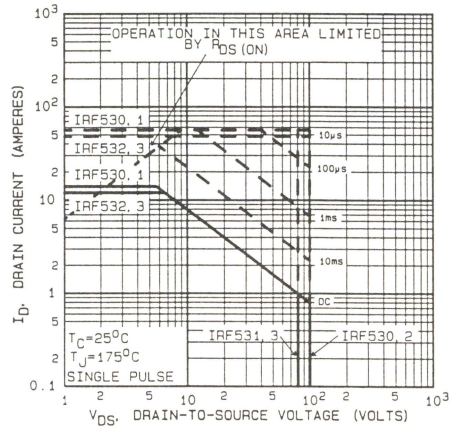


FIGURE 4. MAXIMUM SAFE OPERATING AREA

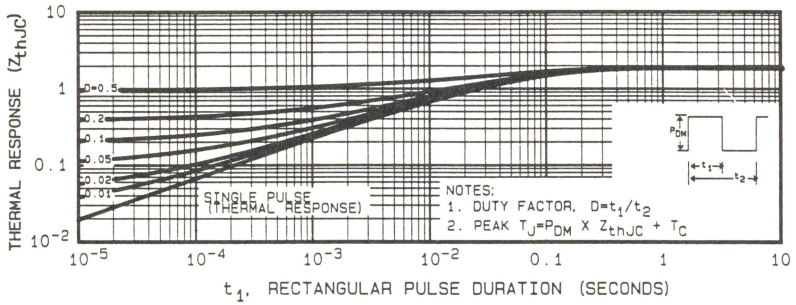


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

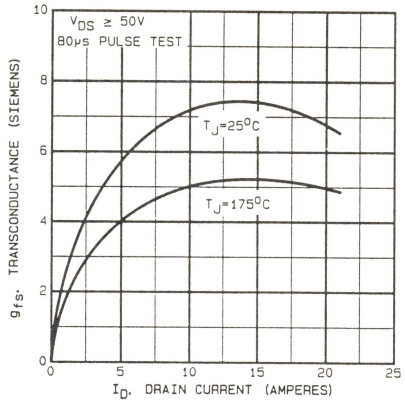


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

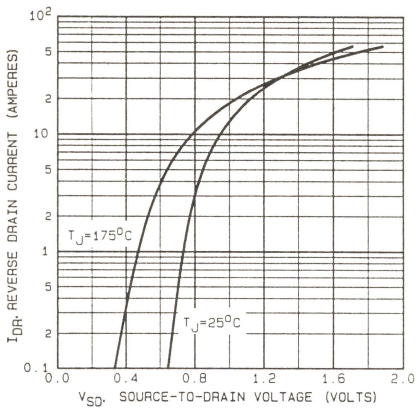


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

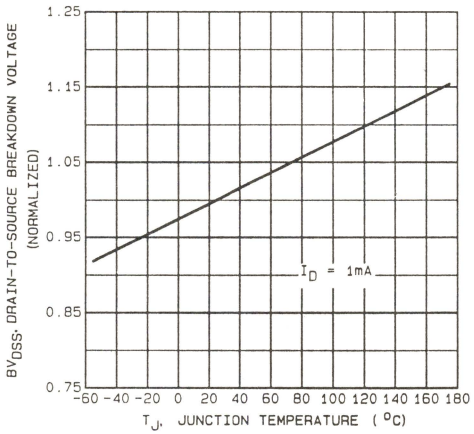


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

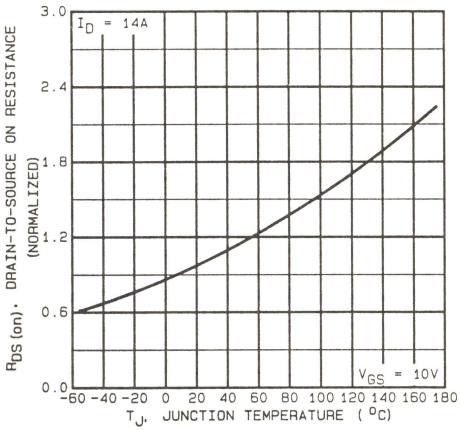


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

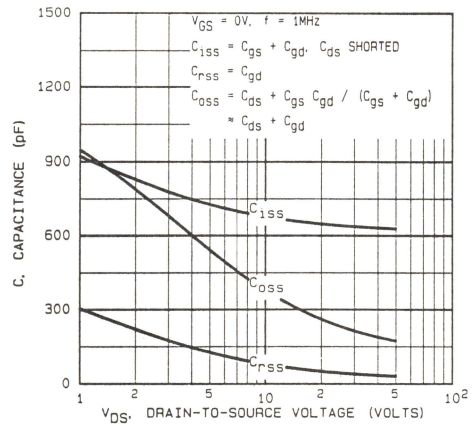


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

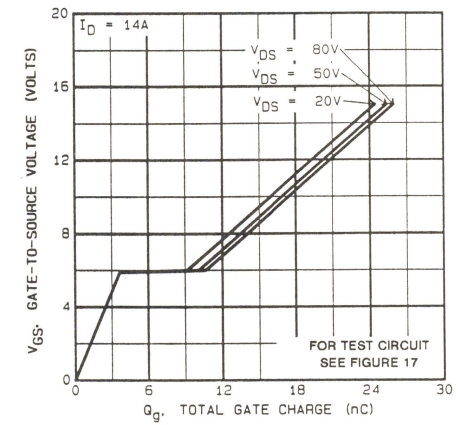


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

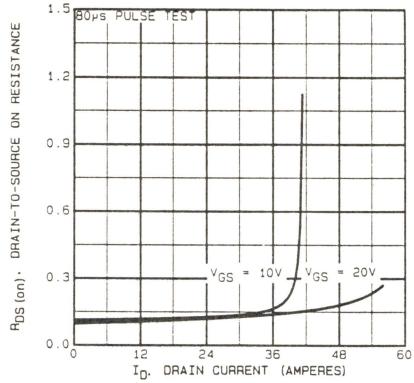


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

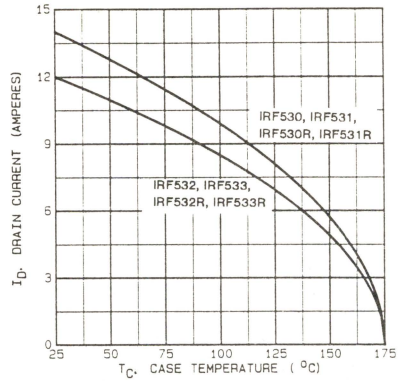


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

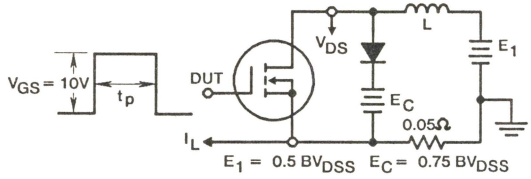


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

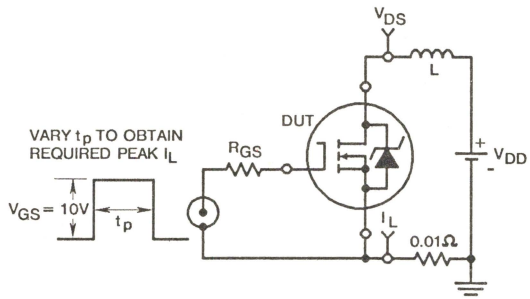


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

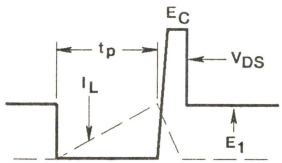


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

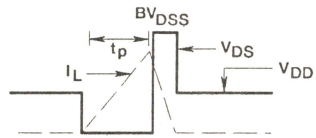


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

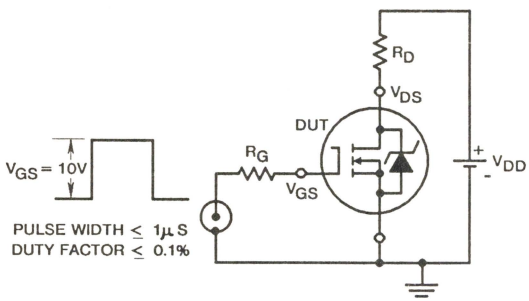


FIGURE 16. SWITCHING TIME TEST CIRCUIT

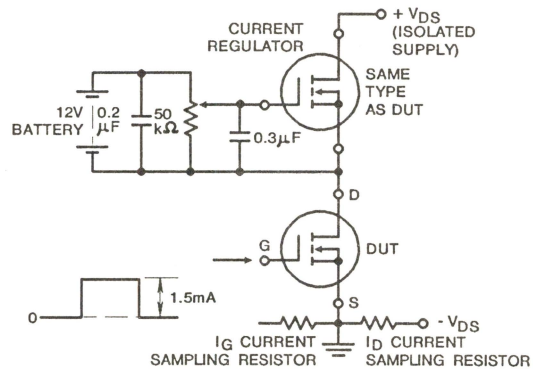


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF540/541/542/543
IRF540R/541R/542R/543R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 25A and 28A, 80V - 100V
- $r_{DS}(on)$ = 0.077Ω and 0.10Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

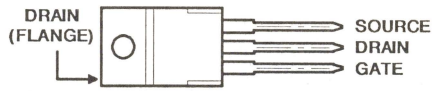
Description

The IRF540, IRF541, IRF542, and IRF543 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF540R, IRF541R, IRF542R and IRF543R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

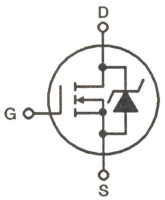
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF540 IRF540R	IRF541 IRF541R	IRF542 IRF542R	IRF543 IRF543R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	28	28	25	25	A
T_C = +100°C ..... I_D	20	20	17	17	A
Pulsed Drain Current (3) ..... I_{DM}	110	110	100	100	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	108	108	96	96	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	230	230	230	230	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 440μH, R_{GS} = 25Ω, I_{PEAK} = 28A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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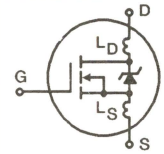
File Number **2309.1**

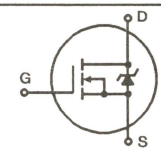
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF540/542, IRF540R/542R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRF541/543, IRF541R/543R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF540/541, IRF540R/541R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\,Max}$, V_{GS} = 10V	28	–	–	A
IRF542/543, IRF542R/543R			25	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF540/541, IRF540R/541R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 17A	–	0.06	0.077	Ω
IRF542/543, IRF542R/543R			–	0.08	0.10	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 17A	8.7	13	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1450	–	pF
Output Capacitance	C_{OSS}		–	550	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \simeq$ 28A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	15	23	ns
Rise Time	t_r		–	70	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	40	60	ns
Fall Time	t_f		–	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 28A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	38	59	nC
Gate-Source Charge	Q_{gs}		–	8	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	21	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	28	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	110	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 27A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/μs	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/μs	0.44	1.0	1.9	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 440μH, R_{GS} = 25Ω, I_{PEAK} = 28A (See Figure 15)

Performance Curves

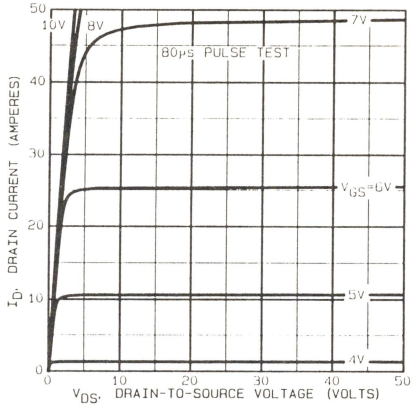


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

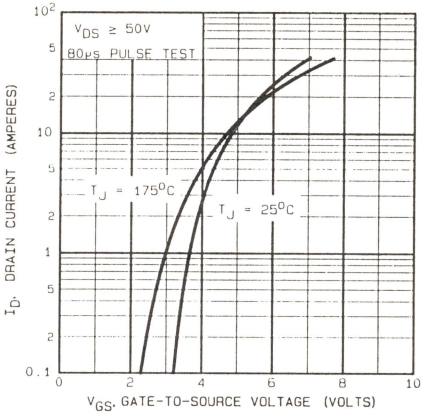


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

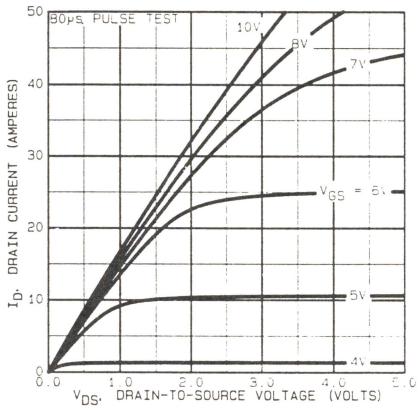


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

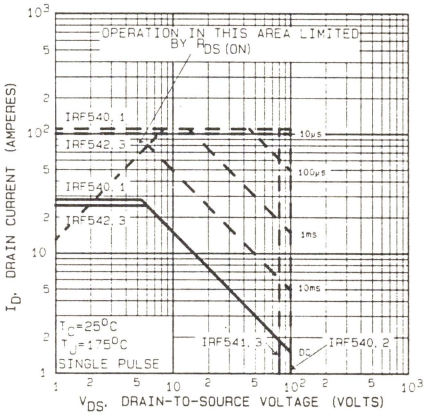


FIGURE 4. MAXIMUM SAFE OPERATING AREA

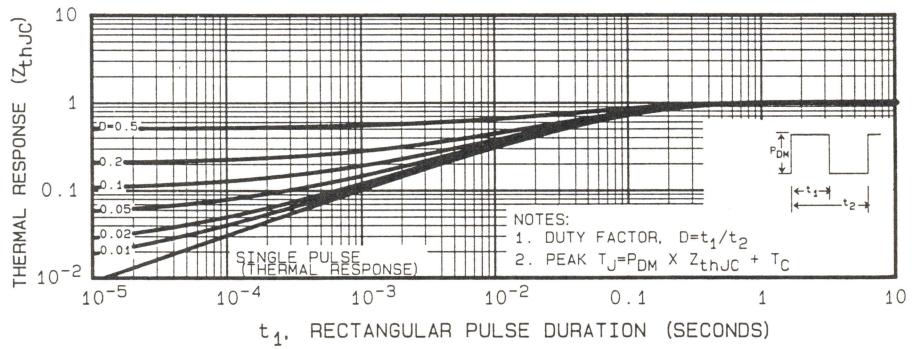


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

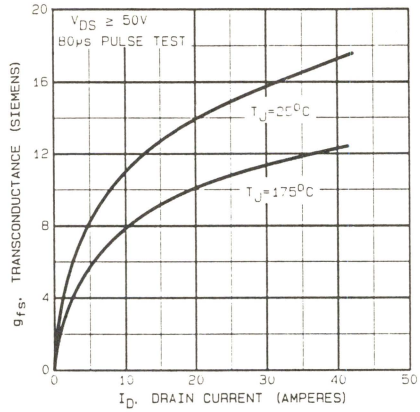


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

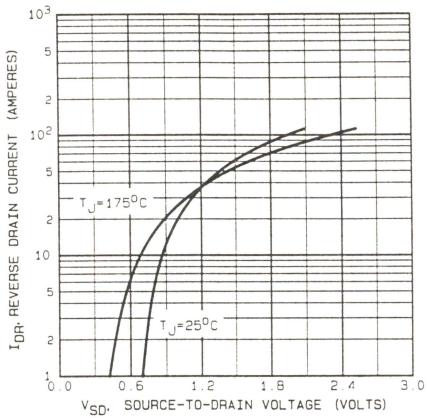


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

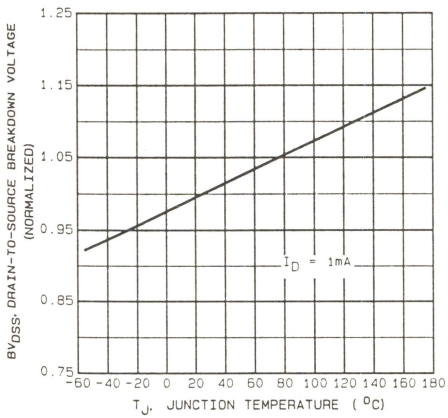


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

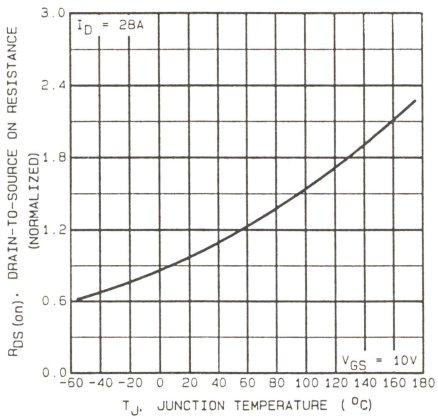


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

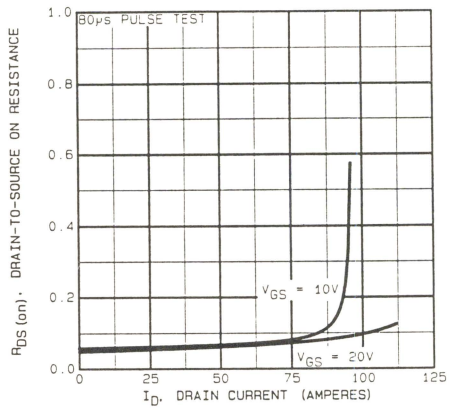


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

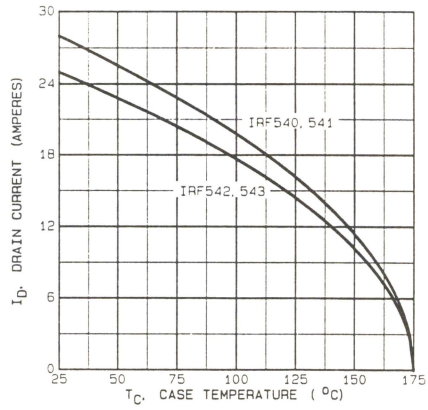


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

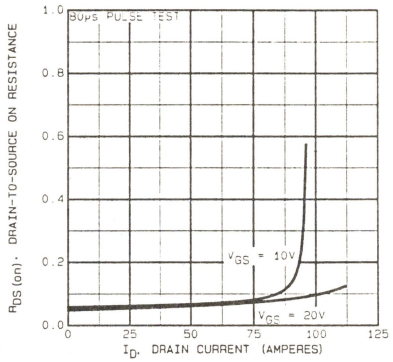


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

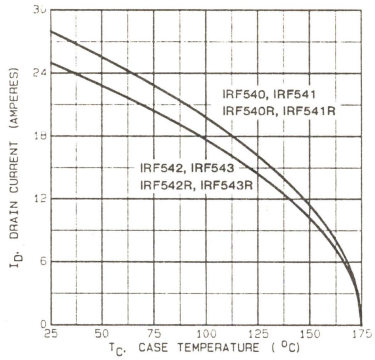


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

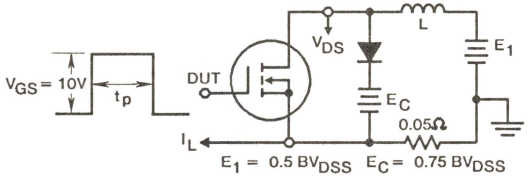


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

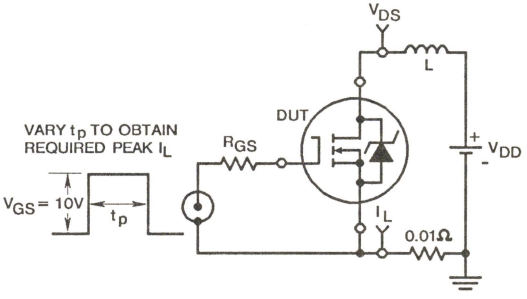


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

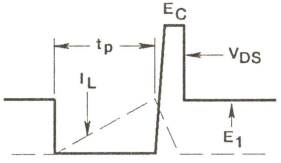


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

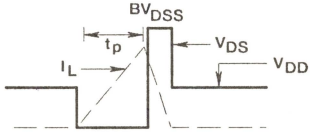


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

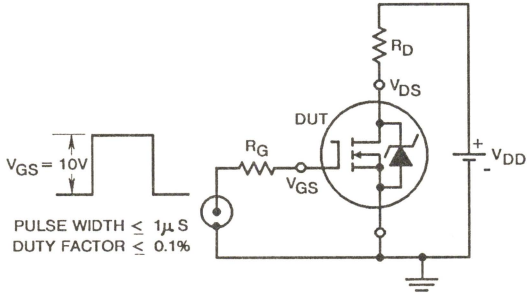


FIGURE 16. SWITCHING TIME TEST CIRCUIT

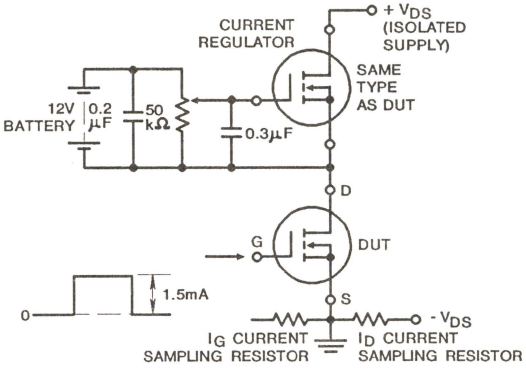


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF610/611/612/613
IRF610R/611R/612R/613R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.6A and 3.3A, 150V - 200V
- $r_{DS}(on)$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

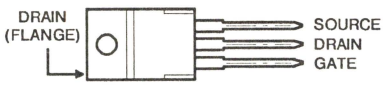
Description

The IRF610, IRF611, IRF612, and IRF613 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF610R, IRF611R, IRF612R and IRF613R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

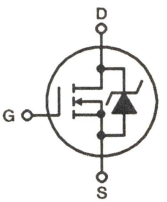
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF610 IRF610R	IRF611 IRF611R	IRF612 IRF612R	IRF613 IRF613R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	3.3	3.3	2.6	2.6	A
T_C = +100°C ..... I_D	2.1	2.1	1.6	1.6	A
Pulsed Drain Current (3) ..... I_{DM}	8	8	6.5	6.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	43	43	43	43	W
Linear Derating Factor	0.34	0.34	0.34	0.34	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	10	10	8.0	8.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	46	46	46	46	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 6.4mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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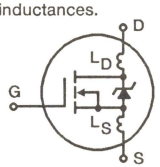
File Number **1576.1**

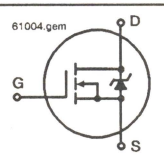
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF610/612, IRF610R/612R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF611/613, IRF611R/613R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF610/611, IRF610R/611R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.3	–	–	A
IRF612/613, IRF612R/613R			2.6	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF610/611, IRF610R/611R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.6A	–	1.0	1.5	Ω
IRF612/613, IRF612R/613R			–	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 1.6A	0.8	1.3	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	60	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	16	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, $I_D \simeq$ 3.3A, R_G = 24Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8	12	ns
Rise Time	t_r		–	17	26	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	13	21	ns
Fall Time	t_f		–	9	13	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.3A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.3	8.2	nC
Gate-Source Charge	Q_{gs}		–	1.2	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	3.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.9	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	3.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	8	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.3A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	75	160	310	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/µs	0.33	0.9	1.4	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 6.4mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A (See Figure 15)

Performance Curves

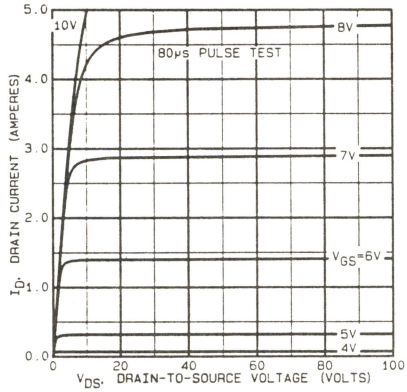


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

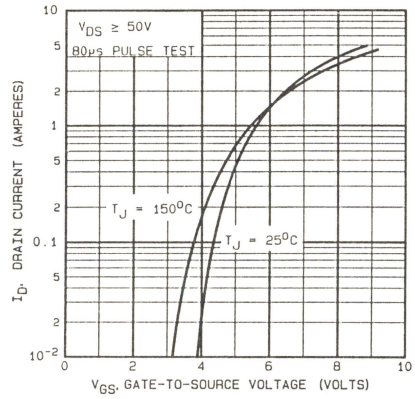


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

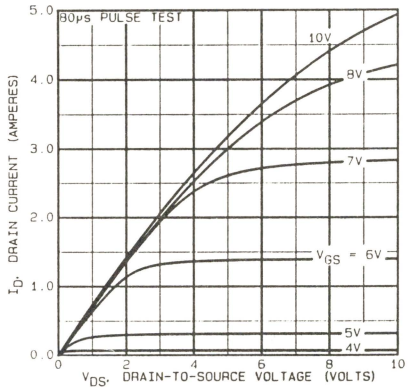


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

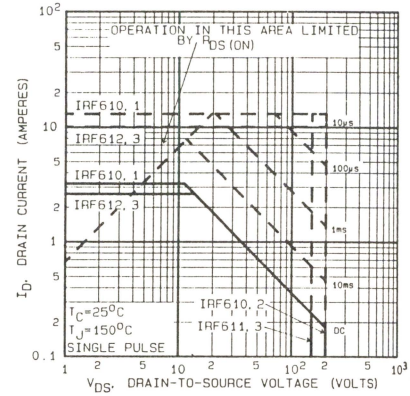


FIGURE 4. MAXIMUM SAFE OPERATING AREA

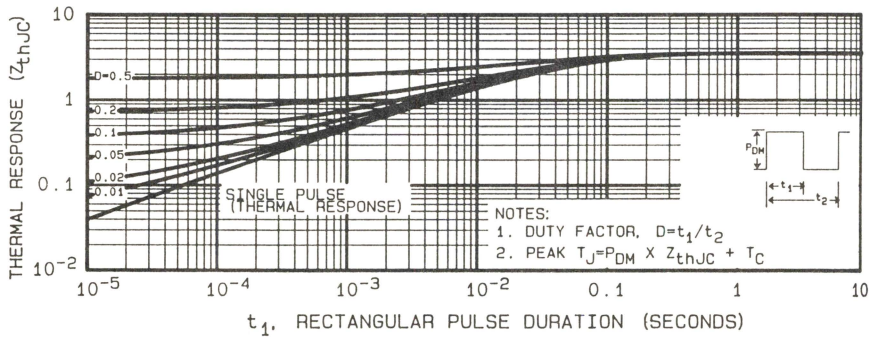


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

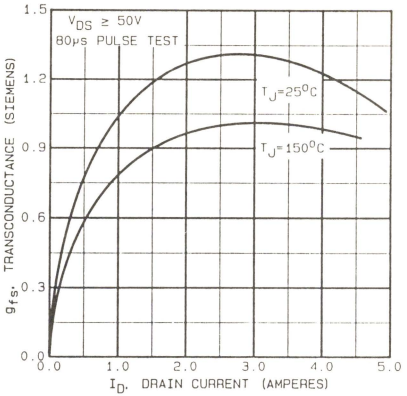


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

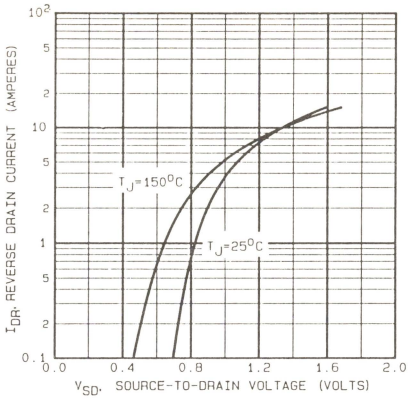


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

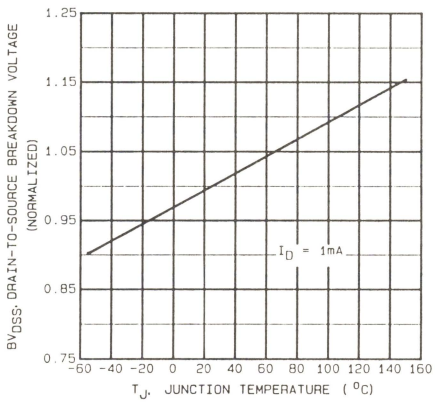


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

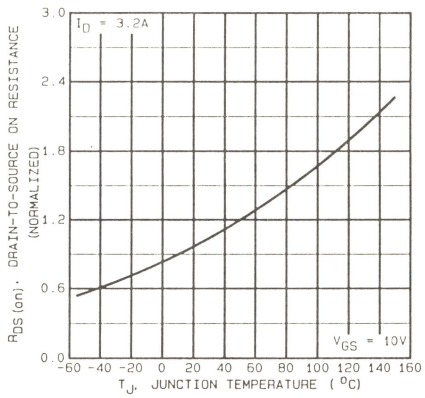


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

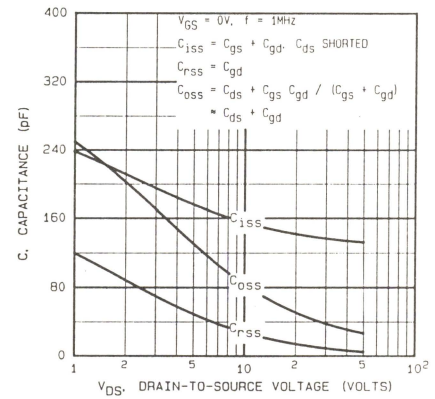


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

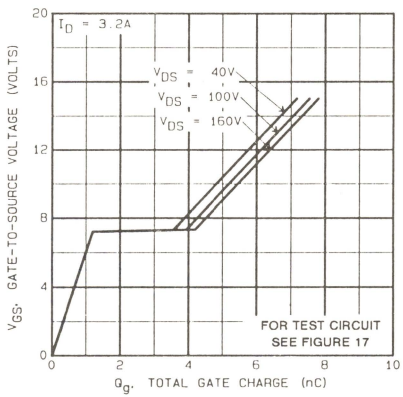


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

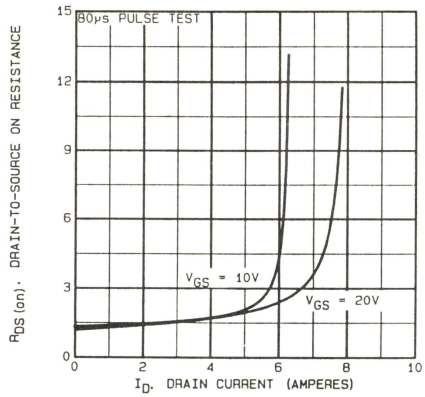


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

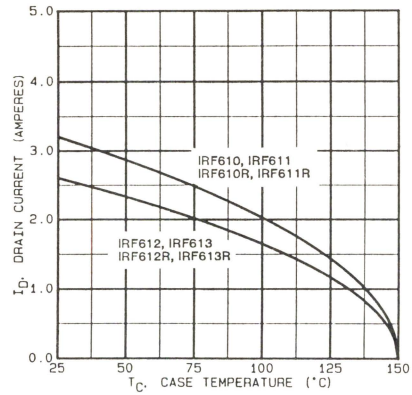


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

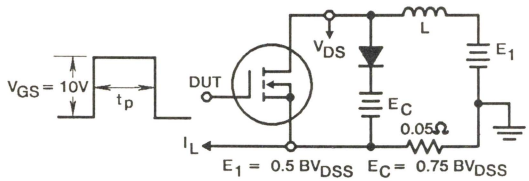


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

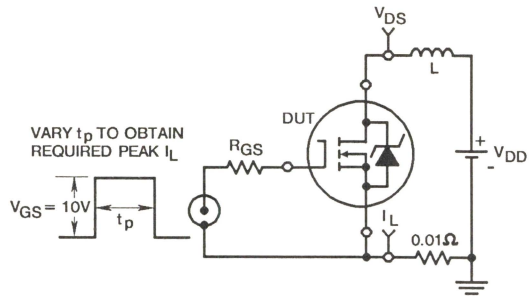


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

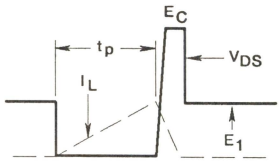


FIGURE14b. CLAMPED INDUCTIVE WAVEFORMS

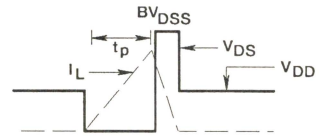


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

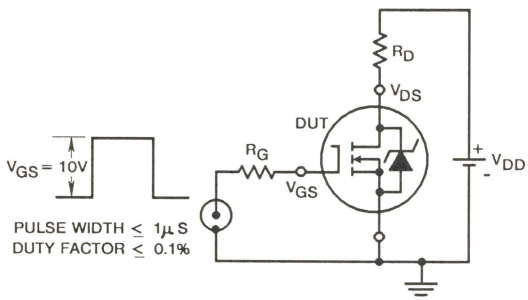


FIGURE 16. SWITCHING TIME TEST CIRCUIT

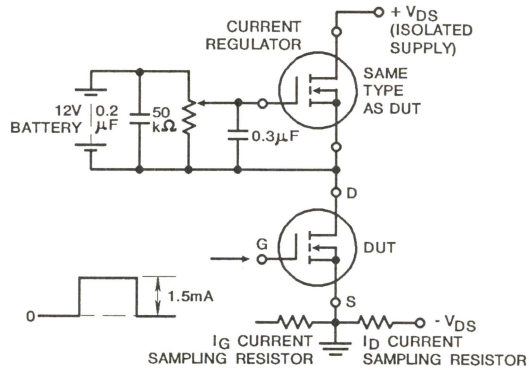


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF614

N-Channel Power MOSFETs Avalanche Energy Rated

May 1992

Features

- 2.0A, 250V
- $r_{DS(ON)}$ = 2.0Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- High Input Impedance
- +150°C Operating Temperature

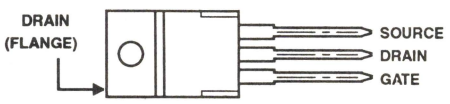
Description

The IRF614 (TA17443) is an n-channel enhancement-mode silicon-gate power field-effect transistor designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The IRF614 is supplied in the JEDEC TO-220AB plastic package.

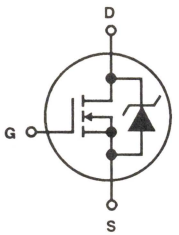
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF614	UNITS
Drain-Source Voltage (1)	V_{DS}	250	V
Drain-Gate Voltage	V_{DGR}	250	V
Continuous Drain Current			
T_C = +25°C	I_D	2.0	A
T_C = +100°C	I_D	1.3	A
Pulsed Drain Current (2)	I_{DM}	8.0	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	20	W
Linear Derating Factor		0.16	W/°C
Single Pulse Avalanche Rating (3) (See Fig. 14)	E_{AS}	61	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Figure 5)
3. V_{DD} = 50V, Starting T_J = +25°C, L = 21mH, R_G = 25Ω, Peak I_L = 2.2A.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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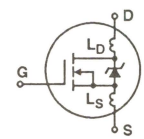
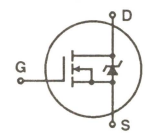
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V	250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA	2	-	4	V
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250V, V_{GS} = 0V	-	-	250	µA
		V_{DS} = 200V, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)Max}$, V_{GS} = 10V	2.0	-	-	A
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 1.0A, V_{GS} = 10V	-	1.6	2.0	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = 2 x V_{GS}, I_{DS} = 1.0A	0.8	1.2	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	180	-	pF
Output Capacitance	C_{OSS}		-	53	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	14	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 2.0A, R_G = 24Ω, R_D = 61Ω, See Figure 16 (MOSFET switching times are essentially independent of operating temperature)	-	8.9	13	ns
Rise Time	t_r		-	12	18	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	18	27	ns
Fall Time	t_f		-	8.9	15	ns
Total Gate Charge	Q_{g10}	V_{GS} = 10V, I_D = 2.0A V_{DS} = 0.8 x Max Rating. See Figure 17 for test circuit (Gate charge is essentially independent of operating temperature)	-	9.6	14.4	nC
Gate-Source Charge	Q_{gs}		-	2.4	3.6	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4.5	6.7	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad. 	-	7.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	6.4	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.50	-	°C/W
Junction to Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	-	-	2.0	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}		-	-	8.0	A
Diode Forward Voltage (Note 1)	V_{SD}	T_J = +25°C, I_{SD} = 2.0A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_{SD} = 2.0A, dI_{SD}/dt = 100A/µs	67	-	340	ns
Reverse Recovery Charge	Q_{RR}	T_J = +25°C, I_{SD} = 2.0A, dI_{SD}/dt = 100A/µs	0.24	0.54	1.2	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

NOTES: 1. Pulse Test: Pulse width ≤ 300µs. Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

Performance Curves

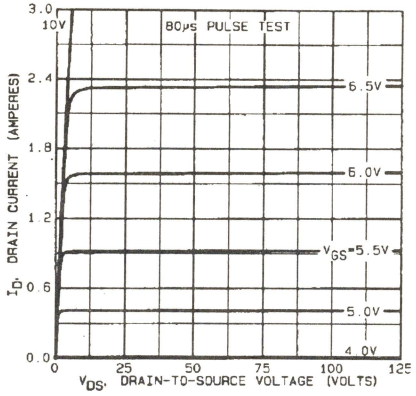


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

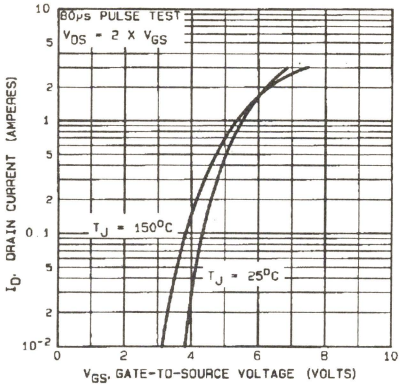


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

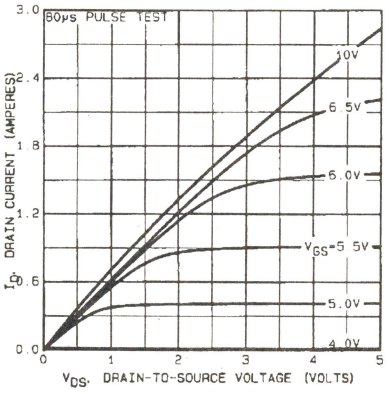


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

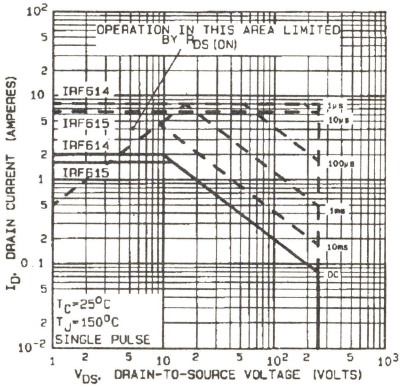


FIGURE 4. MAXIMUM SAFE OPERATING AREA

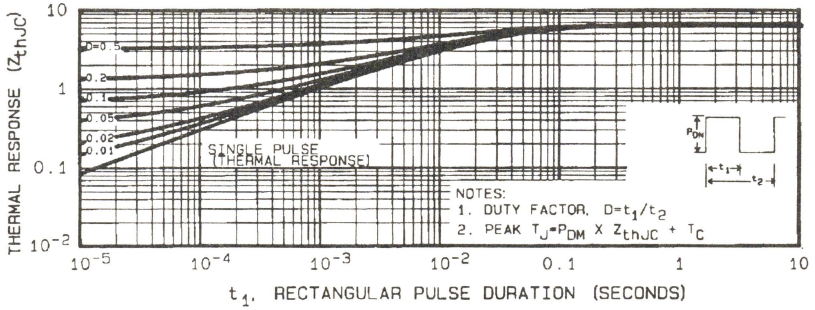


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

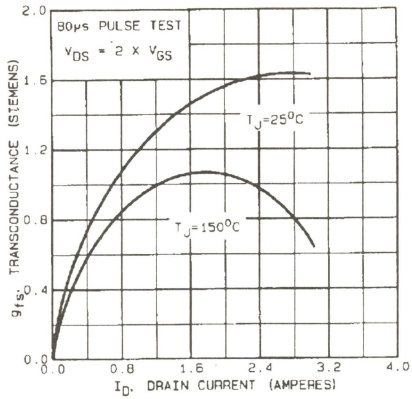


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

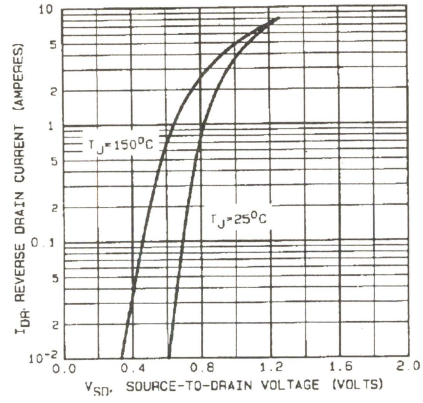


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

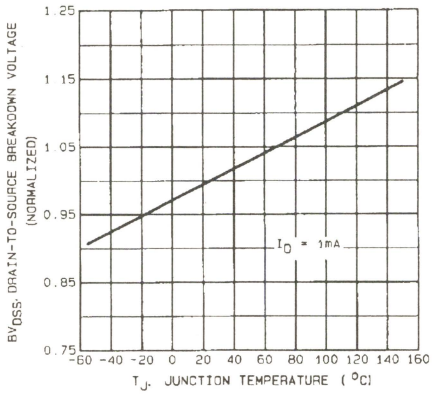


FIGURE 8 BREAKDOWN vs TEMPERATURE

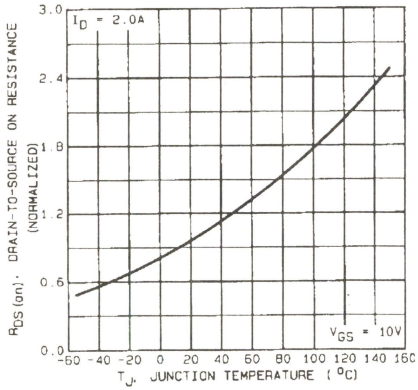


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

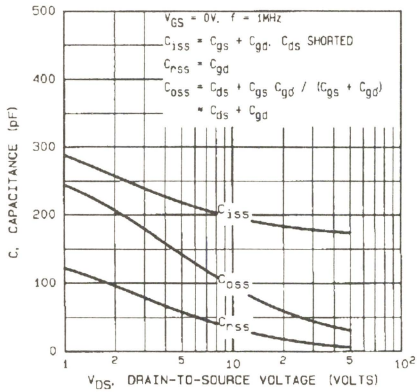


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

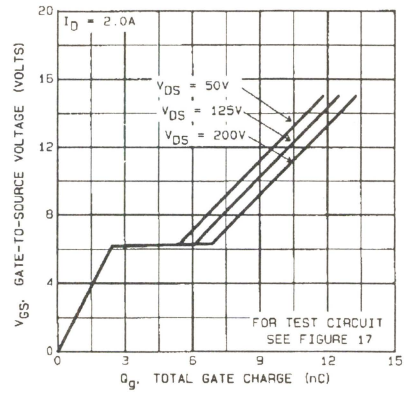


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

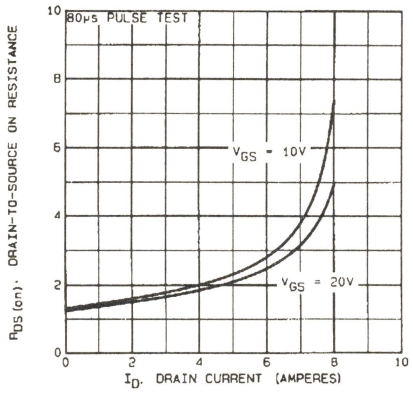


FIGURE 12. TYPICAL ON-RESISTANCE vs DRAIN CURRENT

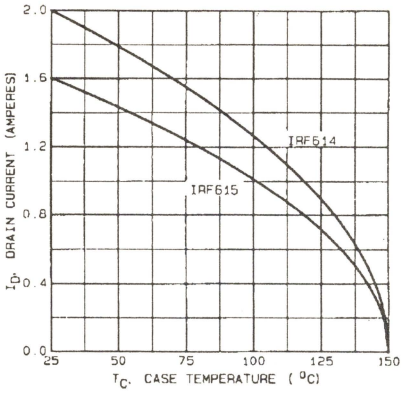


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

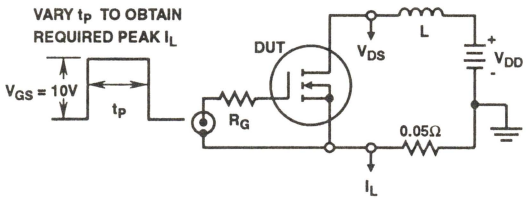


FIGURE 14a. UNCLAMPED INDUCTIVE TEST CIRCUIT

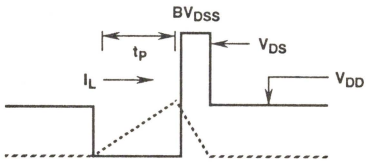


FIGURE 14b. UNCLAMPED INDUCTIVE LOAD TEST WAVEFORMS

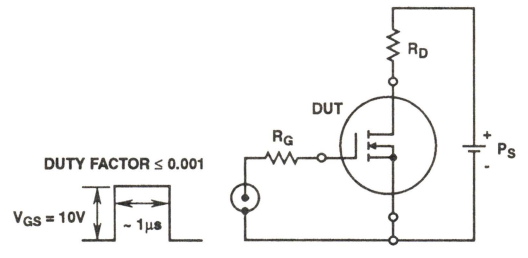


FIGURE 15. SWITCHING TIME TEST CIRCUIT

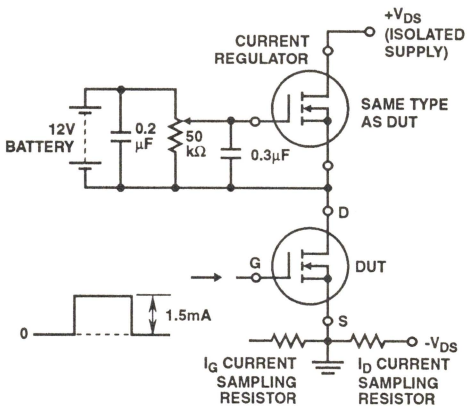


FIGURE 16. GATE CHARGE TEST CIRCUIT

HARRIS

IRF620/621/622/623
IRF620R/621R/622R/623R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.0A and 5.0A, 150V - 200V
- $r_{DS}(on)$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

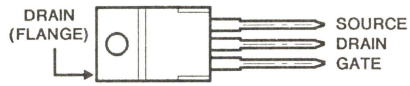
Description

The IRF620, IRF621, IRF622, and IRF623 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF620R, IRF621R, IRF622R and IRF623R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

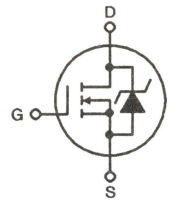
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF620 IRF620R	IRF621 IRF621R	IRF622 IRF622R	IRF623 IRF623R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	5.0	5.0	4.0	4.0	A
T_C = +100°C ..... I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3) ..... I_{DM}	20	20	16	16	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	40	40	40	40	W
Linear Derating Factor	0.32	0.32	0.32	0.32	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	20	20	16	16	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	85	85	85	85	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 10V, starting T_J = +25°C, L = 6.18mH, R_{GS} = 50Ω, I_{PEAK} = 5A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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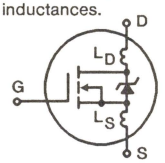
File Number 1577.1

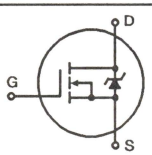
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF620/622, IRF620R/622R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF621/623, IRF621R/623R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF620/621, IRF620R/621R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	5.0	–	–	A
IRF622/623, IRF622R/623R			4.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF620/621, IRF620R/621R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	–	0.5	0.8	Ω
IRF622/623, IRF622R/623R			–	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$Max, I_D = 2.5A	1.3	2.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	450	–	pF
Output Capacitance	C_{OSS}		–	150	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 2.5BVDSS, I_D = 5.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	30	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	5.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	5.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	20	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.0A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 5.0A, dI_F/dt = 100A/µs	–	350	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 5.0A, dI_F/dt = 100A/µs	–	2.3	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 10V, Start T_J = +25°C, L = 6.18mH, R_{GS} = 50Ω, I_{PEAK} = 5A (See Figure 15)

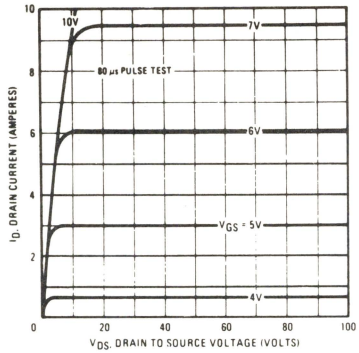


Fig. 1 – Typical Output Characteristics

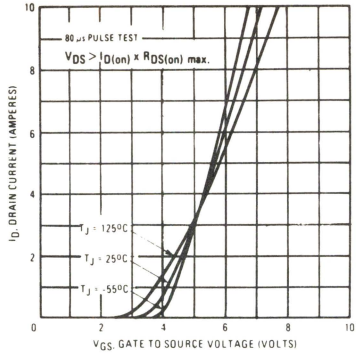


Fig. 2 – Typical Transfer Characteristics

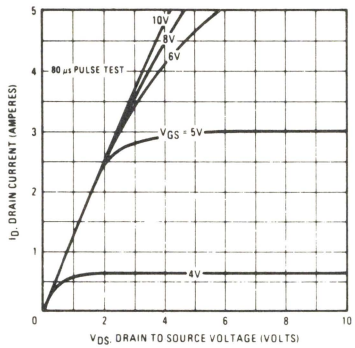


Fig. 3 – Typical Saturation Characteristics

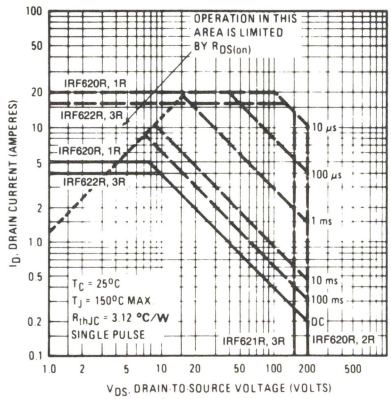


Fig. 4 – Maximum Safe Operating Area

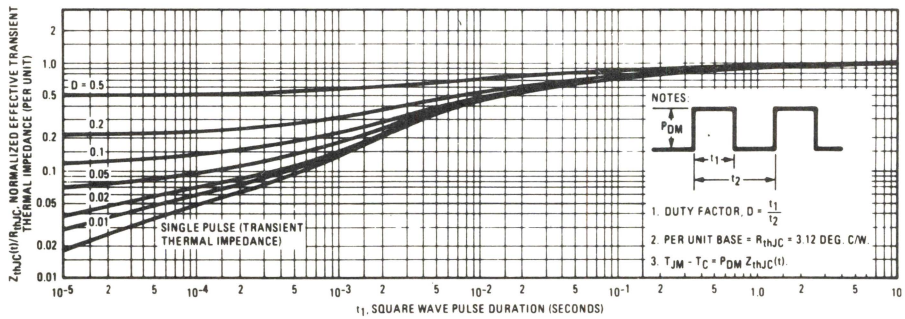


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

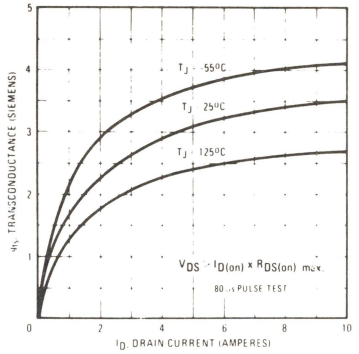


Fig. 6 – Typical Transconductance Vs. Drain Current

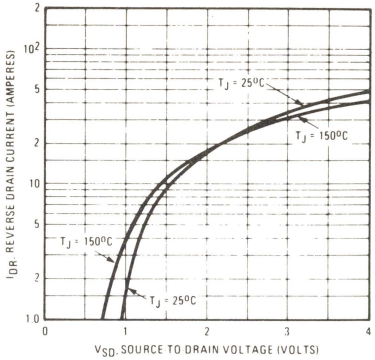


Fig. 7 – Typical Source-Drain Diode Forward Voltage

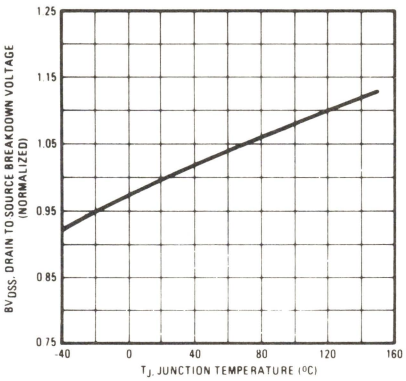


Fig. 8 – Breakdown Voltage Vs. Temperature

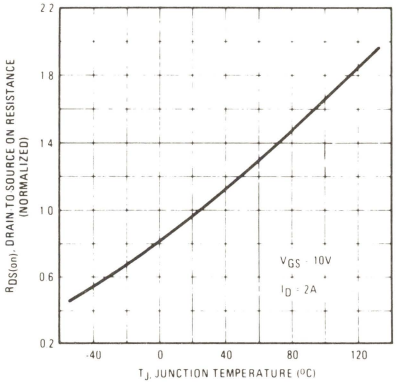


Fig. 9 – Normalized On-Resistance Vs. Temperature

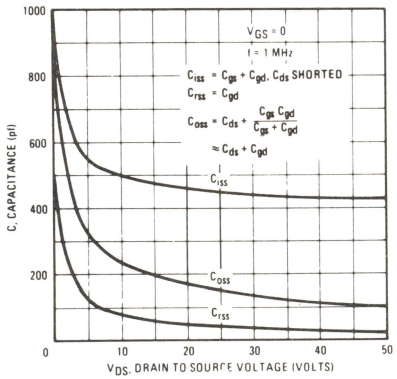


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

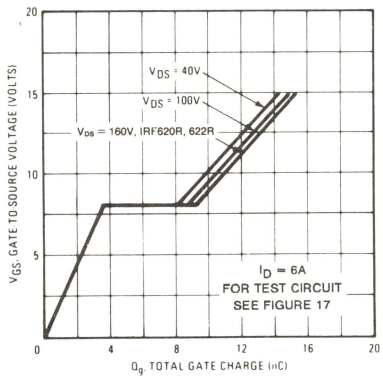


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

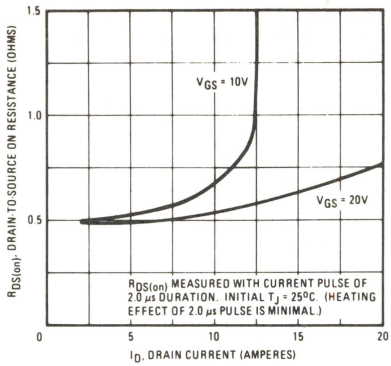


Fig. 12 — Typical On-Resistance Vs. Drain Current

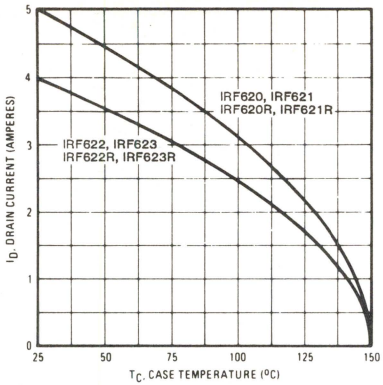


Fig. 13 — Maximum Drain Current Vs. Case Temperature

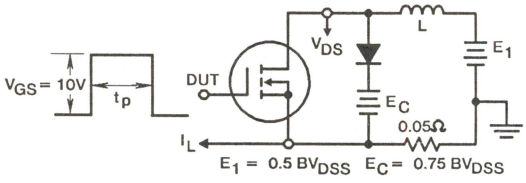


Fig. 14a — Clamped Inductive Test Circuit

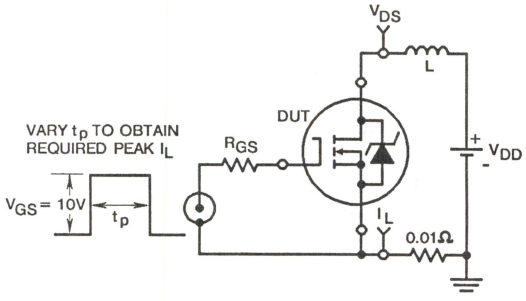


Fig. 15a — Unclamped Energy Test Circuit

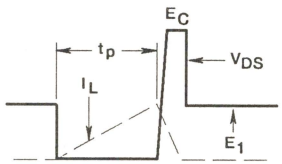


Fig. 14b — Clamped Inductive Waveforms

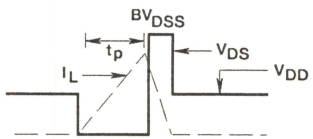


Fig. 15b — Unclamped Energy Waveforms

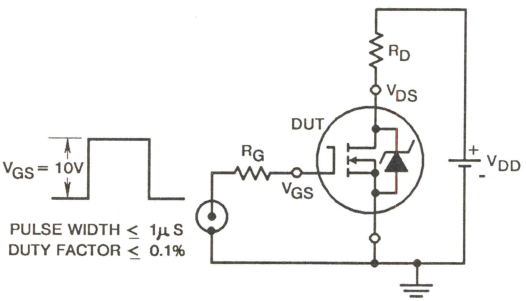


Fig. 16 — Switching Time Test Circuit

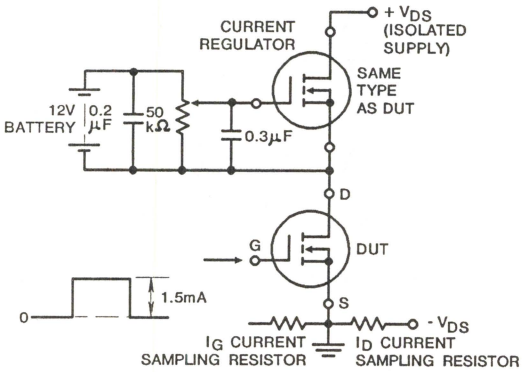


Fig. 17 — Gate Charge Test Circuit

HARRIS

IRF624, IRF625 IRF626, IRF627

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 3.8A and 3.3A, 250V - 275V
- $r_{DS}(on)$ = 1.1Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 250/275V DC Rating - 120V AC Line System Operation

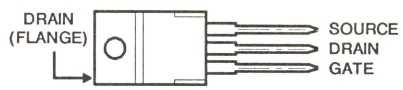
Description

The IRF624, IRF625, IRF626, and IRF627 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

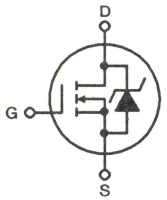
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRF624	IRF625	IRF626	IRF627	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	3.8	3.3	3.8	3.3	A
T_C = +100°C	I_D	2.4	2.1	2.4	2.1	A
Pulsed Drain Current (3)	I_{DM}	15	13	15	13	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	40	40	40	40	W
Linear Derating Factor		0.32	0.32	0.32	0.32	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{AS}	120	120	120	120	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 13.6mH, R_{GS} = 25Ω, I_{PEAK} = 3.8A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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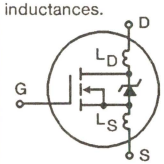
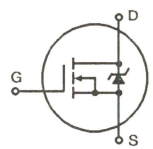
File Number **2167.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF624, IRF625	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	250	–	–	V
IRF626, IRF627			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF624, IRF626	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.8	–	–	A
IRF625, IRF627			3.3	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF624, IRF626	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.4A	–	0.8	1.1	Ω
IRF625, IRF627			–	1.05	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x V_{GS}, I_{DS} = 1.9A	1.4	2.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	340	–	pF
Output Capacitance	C_{OSS}		–	110	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	32	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 3.8A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	11	17	ns
Rise Time	t_r		–	24	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	21	32	ns
Fall Time	t_f		–	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.8A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	15	22	nC
Gate-Source Charge	Q_{gs}		–	4.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	7.2	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	3.8	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	15	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.8A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.8A, dI_F/dt = 100A/µs	81	180	370	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.8A, dI_F/dt = 100A/µs	0.44	0.93	2.0	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, starting T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A. See Figure 15.

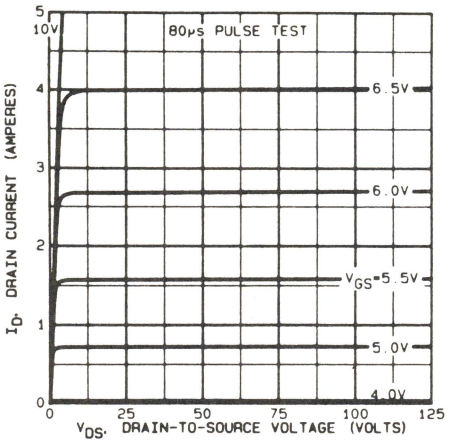


Fig. 1 — Typical Output Characteristics

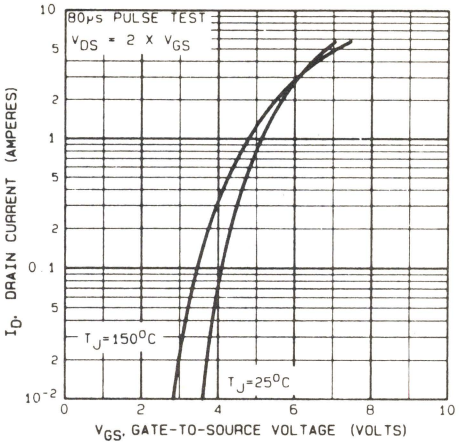


Fig. 2 — Typical Transfer Characteristics

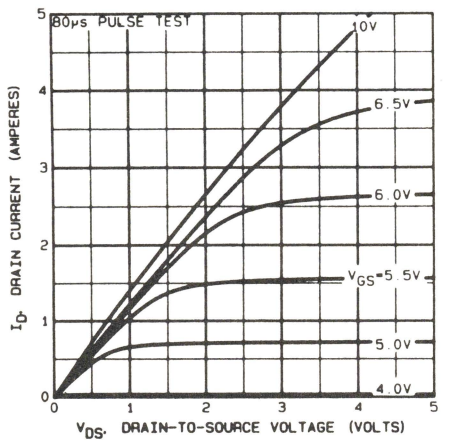


Fig. 3 — Typical Saturation Characteristics

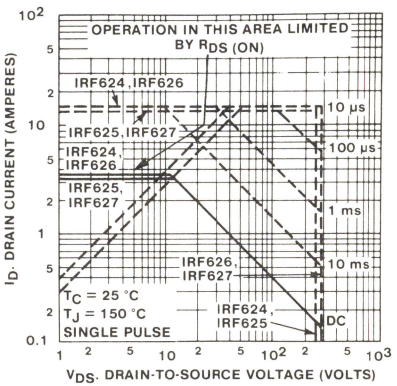


Fig. 4 — Maximum Safe Operating Area

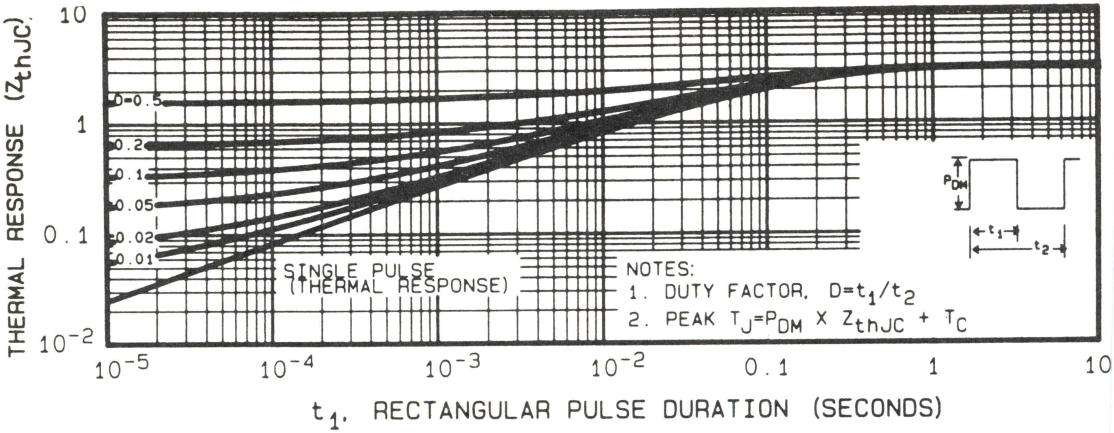


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

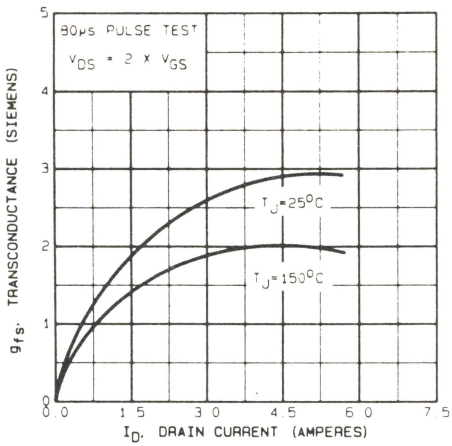


Fig. 6 — Typical Transconductance Vs. Drain Current

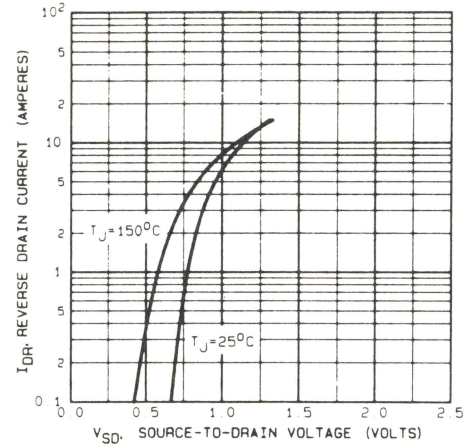


Fig. 7 — Typical Source-Drain Diode Forward Voltage

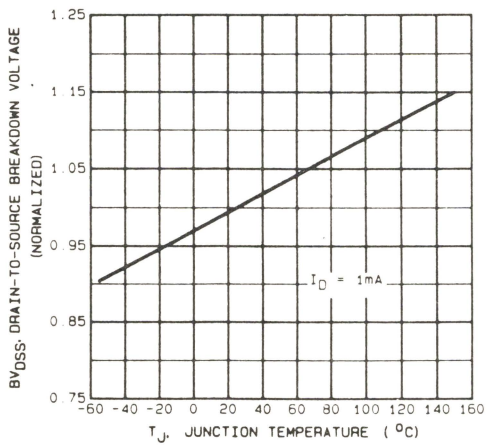


Fig. 8 — Breakdown Voltage Vs. Temperature

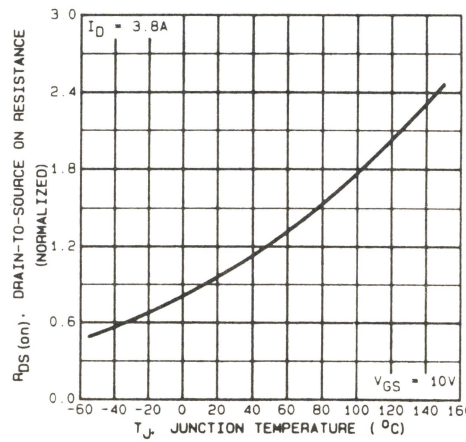


Fig. 9 — Normalized On-Resistance Vs. Temperature

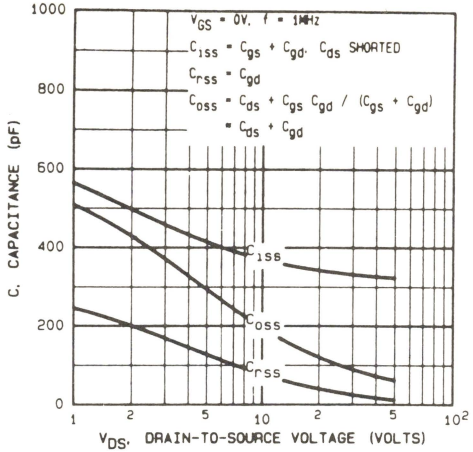


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

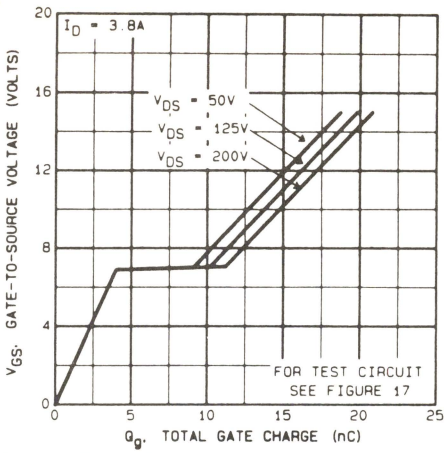


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

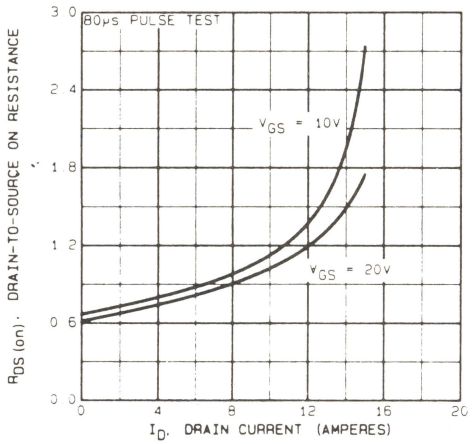


Fig. 12 — Typical On-Resistance Vs. Drain Current

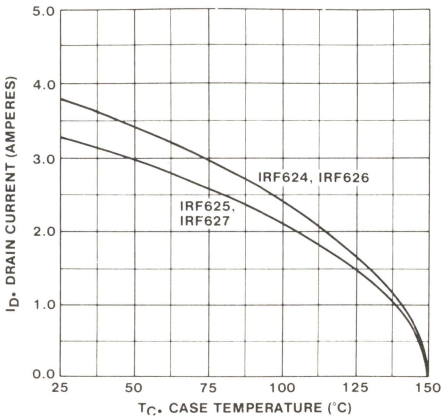


Fig. 13 — Maximum Drain Current Vs. Case Temperature

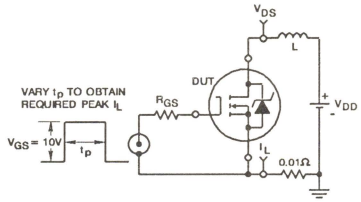


Fig. 14 — Unclamped Energy Test Circuit

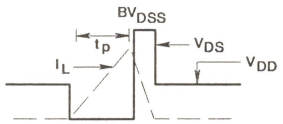


Fig. 15 — Unclamped Energy Waveforms

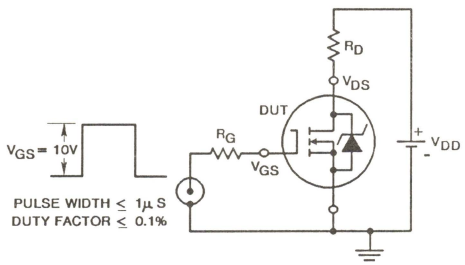


Fig. 16 — Switching Time Test Circuit

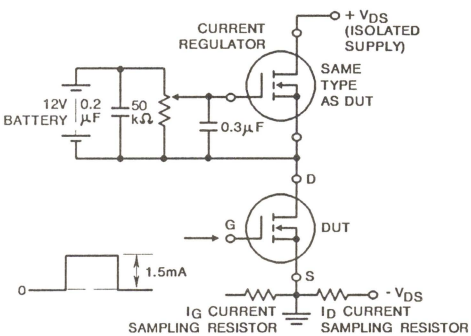


Fig. 17 — Gate Charge Test Circuit

HARRIS

IRF630/631/632/633
IRF630R/631R/632R/633R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 8.0A and 9.0A, 150V - 200V
- $r_{DS}(on)$ = 0.4Ω and 0.6Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

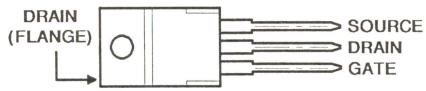
Description

The IRF630, IRF631, IRF632, and IRF633 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF630R, IRF631R, IRF632R and IRF633R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

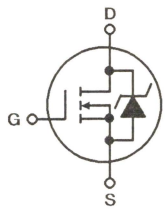
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF630 IRF630R	IRF631 IRF631R	IRF632 IRF632R	IRF633 IRF633R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	9.0	9.0	8.0	8.0	A
T_C = +100°C ..... I_D	6.0	6.0	5.0	5.0	A
Pulsed Drain Current (3) ..... I_{DM}	36	36	32	32	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	36	36	32	32	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	150	150	150	150	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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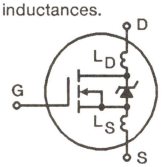
File Number **1578.1**

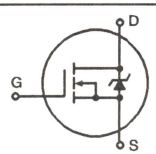
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF630/632, IRF630R/632R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	–	–	V
IRF631/633, IRF631R/633R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF630/631, IRF630R/631R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	9.0	–	–	A
IRF632/633, IRF632R/633R			8.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF630/631, IRF630R/631R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.0A	–	0.25	0.4	Ω
IRF632/633, IRF632R/633R			–	0.4	0.6	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$Max, I_D = 5.0A	3.0	4.8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	250	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 90V, I_D = 9.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	30	ns
Rise Time	t_r		–	–	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	50	ns
Fall Time	t_f		–	–	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 9.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	19	30	nC
Gate-Source Charge	Q_{gs}		–	10	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	9.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	9.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	36	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 9.0A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/μs	–	450	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 9.0A, dI_F/dt = 100A/μs	–	3.0	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, Start T_J = +25°C, L = 3.37mH, R_{GS} = 50Ω, I_{PEAK} = 9A (See Figure 15)

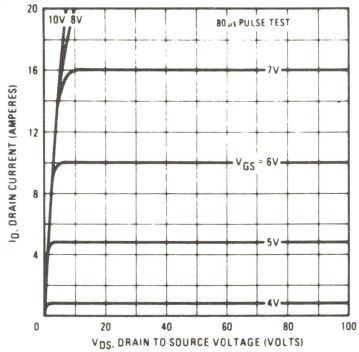


Fig. 1 – Typical Output Characteristics

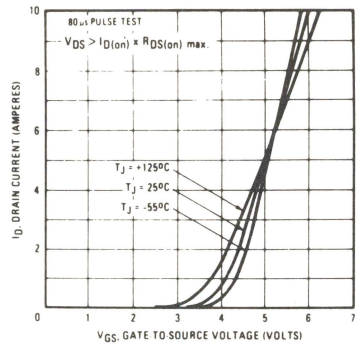


Fig. 2 – Typical Transfer Characteristics

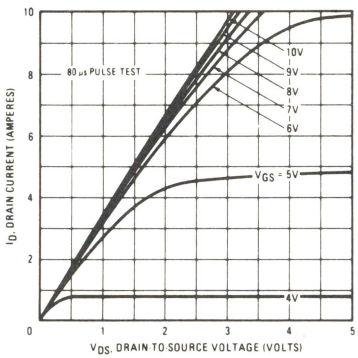


Fig. 3 – Typical Saturation Characteristics

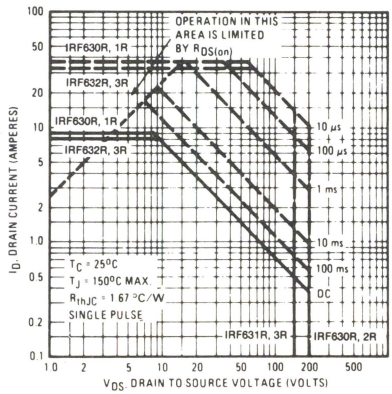


Fig. 4 – Maximum Safe Operating Area

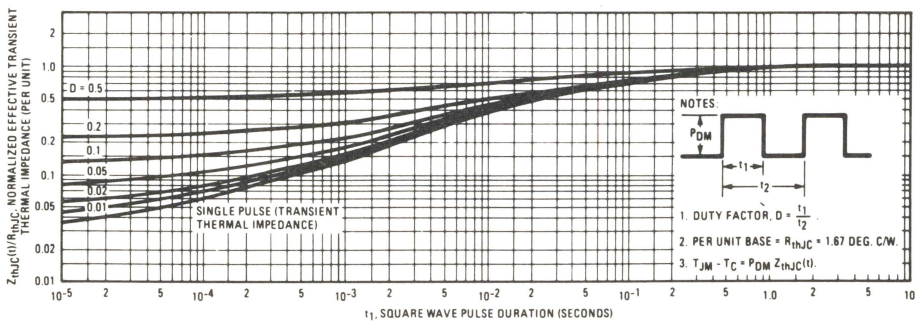


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

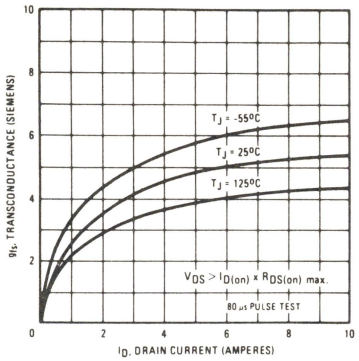


Fig. 6 – Typical Transconductance Vs. Drain Current

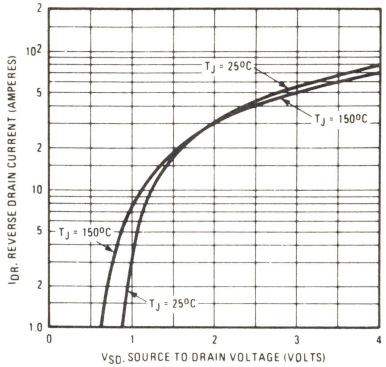


Fig. 7 – Typical Source-Drain Diode Forward Voltage

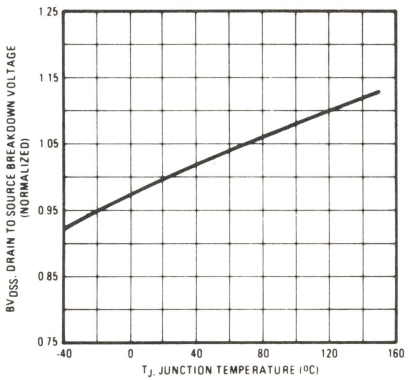


Fig. 8 – Breakdown Voltage Vs. Temperature

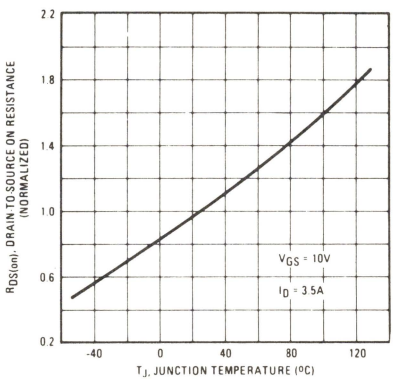


Fig. 9 – Normalized On-Resistance Vs. Temperature

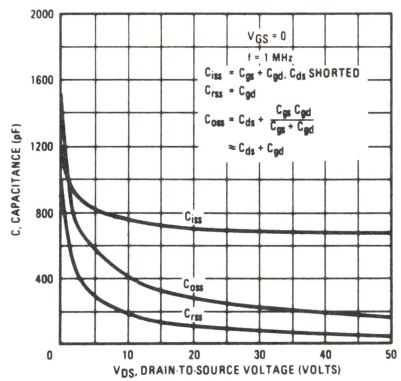


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

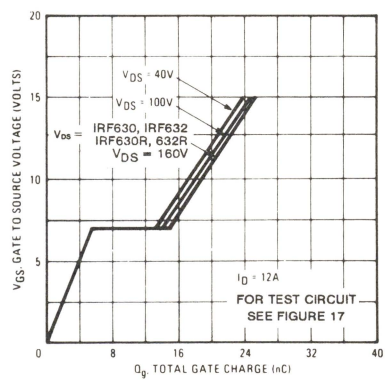


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

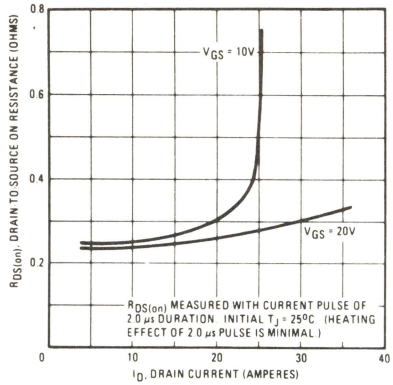


Fig. 12 — Typical On-Resistance Vs. Drain Current

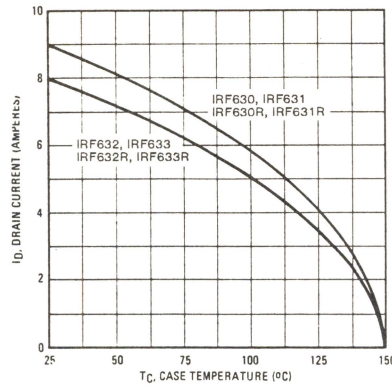


Fig. 13 — Maximum Drain Current Vs. Case Temperature

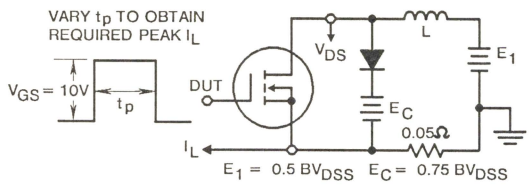


Fig. 14a — Clamped Inductive Test Circuit

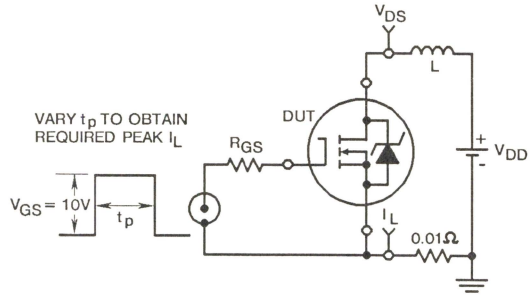


Fig. 15a — Unclamped Energy Test Circuit

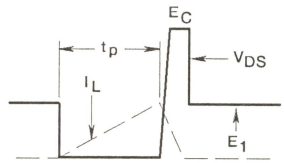


Fig. 14b — Clamped Inductive Waveforms

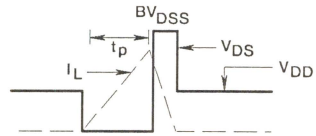


Fig. 15b — Unclamped Energy Waveforms

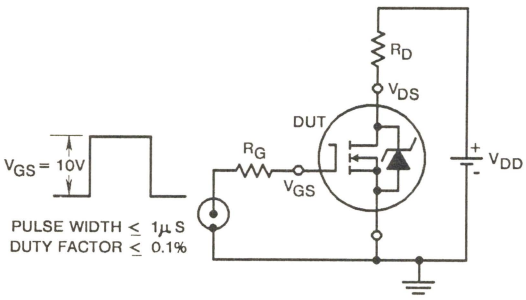


Fig. 16 — Switching Time Test Circuit

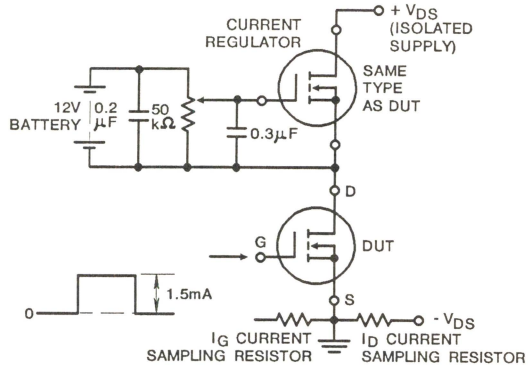


Fig. 17 — Gate Charge Test Circuit

HARRIS

IRF634, IRF635
IRF636, IRF637

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 8.1A and 6.5A, 250V - 275V
- $r_{DS}(on)$ = 0.45Ω and 0.68Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275/250V DC Rating - 120V AC Line System Operation

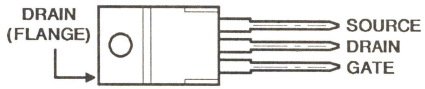
Description

The IRF634, IRF635, IRF636, and IRF637 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

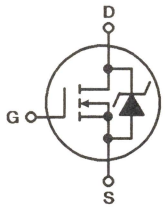
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF634	IRF635	IRF636	IRF637	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.1	6.5	8.1	6.5	A
T_C = +100°C ..... I_D	5.1	4.1	5.1	4.1	A
Pulsed Drain Current (3) ..... I_{DM}	32	26	32	26	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}	180	180	180	180	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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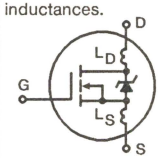
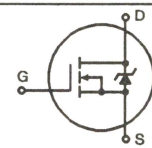
File Number **2168.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF636, IRF637	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	275	-	-	V
IRF634, IRF635			250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF634, IRF636	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	8.1	-	-	A
IRF635, IRF637			6.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF634, IRF636	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.1A	-	0.32	0.45	Ω
IRF635, IRF637			-	0.48	0.68	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x V_{GS} 0V, I_D = 4.1A	2.9	4.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	600	-	pF
Output Capacitance	C_{OSS}		-	180	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	52	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D ≃ 8.1A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	9.1	14	ns
Rise Time	t_r		-	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	47	ns
Fall Time	t_f		-	19	29	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8.1A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	24	35	nC
Gate-Source Charge	Q_{gs}		-	5.1	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	8.1	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.1A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	92	180	390	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.1A, dI_F/dt = 100A/μs	0.63	1.3	2.7	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 8.1A (See Figures 14 & 15)

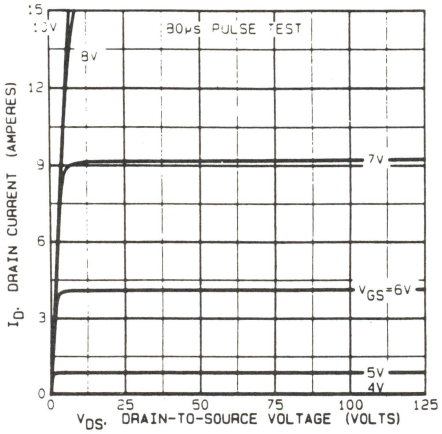


Fig. 1 — Typical Output Characteristics

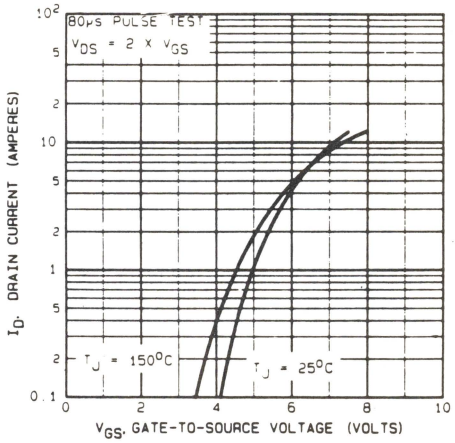


Fig. 2 — Typical Transfer Characteristics

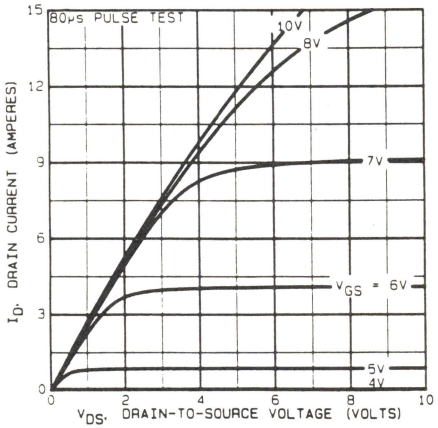


Fig. 3 — Typical Saturation Characteristics

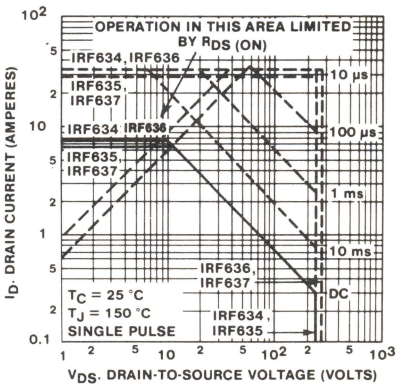


Fig. 4 — Maximum Safe Operating Area

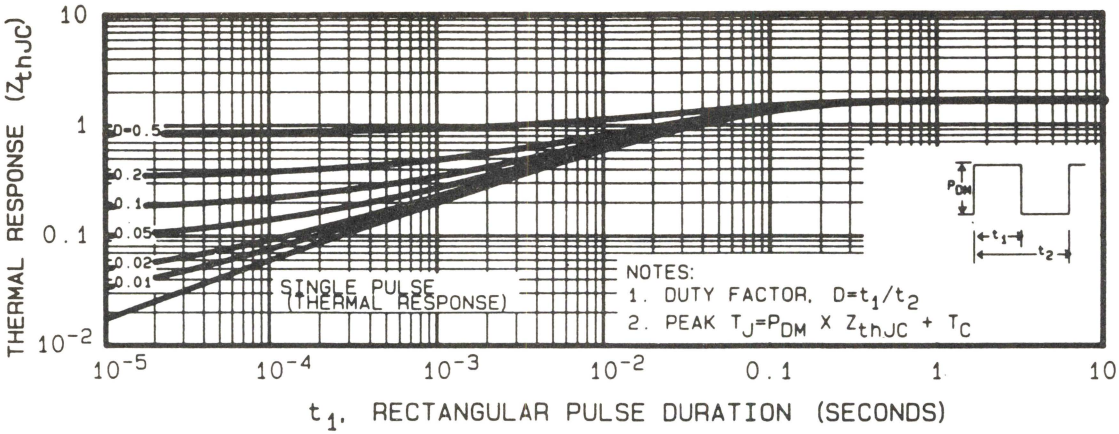


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

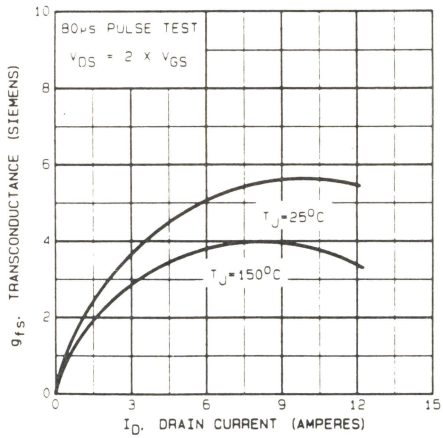


Fig. 6 — Typical Transconductance Vs. Drain Current

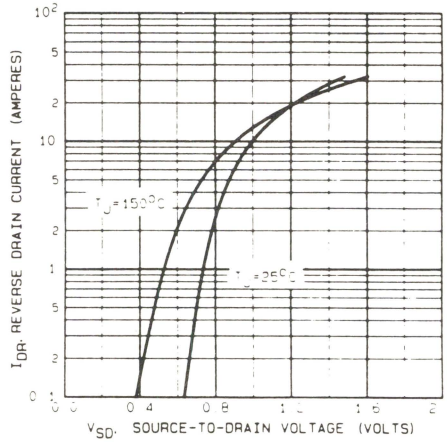


Fig. 7 — Typical Source-Drain Diode Forward Voltage

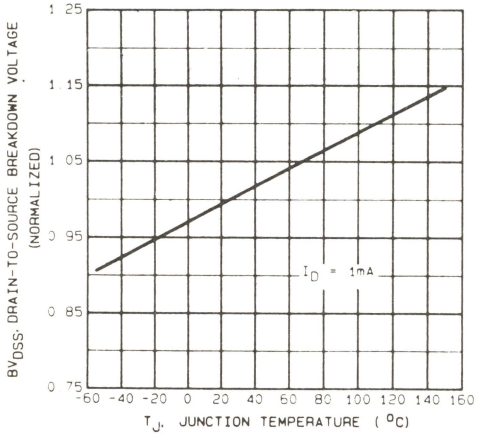


Fig. 8 — Breakdown Voltage Vs. Temperature

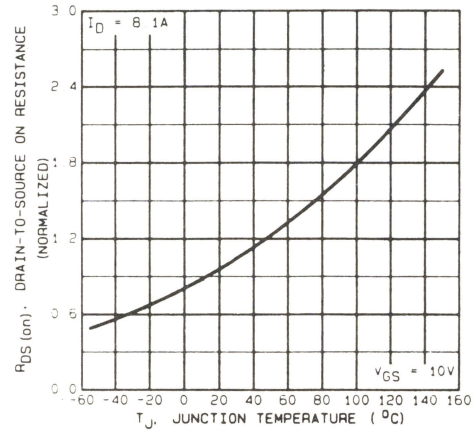


Fig. 9 — Normalized On-Resistance Vs. Temperature

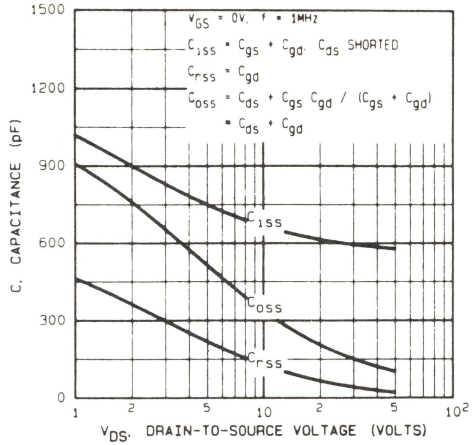


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

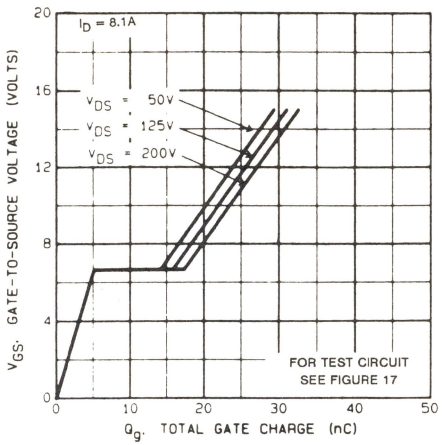


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

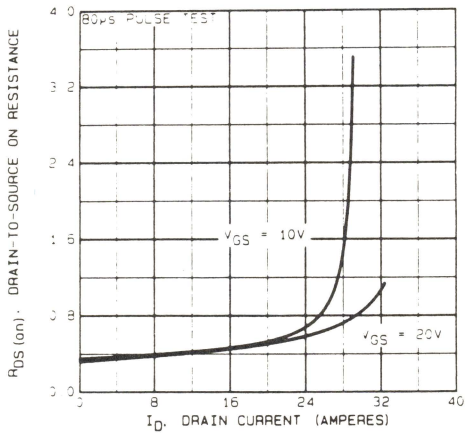


Fig. 12 — Typical On-Resistance Vs. Drain Current

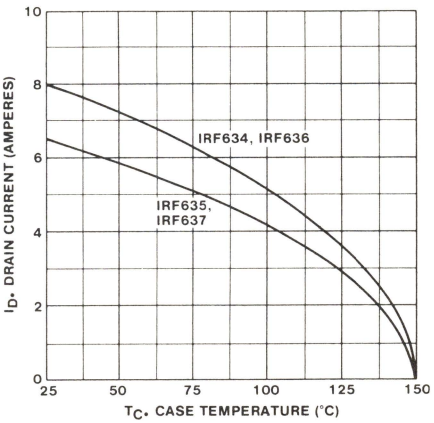


Fig. 13 — Maximum Drain Current Vs. Case Temperature

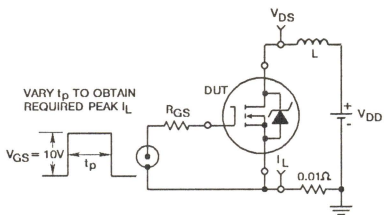


Fig. 14 — Unclamped Energy Test Circuit

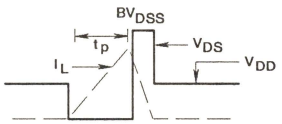


Fig. 15 — Unclamped Energy Waveforms

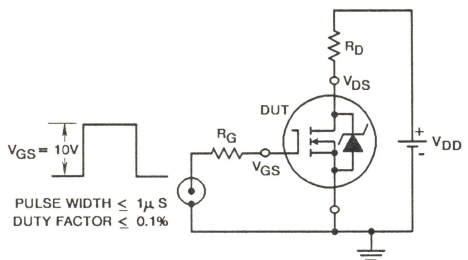


Fig. 16 — Switching Time Test Circuit

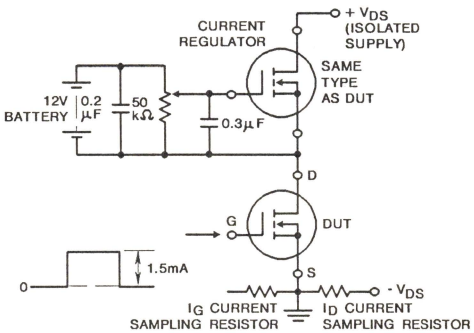


Fig. 17 — Gate Charge Test Circuit

HARRIS

IRF640/641/642/643
IRF640R/641R/642R/643R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 16A and 18A, 150V - 200V
- $r_{DS}(on)$ = 0.18Ω and 0.22Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

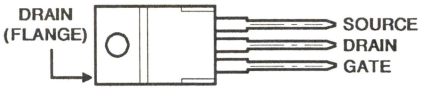
Description

The IRF640, IRF641, IRF642, and IRF643 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF640R, IRF641R, IRF642R and IRF643R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

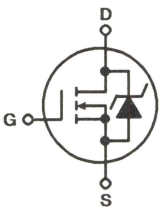
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF640 IRF640R	IRF641 IRF641R	IRF642 IRF642R	IRF643 IRF643R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	18	18	16	16	A
T_C = +100°C ..... I_D	11	11	10	10	A
Pulsed Drain Current (3) ..... I_{DM}	72	72	64	64	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	72	72	64	64	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	580	580	580	580	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 2.7mH, R_{GS} = 25Ω, I_{PEAK} = 18A. See Figure 15.

*R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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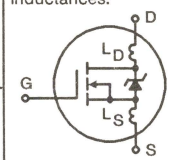
File Number **1585.1**

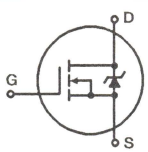
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF640/642, IRF640R/642R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRF641/643, IRF641R/643R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF640/641, IRF640R/641R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	18	–	–	A
IRF642/643, IRF642R/643R			16	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF640/641, IRF640R/641R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	–	0.14	0.18	Ω
IRF642/643, IRF642R/643R			–	0.20	0.22	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 10A	6.7	10	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1275	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 18A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	13	21	ns
Rise Time	t_r		–	50	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	46	68	ns
Fall Time	t_f		–	35	54	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	43	64	nC
Gate-Source Charge	Q_{gs}		–	8	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	22	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	18	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	72	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 18A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 18A, dI_F/dt = 100A/µs	120	240	530	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 18A, dI_F/dt = 100A/µs	1.3	2.8	5.6	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 20V, Start T_J = +25°C, L = 3.37mH, R_{GS} = 25Ω, I_{PEAK} = 18A (See Figure 15)

Performance Curves

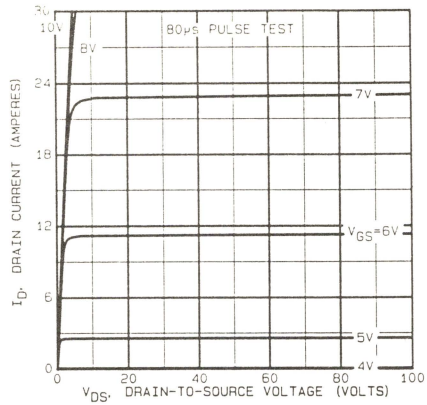


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

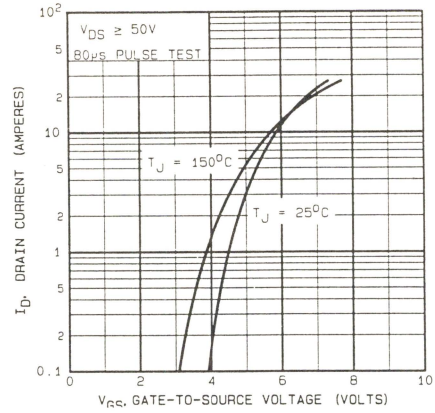


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

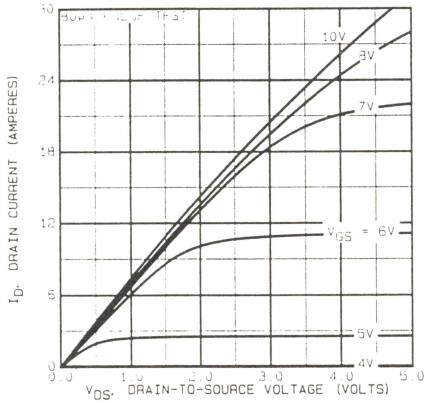


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

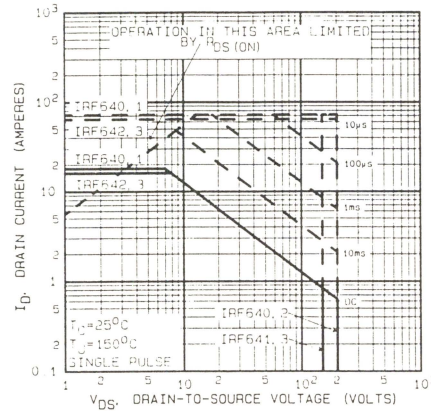


FIGURE 4. MAXIMUM SAFE OPERATING AREA

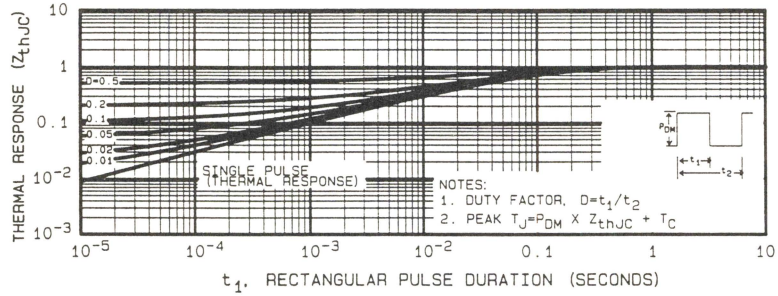


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

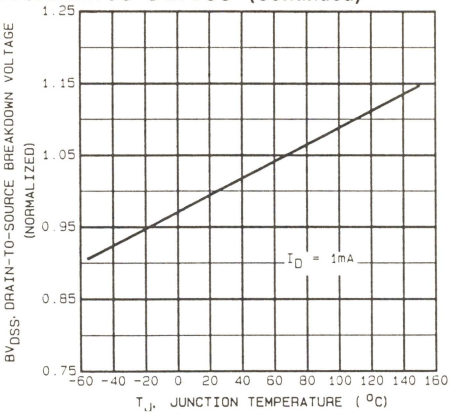


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

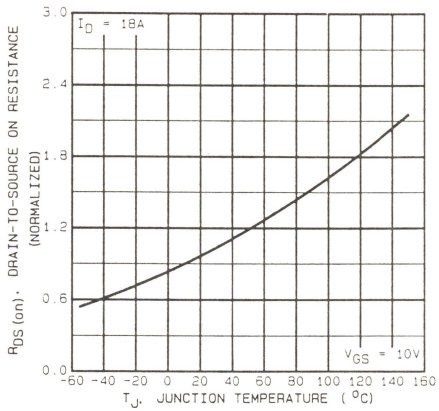


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

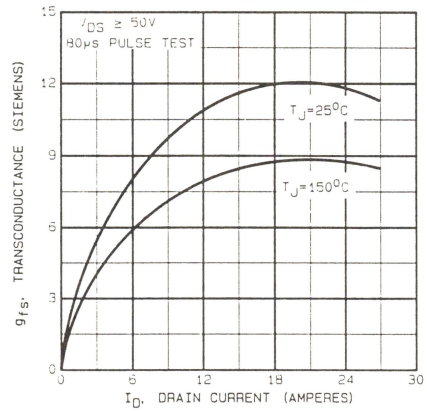


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

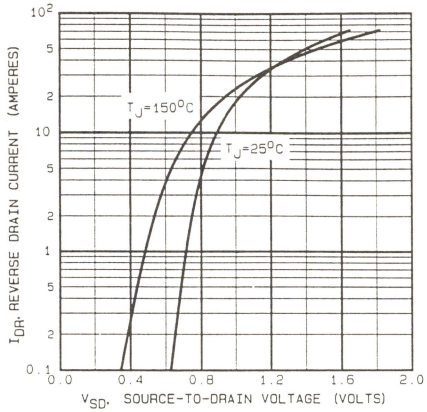


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

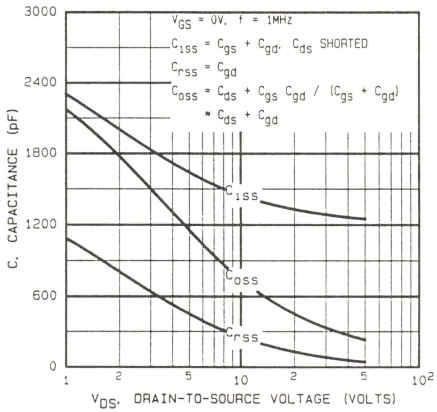


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

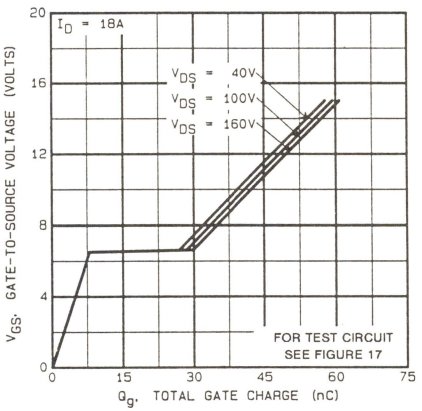


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

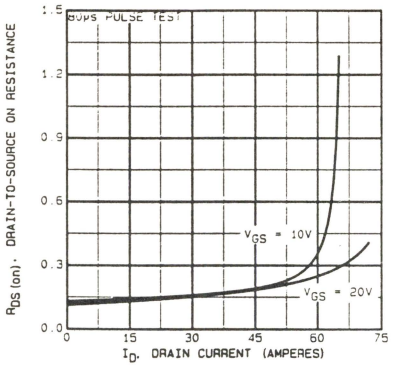


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

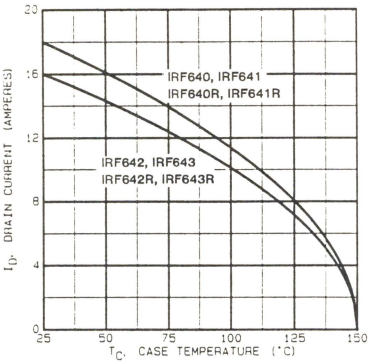


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

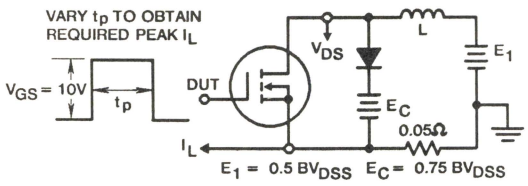


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

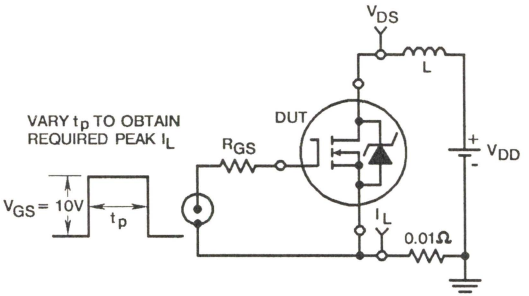


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

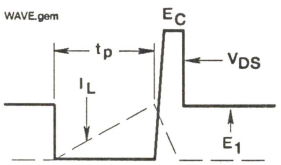


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

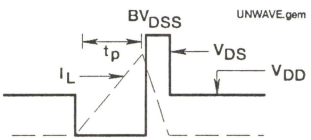


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

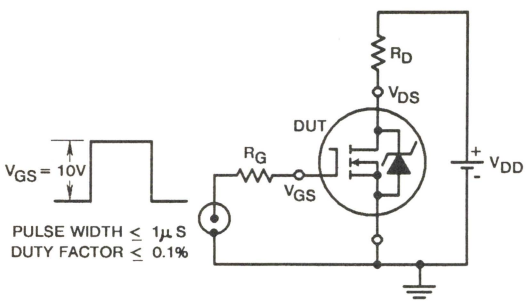


FIGURE 16. SWITCHING TIME TEST CIRCUIT

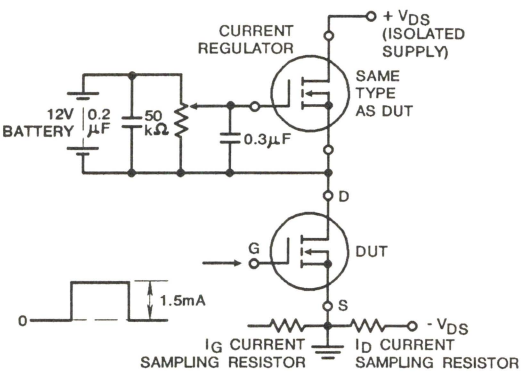


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF644, IRF645
IRF646, IRF647

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 13A and 14A, 250V - 275V
- $r_{DS}(on)$ = 0.28Ω and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275/250V DC Rating - 120V AC Line System Operation

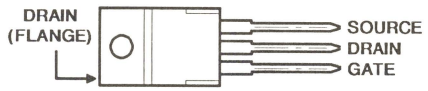
Description

The IRF644, IRF645, IRF646, and IRF647 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

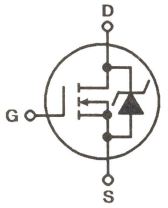
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF644	IRF645	IRF646	IRF647	UNITS
Drain-Source Voltage (1) ..... V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	250	250	275	275	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	13	14	13	A
T_C = +100°C ..... I_D	8.8	8.0	8.8	8.0	A
Pulsed Drain Current (3) ..... I_{DM}	56	52	56	52	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}	550	550	550	550	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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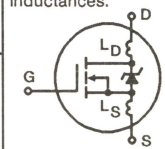
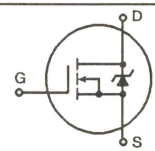
File Number **2169.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF646, IRF647	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	275	–	–	V
IRF644, IRF645			250	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF644, IRF646	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	14	–	–	A
IRF645, IRF647			13	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF644, IRF646	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8A	–	0.20	0.28	Ω
IRF645, IRF647			–	0.28	0.34	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 8A	6.7	10	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1300	–	pF
Output Capacitance	C_{OSS}		–	320	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	69	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 14A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	24	ns
Rise Time	t_r		–	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	53	80	ns
Fall Time	t_f		–	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	39	59	nC
Gate-Source Charge	Q_{gs}		–	6.6	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	20	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/µs	1.6	3.4	7.2	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.5mH, R_{GS} = 25Ω, I_{PEAK} = 14A (See Figures 14 & 15)

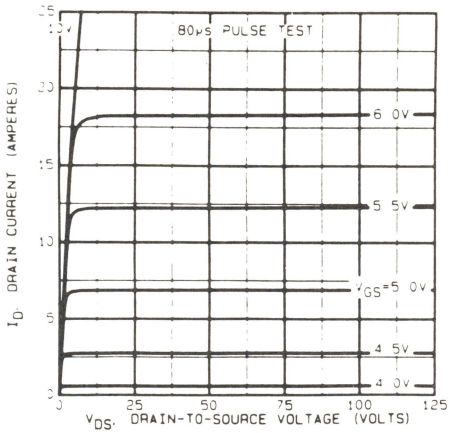


Fig. 1 — Typical Output Characteristics

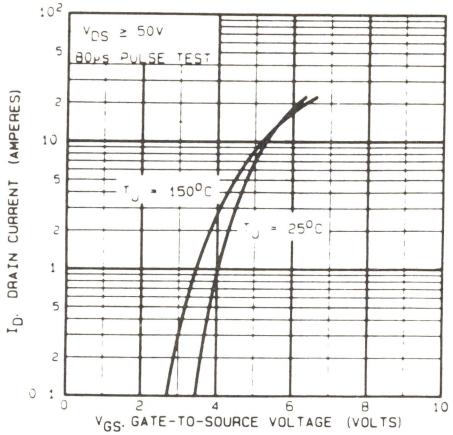


Fig. 2 — Typical Transfer Characteristics

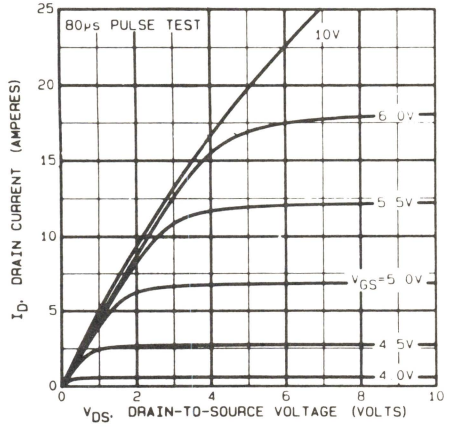


Fig. 3 — Typical Saturation Characteristics

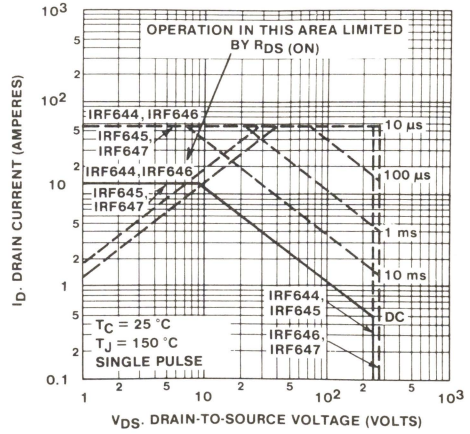


Fig. 4 — Maximum Safe Operating Area

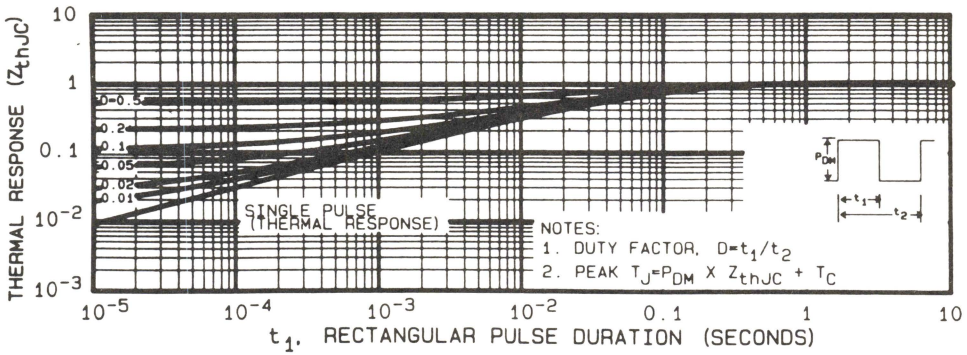


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

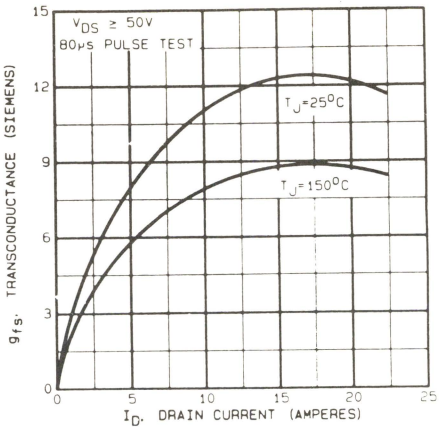


Fig. 6 — Typical Transconductance Vs. Drain Current

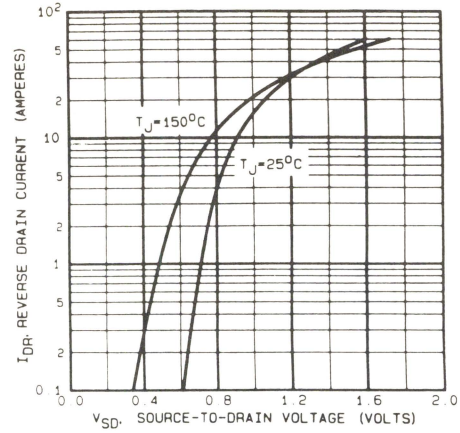


Fig. 7 — Typical Source-Drain Diode Forward Voltage

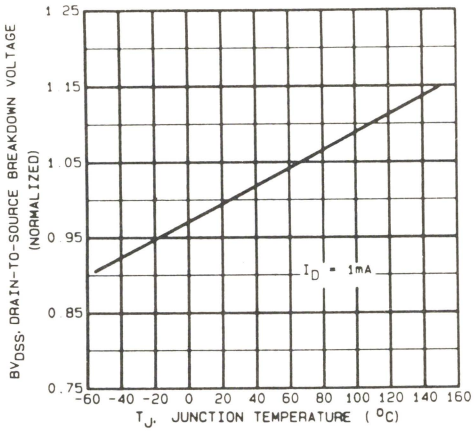


Fig. 8 — Breakdown Voltage Vs. Temperature

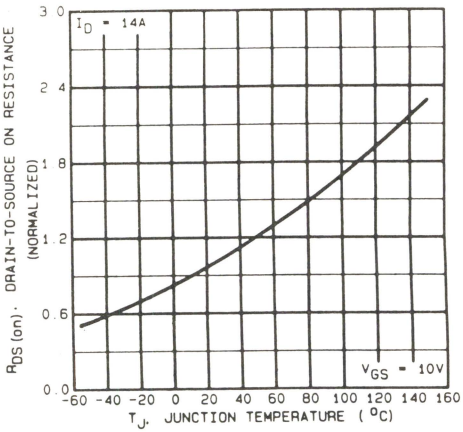


Fig. 9 — Normalized On-Resistance Vs. Temperature

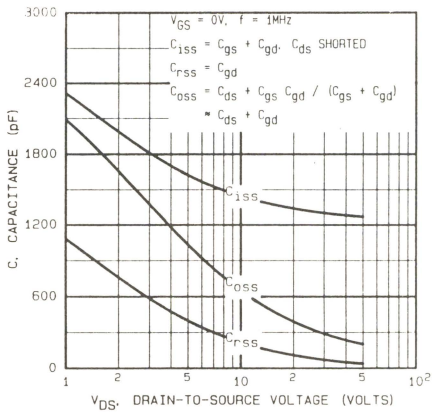


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

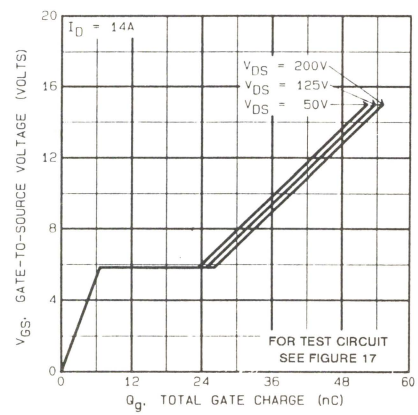


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

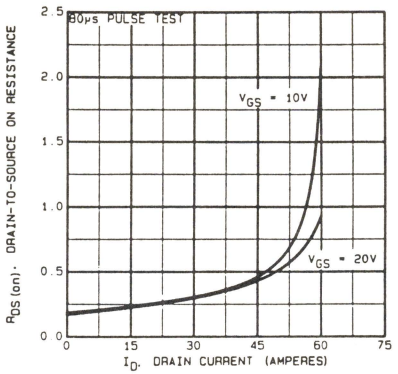


Figure 12 — Typical On Resistance Vs. Drain Current

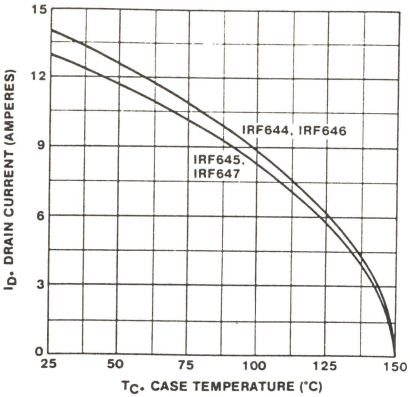


Figure 13 — Maximum Drain Current Vs. Case Temperature

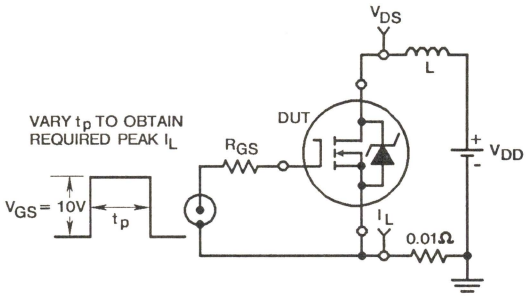


Figure 14 — Unclamped Energy Test Circuit

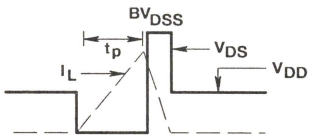


Figure 15 — Unclamped Energy Waveforms

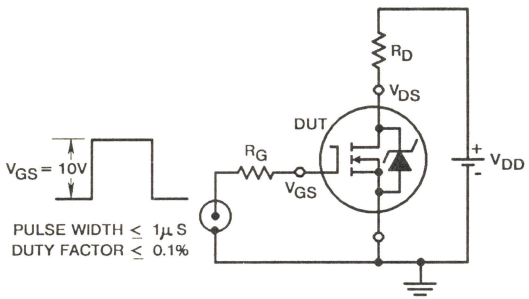


Figure16 — Switching Time Test Circuit

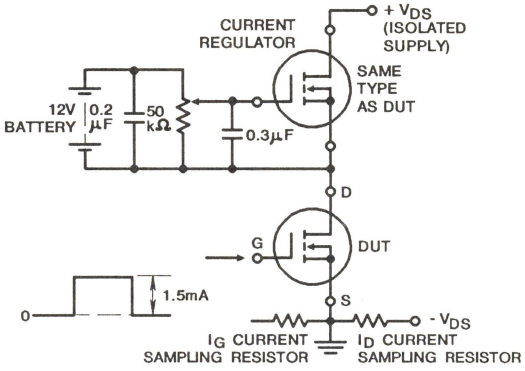


Figure 17 — Gate Charge Test Circuit

HARRIS

IRF710/711/712/713
IRF710R/711R/712R/713R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 1.7A and 2.0A, 350V - 400V
- $r_{DS}(on)$ = 3.6Ω and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

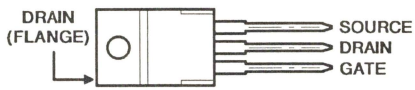
Description

The IRF710, IRF711, IRF712, and IRF713 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF710R, IRF711R, IRF712R and IRF713R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

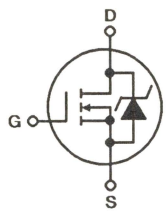
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF710 IRF710R	IRF711 IRF711R	IRF712 IRF712R	IRF713 IRF713R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	2	2	1.7	1.7	A
T_C = +100°C ..... I_D	1.2	1.2	1.1	1.1	A
Pulsed Drain Current (3) ..... I_{DM}	5	5	4.3	4.3	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	36	36	36	36	W
Linear Derating Factor	0.29	0.29	0.29	0.29	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	6.0	6.0	5.0	5.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	120	120	120	120	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 53mH, R_{GS} = 25Ω, I_{PEAK} = 2A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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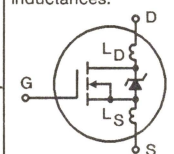
File Number **2310.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

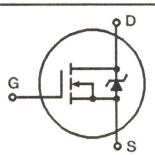
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF710/712, IRF710R/712R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRF711/713, IRF711R/713R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF710/711, IRF710R/711R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	2.0	–	–	A
IRF712/713, IRF712R/713R			1.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF710/711, IRF710R/711R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.1A	–	3.3	3.6	Ω
IRF712/713, IRF712R/713R			–	3.6	5.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 1.1A	1.0	1.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	35	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	8.0	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≃ 5.6A, R_G = 24Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8.0	12	ns
Rise Time	t_r		–	10	15	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	21	32	ns
Fall Time	t_f		–	11	17	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	7.0	12	nC
Gate-Source Charge	Q_{gs}		–	1.2	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	4.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	3.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	2.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	5.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.0A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 2.0A, dI_F/dt = 100A/µs	110	–	520	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 2.0A, dI_F/dt = 100A/µs	0.40	–	1.4	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 53mH, R_{GS} = 25Ω, I_{PEAK} = 2A (See Figure 15)

Performance Curves

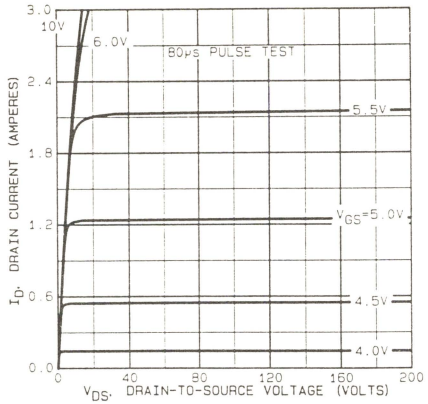


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

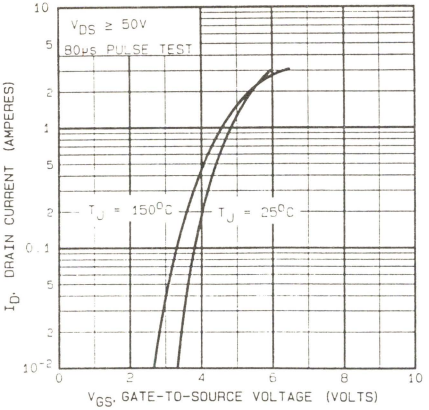


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

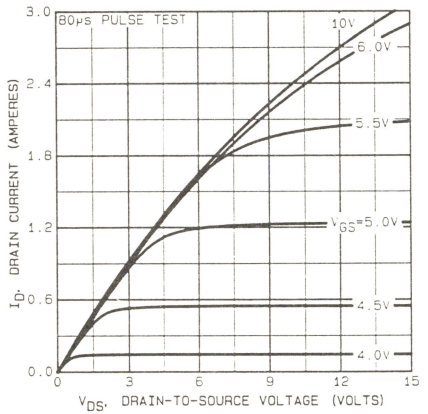


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

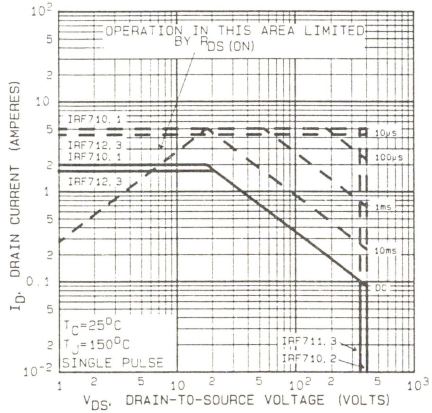


FIGURE 4. MAXIMUM SAFE OPERATING AREA

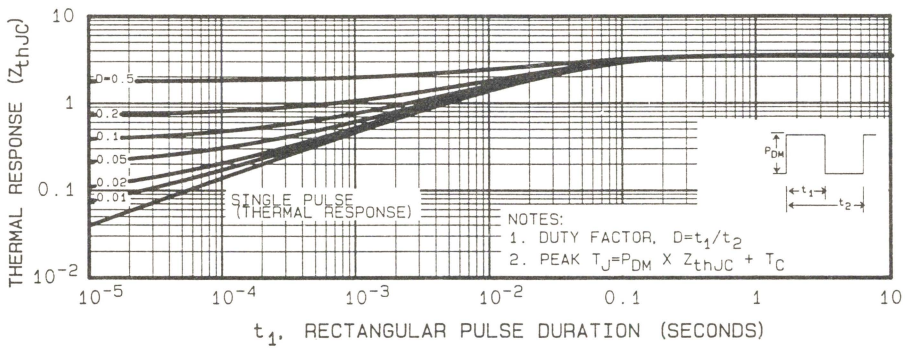


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

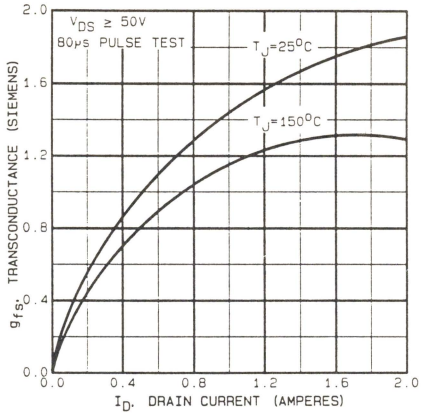


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

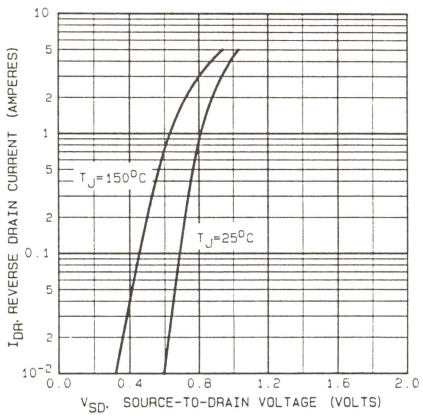


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

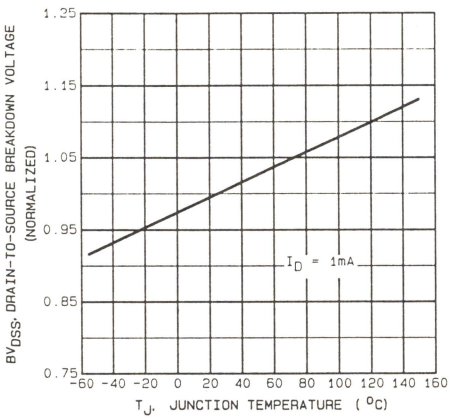


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

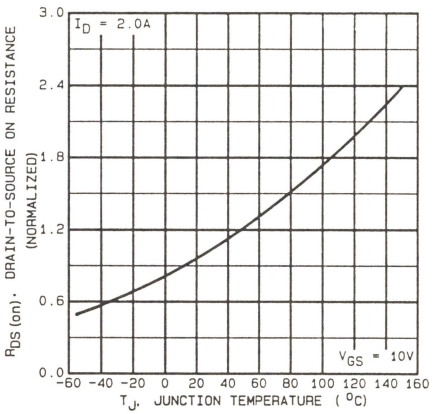


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

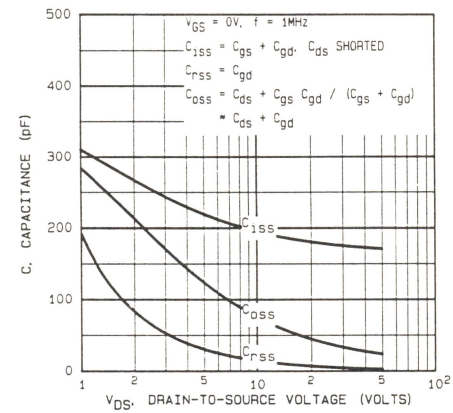


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

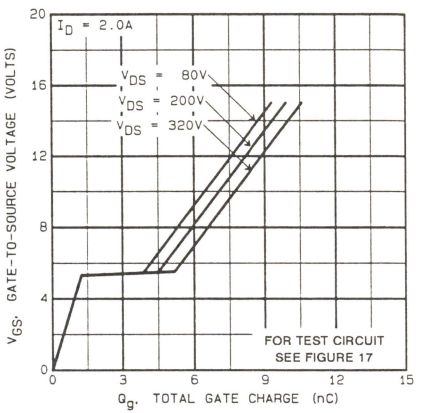


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

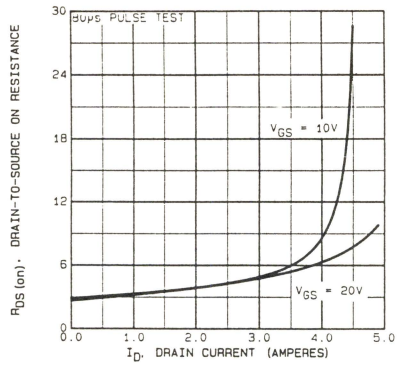


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

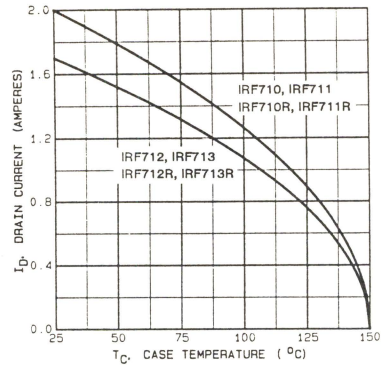


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

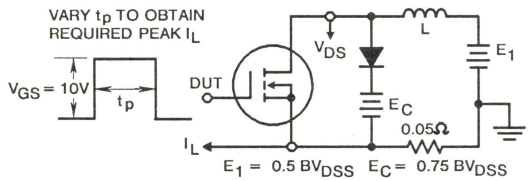


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

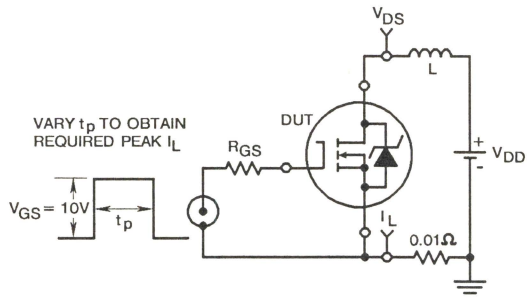


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

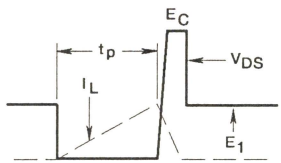


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

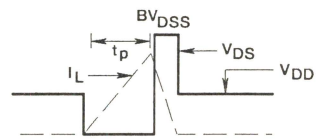


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

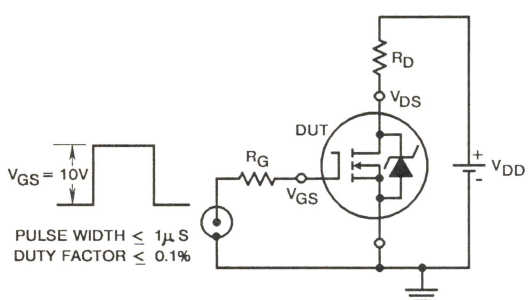


FIGURE 16. SWITCHING TIME TEST CIRCUIT

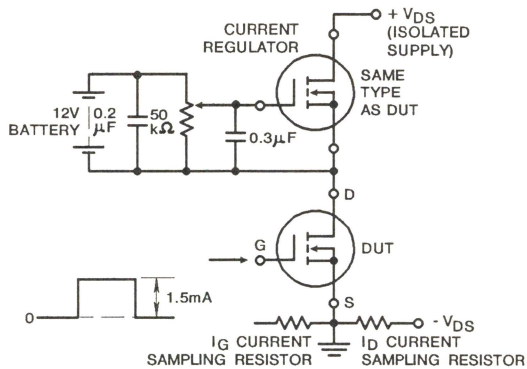


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF720/721/722/723
IRF720R/721R/722R/723R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.8A and 3.3A, 350V - 400V
- $r_{DS}(on)$ = 1.8Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

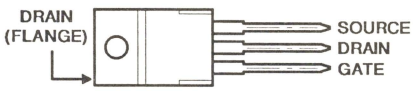
Description

The IRF720, IRF721, IRF722, and IRF723 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF720R, IRF721R, IRF722R and IRF723R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

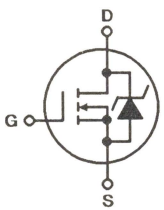
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF720 IRF720R	IRF721 IRF721R	IRF722 IRF722R	IRF723 IRF723R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	3.3	3.3	2.8	2.8	A
T_C = +100°C ..... I_D	2.1	2.1	1.8	1.8	A
Pulsed Drain Current (3) ..... I_{DM}	13	13	11	11	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	50	50	50	50	W
Linear Derating Factor	0.4	0.4	0.4	0.4	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	12	12	10	10	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	190	190	190	190	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 31mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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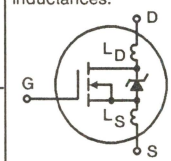
File Number 1579.1

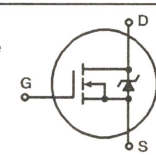
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF720/722, IRF720R/722R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
IRF721/723, IRF721R/723R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF720/721, IRF720R/721R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	3.3	–	–	A
IRF722/723, IRF722R/723R			2.8	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF720/721, IRF720R/721R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.8A	–	1.5	1.8	Ω
IRF722/723, IRF722R/723R			–	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 1.8A	1.8	2.7	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	360	–	pF
Output Capacitance	C_{OSS}		–	55	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D ≃ 3.3A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	15	ns
Rise Time	t_r		–	14	21	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	30	45	ns
Fall Time	t_f		–	13	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.3A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	12	20	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	3.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	13	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.3A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/μs	120	–	600	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 3.3A, dI_F/dt = 100A/μs	0.64	–	3.0	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 31mH, R_{GS} = 25Ω, I_{PEAK} = 3.3A (See Figure 15)

Performance Curves

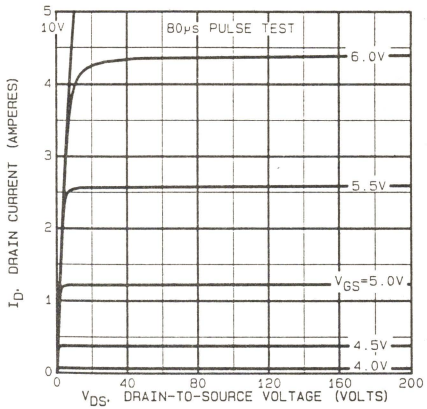


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

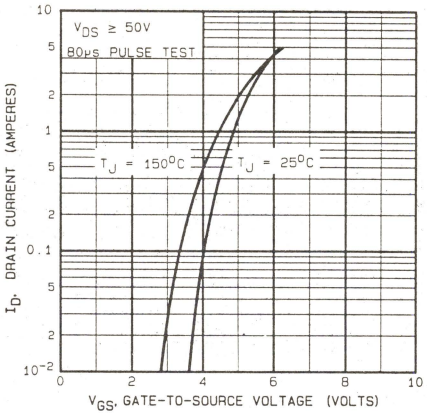


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

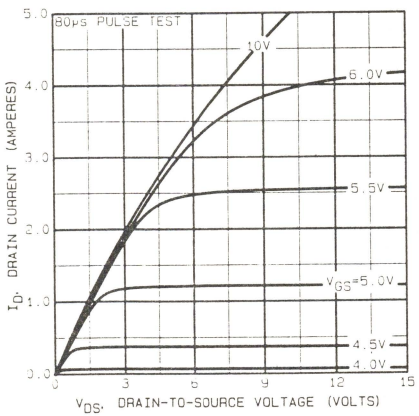


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

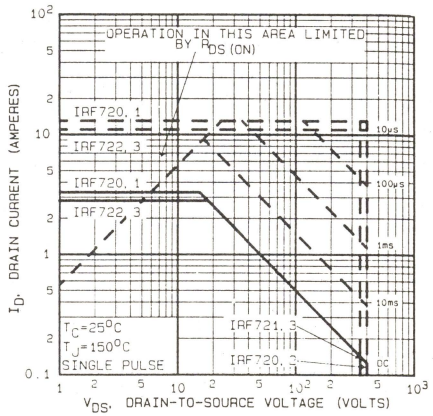


FIGURE 4. MAXIMUM SAFE OPERATING AREA

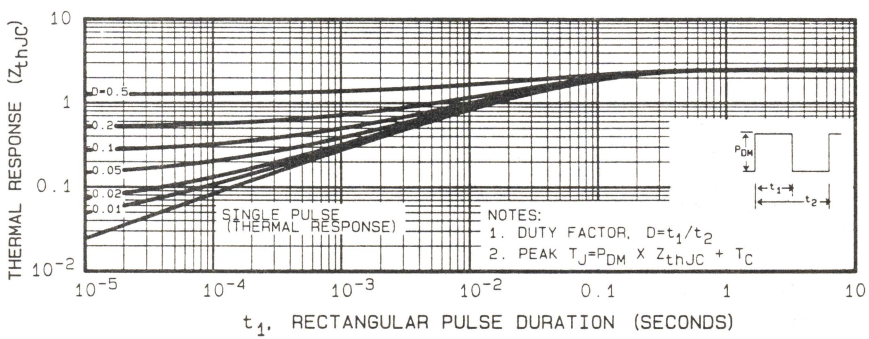


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

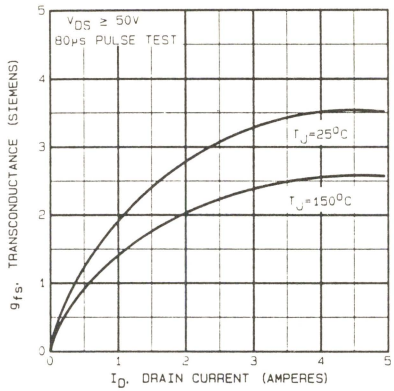


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

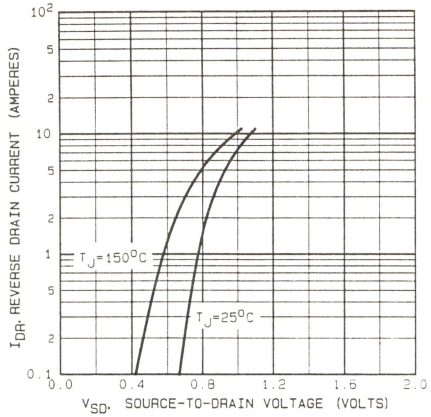


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

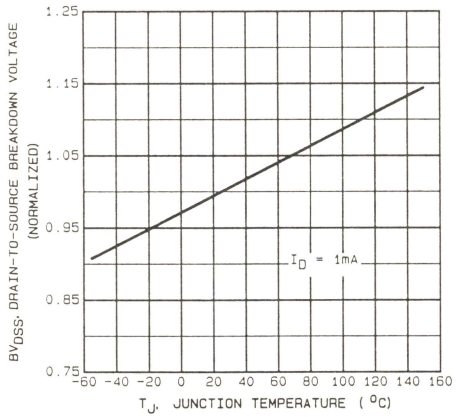


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

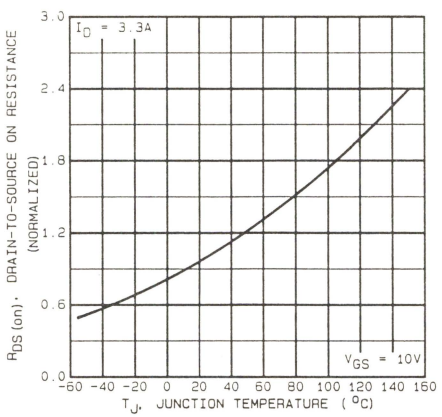


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

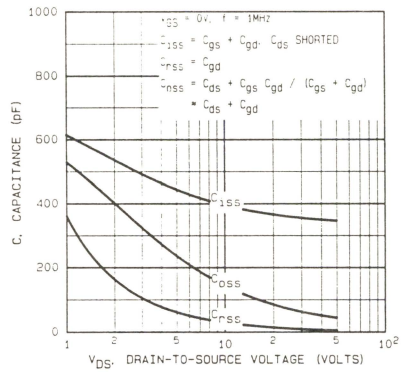


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

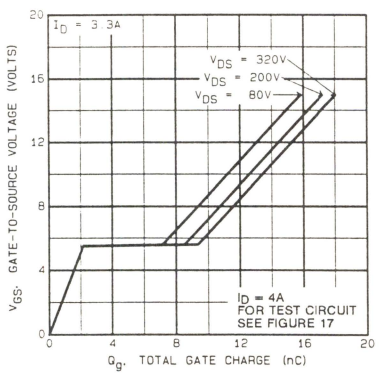


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

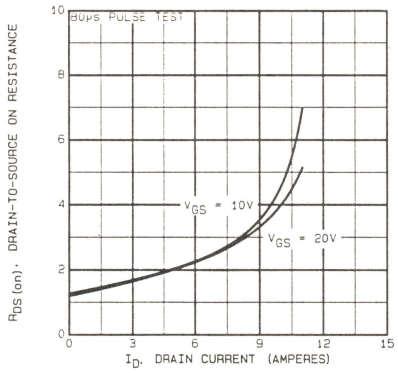


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

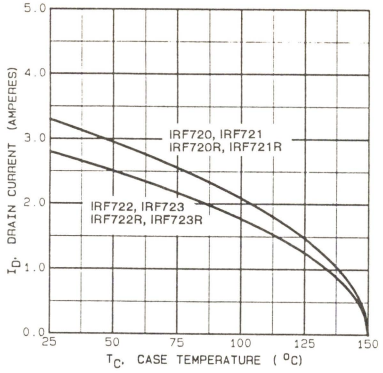


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

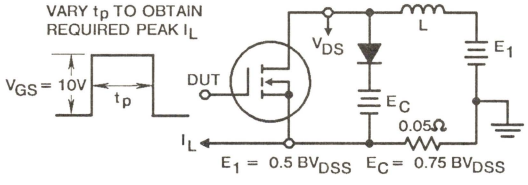


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

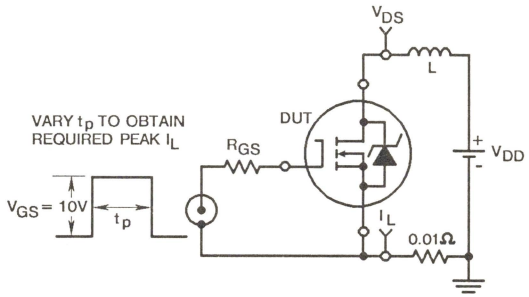


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

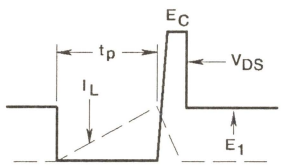


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

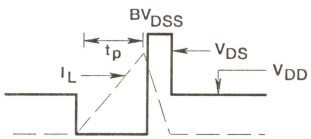


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

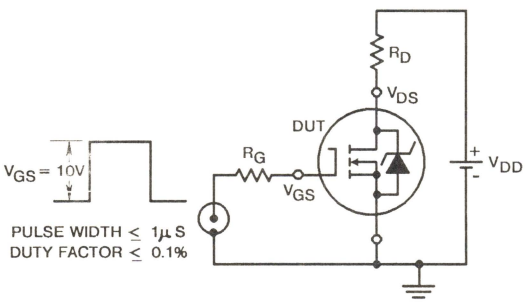


FIGURE 16. SWITCHING TIME TEST CIRCUIT

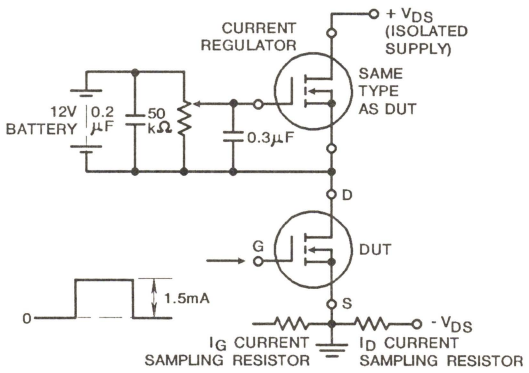


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF730/731/732/733
IRF730R/731R/732R/733R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.5A and 5.5A, 350V - 400V
- $r_{DS}(on)$ = 1.0Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

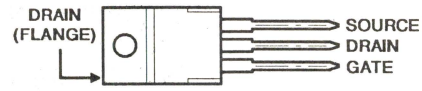
Description

The IRF730, IRF731, IRF732, and IRF733 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF730R, IRF731R, IRF732R and IRF733R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

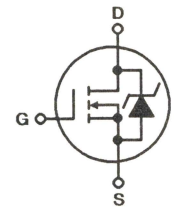
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF730 IRF730R	IRF731 IRF731R	IRF732 IRF732R	IRF733 IRF733R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	5.5	5.5	4.5	4.5	A
T_C = +100°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	22	22	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	22	22	18	18	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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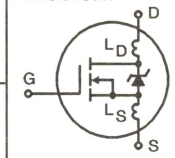
File Number **1580.1**

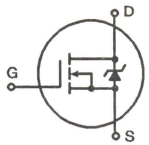
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF730/732, IRF730R/732R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRF731/733, IRF731R/733R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF730/731, IRF730R/731R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	5.5	–	–	A
IRF732/733, IRF732R/733R			4.5	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF730/731, IRF730R/731R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	–	0.8	1.0	Ω
IRF732/733, IRF732R/733R			–	1.0	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 3.0A	2.9	4.4	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	150	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, $I_D \simeq$ 5.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	17	ns
Rise Time	t_r		–	20	29	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	35	56	ns
Fall Time	t_f		–	15	24	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.5A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	20	35	nC
Gate-Source Charge	Q_{gs}		–	3.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	10	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	5.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	22	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.5A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	140	300	660	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 5.5A, dI_F/dt = 100A/µs	0.93	2.1	4.3	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17mH, R_{GS} = 25Ω, I_{PEAK} = 5.5A (See Figure 15)

Performance Curves

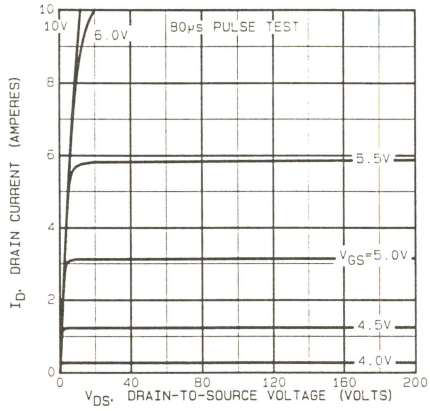


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

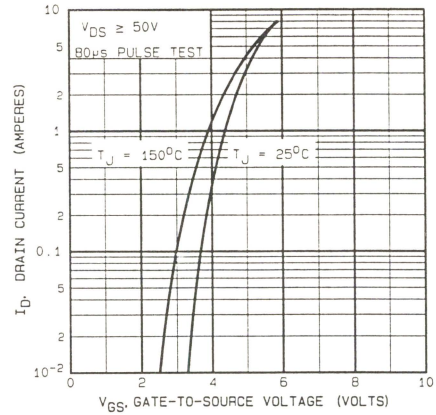


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

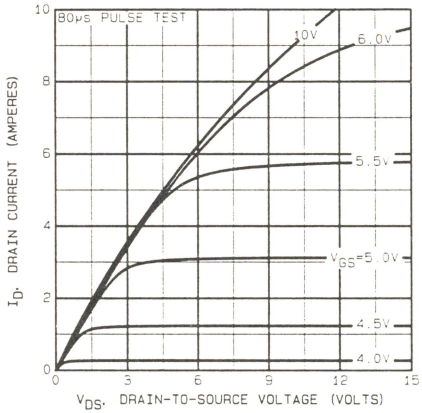


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

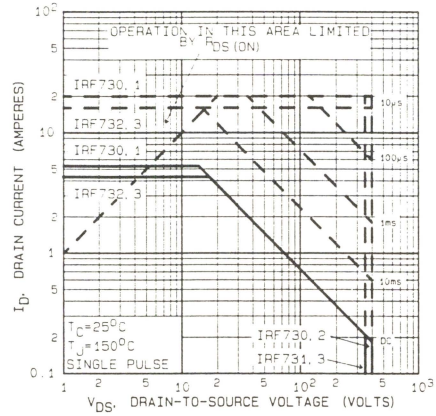


FIGURE 4. MAXIMUM SAFE OPERATING AREA

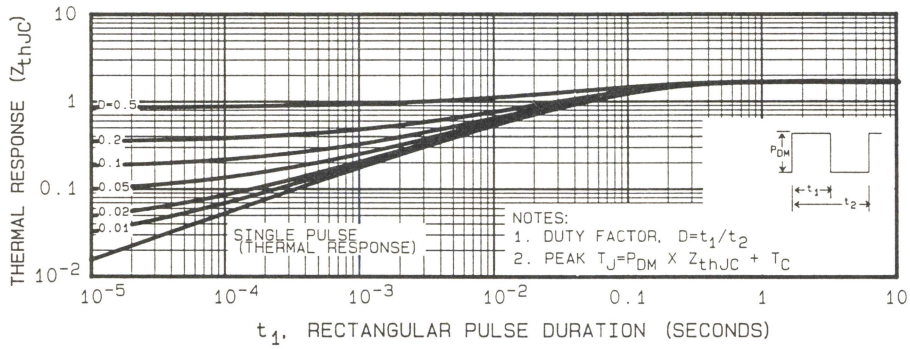


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

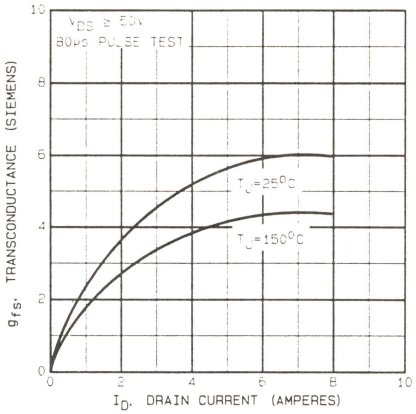


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

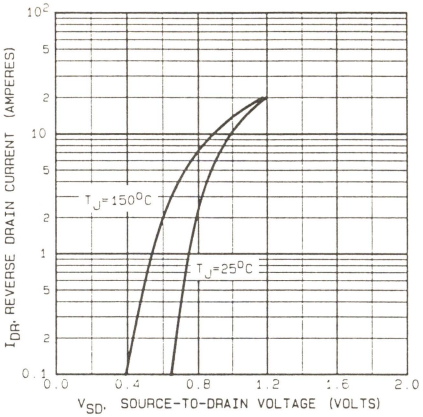


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

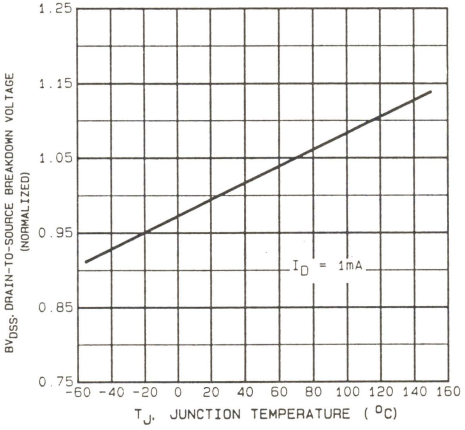


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

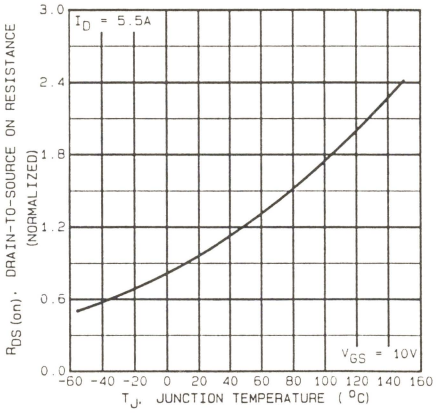


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

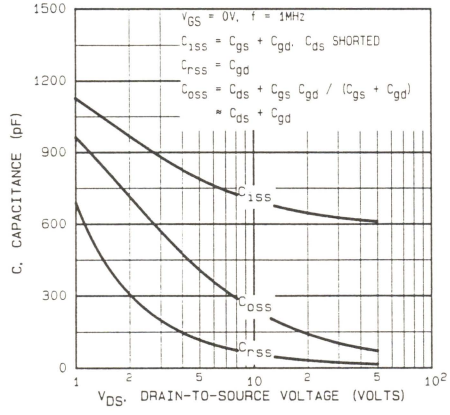


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

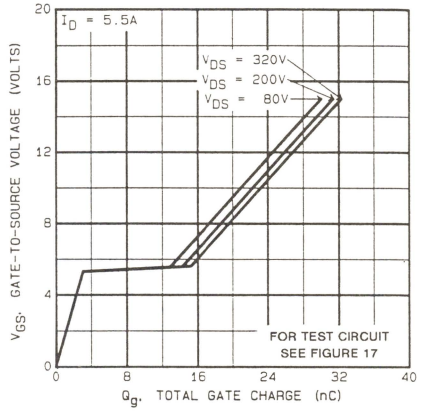


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

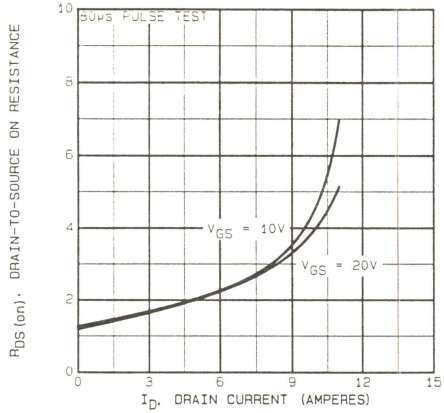


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

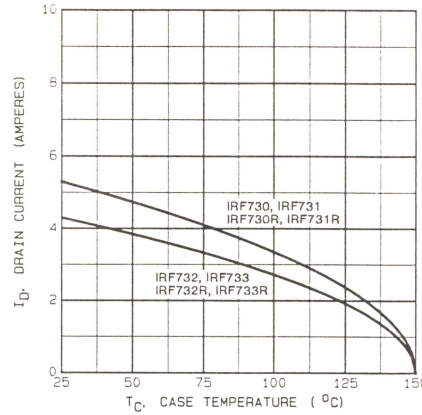


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

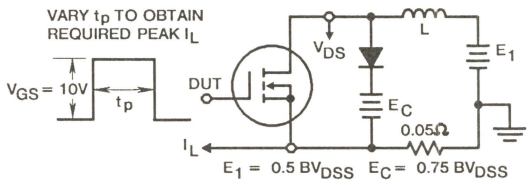


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

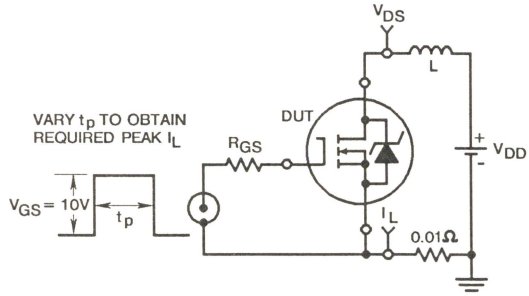


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

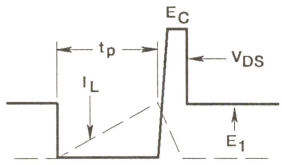


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

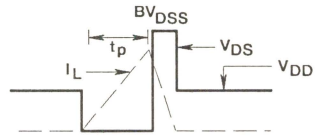


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

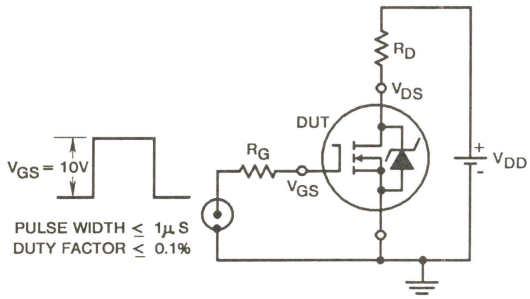


FIGURE 16. SWITCHING TIME TEST CIRCUIT

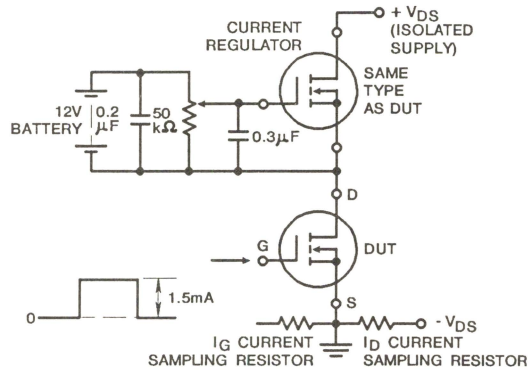


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRF740/741/742/743
IRF740R/741R/742R/743R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 8A and 10A, 350V - 400V
- $r_{DS}(on)$ = 0.55Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

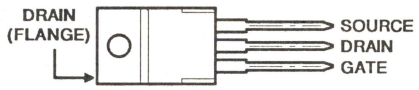
Description

The IRF740, IRF741, IRF742, and IRF743 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF740R, IRF741R, IRF742R and IRF743R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

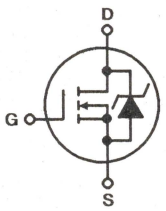
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF740 IRF740R	IRF741 IRF741R	IRF742 IRF742R	IRF743 IRF743R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	10	10	8.0	8.0	A
T_C = +100°C ..... I_D	6.3	6.3	5.2	5.2	A
Pulsed Drain Current (3) ..... I_{DM}	40	40	33	33	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	40	40	32	32	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	520	520	520	520	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 9.1mH, R_{GS} = 25Ω, I_{PEAK} = 10A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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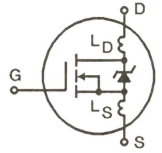
File Number **2311.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

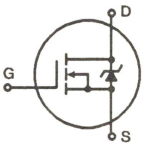
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF740/742, IRF740R/742R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
IRF741/743, IRF741R/743R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF740/741, IRF740R/741R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	10	–	–	A
IRF742/743, IRF742R/743R			8.3	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF740/741, IRF740R/741R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.2A	–	0.47	0.55	Ω
IRF742/743, IRF742R/743R			–	0.68	0.80	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 5.2A	5.8	8.9	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1250	–	pF
Output Capacitance	C_{OSS}		–	300	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 10A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	15	21	ns
Rise Time	t_r		–	25	41	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	52	75	ns
Fall Time	t_f		–	25	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	41	63	nC
Gate-Source Charge	Q_{gs}		–	6.5	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	23	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Modified MOSFET symbol showing the internal device inductances.



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	10	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	40	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 10A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	170	390	790	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	1.6	4.5	8.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.1mH, R_{GS} = 25Ω, I_{PEAK} = 10A (See Figure 15)

Performance Curves

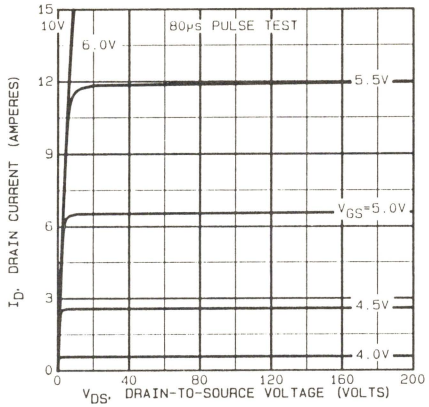


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

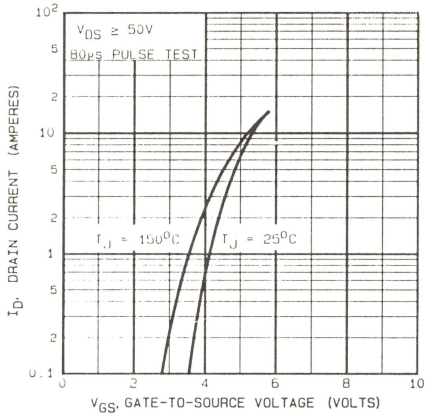


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

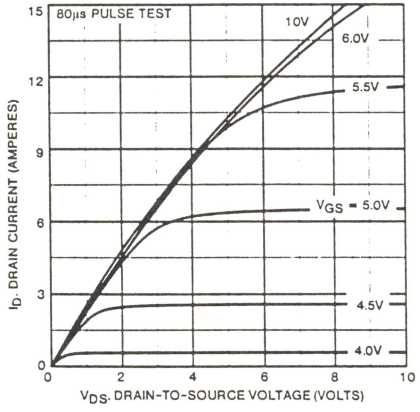


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

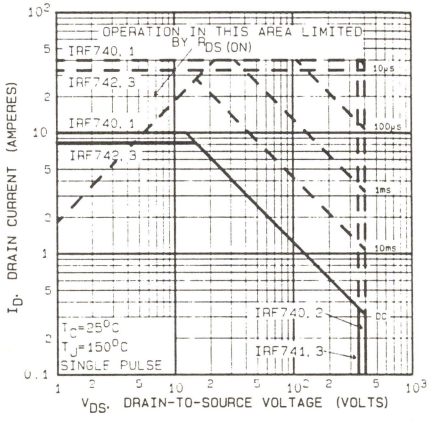


FIGURE 4. MAXIMUM SAFE OPERATING AREA

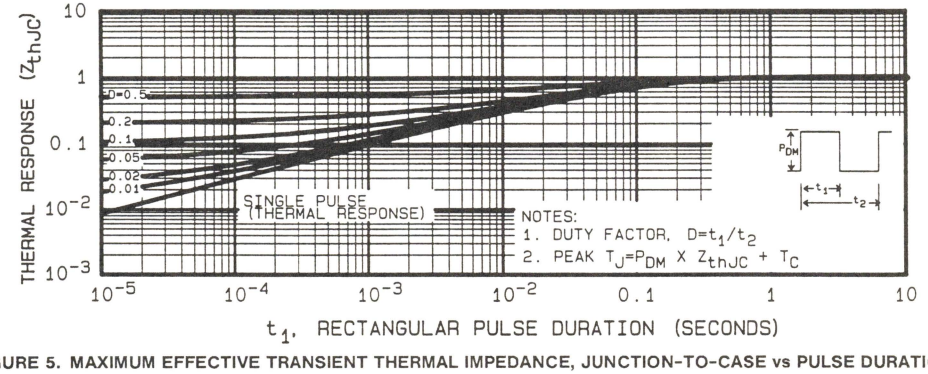


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

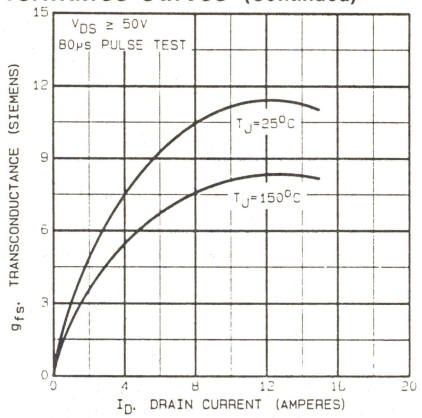


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

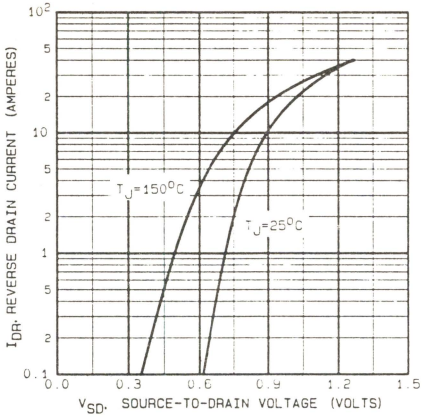


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

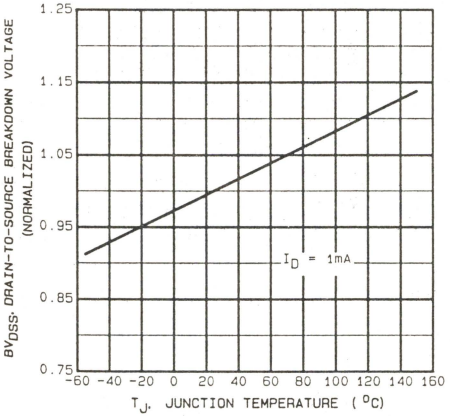


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

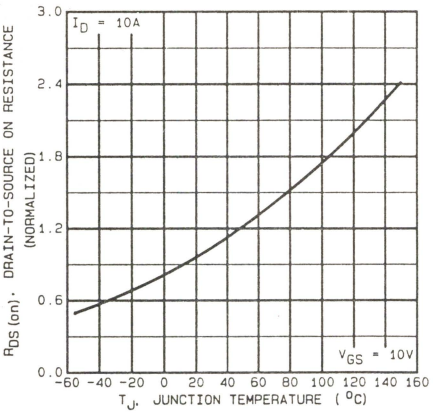


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

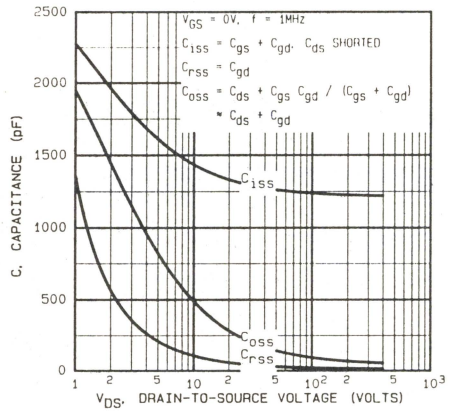


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

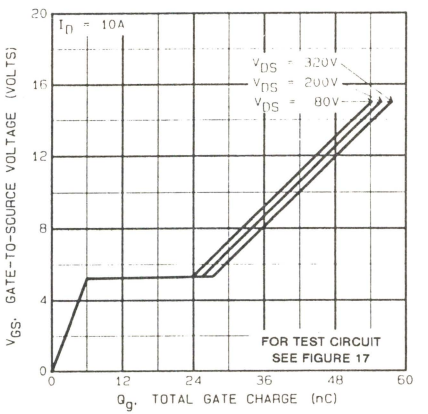


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

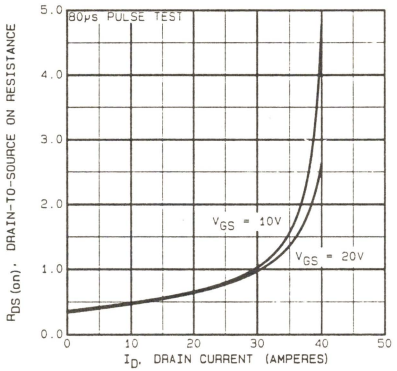


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

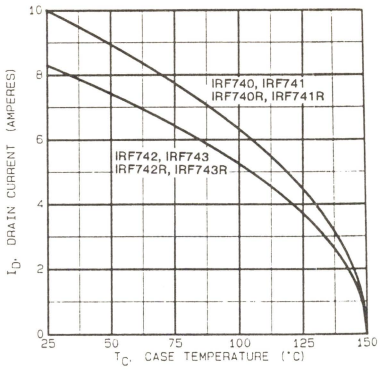


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

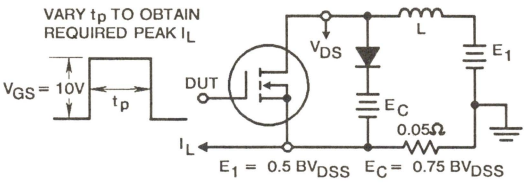


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

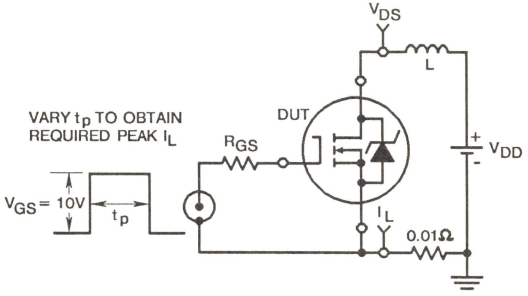


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

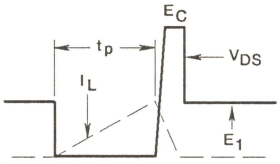


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

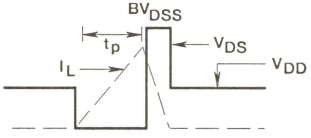


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

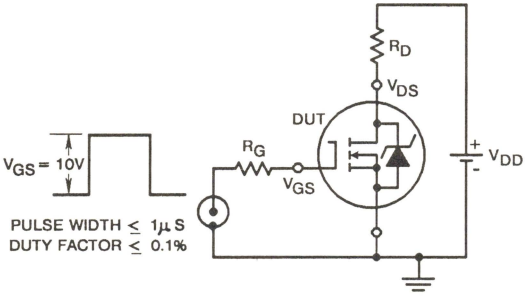


FIGURE 16. SWITCHING TIME TEST CIRCUIT

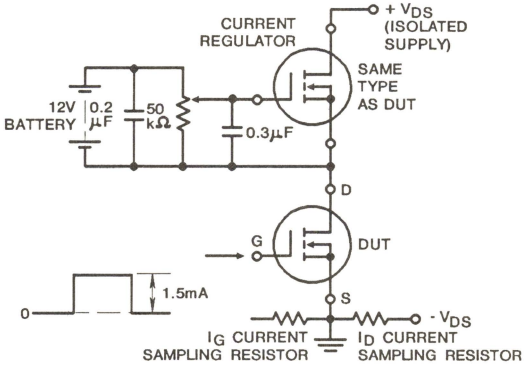


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF820/821/822/823
IRF820R/821R/822R/823R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.2 and 2.5A, 450V - 500V
- $r_{DS}(on)$ = 3.0Ω and 4.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

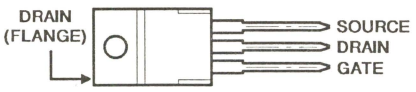
Description

The IRF820, IRF821, IRF822, and IRF823 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF820R, IRF821R, IRF822R and IRF823R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF820 IRF820R	IRF821 IRF821R	IRF822 IRF822R	IRF823 IRF823R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	2.5	2.5	2.0	2.0	A
T_C = +100°C ..... I_D	1.6	1.6	1.4	1.4	A
Pulsed Drain Current (3) ..... I_{DM}	8.0	8.0	7.0	7.0	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	50	50	50	50	W
Linear Derating Factor	0.40	0.40	0.40	0.40	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	10	10	8.0	8.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	210	210	210	210	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 60mH, R_{GS} = 25Ω, I_{PEAK} = 2.5A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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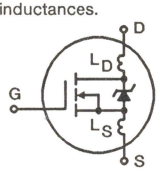
File Number **1581.1**

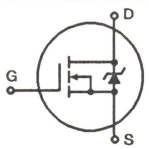
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF820/822, IRF820R/822R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	-	-	V
IRF821/823, IRF821R/823R			450	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRF820/821, IRF820R/821R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V	2.5	-	-	A
IRF822/823, IRF822R/823R			2.2	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF820/821, IRF820R/821R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.4A	-	2.5	3.0	Ω
IRF822/823, IRF822R/823R			-	3.0	4.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 1.4A	1.5	2.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	360	-	pF
Output Capacitance	C_{OSS}		-	60	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	10	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 2.5A, R_G = 18Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	11	15	ns
Rise Time	t_r		-	11	18	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	29	42	ns
Fall Time	t_f		-	12	18	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	12	19	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	6.0	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	2.5	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	8.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.5A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	130	300	540	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 2.5A, dI_F/dt = 100A/μs	0.57	1.4	2.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 60mH, R_{GS} = 25Ω, I_{PEAK} = 2.5A (See Figure 15)

Performance Curves

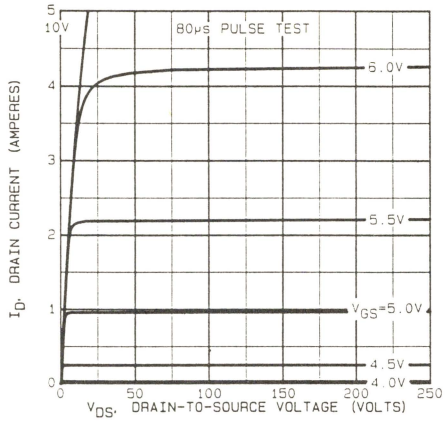


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

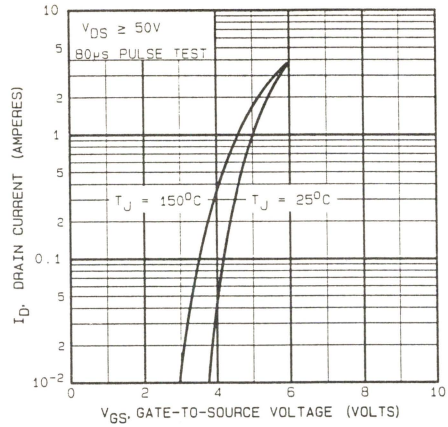


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

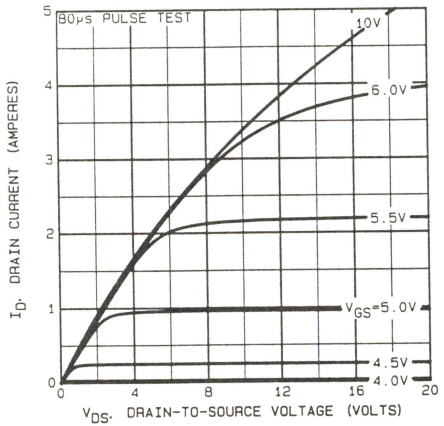


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

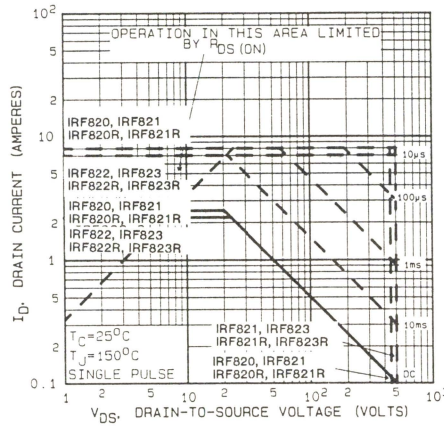


FIGURE 4. MAXIMUM SAFE OPERATING AREA

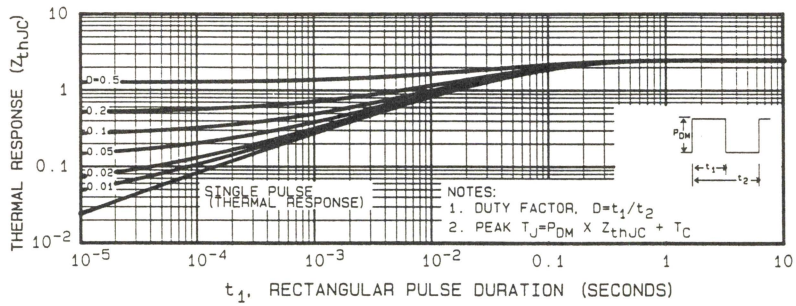


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

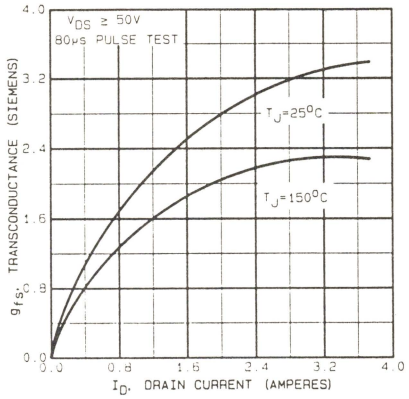


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

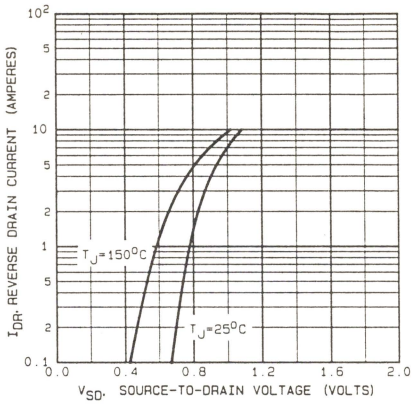


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

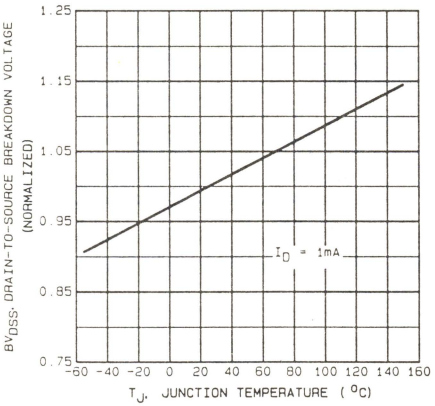


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

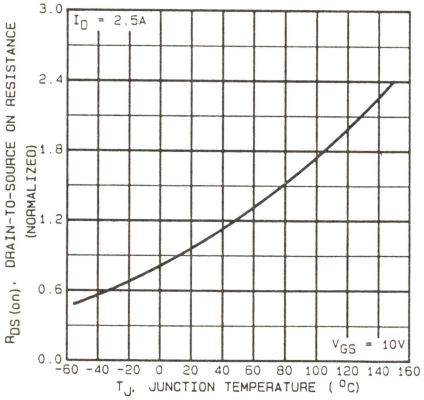


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

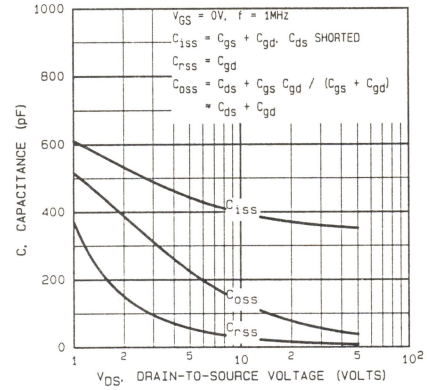


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

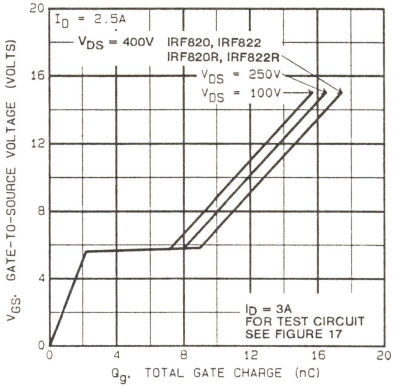


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

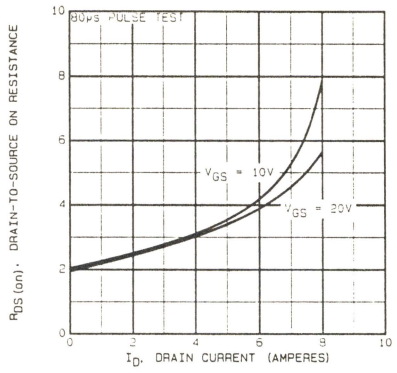


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

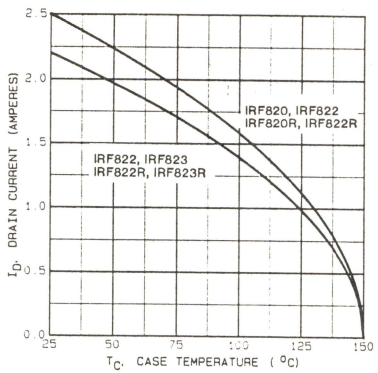


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

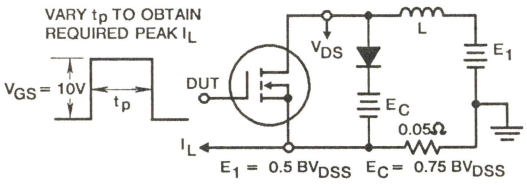


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

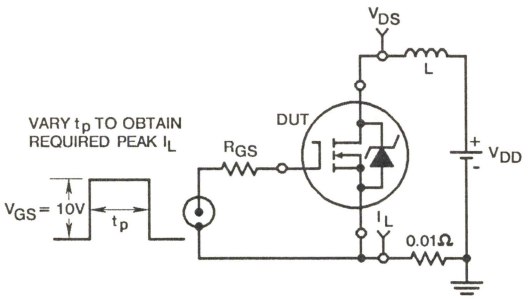


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

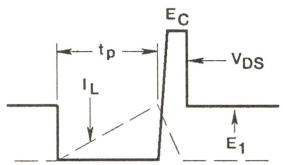


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

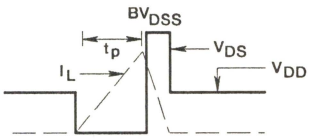


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

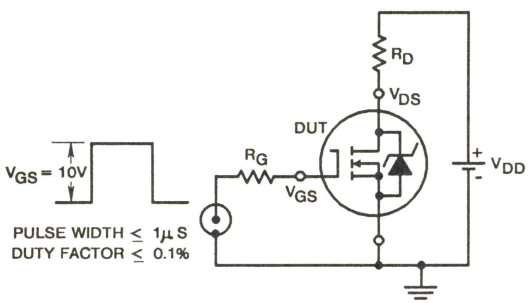


FIGURE 16. SWITCHING TIME TEST CIRCUIT

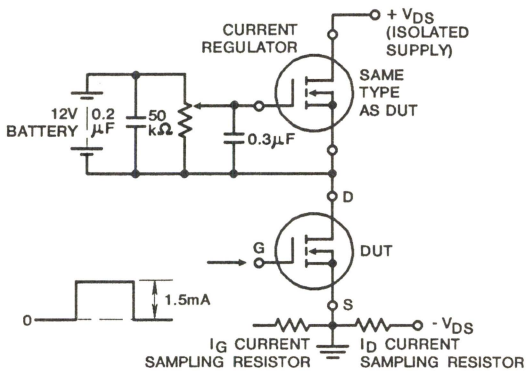


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRF830/831/832/833
IRF830R/831R/832R/833R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.0A and 4.5A, 450V - 500V
- $r_{DS}(on)$ = 1.5Ω and 2.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

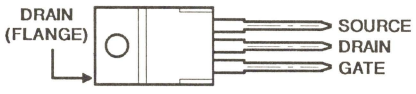
Description

The IRF830, IRF831, IRF832, and IRF833 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF830R, IRF831R, IRF832R and IRF833R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

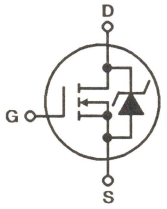
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF830 IRF830R	IRF831 IRF831R	IRF832 IRF832R	IRF833 IRF833R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	4.5	4.5	4.0	4.0	A
T_C = +100°C ..... I_D	3.0	3.0	2.5	2.5	A
Pulsed Drain Current (3) ..... I_{DM}	18	18	16	16	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	75	75	W
Linear Derating Factor	0.6	0.6	0.6	0.6	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	18	18	16	16	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 25mH, R_{GS} = 25Ω, I_{PEAK} = 4.5A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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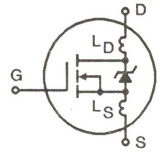
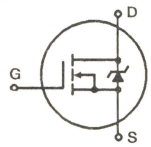
File Number **1582.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF830/832, IRF830R/832R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	500	–	–	V
IRF831/833, IRF831R/833R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRF830/831, IRF830R/831R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times R_{DS(ON)}$ Max, V_{GS} = 10V	4.5	–	–	A
IRF832/833, IRF832R/833R			4.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF830/831, IRF830R/831R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A	–	1.3	1.5	Ω
IRF832/833, IRF832R/833R			–	1.5	2.0	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 2.5A	2.7	4.2	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	100	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 4.5A, R_G = 12Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	17	ns
Rise Time	t_r		–	15	23	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	33	53	ns
Fall Time	t_f		–	16	23	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 4.5A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	22	32	nC
Gate-Source Charge	Q_{gs}		–	3.5	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	11	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die. 	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	4.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	18	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 4.5A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/μs	180	350	760	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 4.5A, dI_F/dt = 100A/μs	0.96	2.2	4.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 25mH, R_{GS} = 25Ω, I_{PEAK} = 4.5A (See Figure 15)

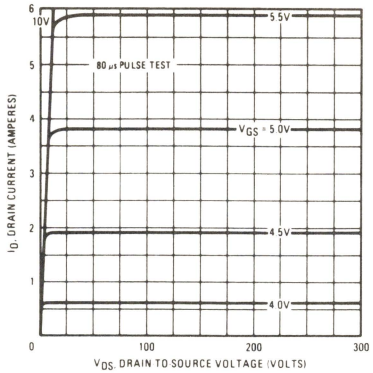


Fig. 1 – Typical Output Characteristics

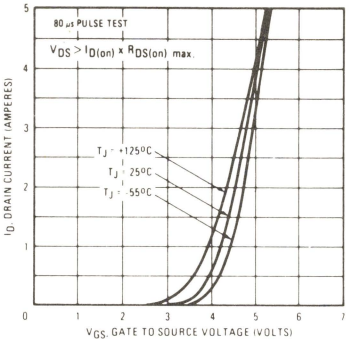


Fig. 2 – Typical Transfer Characteristics

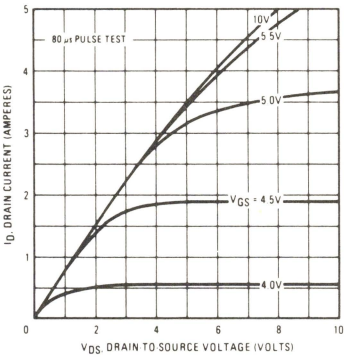


Fig. 3 – Typical Saturation Characteristics

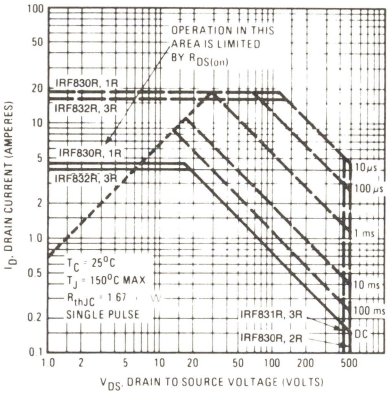


Fig. 4 – Maximum Safe Operating Area

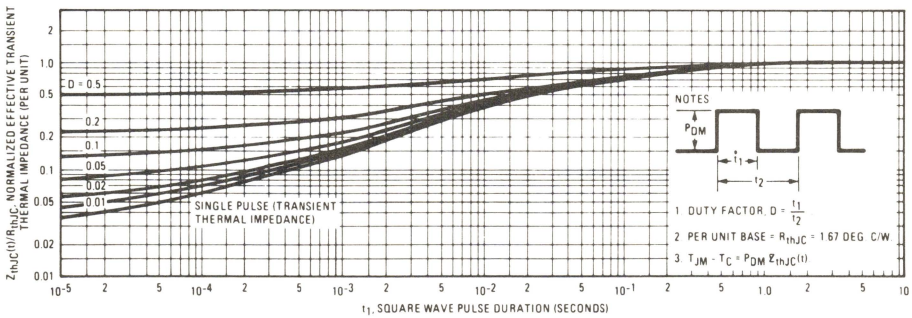


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

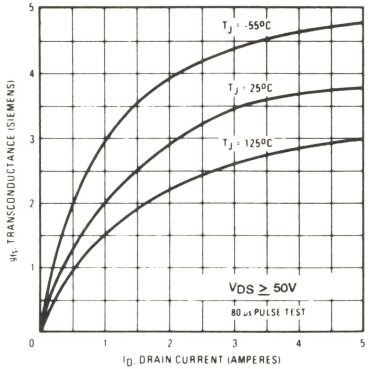


Fig. 6 – Typical Transconductance Vs. Drain Current

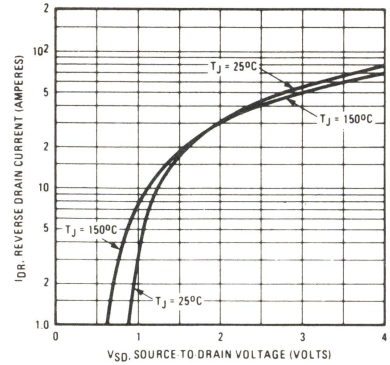


Fig. 7 – Typical Source-Drain Diode Forward Voltage

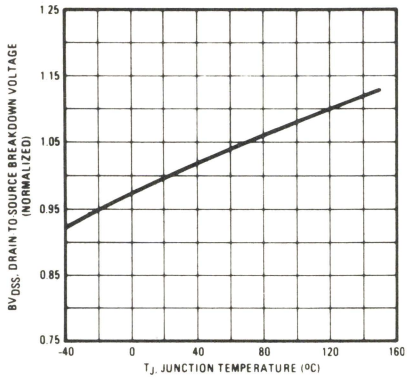


Fig. 8 – Breakdown Voltage Vs. Temperature

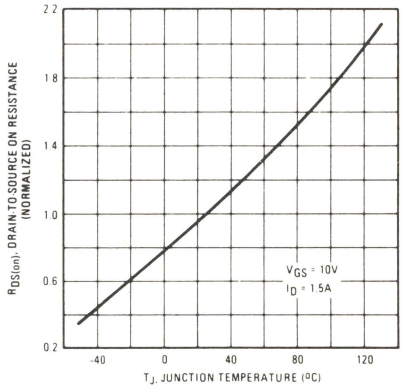


Fig. 9 – Normalized On-Resistance Vs. Temperature

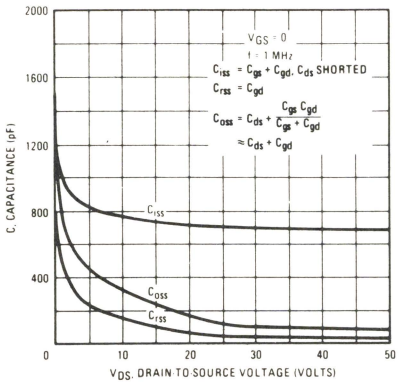


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

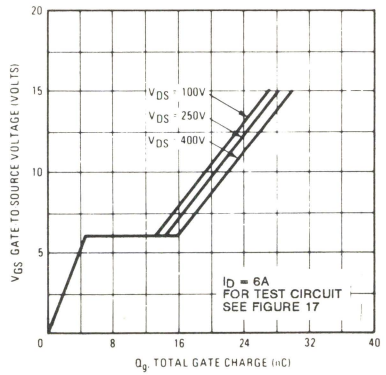


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

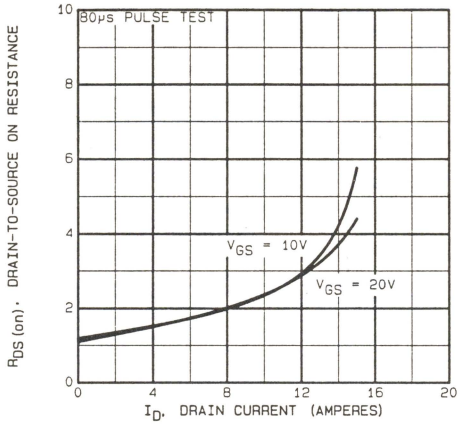


Fig. 12 — Typical On-Resistance Vs. Drain Current

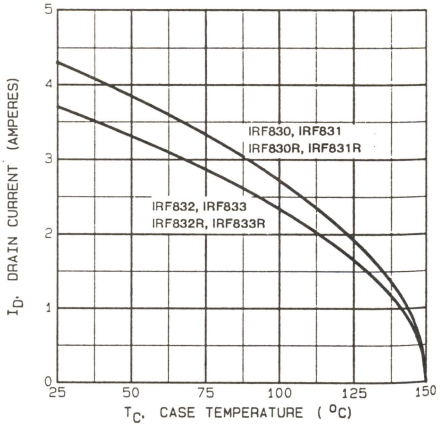


Fig. 13 — Maximum Drain Current Vs. Case Temperature

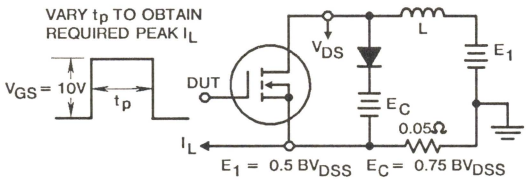


Fig. 14a — Clamped Inductive Test Circuit

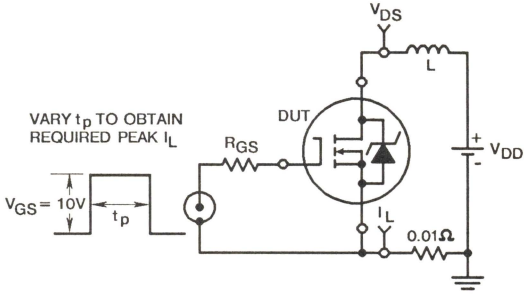


Fig. 15a — Unclamped Energy Test Circuit

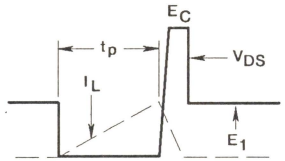


Fig. 14b — Clamped Inductive Waveforms

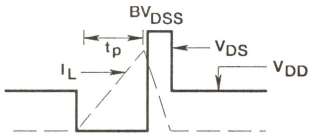


Fig. 15b — Unclamped Energy Waveforms

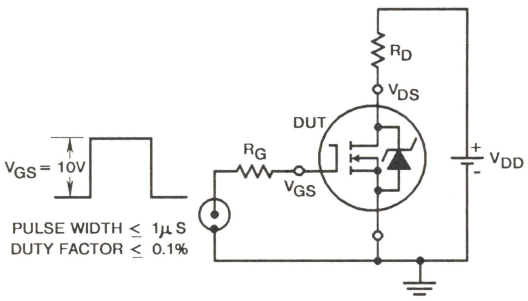


Fig. 16 — Switching Time Test Circuit

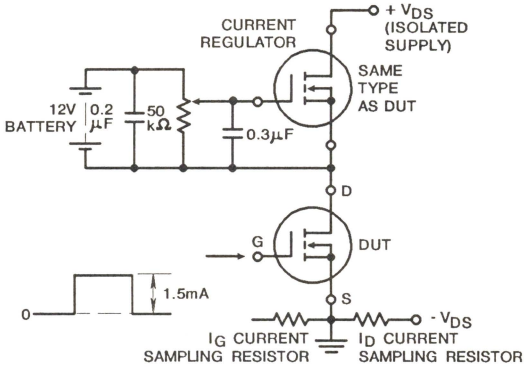


Fig. 17 — Gate Charge Test Circuit

HARRIS

IRF840/841/842/843
IRF840R/841R/842R/843R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 7A and 8A, 450V - 500V
- $r_{DS}(on)$ = 0.85Ω and 1.1Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

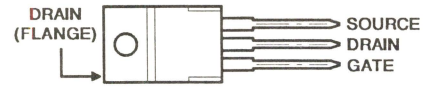
Description

The IRF840, IRF841, IRF842, and IRF843 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF840R, IRF841R, IRF842R and IRF843R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

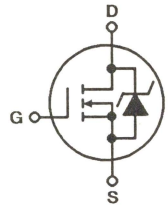
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRF840 IRF840R	IRF841 IRF841R	IRF842 IRF842R	IRF843 IRF843R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.0	8.0	7.0	7.0	A
T_C = +100°C ..... I_D	5.1	5.1	4.4	4.4	A
Pulsed Drain Current (3) ..... I_{DM}	32	32	28	28	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	32	32	28	28	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	510	510	510	510	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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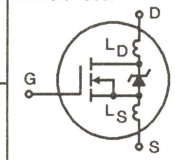
File Number **2312.1**

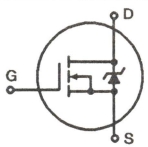
Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF840/842, IRF840R/842R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRF841/843, IRF841R/843R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRF840/841, IRF840R/841R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times R_{DS(ON)}$ Max, V_{GS} = 10V	8.0	–	–	A
IRF842/843, IRF842R/843R			7.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRF840/841, IRF840R/841R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.4A	–	0.8	0.85	Ω
IRF842/843, IRF842R/843R			–	1.0	1.1	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 4.4A	4.9	7.4	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1225	–	pF
Output Capacitance	C_{OSS}		–	200	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	85	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, $I_D \simeq$ 8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	15	21	ns
Rise Time	t_r		–	21	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	74	ns
Fall Time	t_f		–	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	42	63	nC
Gate-Source Charge	Q_{gs}		–	7.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	22	–	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	–	3.5	–	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	–	4.5	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	7.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	1.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.5	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	–	–	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.0A, V_{GS} = 100A/µs	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	210	475	970	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	2.0	4.6	8.2	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 14mH, R_{GS} = 25Ω, I_{PEAK} = 8A (See Figure 15)

Performance Curves

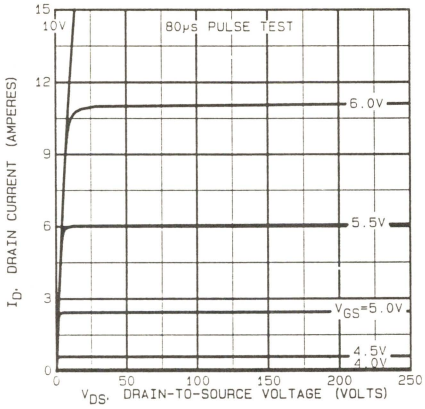


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

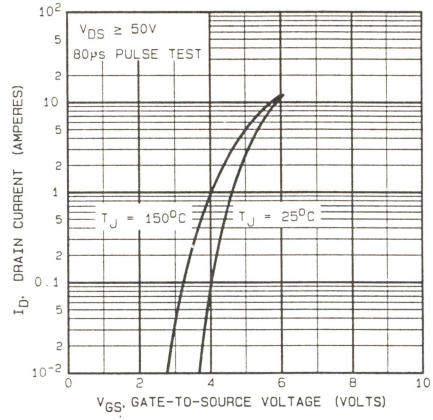


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

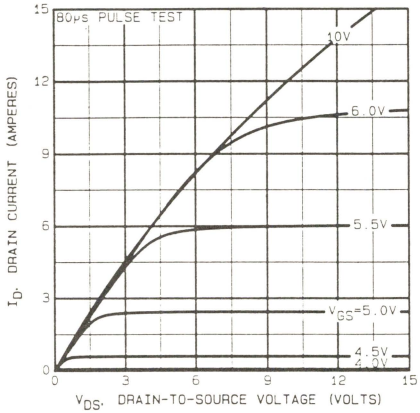


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

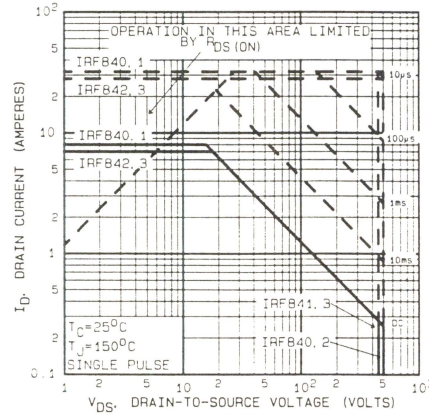


FIGURE 4. MAXIMUM SAFE OPERATING AREA

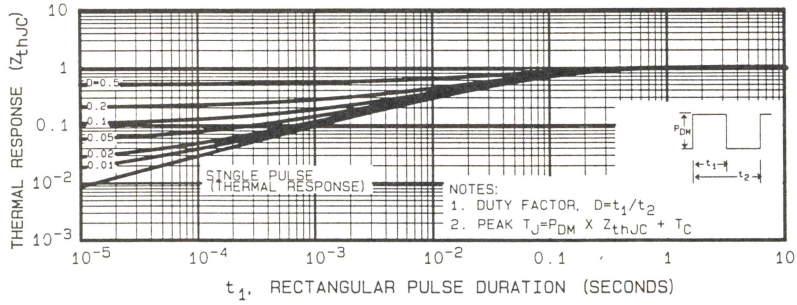


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

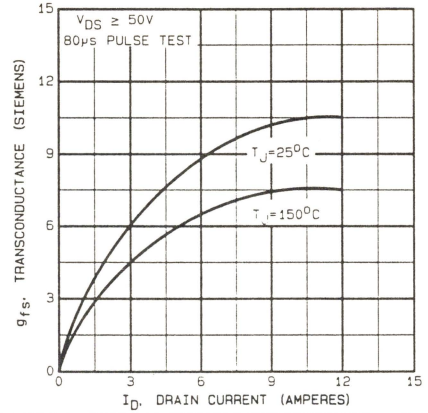


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

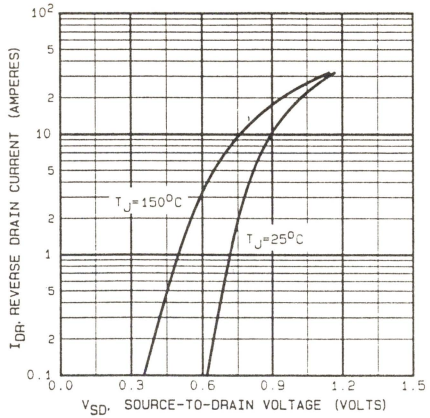


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

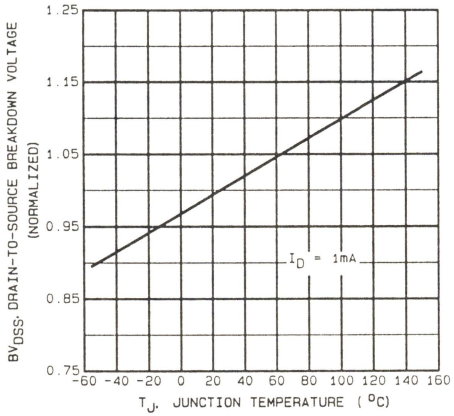


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

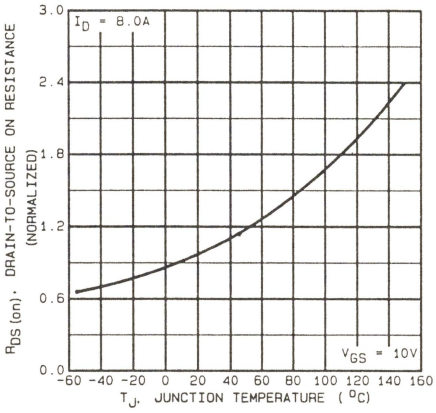


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

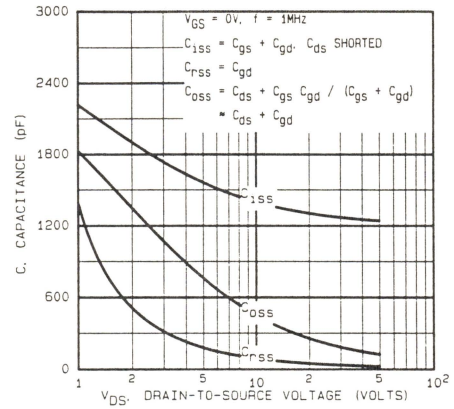


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

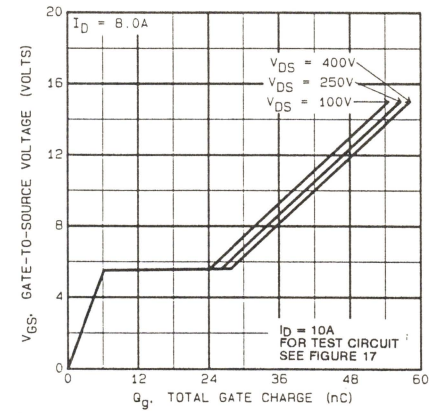


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

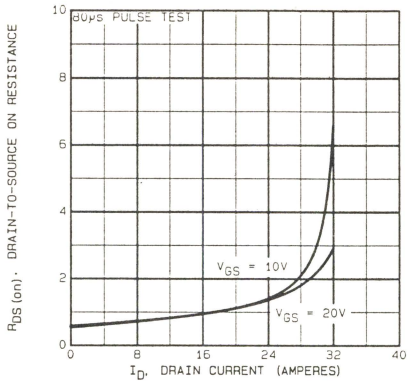


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

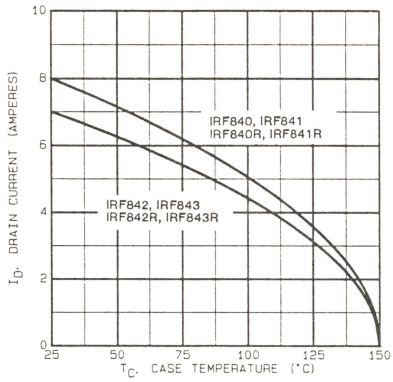


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

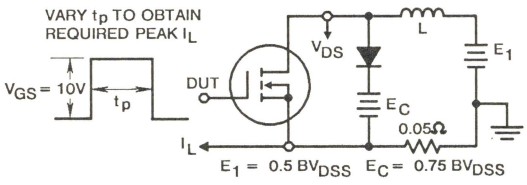


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

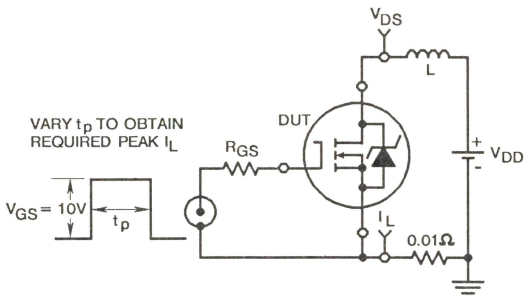


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

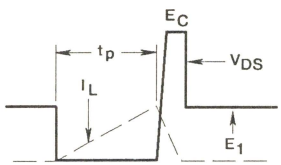


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

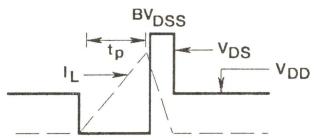


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

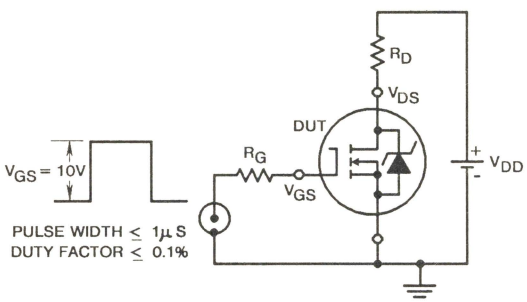


FIGURE 16. SWITCHING TIME TEST CIRCUIT

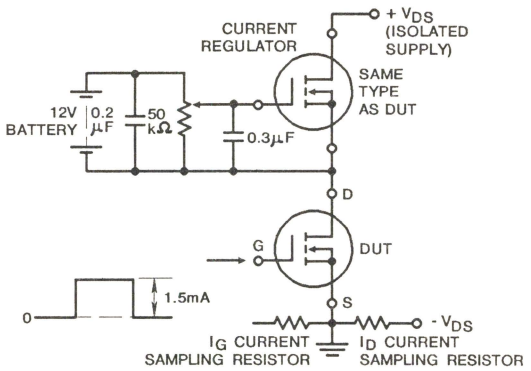


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFAC40R
IRFAC42R

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 6.2A and 5.4A, 600V
- $r_{DS(on)}$ = 1.2Ω and 1.6Ω
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

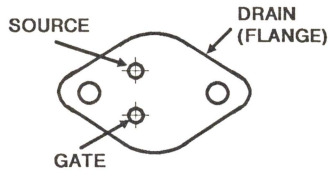
Description

The IRFAC40R and IRFAC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFAC types are supplied in the JEDEC TO-204AA steel package.

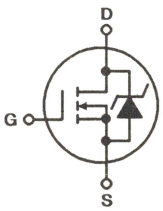
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFAC40R	IRFAC42R	UNITS
Continuous Drain Current			
T_C = +25°C ..... I_D	6.2	5.4	A
T_C = +100°C ..... I_D	3.9	3.4	A
Pulsed Drain Current (1) ..... I_{DM}	25	22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = +25°C ..... P_D	125	125	W
Linear Derating Factor	1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (2) (see Figure 14) ..... E_{as}	570	570	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	°C

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature (see Figure 5).
2. V_{DD} = 50V, Starting T_J = +25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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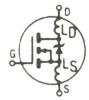
File Number **2156.1**

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFAC40R	600	—	—	V	V_{GS} = 0V, I_D = 250μA
		IRFAC42R					
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFAC40R	—	0.97	1.2	Ω	V_{GS} = 10V, I_D = 3.4A
		IRFAC42R	—	1.2	1.6		
$I_{D(on)}$	On-State Drain Current ③	IRFAC40R	6.2	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
		IRFAC42R	5.4				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	4.7	70	—	S(℧)	$V_{DS} \geq$ 50V, I_{DS} = 3.4A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	40	60	nC	V_{GS} = 10V, I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	ALL	—	5.5	—	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	20	—	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	13	20	ns	V_{DD} = 300V, I_D = 6.2A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	18	27	ns	R_D = 47Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f	Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal inductances.



C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	160	—	pF	f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.12	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	°C/W	Typical-socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifer.
I_{SM}	Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	450	940	ns	T_J = 25°C, I_F = 6.2A, di/dt = 100A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.8	3.8	7.9	μC	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

③ Pulse width ≤ 300μs; Duty Cycle ≤ 2%

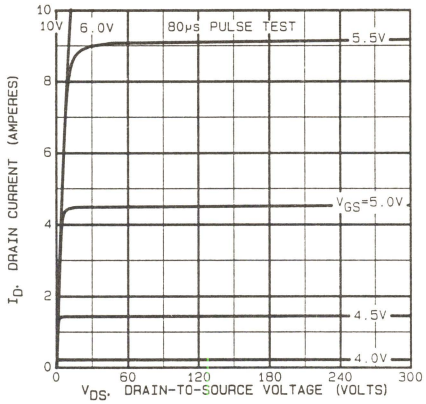


Fig. 1 - Typical Output Characteristics

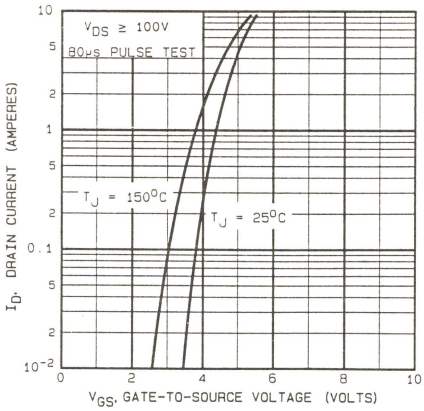


Fig. 2 - Typical Transfer Characteristics

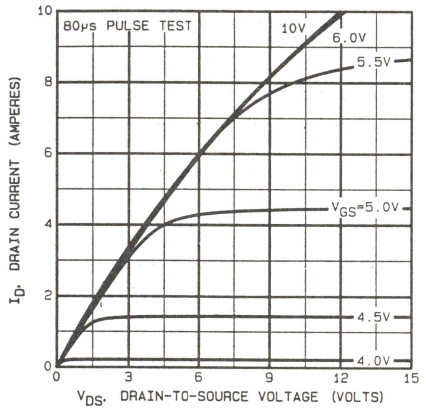


Fig. 3 - Typical Saturation Characteristics

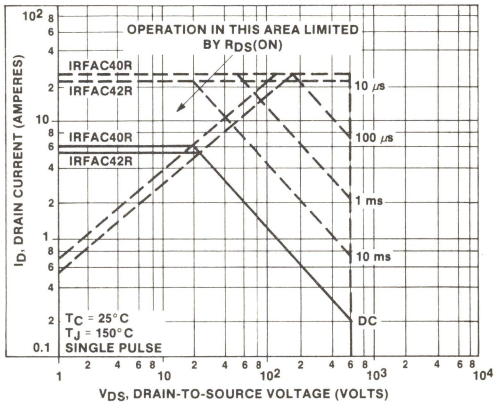


Fig. 4 - Maximum Safe Operating Area

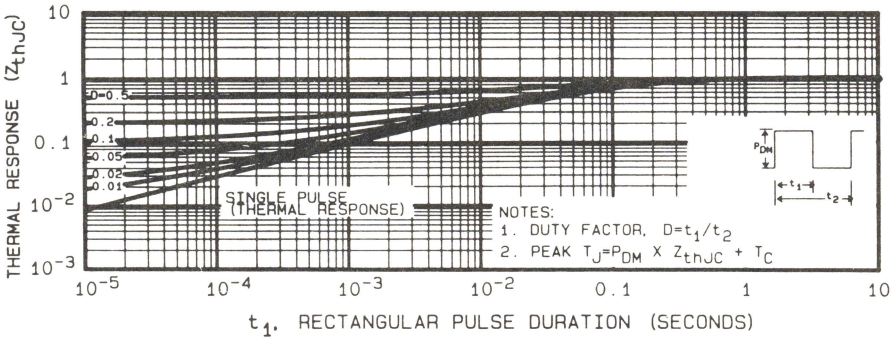


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

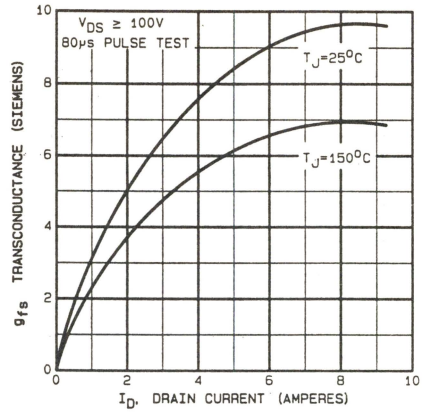


Fig. 6 - Typical Transconductance Vs. Drain Current

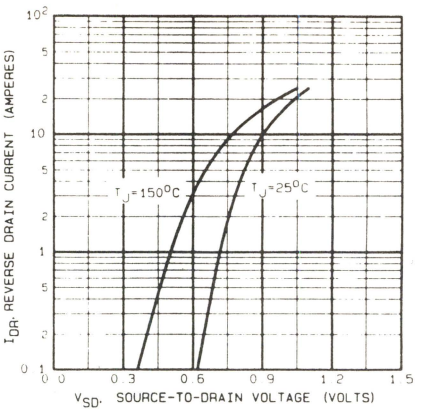


Fig. 7 - Typical Source-Drain Diode Forward Voltage

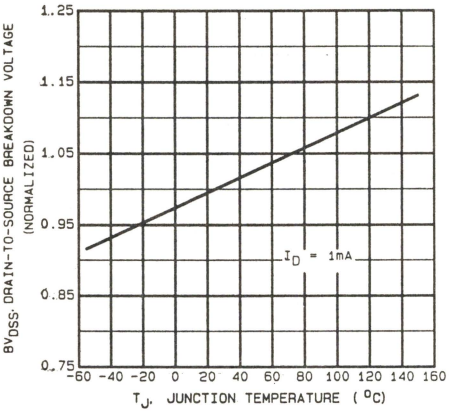


Fig. 8 - Breakdown Voltage Vs. Temperature

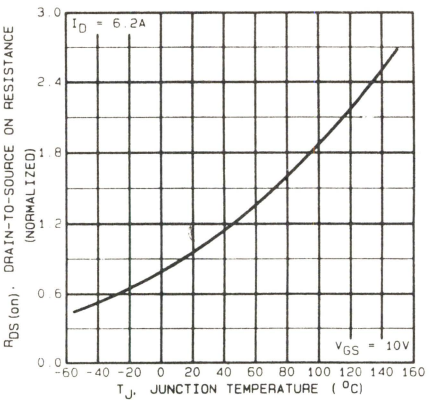


Fig. 9 - Normalized On-Resistance Vs. Temperature

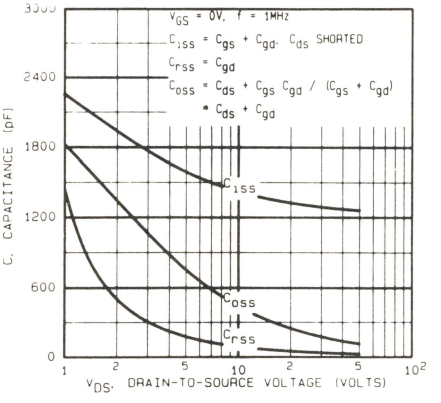


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

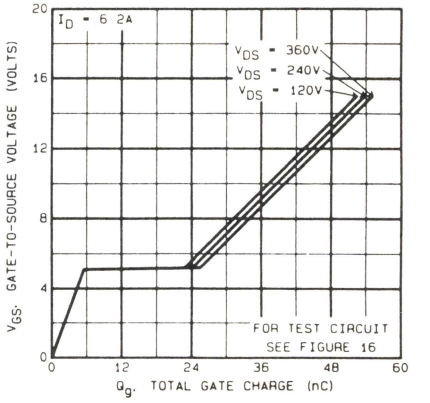


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

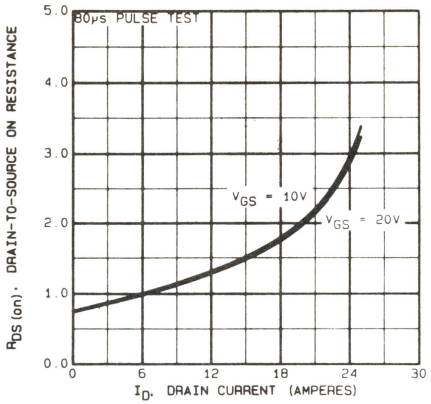


Fig. 12 - Typical On-Resistance Vs. Drain Current

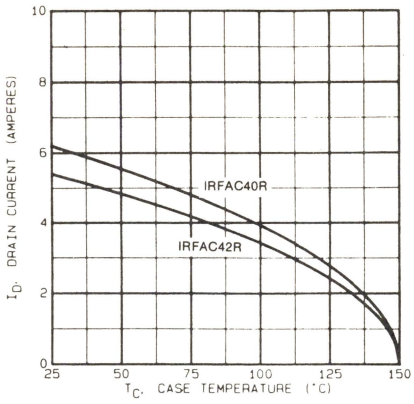


Fig. 13 - Maximum Drain Current Vs. Case Temperature

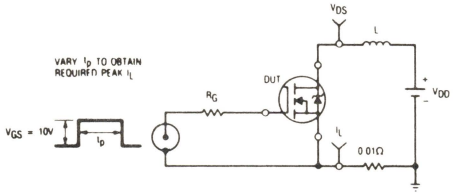


Fig. 14a - Unclamped Inductive Test Circuit

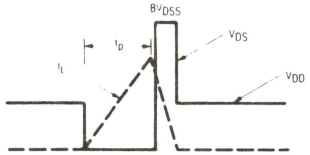


Fig. 14b - Unclamped Inductive Waveforms

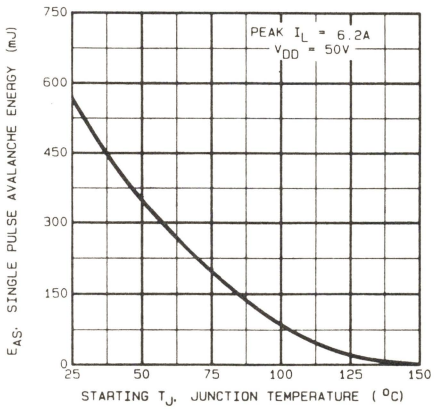


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

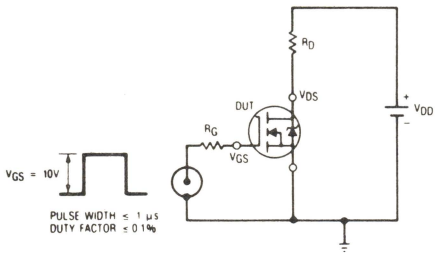


Fig. 15a - Switching Time Test Circuit

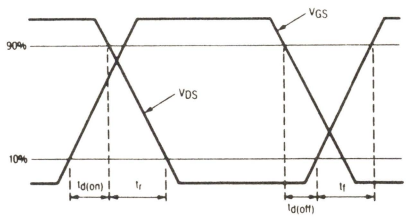


Fig. 15b - Switching Time Waveforms

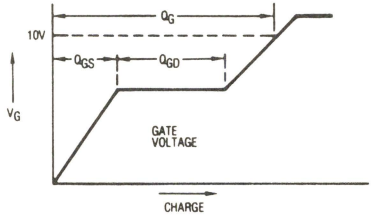
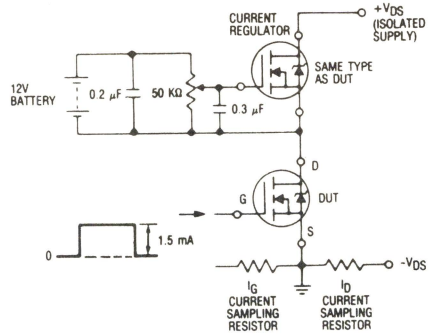


Fig. 16a - Basic Gate Charge Waveform



Fib. 16b - Gate Charge Test Circuit

HARRIS

IRFBC40R
IRFBC42R

N-Channel Power MOSFETs
Avalanche Energy Rated

August 1991

Features

- 6.2A and 5.4A, 600V
- $r_{DS(on)}$ = 1.2Ω and 1.6Ω
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

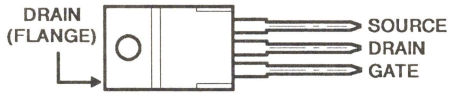
Description

The IRFBC40R and IRFBC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFAC types are supplied in the JEDEC TO-220AB steel package.

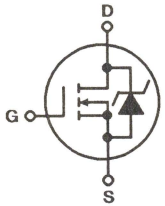
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFBC40R	IRFBC42R	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	6.2	5.4	A
T_C = +100°C	I_D	3.9	3.4	A
Pulsed Drain Current (1)	I_{DM}	25	22	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	125	125	W
Linear Derating Factor		1.0	1.0	W/°C
Single Pulse Avalanche Energy Rating (2) (see Figure 14)	E_{as}	570	570	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature (see Figure 5).
2. V_{DD} = 50V, Starting T_J = +25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2157.1

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFBC40R IRFBC42R	600	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFBC40R	—	0.97	1.2	Ω	V_{GS} = 10V, I_D = 3.4A
		IRFBC42R	—	1.2	1.6		
$I_{D(on)}$	On-State Drain Current ③	IRFBC40R	6.2	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
		IRFBC42R	5.4				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	4.7	70	—	S(℧)	$V_{DS} \geq$ 100V, I_{DS} = 3.4A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	40	60	nC	V_{GS} = 10V, I_D = 6.2A
Q_{gs}	Gate-to-Source Charge	ALL	—	5.5	—	nC	V_{DS} = 0.7 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	20	—	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	13	20	ns	V_{DD} = 300V, I_D = 6.2A, R_G = 9.1Ω
t_r	Rise Time	ALL	—	18	27	ns	R_D = 47Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	55	83	ns	See Fig. 15
t_f	Fall Time	ALL	—	20	30	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
							Modified MOSFET symbol showing the internal inductances.
C_{iss}	Input Capacitance	ALL	—	1300	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	160	—	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	45	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.50	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	°C/W	Typical-socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	6.2	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ①	ALL	—	—	25	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.5	V	T_J = 25°C, I_S = 6.2A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	450	940	ns	T_J = 25°C, I_F = 6.2A, di/dt = 100A/μs
Q_{RR}	Reverse Recovery Charge	ALL	1.8	3.8	8.0	μC	
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① **Repetitive Rating: Pulse width limited by maximum junction temperature (see figure 5).**

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

③ Pulse width ≤ 300μs; Duty Cycle ≤ 2%

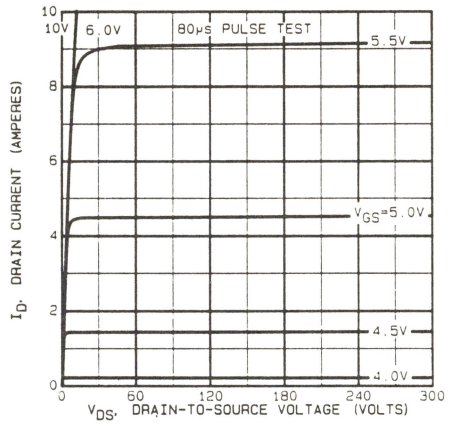


Fig. 1 - Typical Output Characteristics

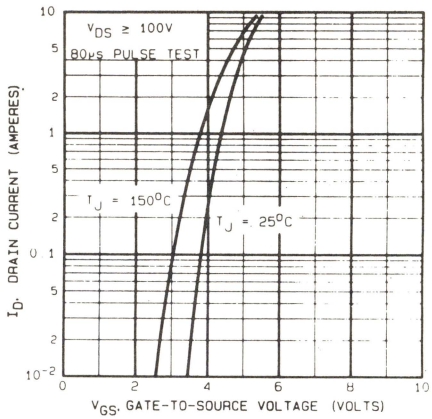


Fig. 2 - Typical Transfer Characteristics

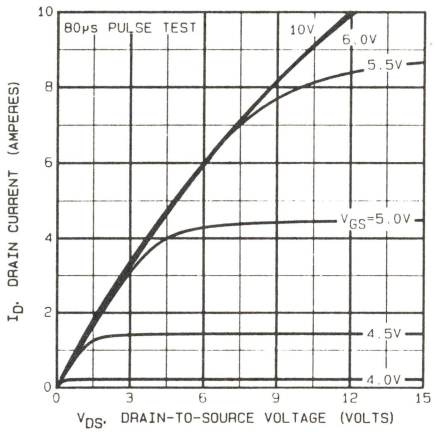


Fig. 3 - Typical Saturation Characteristics

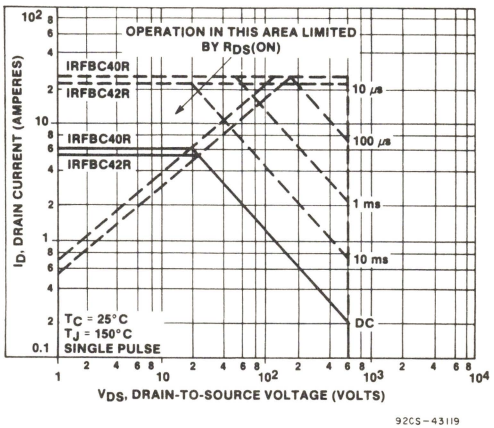


Fig. 4 - Maximum Safe Operating Area

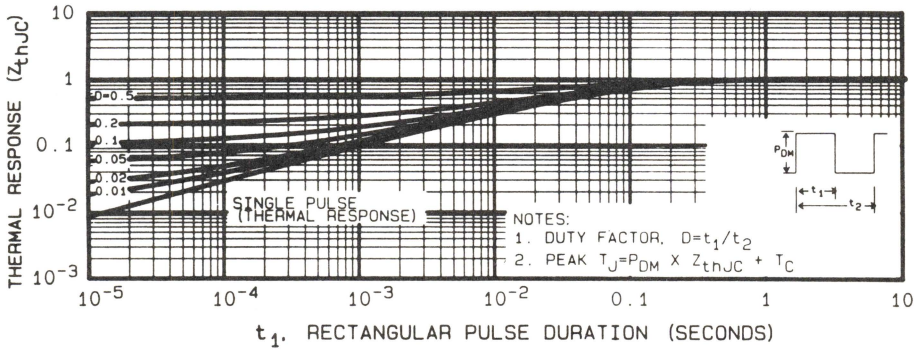


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

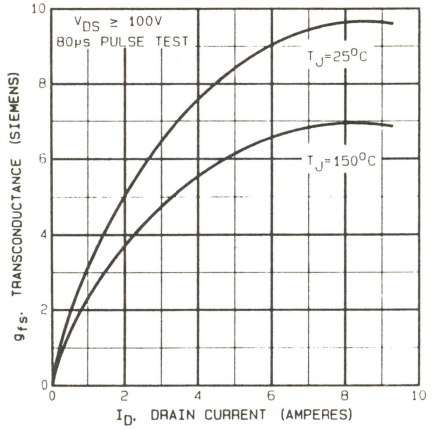


Fig. 6 - Typical Transconductance Vs. Drain Current

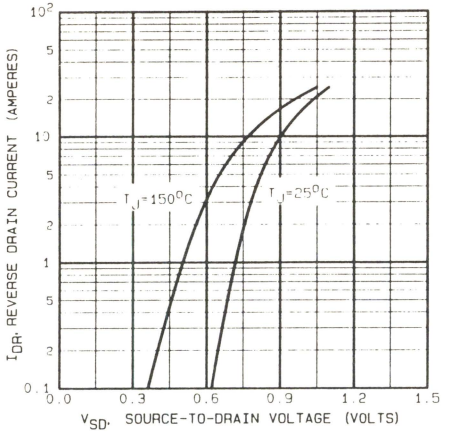


Fig. 7 - Typical Source-Drain Diode Forward Voltage

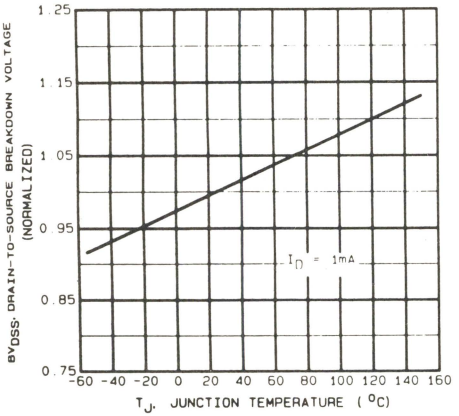


Fig. 8 - Breakdown Voltage Vs. Temperature

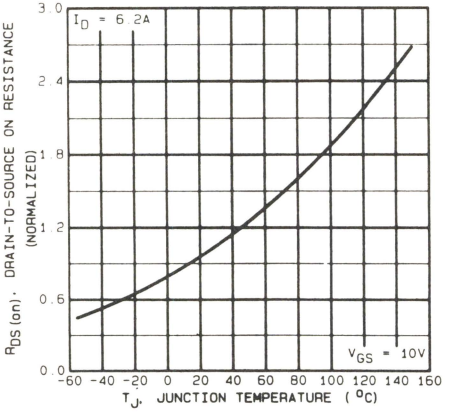


Fig. 9 - Normalized On-Resistance Vs. Temperature

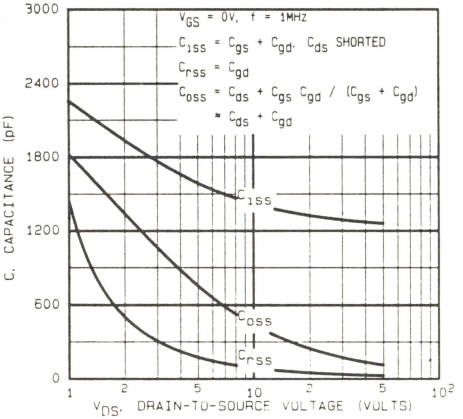


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

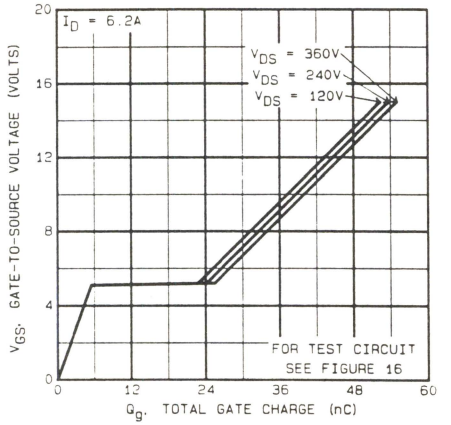


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

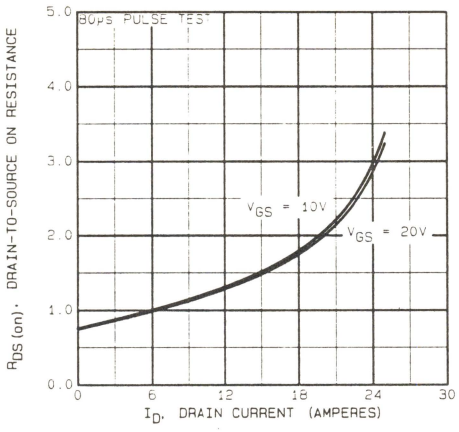


Fig. 12 - Typical On-Resistance Vs. Drain Current

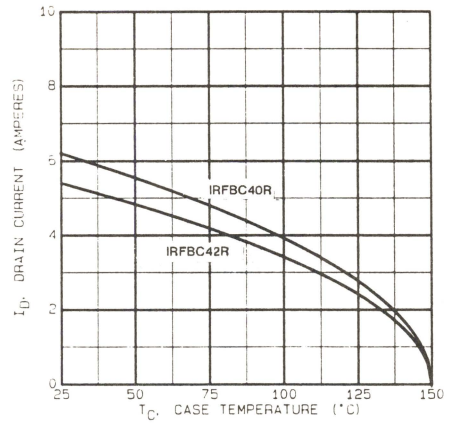


Fig. 13 - Maximum Drain Current Vs. Case Temperature

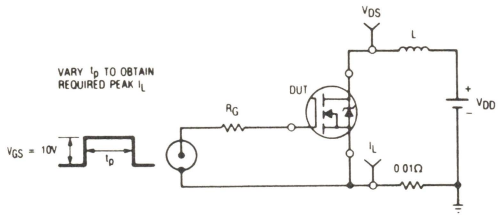


Fig. 14a - Unclamped Inductive Test Circuit

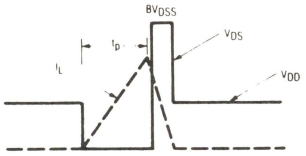


Fig. 14b - Unclamped Inductive Waveforms

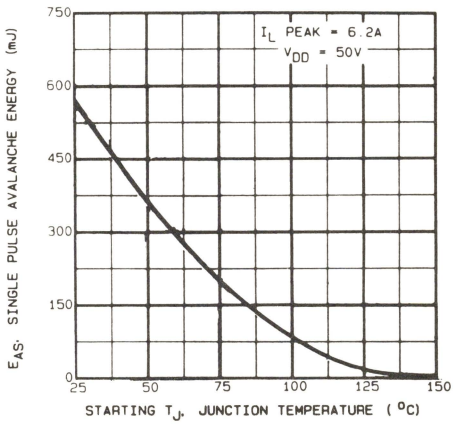


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

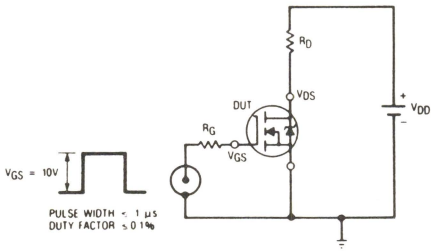


Fig. 15a - Switching Time Test Circuit

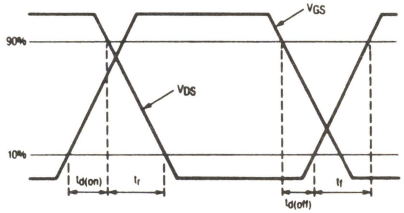


Fig. 15b - Switching Time Waveforms

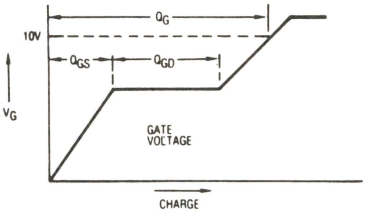


Fig. 16a - Basic Gate Charge Waveform

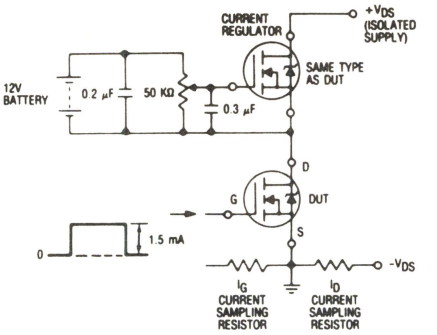


Fig. 16b - Gate Charge Test Circuit

HARRIS

IRFD110/111/112/113
IRFD110R/111R/112R/113R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 1A and 0.8A, 80V - 100V
- $r_{DS(on)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

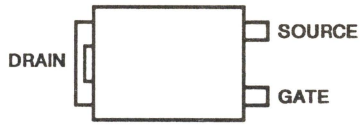
Description

The IRFD110, IRFD111, IRFD112, and IRFD113 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD110R, IRFD111R, IRFD112R, and IRFD113R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

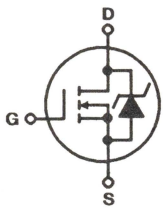
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD110 IRFD110R	IRFD111 IRFD111R	IRFD112 IRFD112R	IRFD113 IRFD113R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	1.0	1.0	0.8	0.8	A
Pulsed Drain Current ..... I_{DM}	8.0	8.0	6.4	6.4	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	8.0	8.0	6.4	6.4	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	19	19	19	19	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 25V, starting T_J = +25°C, L = 28.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.0A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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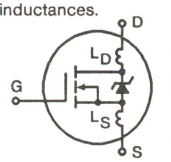
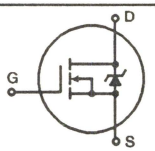
File Number **2314.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD110/112, IRFD110R/112R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRFD111/113, IRFD111R/113R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFD110/111, IRFD110R/111R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	1.0	–	–	A
IRFD112/113, IRFD112R/113R			0.8	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD110/111, IRFD110R/111R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.8A	–	0.5	0.6	Ω
IRFD112/113, IRFD112R/113R			–	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.8A	0.8	1.2	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	80	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 1.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	10	20	ns
Rise Time	t_r		–	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	15	25	ns
Fall Time	t_f		–	10	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.0	7.0	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	7.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	1.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	8.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.0A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.0A, dI_F/dt = 100A/μs	–	100	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.0A, dI_F/dt = 100A/μs	–	0.2	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, starting T_J = +25°C, L = 28.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.0A. (See Figure 15.)

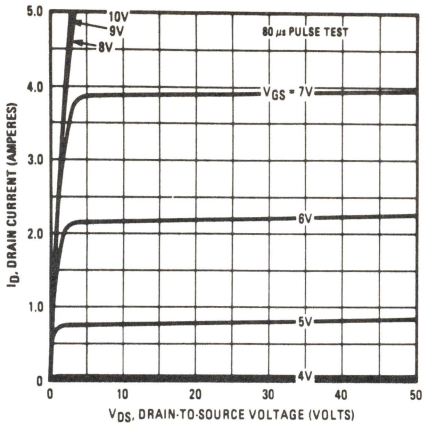


Fig. 1 – Typical Output Characteristics

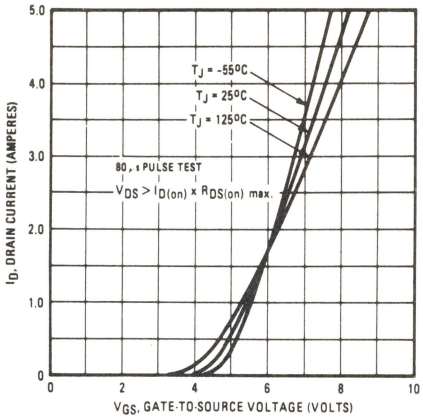


Fig. 2 – Typical Transfer Characteristics

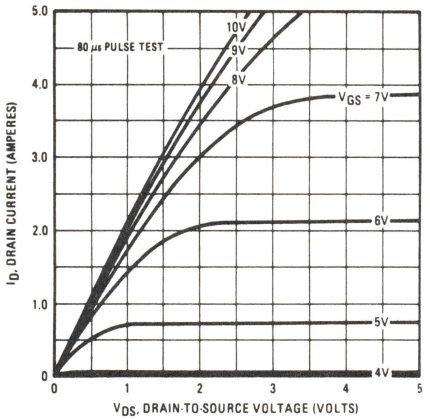


Fig. 3 – Typical Saturation Characteristics

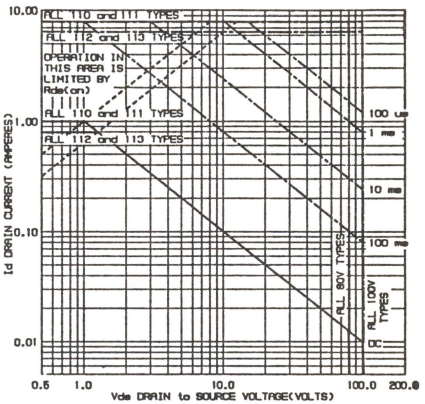


Fig. 4 – Maximum Safe Operating Area

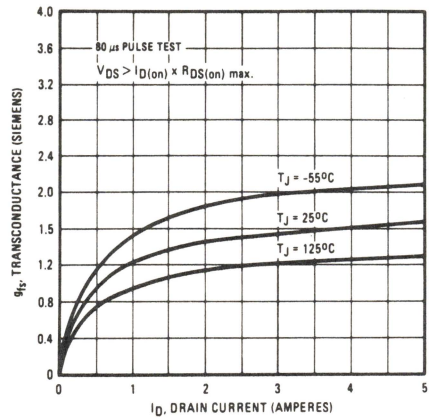


Fig. 5 – Typical Transconductance Vs. Drain Current

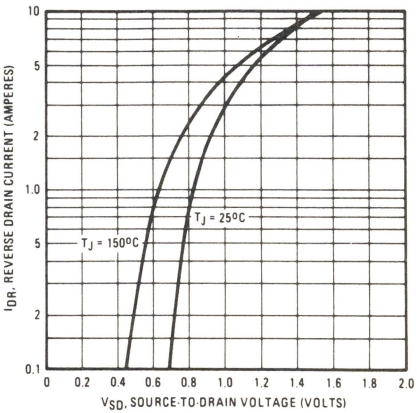


Fig. 6 – Typical Source-Drain Diode Forward Voltage

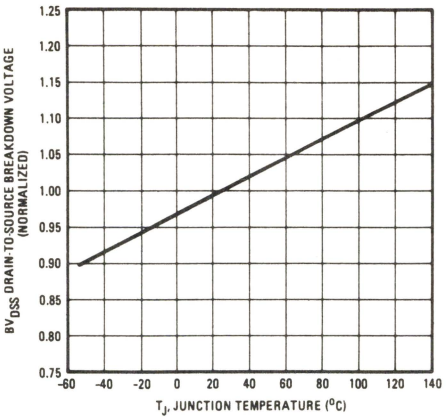


Fig. 7 — Breakdown Voltage Vs. Temperature

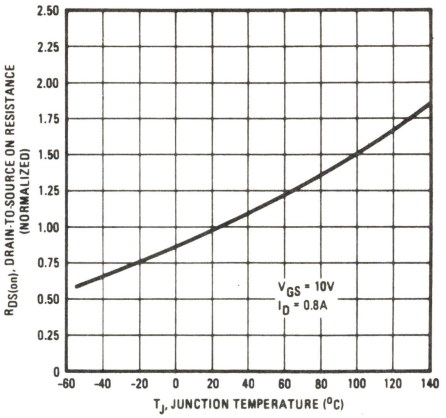


Fig. 8 — Normalized On-Resistance Vs. Temperature

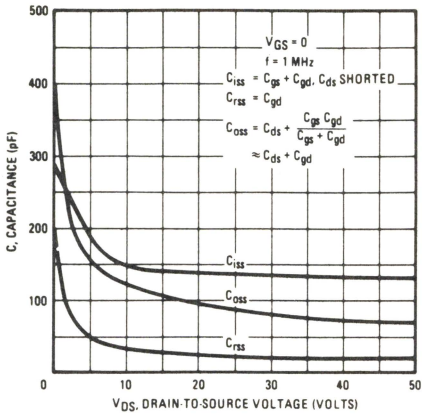


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

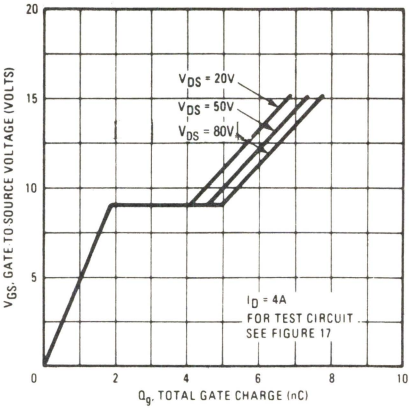


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

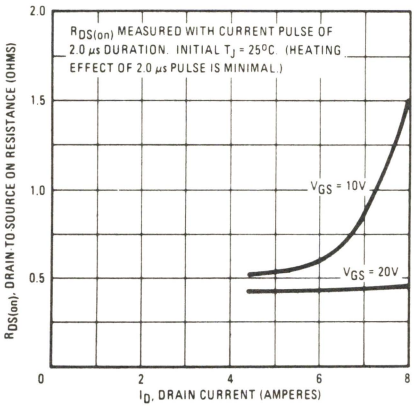


Fig. 11 — Typical On-Resistance Vs. Drain Current

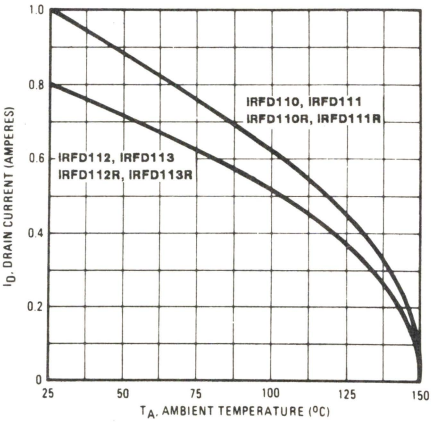


Fig. 12 — Maximum Drain Current Vs. Case Temperature

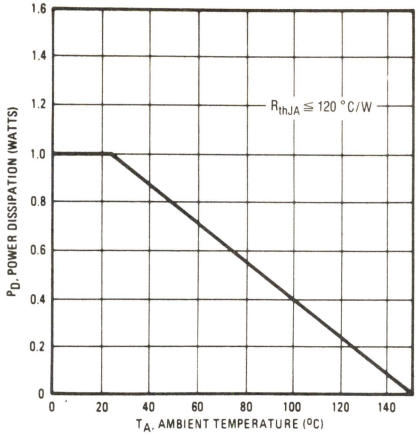


Fig. 13 - Power Vs. Temperature Derating Curve

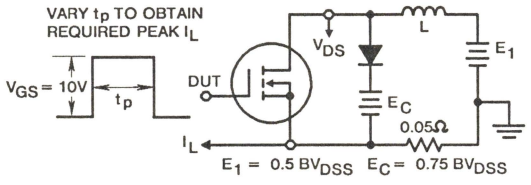


Fig. 14a - Clamped Inductive Test Circuit

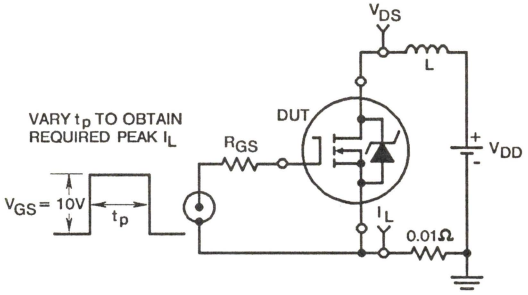


Fig. 15a - Unclamped Energy Test Circuit

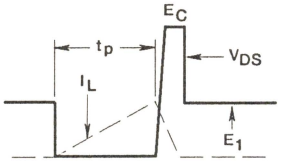


Fig. 14b - Clamped Inductive Waveforms

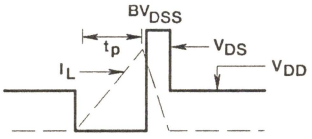


Fig. 15b - Unclamped Energy Waveforms

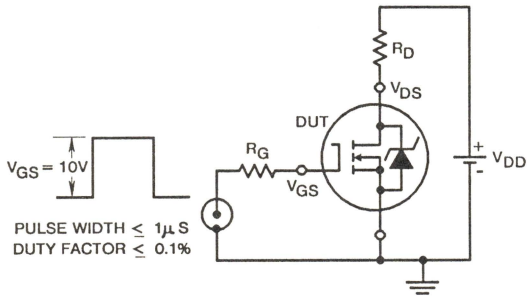


Fig. 16 - Switching Time Test Circuit

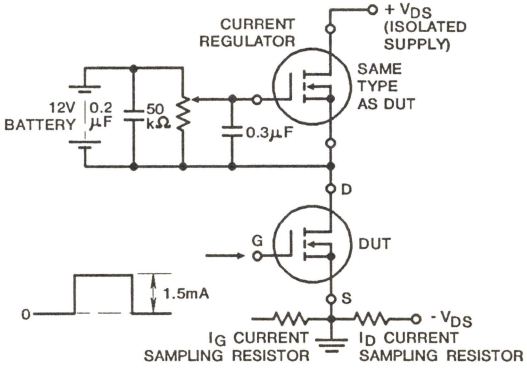


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFD120/121/122/123
IRFD120R/121R/122R/123R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 1.3A and 1.1A, 80V - 100V
- $r_{DS(on)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

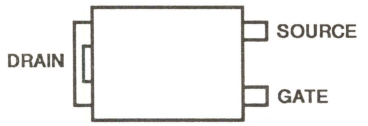
Description

The IRFD120, IRFD121, IRFD122, and IRFD123 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD120R, IRFD121R, IRFD122R, and IRFD123R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

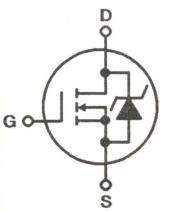
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD120 IRFD120R	IRFD121 IRFD121R	IRFD122 IRFD122R	IRFD123 IRFD123R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	1.3	1.3	1.1	1.1	A
Pulsed Drain Current ..... I_{DM}	5.2	5.2	4.4	4.4	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	5.2	5.2	4.4	4.4	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	36	36	36	36	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 25V, starting T_J = +25°C, L = 32mH, R_{GS} = 25Ω, I_{PEAK} = 1.3A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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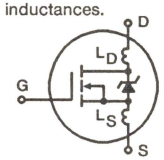
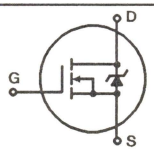
File Number **2315.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD120/122, IRFD120R/122R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRFD121/123, IRFD121R/123R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFD120/121, IRFD120R/121R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	1.3	–	–	A
IRFD122/123, IRFD122R/123R			1.1	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD120/121, IRFD120R/121R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.6A	–	0.25	0.30	Ω
IRFD122/123, IRFD122R/123R			–	0.30	0.40	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.6A	0.9	1.0	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 9	–	450	–	pF
Output Capacitance	C_{OSS}		–	200	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	50	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.3A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	35	70	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	35	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.3A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	6.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	5.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	1.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	5.2	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.3A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.3A, dI_F/dt = 100A/μs	–	280	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.3A, dI_F/dt = 100A/μs	–	1.6	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, starting T_J = +25°C, L = 32mH, R_{GS} = 25Ω, I_{PEAK} = 1.3A. (See Figure 15.)

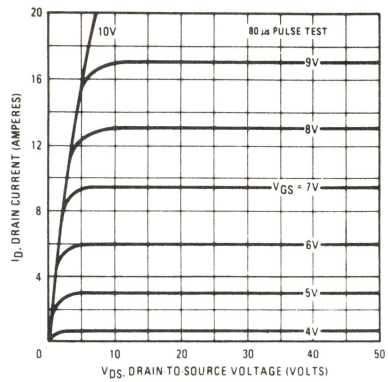


Fig. 1 – Typical Output Characteristics

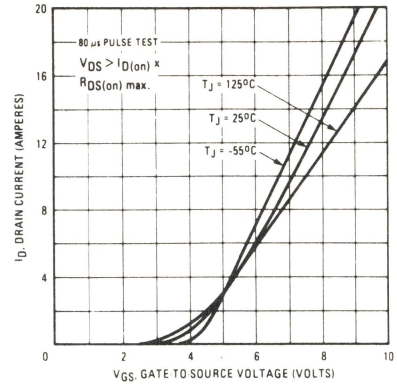


Fig. 2 – Typical Transfer Characteristics

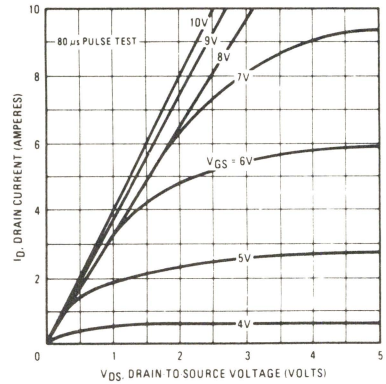


Fig. 3 – Typical Saturation Characteristics

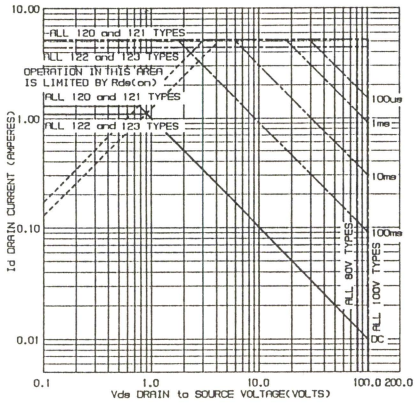


Fig. 4 – Maximum Safe Operating Area

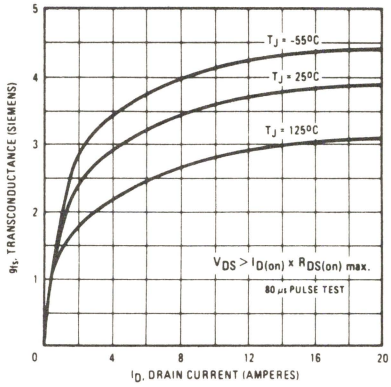


Fig. 5 – Typical Transconductance Vs. Drain Current

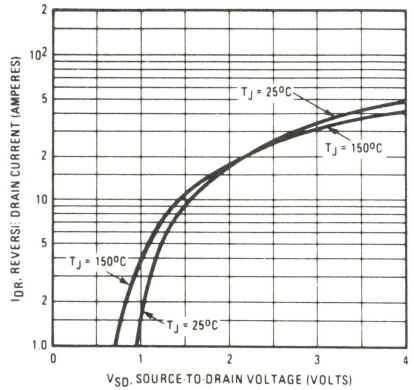


Fig. 6 – Typical Source-Drain Diode Forward Voltage

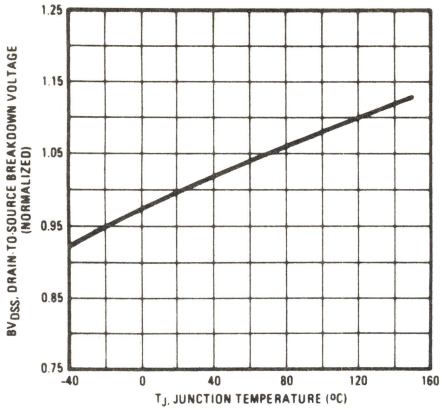


Fig. 7 — Breakdown Voltage Vs. Temperature

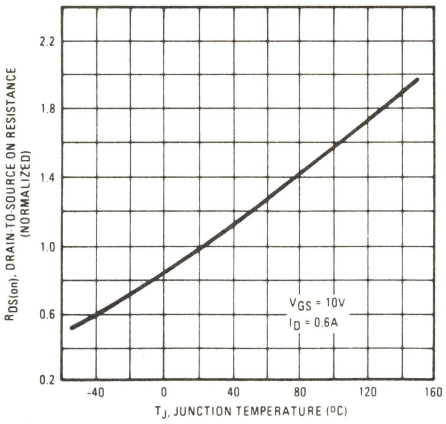


Fig. 8 — Normalized On-Resistance Vs. Temperature

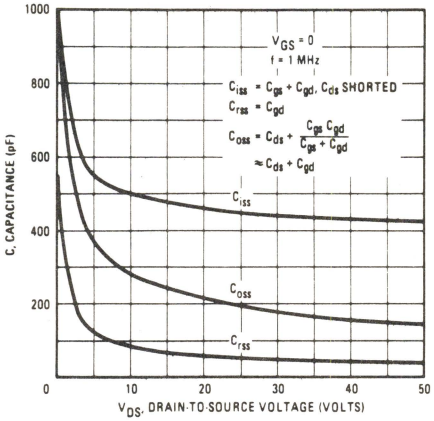


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

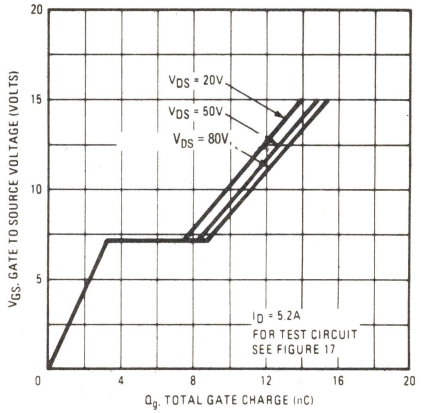


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

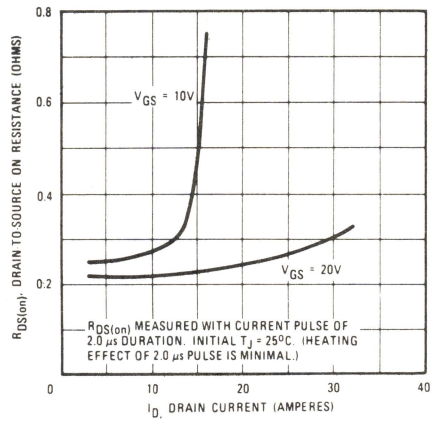


Fig. 11 — Typical On-Resistance Vs. Drain Current

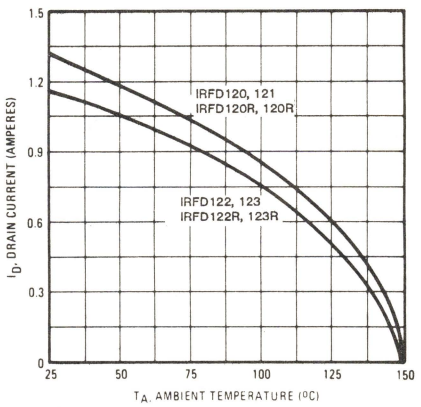


Fig. 12 — Maximum Drain Current Vs. Case Temperature

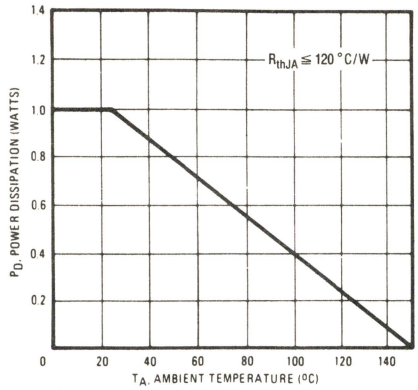


Fig. 13 - Power Vs. Temperature Derating Curve

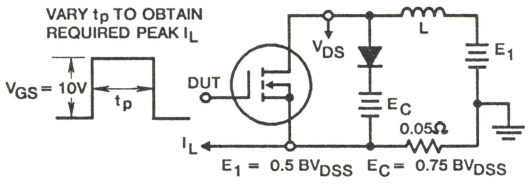


Fig. 14a - Clamped Inductive Test Circuit

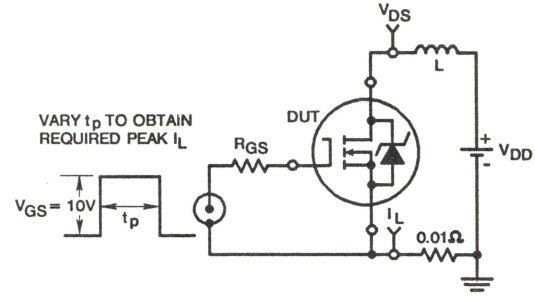


Fig. 15a - Unclamped Energy Test Circuit

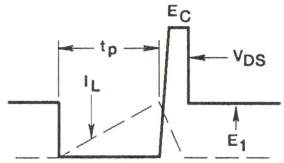


Fig. 14b - Clamped Inductive Waveforms

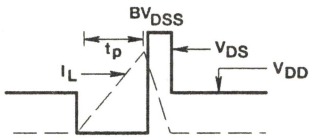


Fig. 15b - Unclamped Energy Waveforms

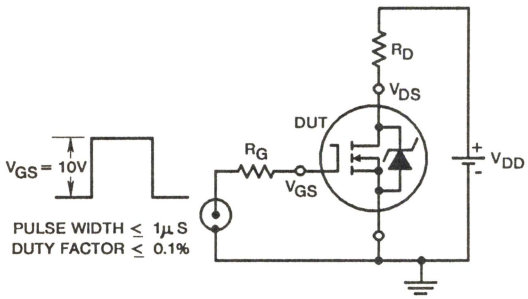


Fig. 16 - Switching Time Test Circuit

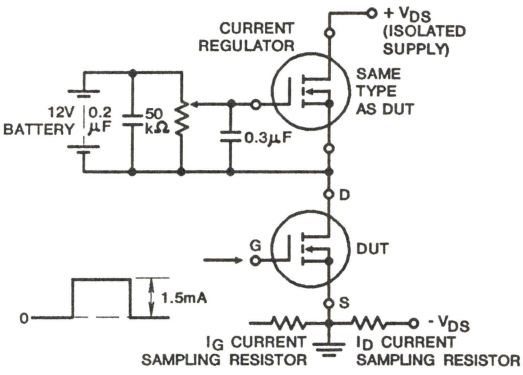


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFD1Z0, IRFD1Z1 IRFD1Z2, IRFD1Z3

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 0.4A and 0.5A, 60V - 100V
- $r_{DS(on)}$ = 2.4Ω and 3.2Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The IRFD1Z0, IRFD1Z1, IRFD1Z2, and IRFD1Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

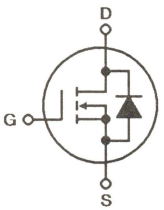
The IRFD types are supplied in the 4-pin DIP package.

Package

4-PIN DIP
TOP VIEW

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFD1Z0	IRFD1Z1	IRFD1Z2	IRFD1Z3	UNITS
Drain-Source Voltage (1)	V_{DS}	100	60	100	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	100	60	100	60	V
Continuous Drain Current T_C = +25°C	I_D	0.5	0.5	0.4	0.4	A
Pulsed Drain Current	I_{DM}	4.0	4.0	3.2	3.2	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13)	P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped (See Figures 14 and 15, L 100μH)	I_{LM}	4.0	4.0	3.2	3.2	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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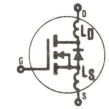
File Number 2313

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD1Z0, 2	100	–	–	V	V_{GS} = 0V
		IRFD1Z1, 3	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD1Z0, 1	0.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD1Z2, 3	0.4	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD1Z0, 1	–	2.2	2.4	Ω	V_{GS} = 10V, I_D = 0.25A
		IRFD1Z2, 3	–	2.8	3.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.25	0.35	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.25A
C_{iss}	Input Capacitance	ALL	–	50	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	20	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	5.0	–	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.25A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	2.0	3.0	nC	V_{GS} = 10V, I_D = 1.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	1.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	1.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD1Z0, 1	–	–	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD1Z2, 3	–	–	0.4	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD1Z0, 1	–	–	4.0	A	
		IRFD1Z2, 3	–	–	3.2	A	
V_{SD}	Diode Forward Voltage ②	IRFD1Z0, 1	–	–	1.4	V	T_A = 25°C, I_S = 0.5A, V_{GS} = 0V
		IRFD1Z2, 3	–	–	1.3	V	T_A = 25°C, I_S = 0.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	μC	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

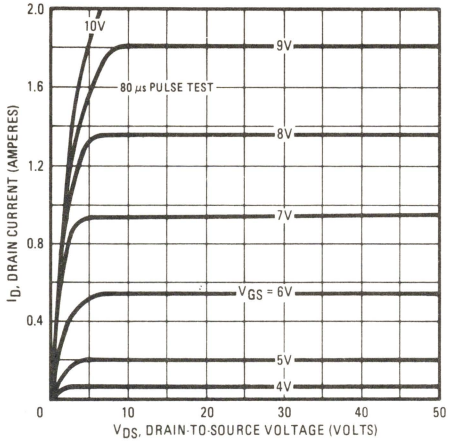


Fig. 1 — Typical Output Characteristics

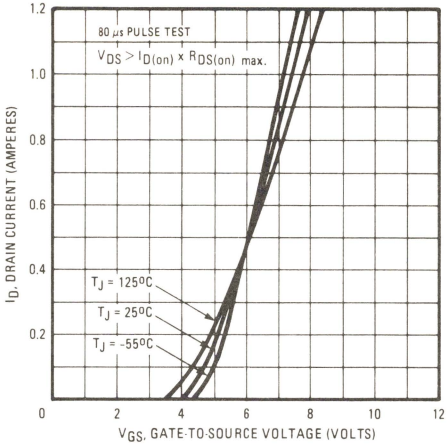


Fig. 2 — Typical Transfer Characteristics

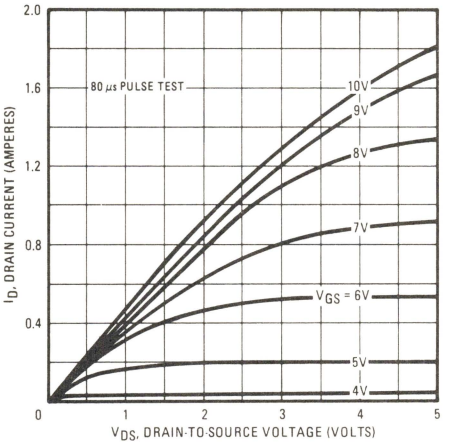


Fig. 3 — Typical Saturation Characteristics

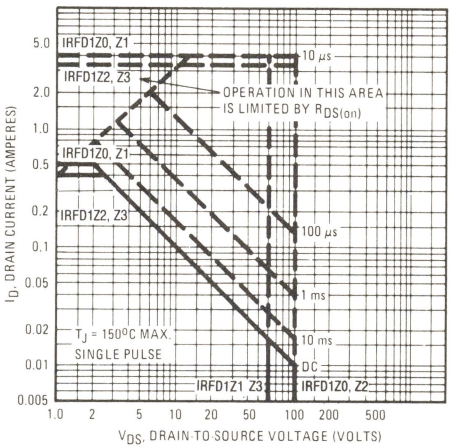


Fig. 4 — Maximum Safe Operating Area

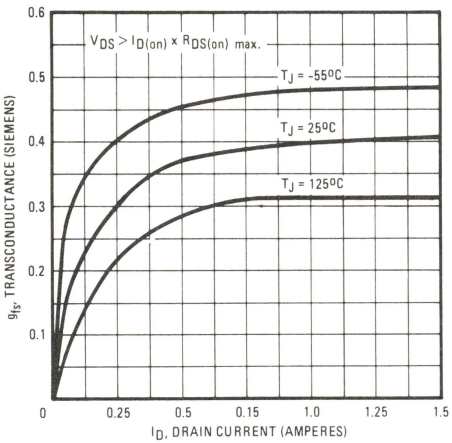


Fig. 5 — Typical Transconductance Vs. Drain Current

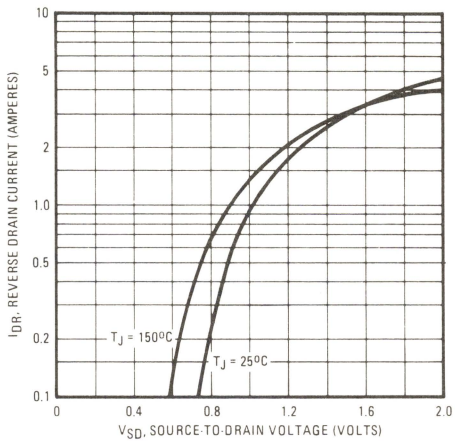


Fig. 6 — Typical Source-Drain Diode Forward Voltage

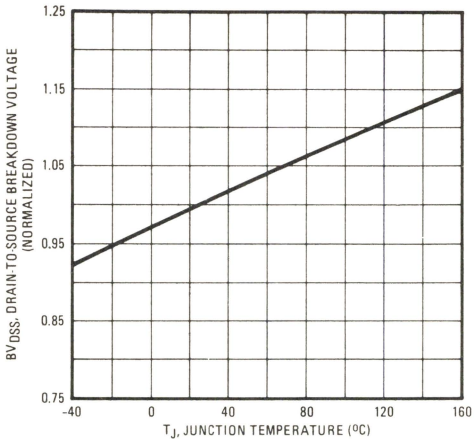


Fig. 7 — Breakdown Voltage Vs. Temperature

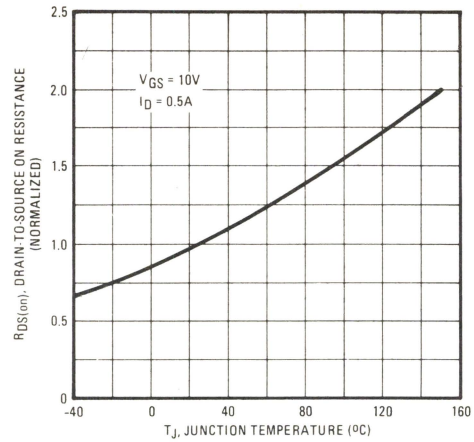


Fig. 8 — Normalized On-Resistance Vs. Temperature

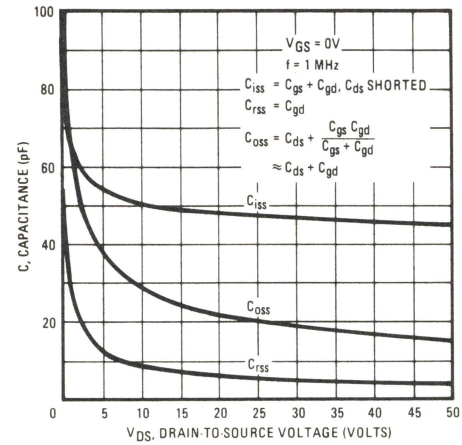


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

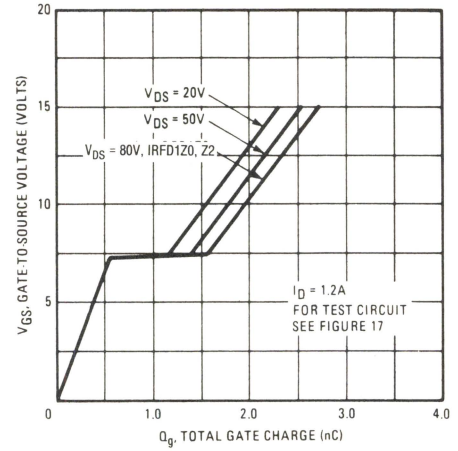


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

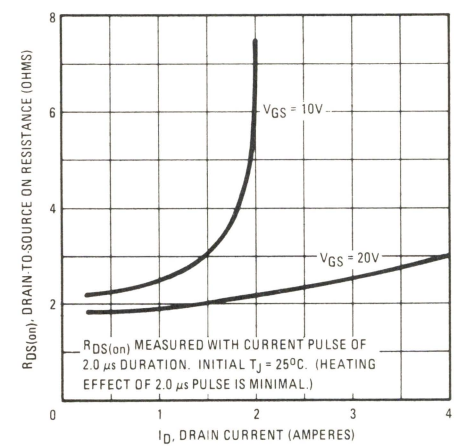


Fig. 11 — Typical On-Resistance Vs. Drain Current

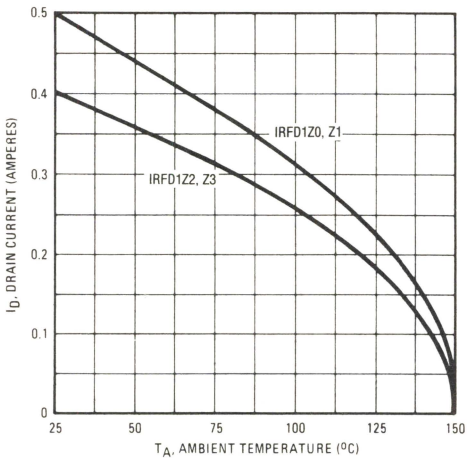


Fig. 12 — Maximum Drain Current Vs. Case Temperature

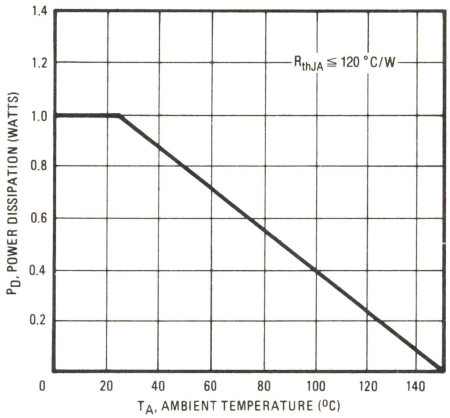


Fig. 13 – Power Vs. Temperature Derating Curve

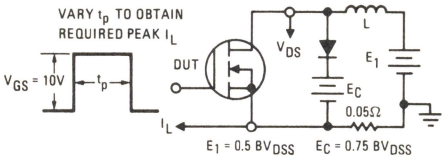


Fig. 14 – Clamped Inductive Test Circuit

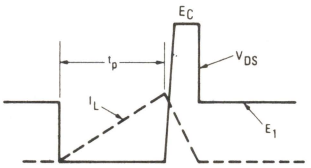


Fig. 15 – Clamped Inductive Waveforms

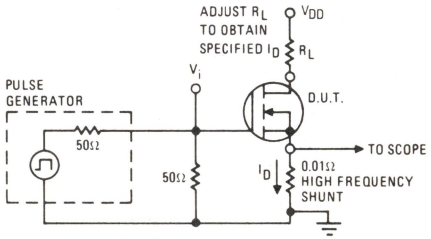


Fig. 16 – Switching Time Test Circuit

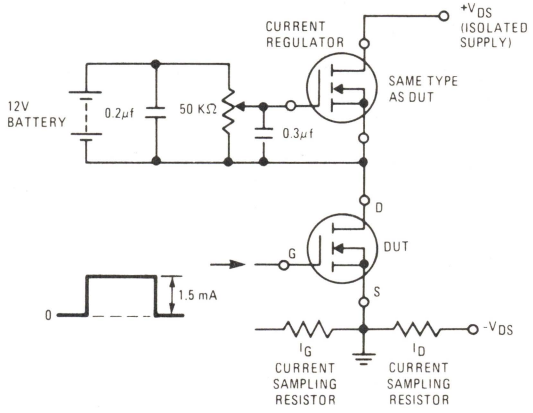


Fig. 17 – Gate Charge Test Circuit

HARRIS

IRFD210/211/212/213
IRFD210R/211R/212R/213R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 0.6A and 0.45A, 150V - 200V
- $r_{DS(on)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

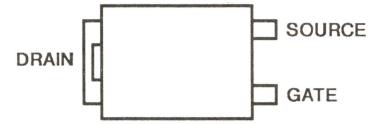
Description

The IRFD210, IRFD211, IRFD212, and IRFD213 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD210R, IRFD211R, IRFD212R, and IRFD213R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

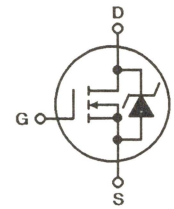
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD210 IRFD210R	IRFD211 IRFD211R	IRFD212 IRFD212R	IRFD213 IRFD213R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	0.6	0.6	0.45	0.45	A
Pulsed Drain Current ..... I_{DM}	2.5	2.5	1.8	1.8	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	2.5	2.5	1.8	1.8	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	30	30	30	30	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 20V, starting T_J = +25°C, L = 112.7mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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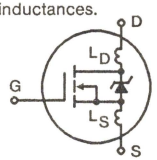
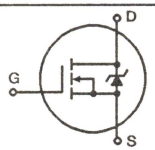
File Number **2316.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD210/212, IRFD210R/212R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRFD211/213, IRFD211R/213R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFD210/211, IRFD210R/211R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	0.6	–	–	A
IRFD212/213, IRFD212R/213R			0.45	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD210/211, IRFD210R/211R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.3A	–	1.0	1.5	Ω
IRFD212/213, IRFD212R/213R			–	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.3A	0.5	0.8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 9	–	135	–	pF
Output Capacitance	C_{OSS}		–	60	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	16	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 0.6A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	8.0	15	ns
Rise Time	t_r		–	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	10	15	ns
Fall Time	t_f		–	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	5.0	7.5	nC
Gate-Source Charge	Q_{gs}		–	2.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	3.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	0.6	A
Pulse Source Current (Body Diode)	I_{SM}		–	–	2.5	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 0.6A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 0.6A, dI_F/dt = 100A/µs	–	290	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 0.6A, dI_F/dt = 100A/µs	–	2.0	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. V_{DD} = 20V, starting T_J = +25°C, L = 112.7mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. (See Figure 15.)

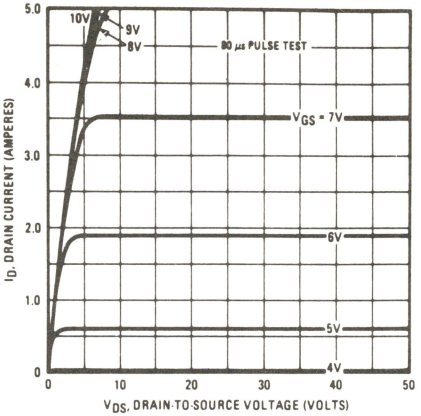


Fig. 1 — Typical Output Characteristics

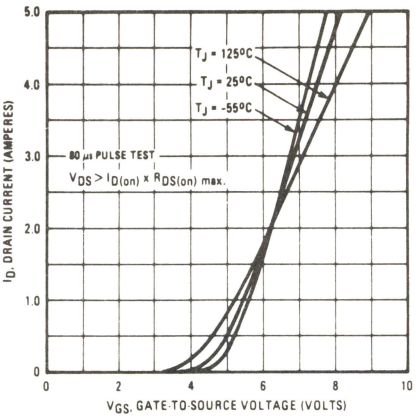


Fig. 2 — Typical Transfer Characteristics

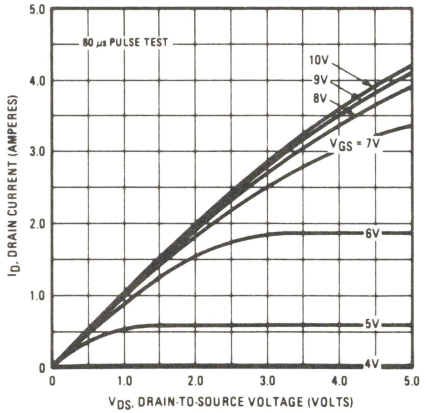


Fig. 3 — Typical Saturation Characteristics

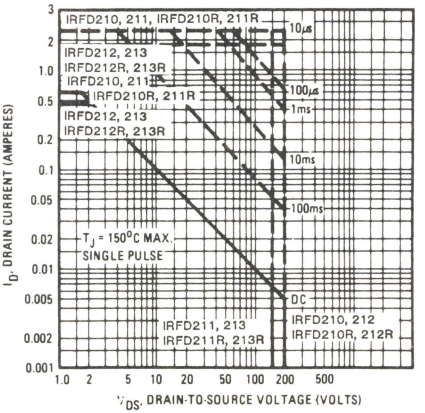


Fig. 4 — Maximum Safe Operating Area

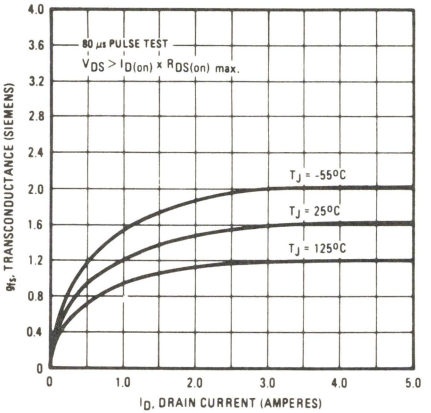


Fig. 5 — Typical Transconductance Vs. Drain Current

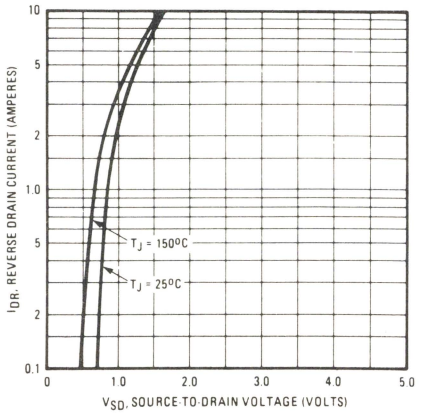


Fig. 6 — Typical Source-Drain Diode Forward Voltage

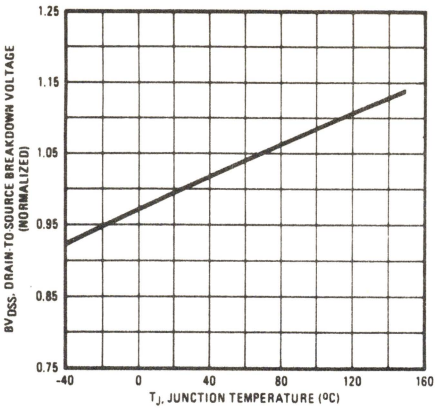


Fig. 7 — Breakdown Voltage Vs. Temperature

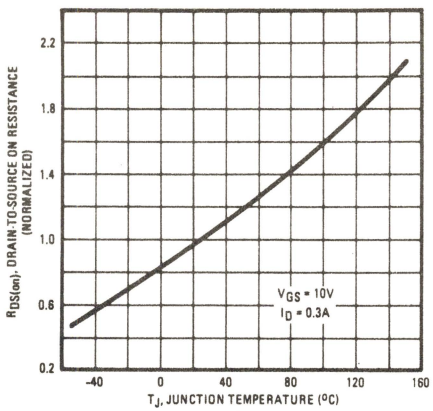


Fig. 8 — Normalized On-Resistance Vs. Temperature

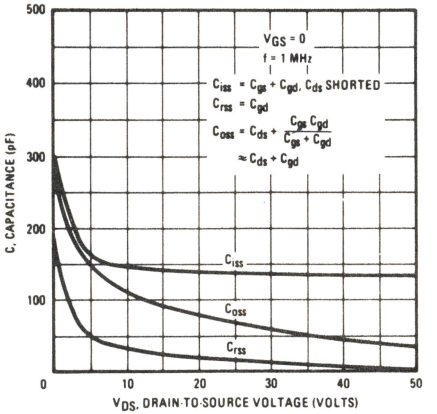


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

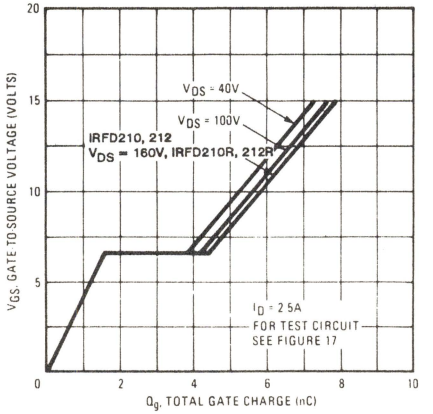


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

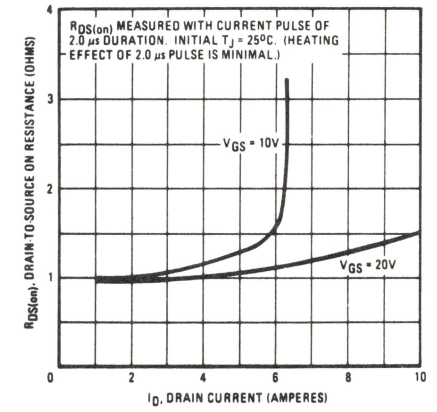


Fig. 11 — Typical On-Resistance Vs. Drain Current

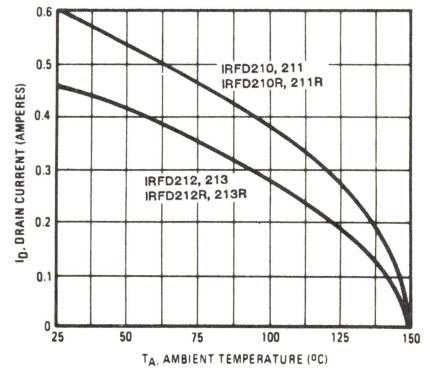


Fig. 12 — Maximum Drain Current Vs. Case Temperature

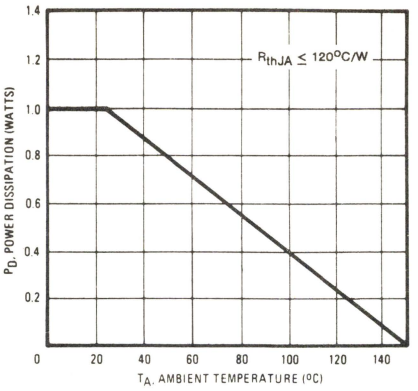


Fig. 13 - Power Vs. Temperature Derating Curve

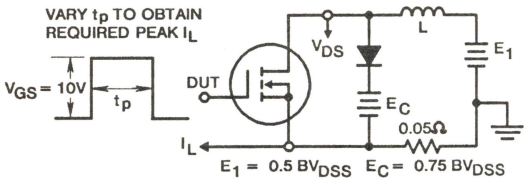


Fig. 14a - Clamped Inductive Test Circuit

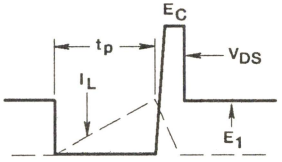


Fig. 14b - Clamped Inductive Waveforms

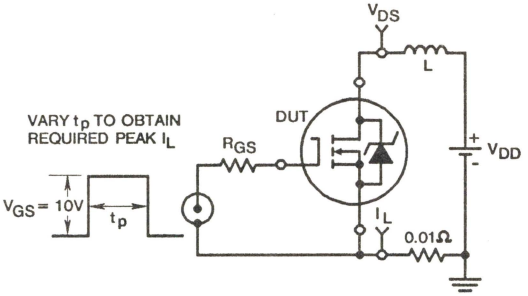


Fig. 15a - Unclamped Energy Test Circuit

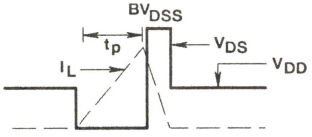


Fig. 15b - Unclamped Energy Waveforms

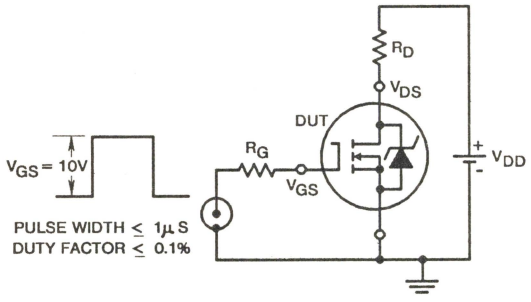


Fig. 16 - Switching Time Test Circuit

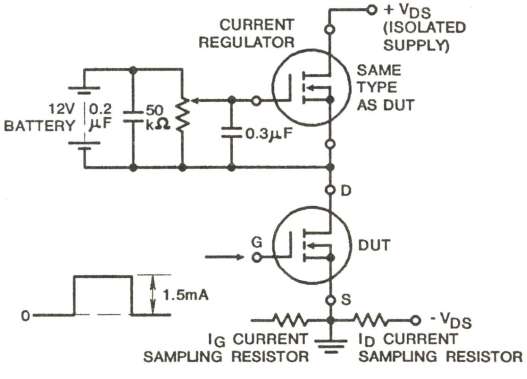


Fig. 17 - Gate Charge Test Circuit

IRFD220/221/222/223
IRFD220R/221R/222R/223R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 0.7A and 0.8A, 150V - 200V
- $r_{DS(on)}$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

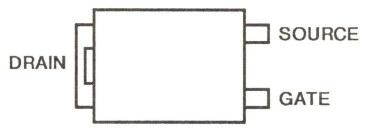
Description

The IRFD220, IRFD221, IRFD222, and IRFD223 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD220R, IRFD221R, IRFD222R, and IRFD223R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

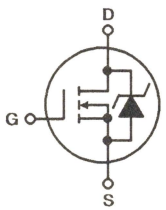
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD220 IRFD220R	IRFD221 IRFD221R	IRFD222 IRFD222R	IRFD223 IRFD223R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	0.8	0.8	0.7	0.7	A
Pulsed Drain Current ..... I_{DM}	6.4	6.4	5.6	5.6	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	6.4	6.4	5.6	5.6	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	85	85	85	85	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 25V, starting T_J = +25°C, L = 12.62mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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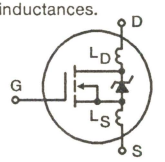
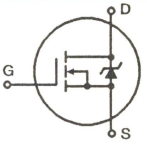
File Number **2317.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD220/222, IRFD220R/222R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRFD221/223, IRFD221R/223R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFD220/221, IRFD220R/221R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	0.8	–	–	A
IRFD222/223, IRFD222R/223R			0.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFD220/221, IRFD220R/221R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.4A	–	0.5	0.8	Ω
IRFD222/223, IRFD222R/223R			–	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)\,Max}$, I_D = 0.4A	0.5	1.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 9	–	450	–	pF
Output Capacitance	C_{OSS}		–	150	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	30	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.8A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	6.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	5.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	4.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	–	6.0	–	nH
Junction-to-Case	$R_{\theta JC}$	Free air operation	–	–	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	0.8	A
Pulse Source Current (Body Diode)	I_{SM}		–	–	6.4	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 0.8A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 0.8A, dI_F/dt = 100A/µs	–	150	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 0.8A, dI_F/dt = 100A/µs	–	0.6	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, starting T_J = +25°C, L = 12.62mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. (See Figure 15.)

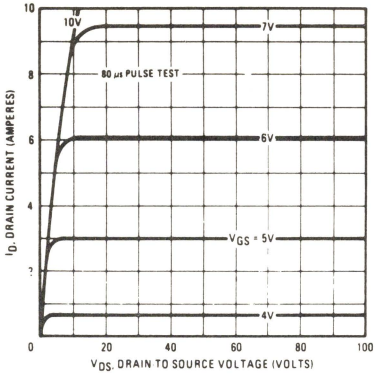


Fig. 1 — Typical Output Characteristics

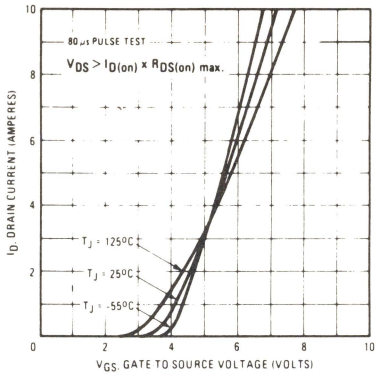


Fig. 2 — Typical Transfer Characteristics

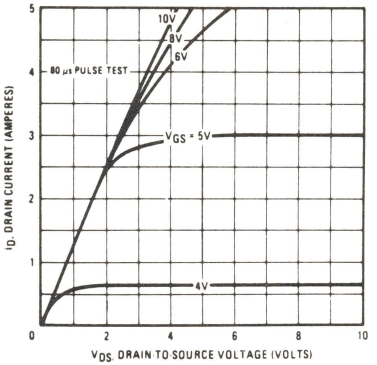


Fig. 3 — Typical Saturation Characteristics

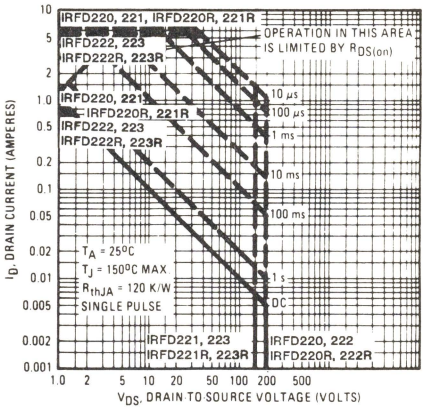


Fig. 4 — Maximum Safe Operating Area

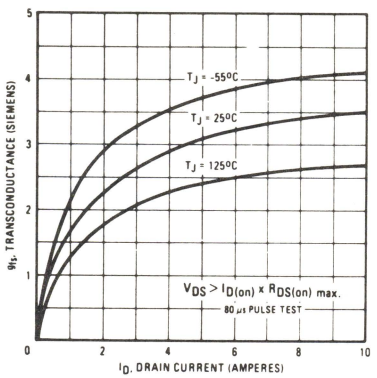


Fig. 5 — Typical Transconductance Vs. Drain Current

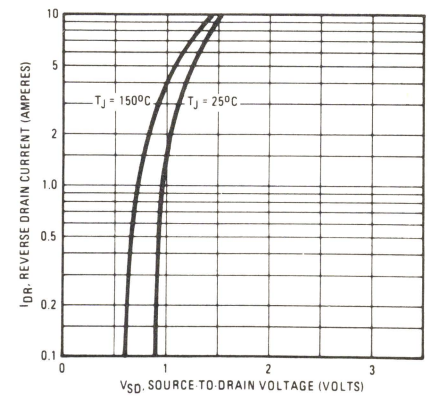


Fig. 6 — Typical Source-Drain Diode Forward Voltage

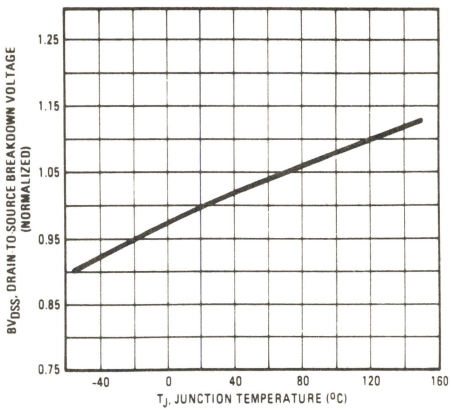


Fig. 7 — Breakdown Voltage Vs. Temperature

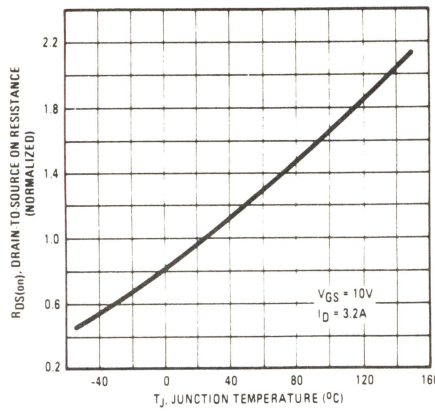


Fig. 8 — Normalized On-Resistance Vs. Temperature

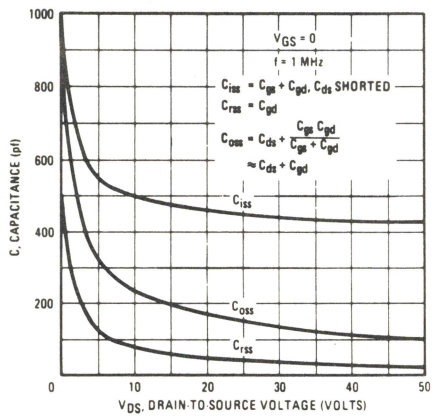


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

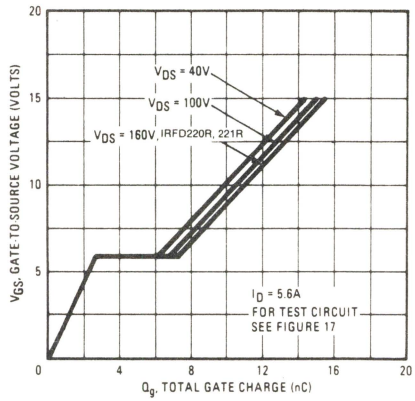


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

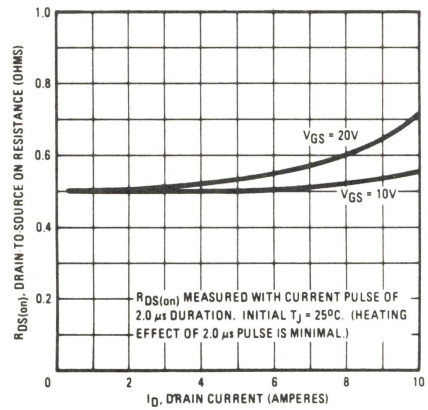


Fig. 11 — Typical On-Resistance Vs. Drain Current

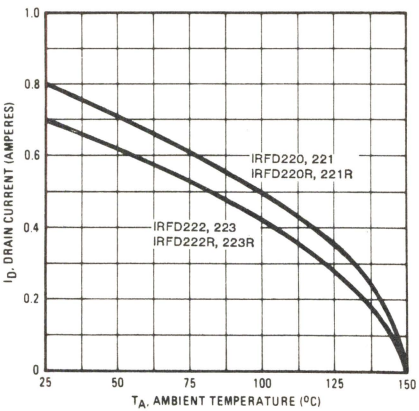


Fig. 12 — Maximum Drain Current Vs. Case Temperature

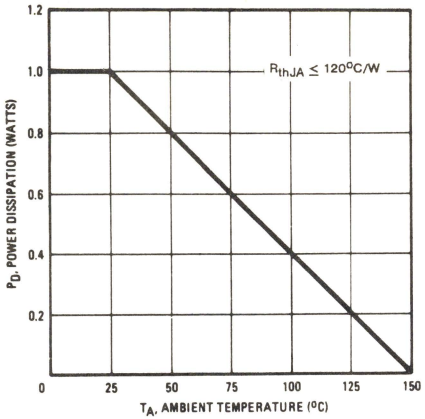


Fig. 13 - Power Vs. Temperature Derating Curve

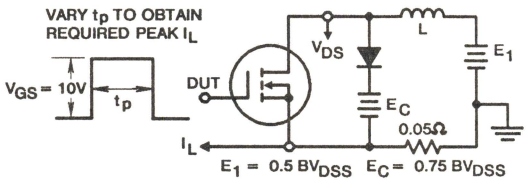


Fig. 14a - Clamped Inductive Test Circuit

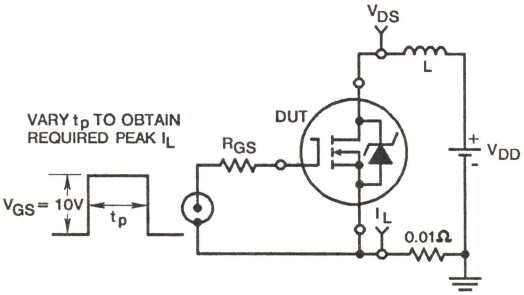


Fig. 15a - Unclamped Energy Test Circuit

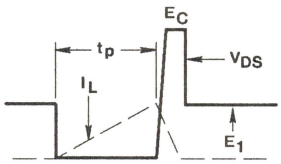


Fig. 14b - Clamped Inductive Waveforms

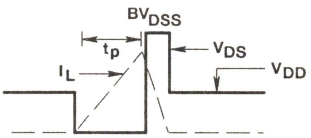


Fig. 15b - Unclamped Energy Waveforms

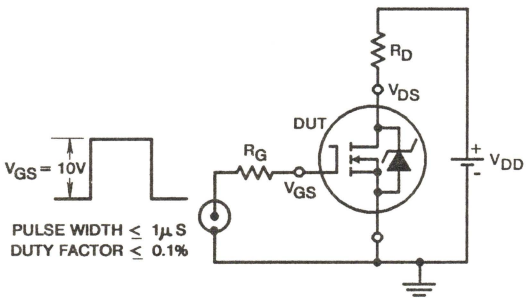


Fig. 16 - Switching Time Test Circuit

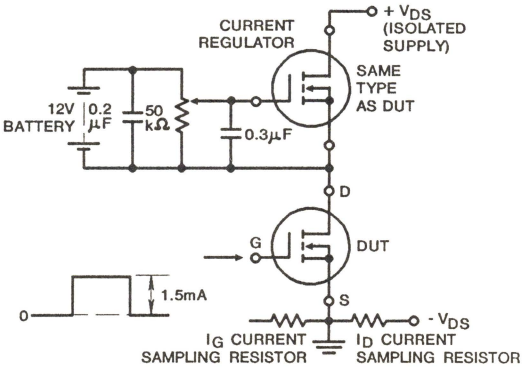


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFD2Z0, IRFD2Z1 IRFD2Z2, IRFD2Z3

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 0.30A and 0.32A, 150V - 200V
- $r_{DS(on)}$ = 5.0Ω and 6.5Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The IRFD2Z0, IRFD2Z1, IRFD2Z2, and IRFD2Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

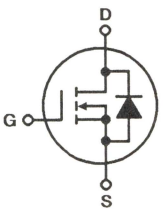
The IRFD types are supplied in the 4-pin DIP package.

Package

4-PIN DIP
TOP VIEW

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD2Z0	IRFD2Z1	IRFD2Z2	IRFD2Z3	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	0.32	0.32	0.30	0.30	A
Pulsed Drain Current ..... I_{DM}	1.5	1.5	1.4	1.4	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped (3) ..... I_{LM}	1.5	1.5	1.4	1.4	A
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. See Figures 14 and 15. L = 100μH

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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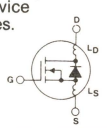
File Number **2329.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C Unless Otherwise Specified*

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Drain-Source Breakdown Voltage	BV_{DSS}	IRFD2Z0 IRFD2Z2	200	—	—	V	V_{GS} = 0 V
		IRFD2Z1 IRFD2Z3	150	—	—	V	I_D = 250 μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	500	nA	V_{GS} = 20 V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-500	nA	V_{GS} = −20 V
Zero-Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125°C
On-State Drain Current ②	$I_{D(on)}$	IRFD2Z0 IRFD2Z1	0.32	—	—	A	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, V_{GS} = −10 V
		IRFD2Z2 IRFD2Z3	0.30	—	—	A	
Static Drain-Source On-State Resistance ②	$r_{DS(on)}$	IRFD2Z0 IRFD2Z1	—	4.6	5.0	Ω	V_{GS} = 10 V, I_D = 0.15 A
		IRFD2Z2 IRFD2Z3	—	5.7	6.5	Ω	
Forward Transconductance ②	g_{fs}	ALL	0.06	0.11	—	S(℧)	$V_{DS} > I_{D(on)} \times r_{DS(on)\ max.}$, I_D = 0.15 A
Input Capacitance	C_{iss}	ALL	—	37	—	pF	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz See Fig. 9
Output Capacitance	C_{oss}	ALL	—	15	—	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	4.0	—	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	15	—	ns	$V_{DD} \cong 0.5\ BV_{DSS}$, I_D = 0.15 A, Z_O = 50 Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	10	—	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	22	—	ns	
Fall Time	t_f	ALL	—	28	—	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	2.5	4.0	nC	V_{GS} = 10 V, I_D = 1.5 A, V_{DS} = 0.8 V Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	1.5	—	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	1.5	—	nC	
Internal Drain Inductance	L_D	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0 mm (0.08 in.) from package to center of die.
Internal Source Inductance	L_S	ALL	—	6.0	—	nH	Measured from the source lead, 2.0 mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

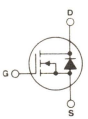


THERMAL RESISTANCE

Junction-to-Ambient	$R_{\theta JA}$	ALL	—	—	120	°C/W	Free Air Operation

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Continuous Source Current (Body Diode)	I_S	IRFD2Z0 IRFD2Z1	—	—	0.32	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD2Z2 IRFD2Z3	—	—	0.30	A	
Pulse Source Current (Body Diode)	I_{SM}	IRFD2Z0 IRFD2Z1	—	—	1.5	A	
		IRFD2Z2 IRFD2Z3	—	—	1.4	A	
Diode Forward Voltage ②	V_{SD}	IRFD2Z0 IRFD2Z1	—	—	1.3	V	T_C = 25°C, I_S = 0.32 A, V_{GS} = 0 V
		IRFD2Z2 IRFD2Z3	—	—	1.3	V	T_C = 25°C, I_S = 0.30 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	ALL	—	125	—	ns	T_J = 150°C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Reverse Recovered Charge	Q_{RR}	ALL	—	0.2	—	μC	T_J = 150°C, I_F = 0.30 A, dI_F/dt = 100 A/μs
Forward Turn-on Time	t_{on}	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C.
② Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%.
③ (See Fig. 14 and 15) L = 100 μH

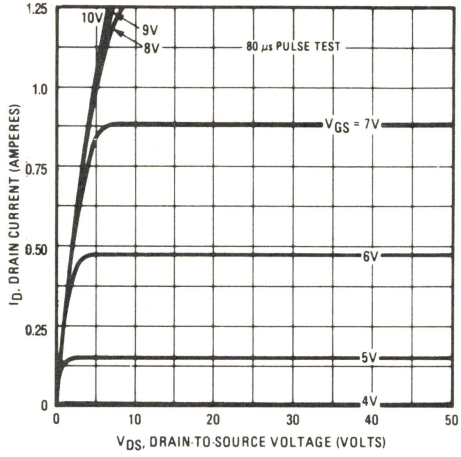


Fig. 1 — Typical Output Characteristics

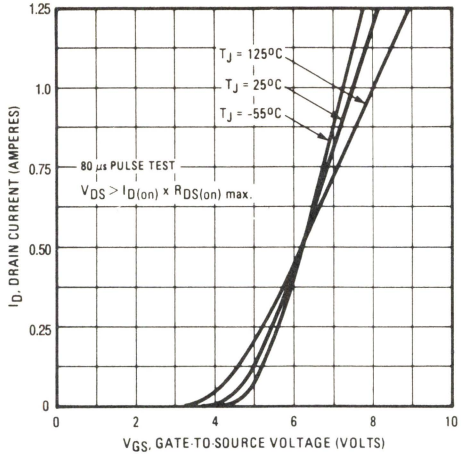


Fig. 2 — Typical Transfer Characteristics

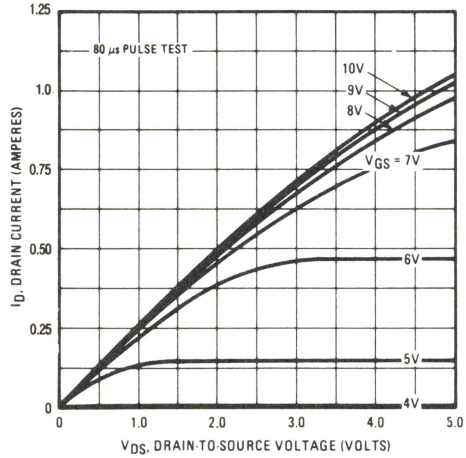


Fig. 3 — Typical Saturation Characteristics

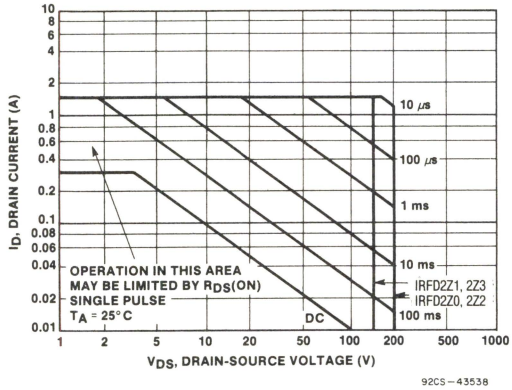


Fig. 4 — Maximum Safe Operating Area

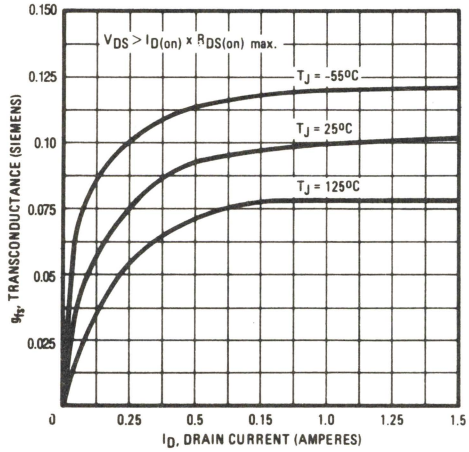


Fig. 5 — Typical Transconductance Vs. Drain Current

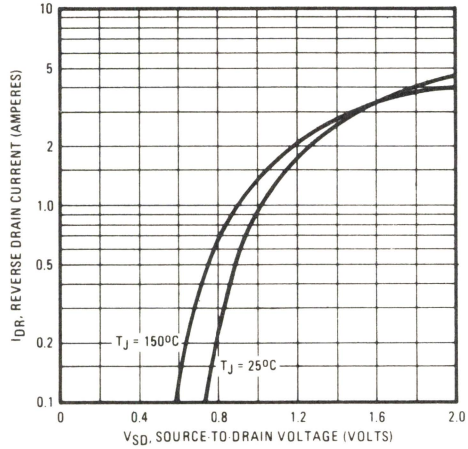


Fig. 6 — Typical Source-Drain Diode Forward Voltage

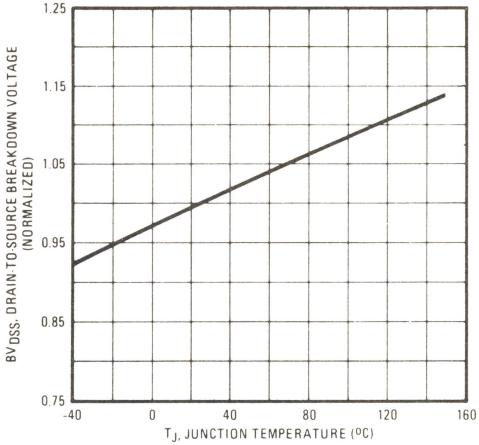


Fig. 7 — Breakdown Voltage Vs. Temperature

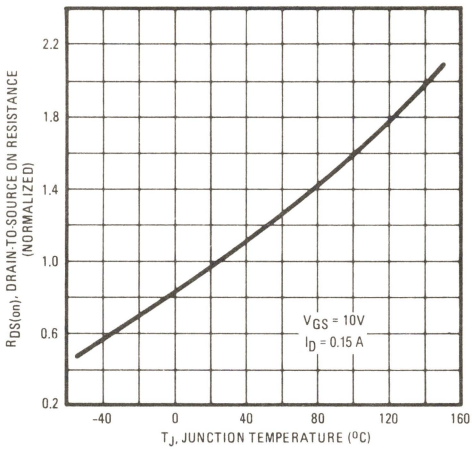


Fig. 8 — Normalized On-Resistance Vs. Temperature

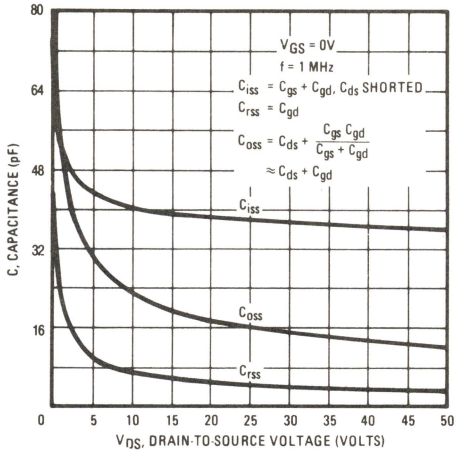


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

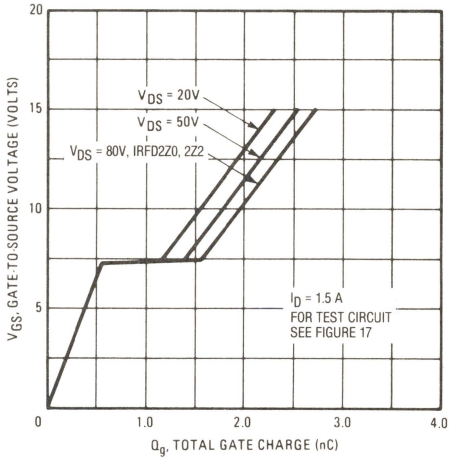


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

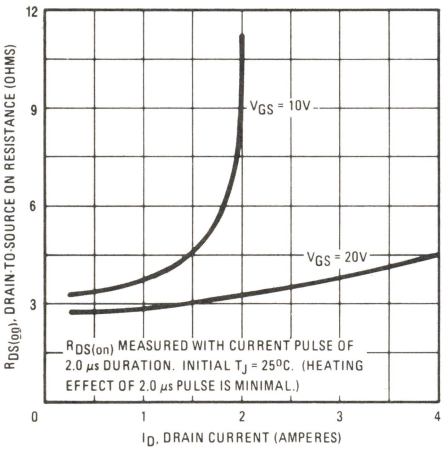


Fig. 11 — Typical On-Resistance Vs. Drain Current

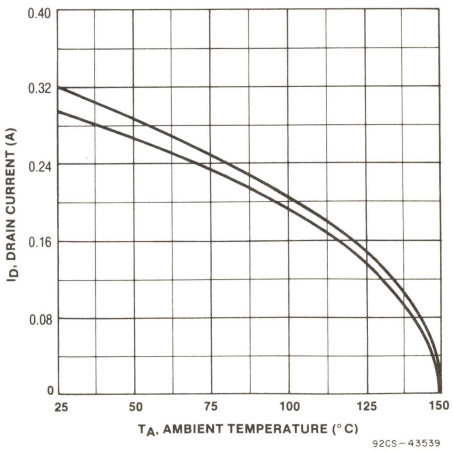
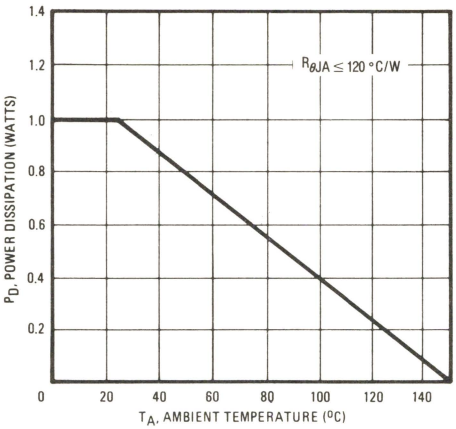


Fig. 12 — Maximum Drain Current Vs. Case Temperature



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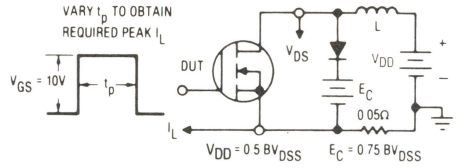


Fig. 14 — Clamped Inductive Test Circuit

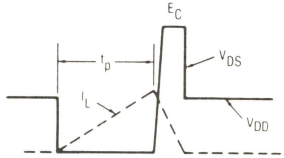


Fig. 15 — Clamped Inductive Waveforms

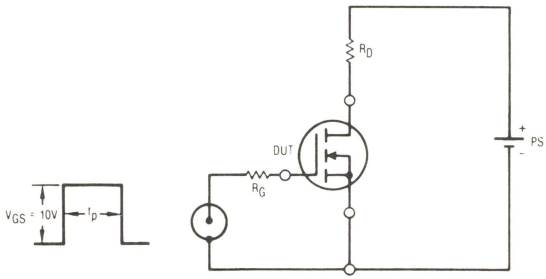


Fig. 16 – Switching Time Test Circuit

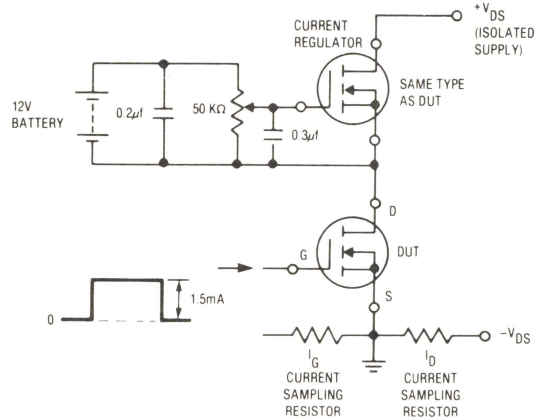


Fig. 17 — Gate Charge Test Circuit

IRFD310/311/312/313
IRFD310R/311R/312R/313R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 0.3A and 0.4A, 350V - 400V
- $r_{DS(on)}$ = 3.6Ω and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFD310, IRFD311, IRFD312, and IRFD313 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD310R, IRFD311R, IRFD312R, and IRFD313R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

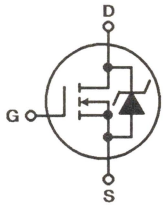
The IRFD types are supplied in the 4-pin dual-in-line plastic package.

Package

4-PIN DIP
TOP VIEW

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD310 IRFD310R	IRFD311 IRFD311R	IRFD312 IRFD312R	IRFD313 IRFD313R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	0.4	0.4	0.3	0.3	A
Pulsed Drain Current (3) ..... I_{DM}	1.6	1.6	1.2	1.2	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 14) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped (See Figure 14, L = 100μH) ..... I_{LM}	1.6	1.6	1.2	1.2	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	45	45	45	45	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 15).
4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.4A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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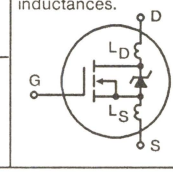
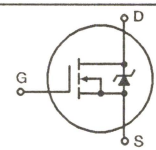
File Number **2324.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD310/312, IRFD310R/312R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
IRFD311/313, IRFD311R/313R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFD310/311, IRFD310R/311R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	0.4	-	-	A
IRFD312/313, IRFD312R/313R			0.3	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD310/311, IRFD310R/311R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.2A	-	3.3	3.6	Ω
IRFD312/313, IRFD312R/313R			-	3.6	5.0	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = 0.2A	0.5	1.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	135	-	pF
Output Capacitance	C_{OSS}		-	35	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	8.0	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.4A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature)	-	3.0	10	ns
Rise Time	t_r		-	10	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	5.0	10	ns
Fall Time	t_f		-	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.4A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	6.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	3.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	0.4	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	1.6	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.6A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/μs	-	380	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/μs	-	2.7	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.4A. (See Figure 15.)

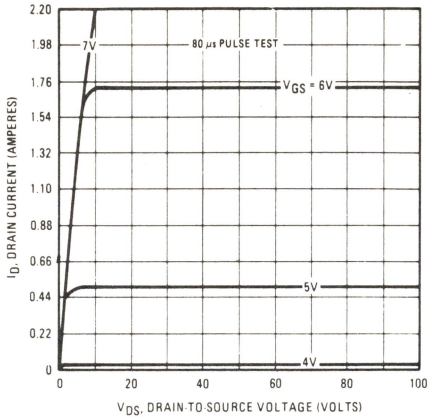


Fig. 1 — Typical Output Characteristics

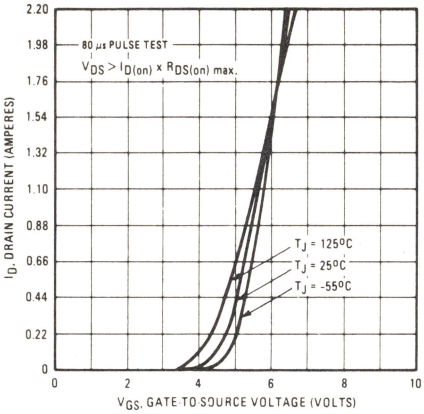


Fig. 2 — Typical Transfer Characteristics

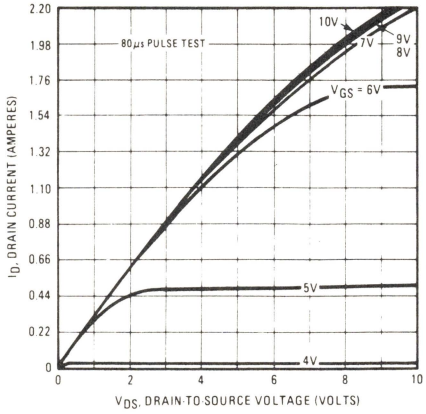


Fig. 3 — Typical Saturation Characteristics

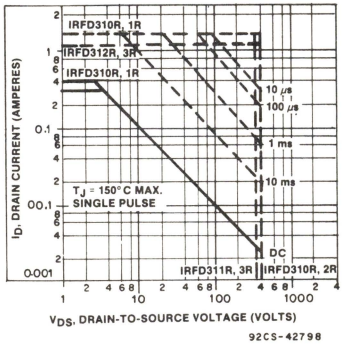


Fig. 4 — Maximum Safe Operating Area

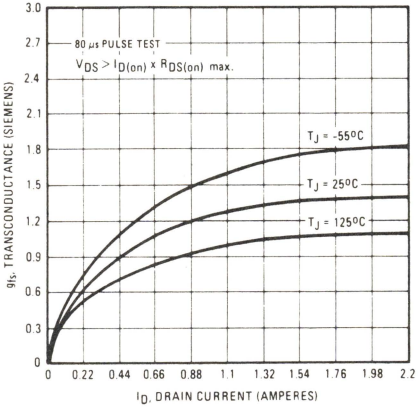


Fig. 5 — Typical Transconductance Vs. Drain Current

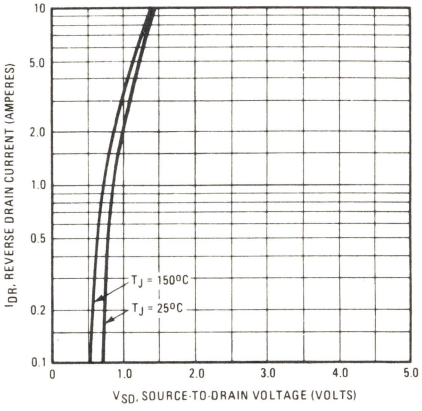


Fig. 6 — Typical Source-Drain Diode Forward Voltage

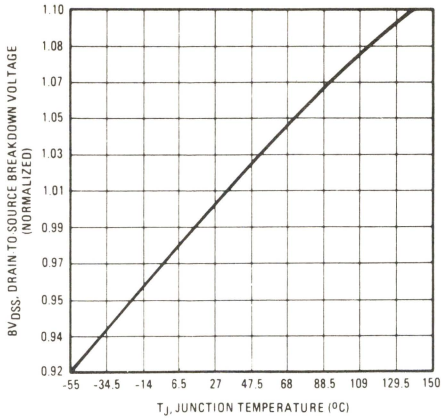


Fig. 7 — Breakdown Voltage Vs. Temperature

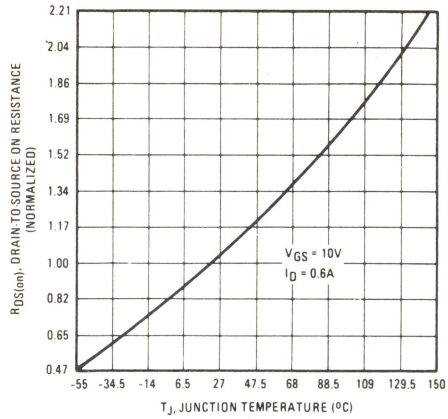


Fig. 8 — Normalized On-Resistance Vs. Temperature

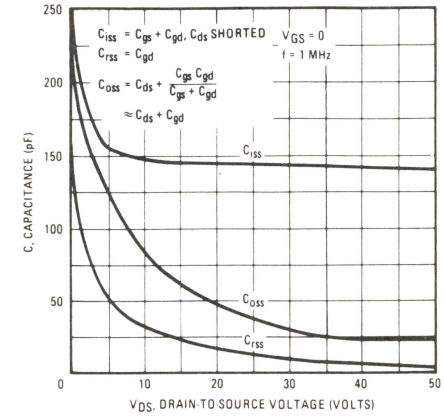


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

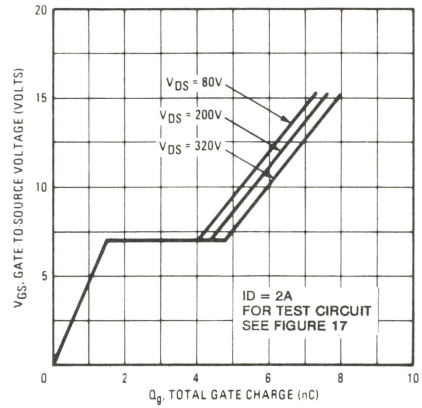


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

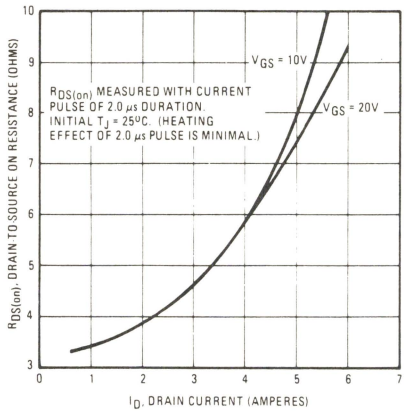


Fig. 11 — Typical On-Resistance Vs. Drain Current

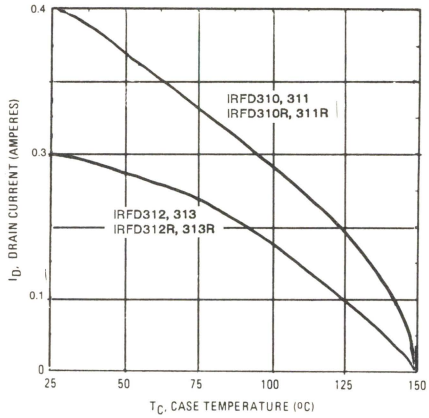


Fig. 12 — Maximum Drain Current Vs. Case Temperature

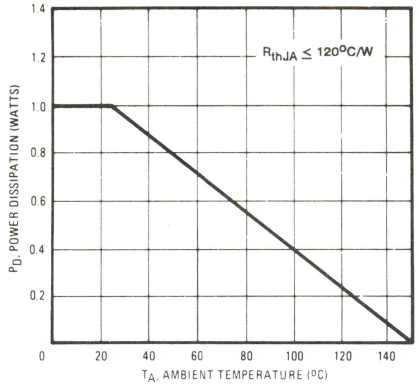


Fig. 13 - Power Vs. Temperature Derating Curve

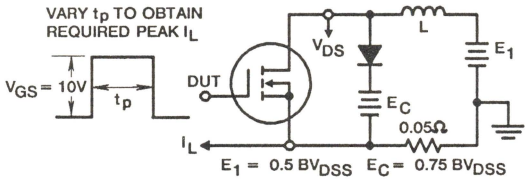


Fig. 14a - Clamped Inductive Test Circuit

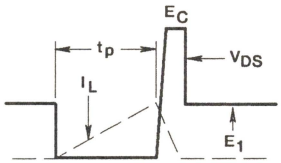


Fig. 14b - Clamped Inductive Waveforms

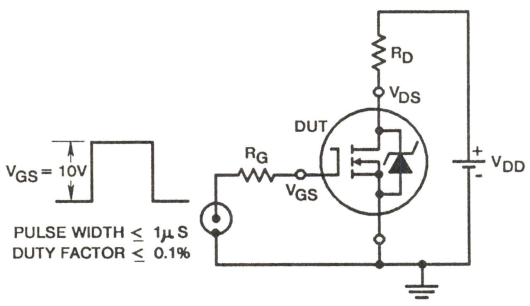


Fig. 16 - Switching Time Test Circuit

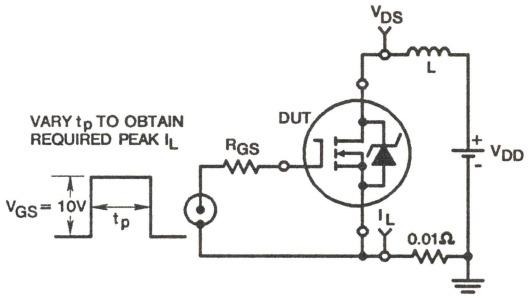


Fig. 15a - Unclamped Energy Test Circuit

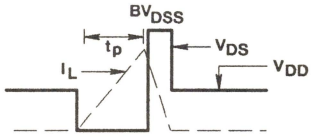


Fig. 15b - Unclamped Energy Waveforms

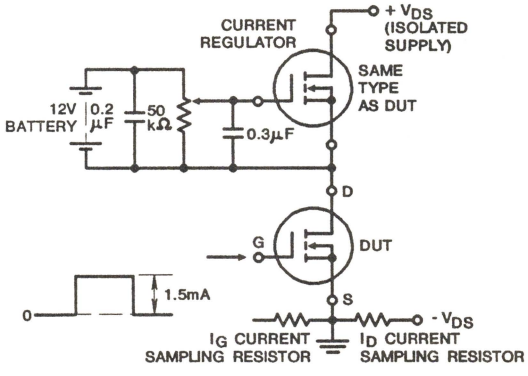


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFD320/321/322/323
IRFD320R/321R/322R/323R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 0.5A and 0.4A, 350V - 400V
- $r_{DS(on)}$ = 1.8Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

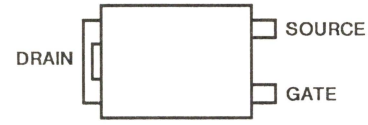
Description

The IRFD320, IRFD332, IRFD322, and IRFD323 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD320R, IRFD332R, IRFD322R, and IRFD323R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

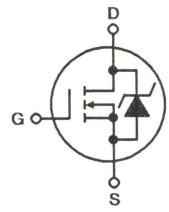
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD320 IRFD320R	IRFD332 IRFD332R	IRFD322 IRFD322R	IRFD323 IRFD323R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	0.5	0.5	0.4	0.4	A
Pulsed Drain Current (3) ..... I_{DM}	2.0	2.0	1.6	1.6	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	2.0	2.0	1.6	1.6	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	100	100	100	100	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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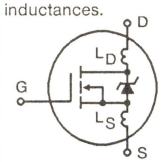
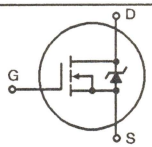
File Number 2325.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD320/322, IRFD320R/322R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
IRFD321/323, IRFD321R/323R			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFD320/321, IRFD320R/321R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	0.5	-	-	A
IRFD322/323, IRFD322R/323R			0.4	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD320/321, IRFD320R/321R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.25A	-	1.5	1.8	Ω
IRFD322/323, IRFD322R/323R			-	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.25A	1.0	2.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	455	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 0.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	25	50	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 0.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	12	15	nC
Gate-Source Charge	Q_{gs}		-	6.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	6.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	0.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	2.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.0A, V_{GS} = 0V	-	-	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.0A, dI_F/dt = 100A/μs	-	450	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.0A, dI_F/dt = 100A/μs	-	3.1	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. (See Figure 15.)

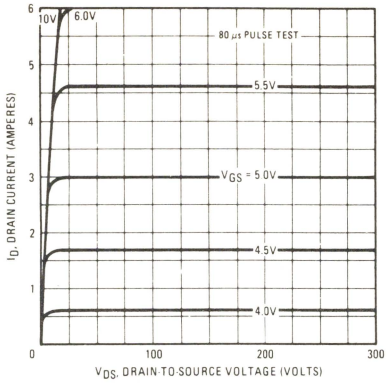


Fig. 1 — Typical Output Characteristics

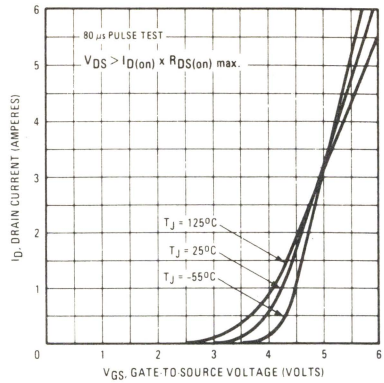


Fig. 2 — Typical Transfer Characteristics

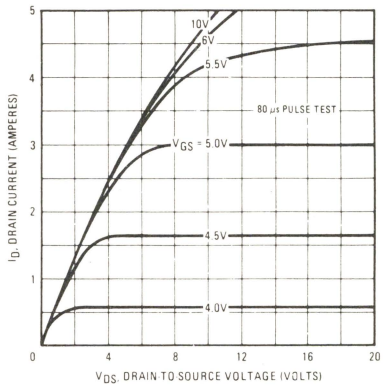


Fig. 3 — Typical Saturation Characteristics

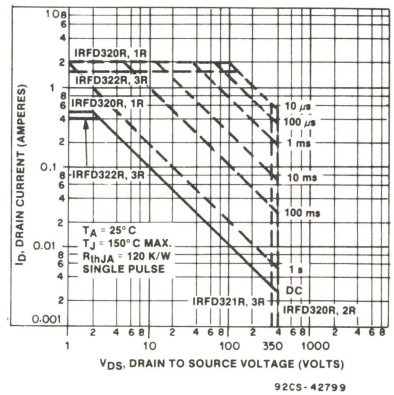


Fig. 4 — Maximum Safe Operating Area

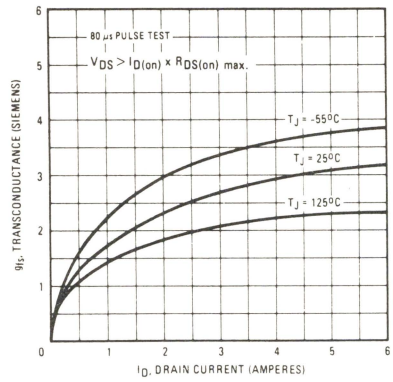


Fig. 5 — Typical Transconductance Vs. Drain Current

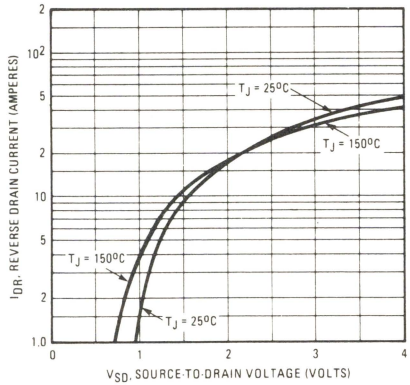


Fig. 6 — Typical Source-Drain Diode Forward Voltage

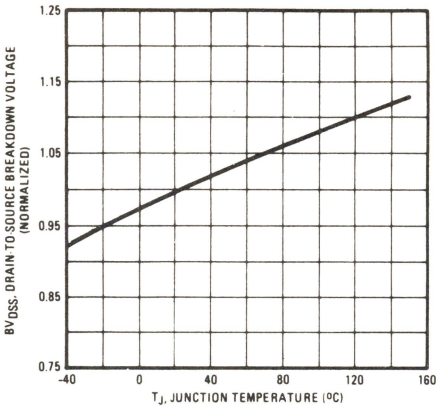


Fig. 7 — Breakdown Voltage Vs. Temperature

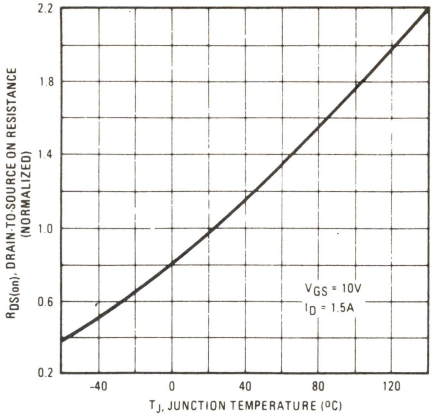


Fig. 8 — Normalized On-Resistance Vs. Temperature

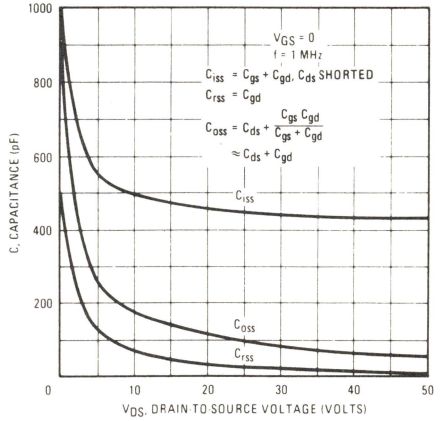


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

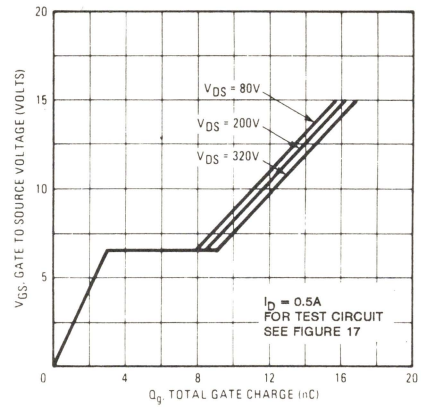


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

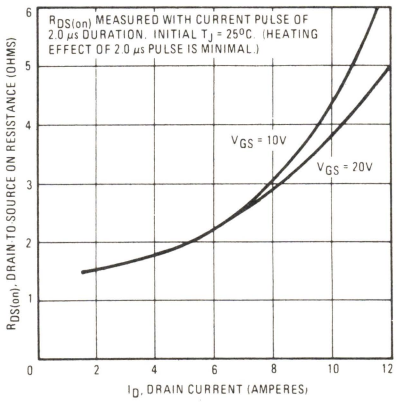


Fig. 11 — Typical On-Resistance Vs. Drain Current

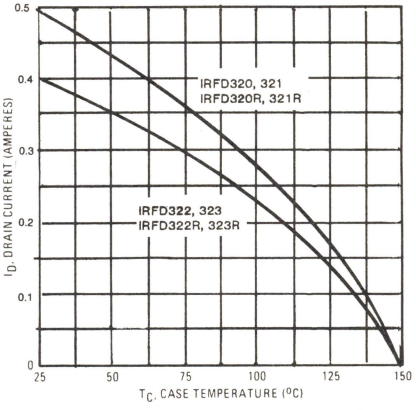


Fig. 12 — Maximum Drain Current Vs. Case Temperature

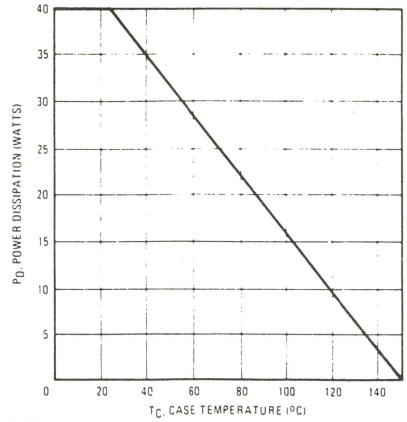


Fig. 13 - Power Vs. Temperature Derating Curve

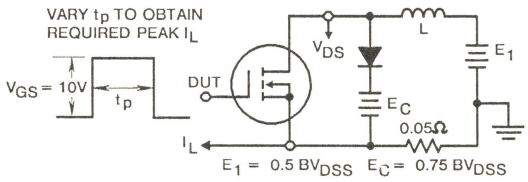


Fig. 14a - Clamped Inductive Test Circuit

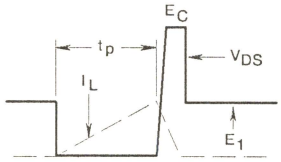


Fig. 14b - Clamped Inductive Waveforms

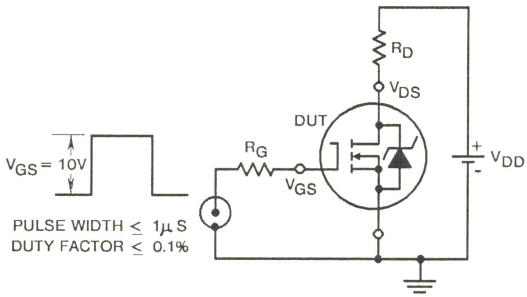


Fig. 16 - Switching Time Test Circuit

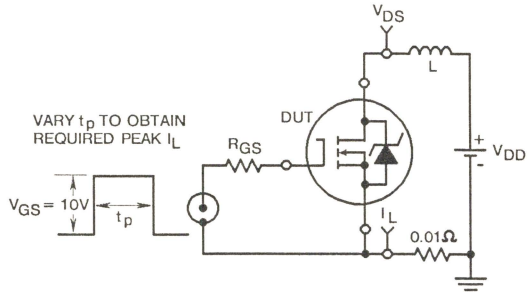


Fig. 15a - Unclamped Energy Test Circuit

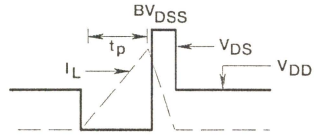


Fig. 15b - Unclamped Energy Waveforms

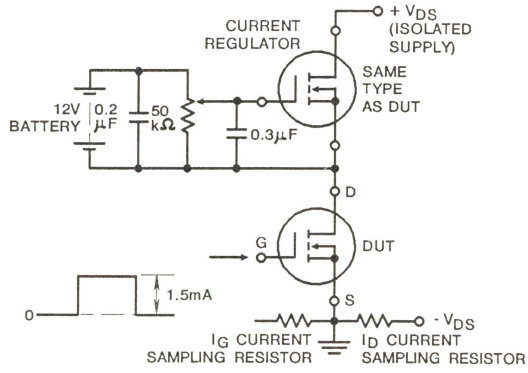


Fig. 17 - Gate Charge Test Circuit

IRFF110/111/112/113
IRFF110R/111R/112R/113R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 3.0A and 3.5A, 80V - 100V
- $r_{DS(on)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

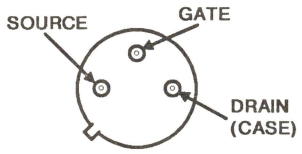
Description

The IRFF110, IRFF111, IRFF112, and IRFF113 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF110R, IRFF111R, IRFF112R, and IRFF113R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

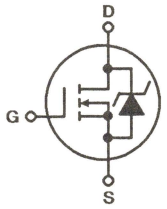
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF110 IRFF110R	IRFF111 IRFF111R	IRFF112 IRFF112R	IRFF113 IRFF113R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	14	14	12	12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	15	15	15	15	W
Linear Derating Factor	0.12	0.12	0.12	0.12	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	14	14	12	12	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	19	19	19	19	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 5V, starting T_J = +25°C, L = 2.3mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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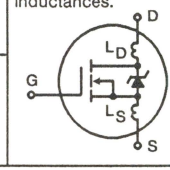
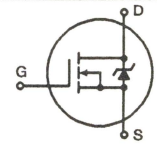
File Number **1562.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF110/112, IRFF110R/112R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	-	-	V
IRFF111/113, IRFF111R/113R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFF110/111, IRFF110R/111R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.5	-	-	A
IRFF112/113, IRFF112R/113R			3.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF110/111, IRFF110R/111R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.5A	-	0.5	0.6	Ω
IRFF112/113, IRFF112R/113R			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.5A	1.0	1.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	135	-	pF
Output Capacitance	C_{OSS}		-	80	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	20	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 3.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	10	20	ns
Rise Time	t_r		-	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	15	25	ns
Fall Time	t_f		-	10	20	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	5.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	2.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	8.33	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.5A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/μs	-	200	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/μs	-	1.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 5V, starting T_J = +25°C, L = 2.3mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. (See Figure 15.)

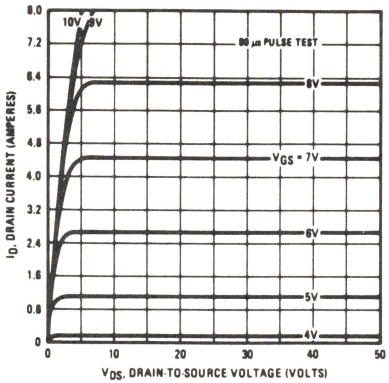


Fig. 1 – Typical Output Characteristics

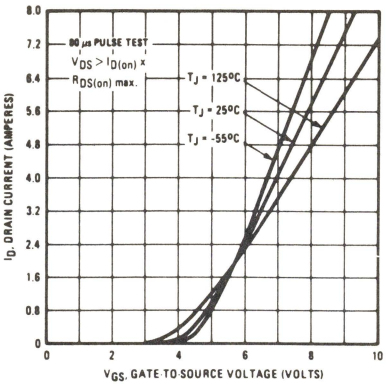


Fig. 2 – Typical Transfer Characteristics

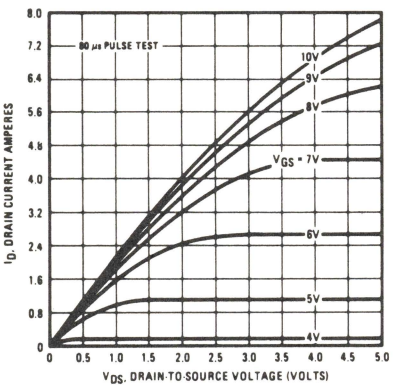


Fig. 3 – Typical Saturation Characteristics

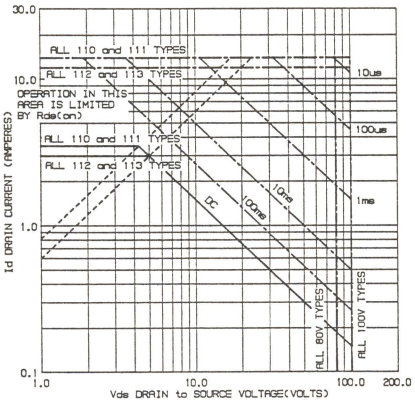


Fig. 4 – Maximum Safe Operating Area

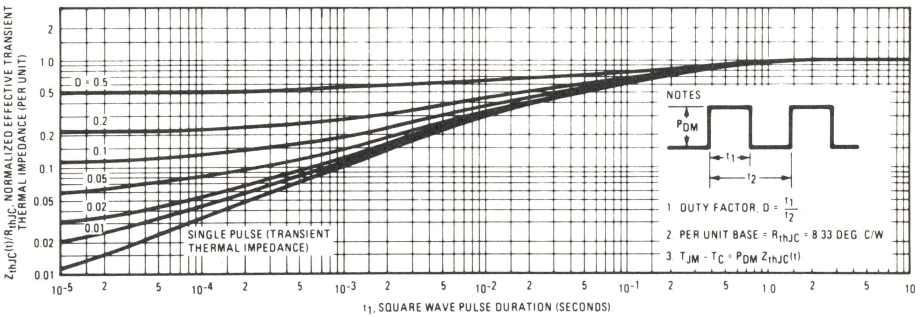


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

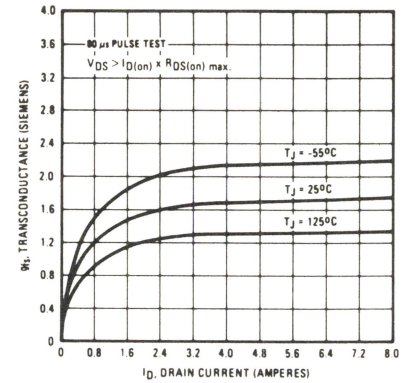


Fig. 6 – Typical Transconductance Vs. Drain Current

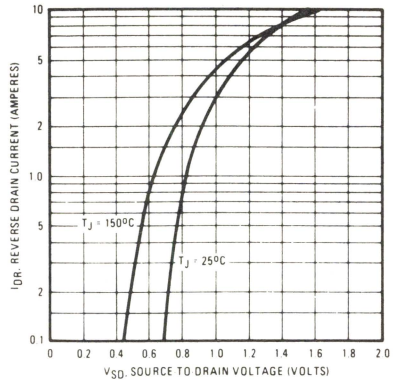


Fig. 7 – Typical Source-Drain Diode Forward Voltage

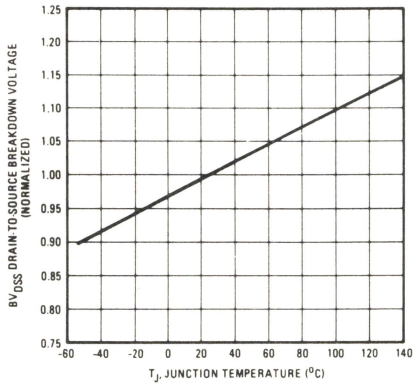


Fig. 8 – Breakdown Voltage Vs. Temperature

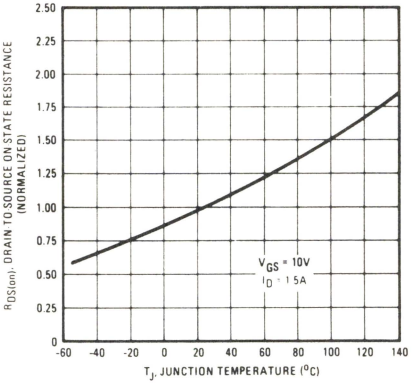


Fig. 9 – Normalized On-Resistance Vs. Temperature

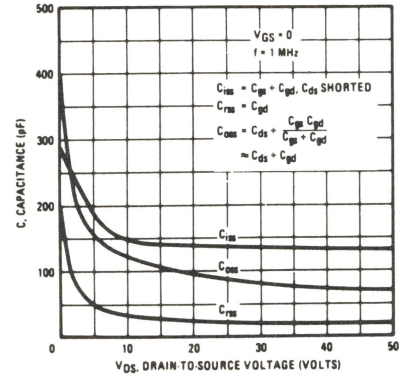


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

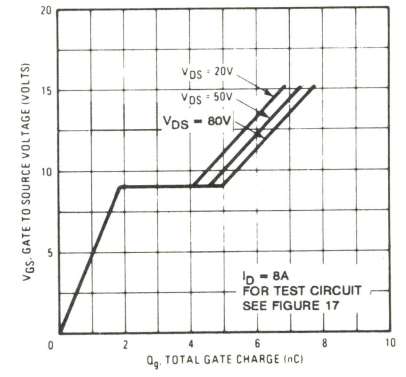


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

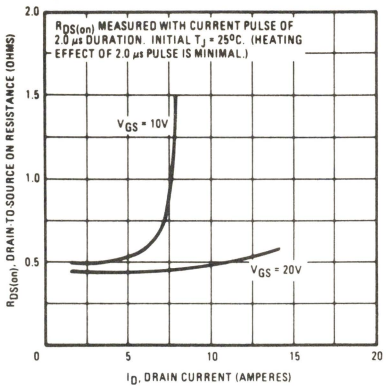


Figure 12 - Typical On-Resistance Vs. Drain Current

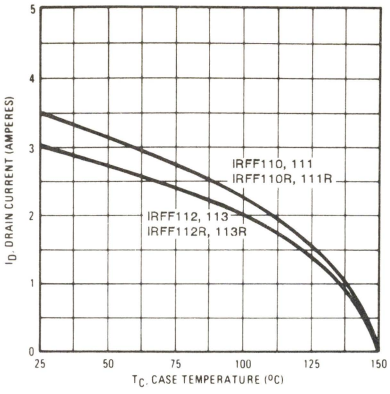


Fig. 13 - Maximum Drain Current Vs. Case Temperature

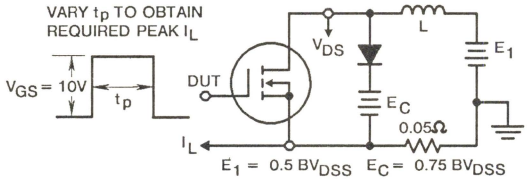


Fig. 14a - Clamped Inductive Test Circuit

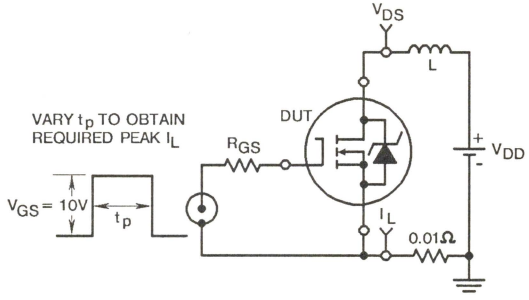


Fig. 15a - Unclamped Energy Test Circuit

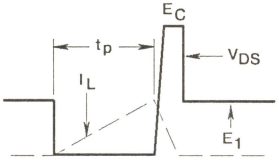


Fig. 14b - Clamped Inductive Waveforms

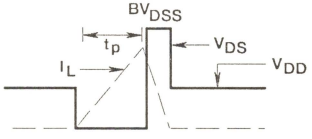


Fig. 15b - Unclamped Energy Waveforms

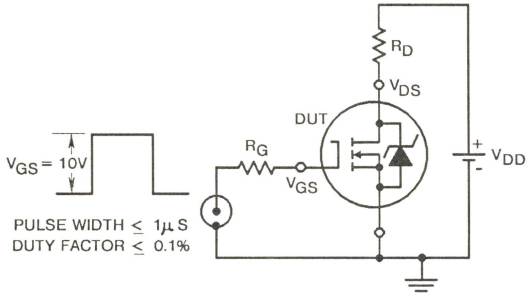


Fig. 16 - Switching Time Test Circuit

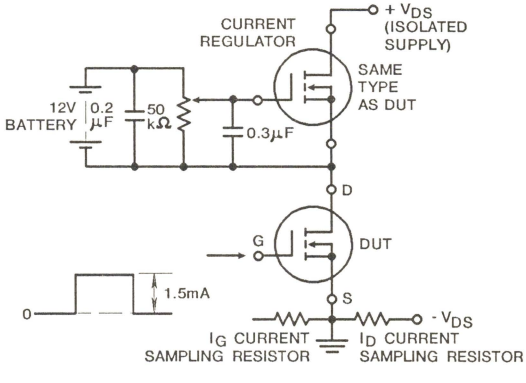


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFF120/121/122/123
IRFF120R/121R/122R/123R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 5.0A and 6.0A, 80V - 100V
- $r_{DS(on)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

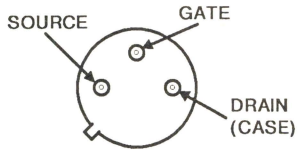
Description

The IRFF120, IRFF121, IRFF122, and IRFF123 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF120R, IRFF121R, IRFF122R, and IRFF123R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

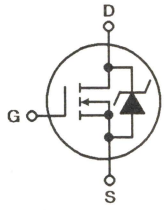
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF120 IRFF120R	IRFF121 IRFF121R	IRFF122 IRFF122R	IRFF123 IRFF123R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	6.0	6.0	5.0	5.0	A
Pulsed Drain Current (3) ..... I_{DM}	24	24	20	20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	24	24	20	20	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	36	36	36	36	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 6.0A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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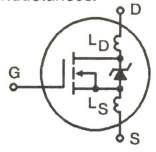
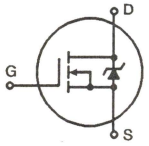
File Number **1563.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF120/122, IRFF120R/122R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	-	-	V
IRFF121/123, IRFF121R/123R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFF120/121, IRFF120R/121R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	6.0	-	-	A
IRFF122/123, IRFF122R/123R			5.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF120/121, IRFF120R/121R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	-	0.25	0.30	Ω
IRFF122/123, IRFF122R/123R			-	0.30	0.40	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 3.0A	1.5	2.9	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	450	-	pF
Output Capacitance	C_{OSS}		-	20	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 6.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t_r		-	37	70	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	35	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	10	15	nC
Gate-Source Charge	Q_{gs}		-	6.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	6.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	24	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 6.0A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 6.0A, dI_F/dt = 100A/μs	-	230	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 6.0A, dI_F/dt = 100A/μs	-	1.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 5V, starting T_J = +25°C, L = 1.5mH, R_{GS} = 25Ω, I_{PEAK} = 6.0A. (See Figure 15.)

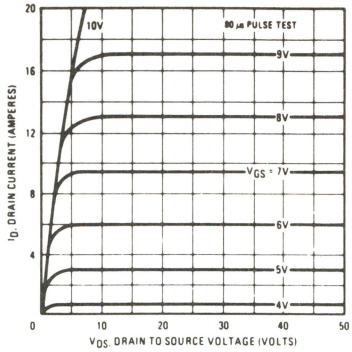


Fig. 1 – Typical Output Characteristics

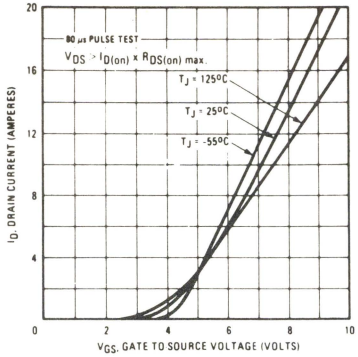


Fig. 2 – Typical Transfer Characteristics

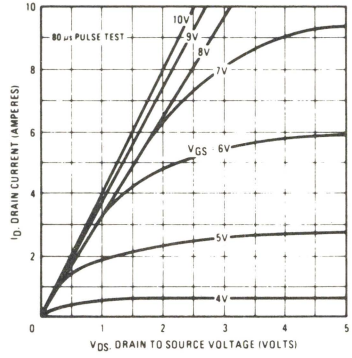


Fig. 3 – Typical Saturation Characteristics

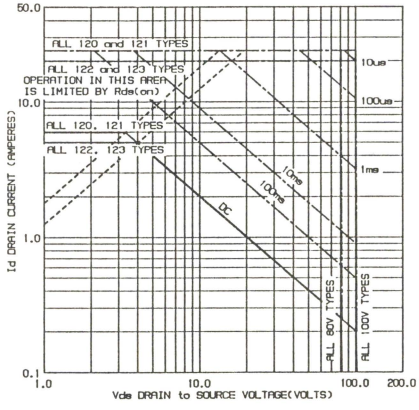


Fig. 4 – Maximum Safe Operating Area

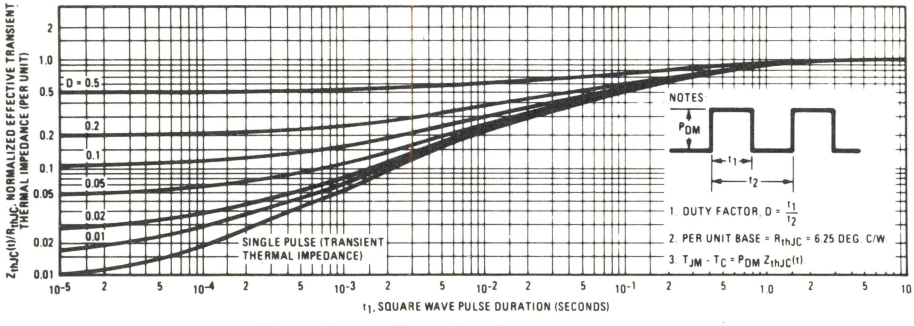


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

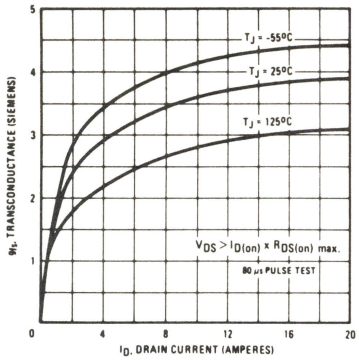


Fig. 6 – Typical Transconductance Vs. Drain Current

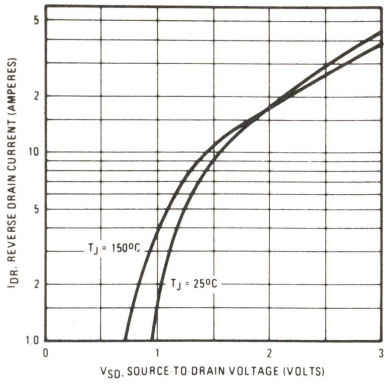


Fig. 7 – Typical Source-Drain Diode Forward Voltage

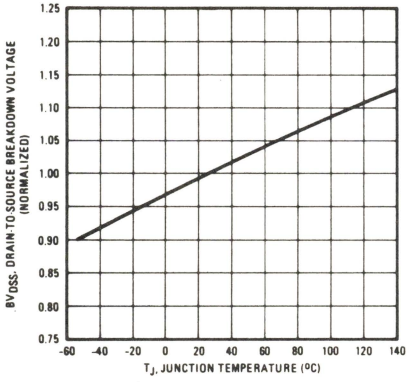


Fig. 8 – Breakdown Voltage Vs. Temperature

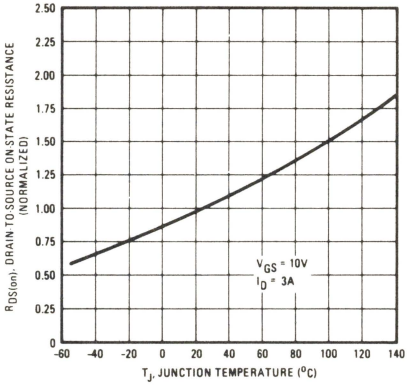


Fig. 9 – Normalized On-Resistance Vs. Temperature

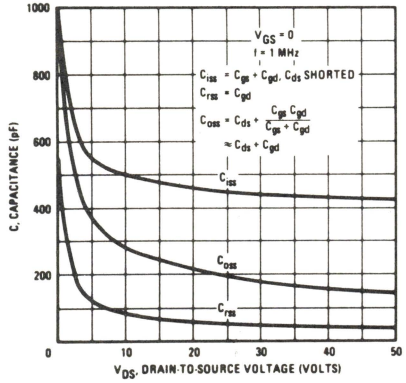


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

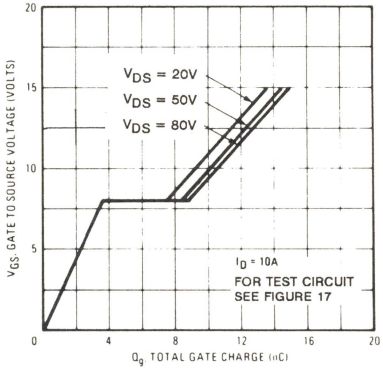


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

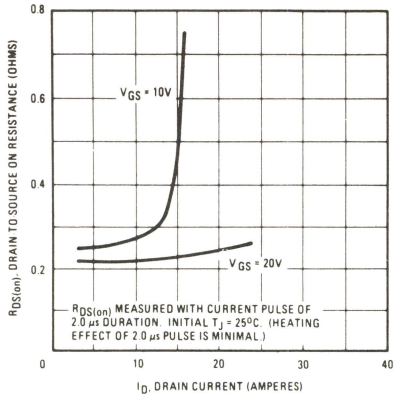


Figure 12 - Typical On-Resistance Vs. Drain Current

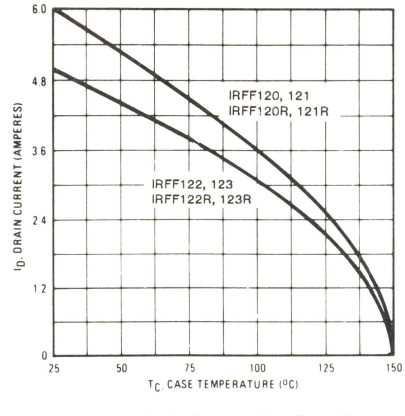


Fig. 13 - Maximum Drain Current Vs. Case Temperature

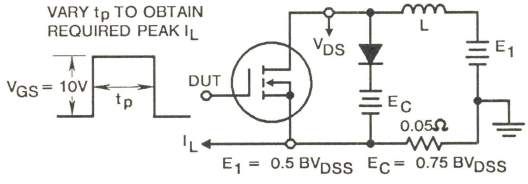


Fig. 14a - Clamped Inductive Test Circuit

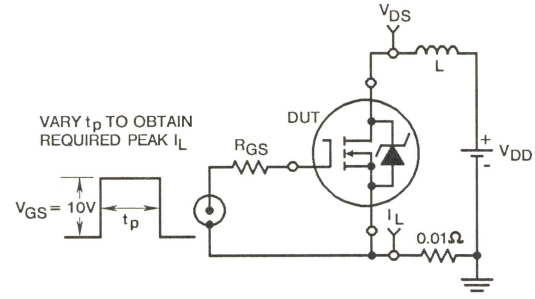


Fig. 15a - Unclamped Energy Test Circuit

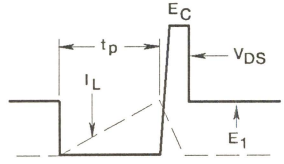


Fig. 14b - Clamped Inductive Waveforms

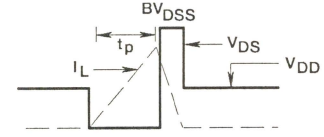


Fig. 15b - Unclamped Energy Waveforms

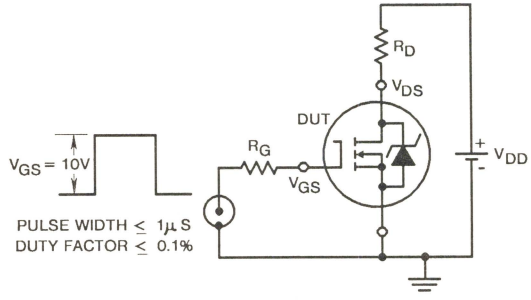


Fig. 16 - Switching Time Test Circuit

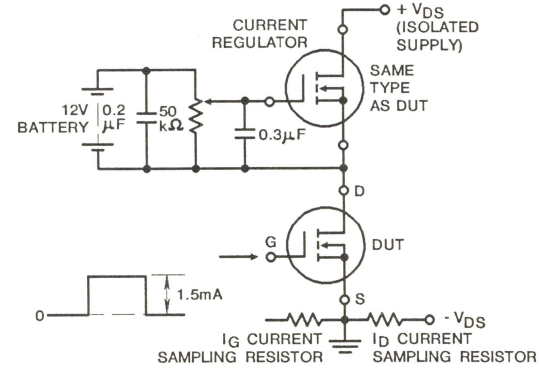


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFF130/131/132/133
IRFF130R/131R/132R/133R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 7.0A and 8.0A, 80V - 100V
- $r_{DS(on)}$ = 0.18Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

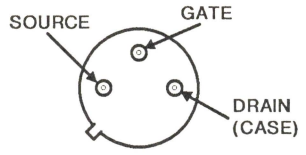
Description

The IRFF130, IRFF131, IRFF132, and IRFF133 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF130R, IRFF131R, IRFF132R, and IRFF133R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

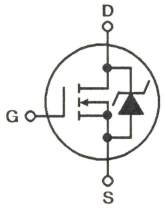
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF130 IRFF130R	IRFF131 IRFF131R	IRFF132 IRFF132R	IRFF133 IRFF133R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	8.0	8.0	7.0	7.0	A
Pulsed Drain Current (3) ..... I_{DM}	32	32	28	28	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	32	32	28	28	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	69	69	69	69	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 1.62mH, R_{GS} = 25Ω, I_{PEAK} = 8.0A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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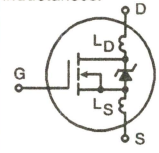
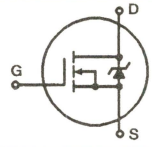
File Number 1564.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF130/132, IRFF130R/132R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	–	–	V
IRFF131/133, IRFF131R/133R			80	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF130/131, IRFF130R/131R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	8.0	–	–	A
IRFF132/133, IRFF132R/133R			7.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF130/131, IRFF130R/131R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.0A	–	0.14	0.18	Ω
IRFF132/133, IRFF132R/133R			–	0.20	0.25	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 4.0A	4.0	5.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	300	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 8.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	30	50	ns
Rise Time	t_r		–	80	150	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	80	150	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	18	30	nC
Gate-Source Charge	Q_{gs}		–	9.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	9.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	8.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	32	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.0A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 8.0A, dI_F/dt = 100A/μs	–	300	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 8.0A, dI_F/dt = 100A/μs	–	1.5	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 25V, starting T_J = +25°C, L = 1.62mH, R_{GS} = 25Ω, I_{PEAK} = 8.0A. (See Figure 15.)

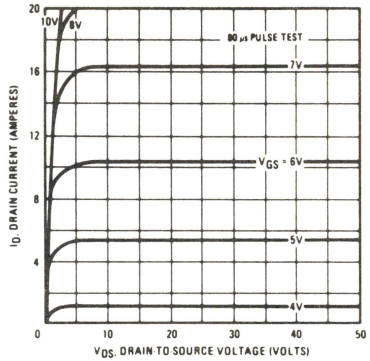


Fig. 1 – Typical Output Characteristics

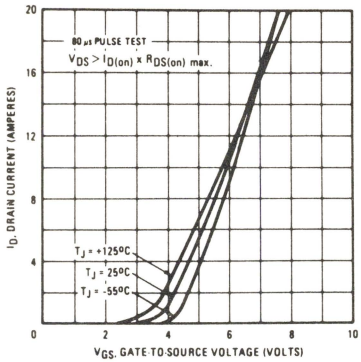


Fig. 2 – Typical Transfer Characteristics

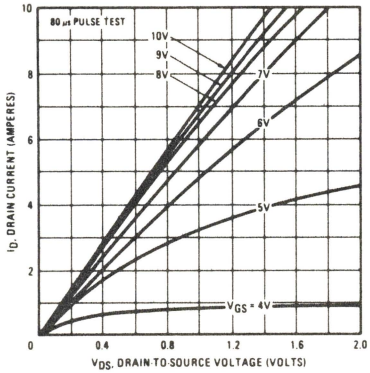


Fig. 3 – Typical Saturation Characteristics

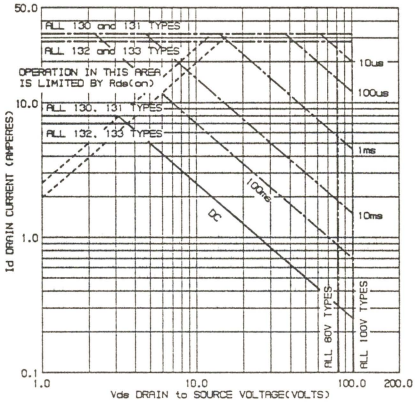


Fig. 4 – Maximum Safe Operating Area

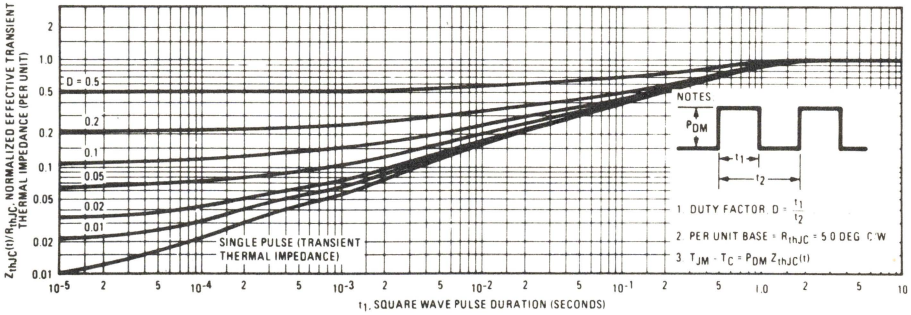


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

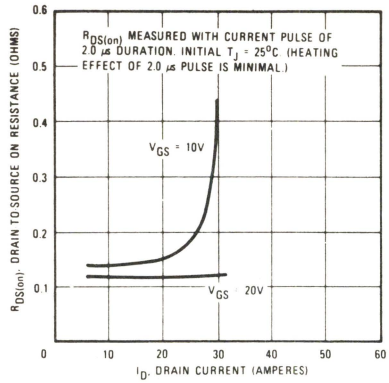


Figure 12 - Typical On-Resistance Vs. Drain Current

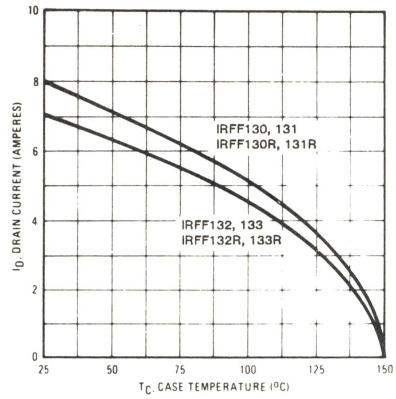


Fig. 13 - Maximum Drain Current Vs. Case Temperature

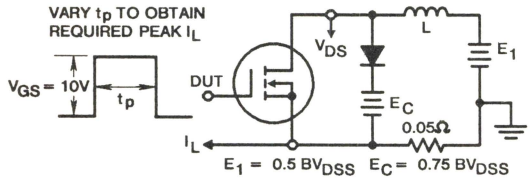


Fig. 14a - Clamped Inductive Test Circuit

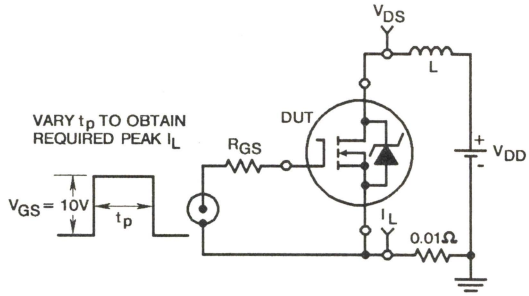


Fig. 15a - Unclamped Energy Test Circuit

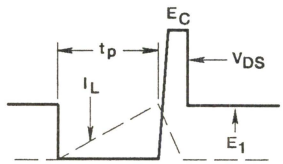


Fig. 14b - Clamped Inductive Waveforms

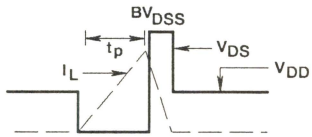


Fig. 15b - Unclamped Energy Waveforms

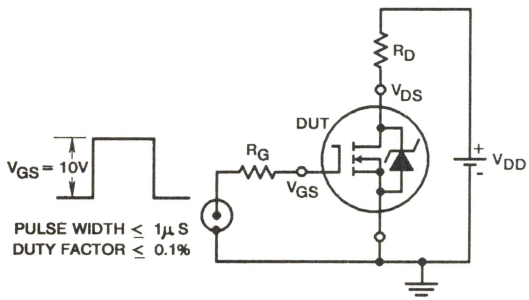


Fig. 16 - Switching Time Test Circuit

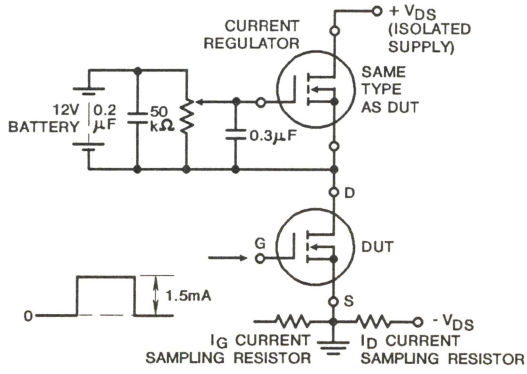


Fig. 17 - Gate Charge Test Circuit

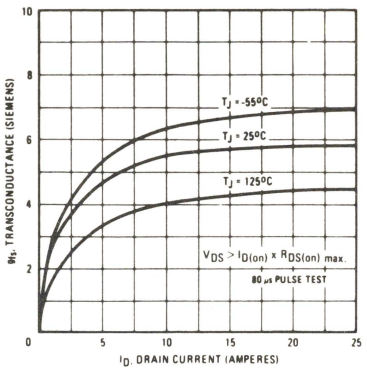


Fig. 6 – Typical Transconductance Vs. Drain Current

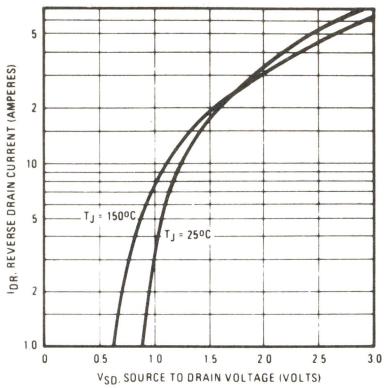


Fig. 7 – Typical Source-Drain Diode Forward Voltage

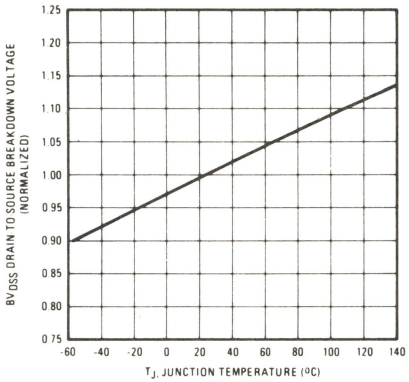


Fig. 8 – Breakdown Voltage Vs. Temperature

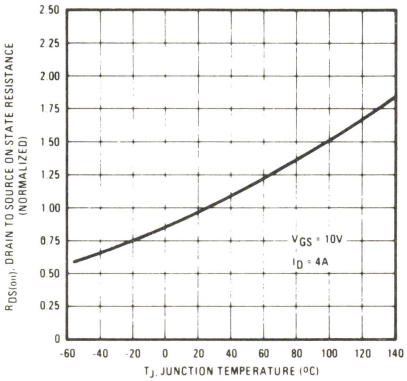


Fig. 9 – Normalized On-Resistance Vs. Temperature

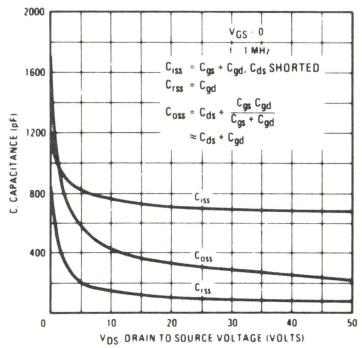


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

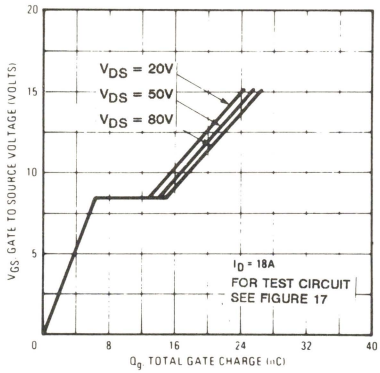


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

HARRIS

IRFF210/211/212/213
IRFF210R/211R/212R/213R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 1.8A and 2.2A, 150V - 200V
- $r_{DS(on)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

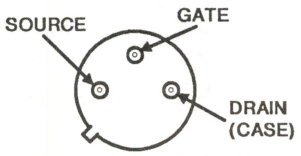
Description

The IRFF210, IRFF211, IRFF212, and IRFF213 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF210R, IRFF211R, IRFF212R, and IRFF213R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

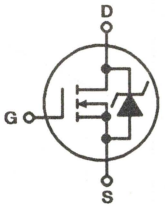
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF210 IRFF210R	IRFF211 IRFF211R	IRFF212 IRFF212R	IRFF213 IRFF213R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	2.2	2.2	1.8	1.8	A
Pulsed Drain Current (3) ..... I_{DM}	9.0	9.0	7.5	7.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	15	15	15	15	W
Linear Derating Factor	0.12	0.12	0.12	0.12	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	9.0	9.0	7.5	7.5	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	30	30	30	30	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 11.16mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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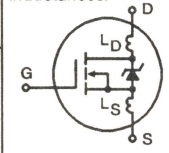
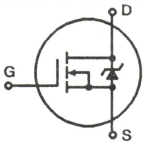
File Number **1887.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF210/212, IRFF210R/212R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	-	-	V
IRFF211/213, IRFF211R/213R			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFF210/211, IRFF210R/211R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	2.2	-	-	A
IRFF212/213, IRFF212R/213R			1.8	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF210/211, IRFF210R/211R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.25A	-	1.0	1.5	Ω
IRFF212/213, IRFF212R/213R			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.25A	0.8	1.3	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	135	-	pF
Output Capacitance	C_{OSS}		-	60	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	16	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 0.5BV_{DSS}, I_D = 2.2A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	8.0	15	ns
Rise Time	t_r		-	15	25	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	10	15	ns
Fall Time	t_f		-	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.2A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	5.0	7.5	nC
Gate-Source Charge	Q_{gs}		-	2.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	3.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	8.33	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	2.2	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	9.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.2A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.2A, dI_F/dt = 100A/μs	-	290	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.2A, dI_F/dt = 100A/μs	-	2.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 20V, starting T_J = +25°C, L = 11.16mH, R_{GS} = 50Ω, I_{PEAK} = 2.2A. (See Figure 15.)

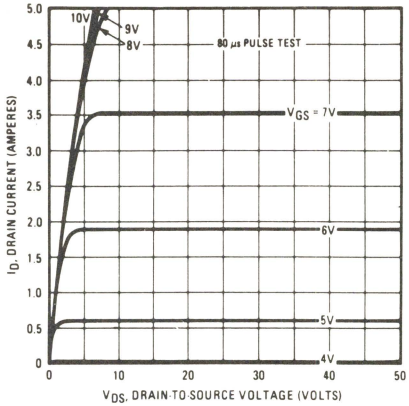


Fig. 1 - Typical output characteristics.

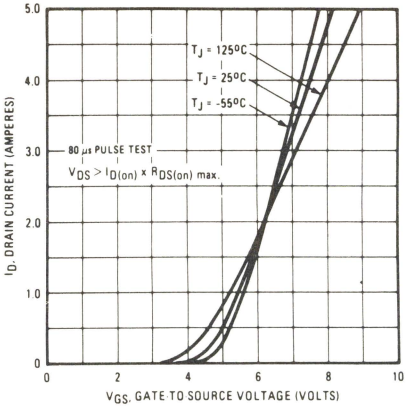


Fig. 2 - Typical transfer characteristics.

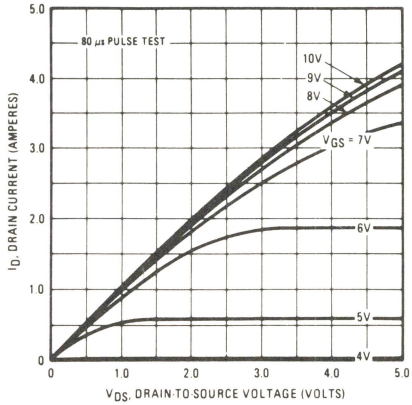


Fig. 3 - Typical saturation characteristics.

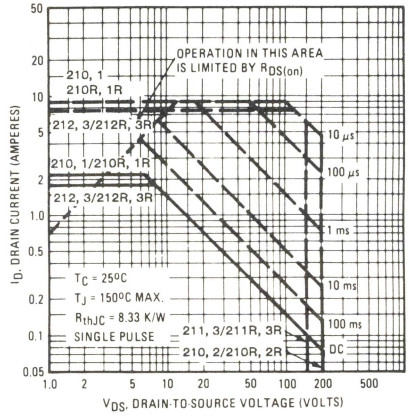


Fig. 4 - Maximum safe operating area.

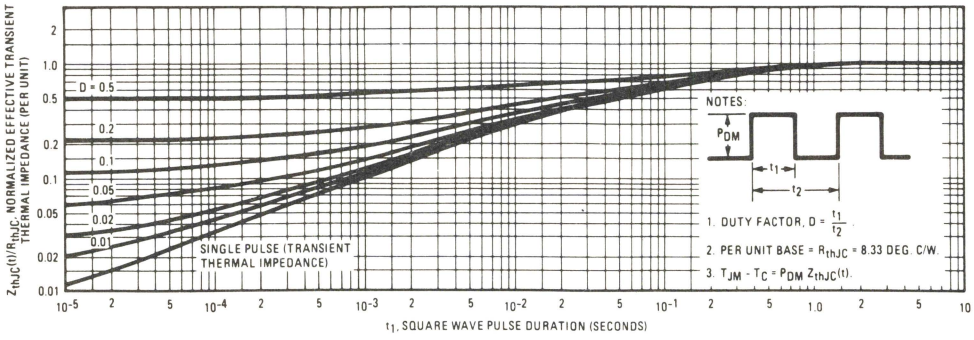


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

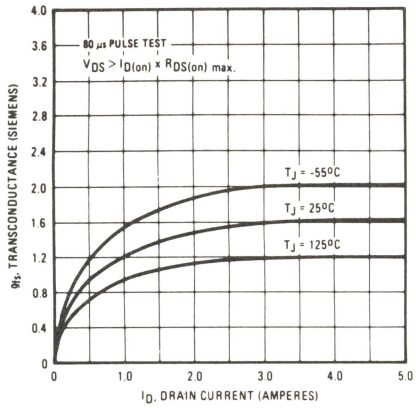


Fig. 6 - Typical transconductance vs. drain current.

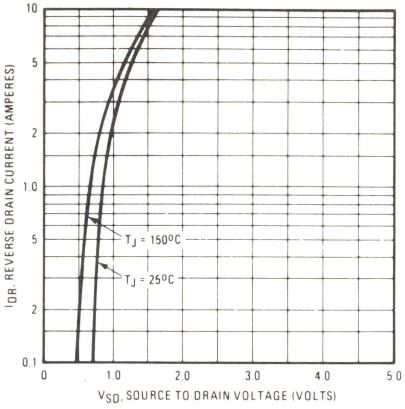


Fig. 7 - Typical source-drain diode forward voltage.

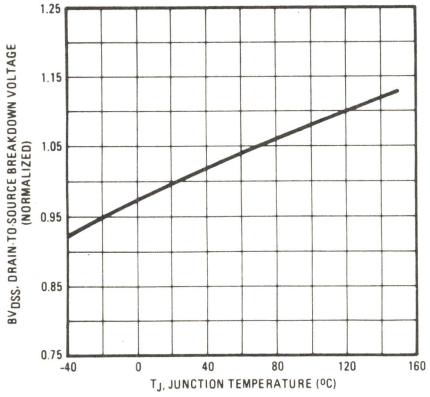


Fig. 8 - Breakdown voltage vs. temperature.

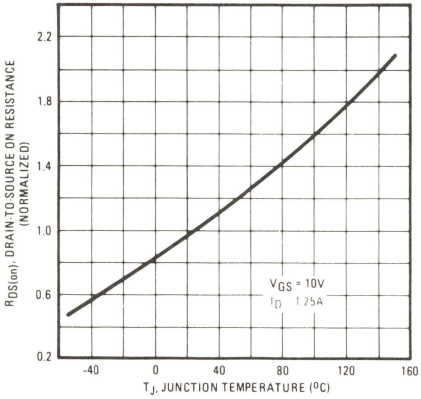


Fig. 9 - Normalized on-resistance vs. temperature.

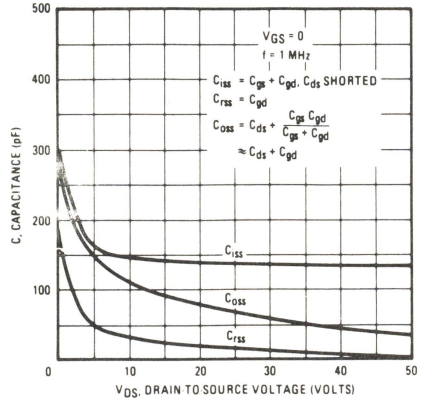


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

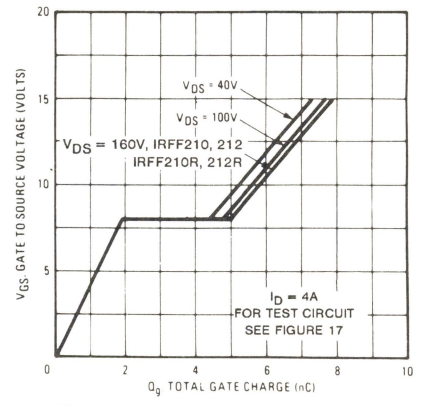


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

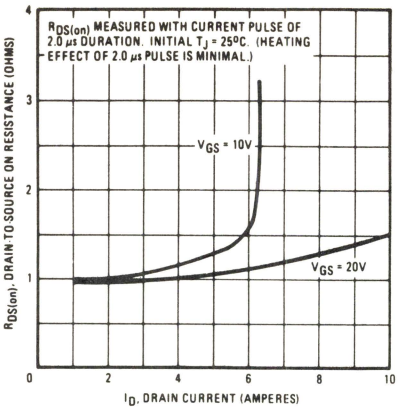


Figure 12 - Typical On-Resistance Vs. Drain Current

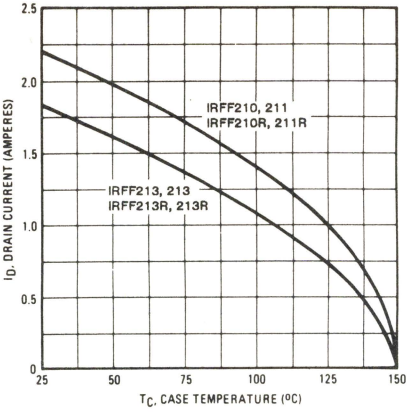


Fig. 13 - Maximum Drain Current Vs. Case Temperature

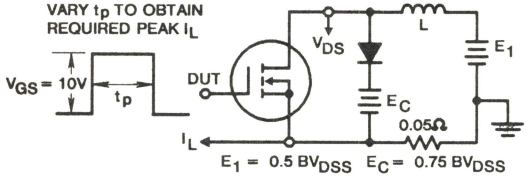


Fig. 14a - Clamped Inductive Test Circuit

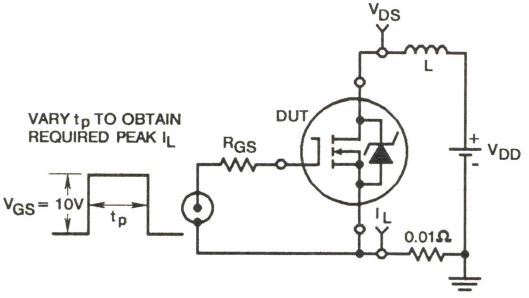


Fig. 15a - Unclamped Energy Test Circuit

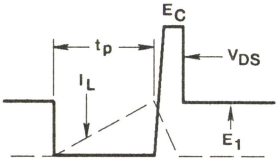


Fig. 14b - Clamped Inductive Waveforms

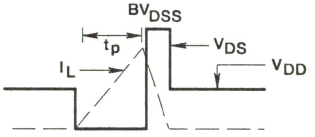


Fig. 15b - Unclamped Energy Waveforms

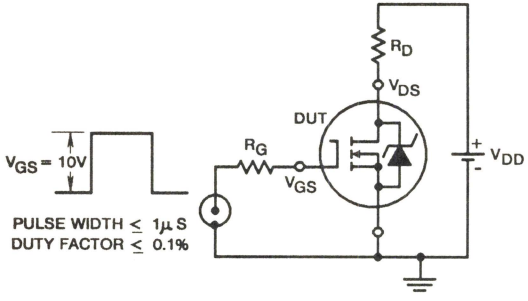


Fig. 16 - Switching Time Test Circuit

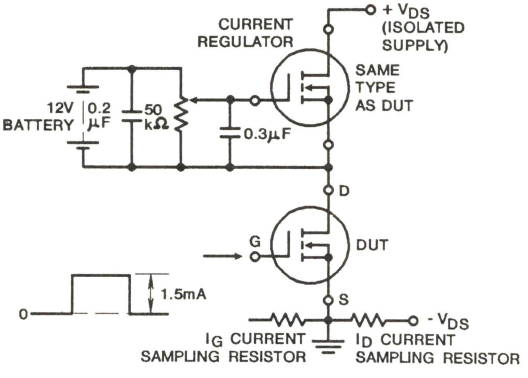


Fig. 17 - Gate Charge Test Circuit

IRFF220/221/222/223
IRFF220R/221R/222R/223R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 3.0A and 3.5A, 150V - 200V
- $r_{DS(on)}$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

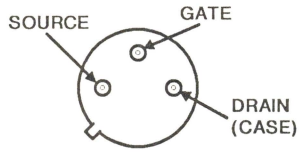
Description

The IRFF220, IRFF221, IRFF222, and IRFF223 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF220R, IRFF221R, IRFF222R, and IRFF223R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

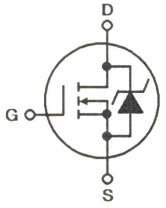
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF220 IRFF220R	IRFF221 IRFF221R	IRFF222 IRFF222R	IRFF223 IRFF223R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	14	14	12	12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	14	14	12	12	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	85	85	85	85	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 12.5mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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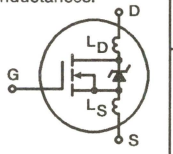
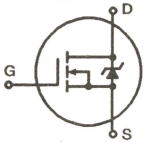
File Number **1889.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF220/222, IRFF220R/222R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRFF221/223, IRFF221R/223R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFF220/221, IRFF220R/221R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.5	–	–	A
IRFF222/223, IRFF222R/223R			3.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF220/221, IRFF220R/221R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.0A	–	0.5	0.8	Ω
IRFF222/223, IRFF222R/223R			–	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 2.0A	1.5	2.25	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	450	–	pF
Output Capacitance	C_{OSS}		–	150	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 3.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	30	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	5.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.5A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	–	350	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/µs	–	2.3	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle < 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 20V, starting T_J = +25°C, L = 12.5mH, R_{GS} = 50Ω, I_{PEAK} = 3.5A. (See Figure 15.)

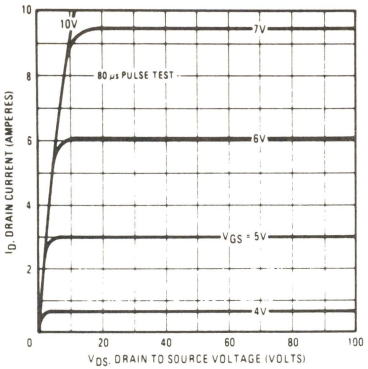


Fig. 1 - Typical output characteristics.

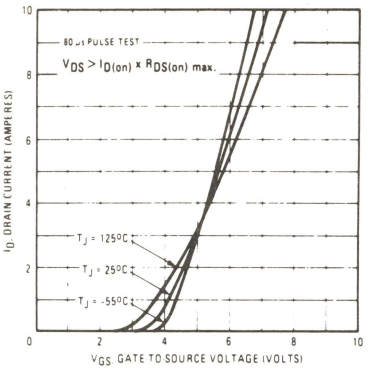


Fig. 2 - Typical transfer characteristics.

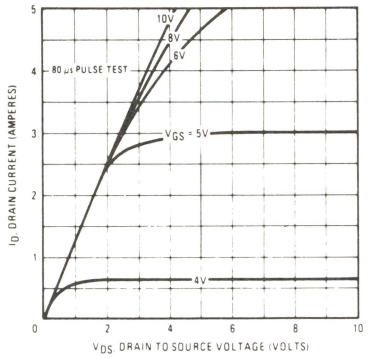


Fig. 3 - Typical saturation characteristics.

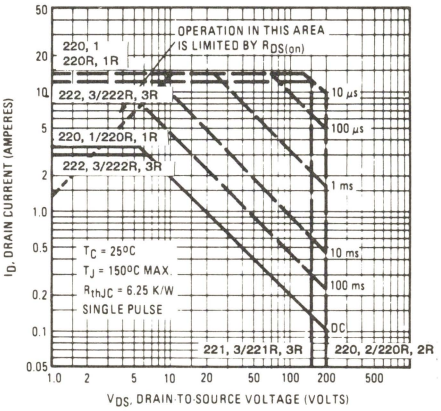


Fig. 4 - Maximum safe operating area.

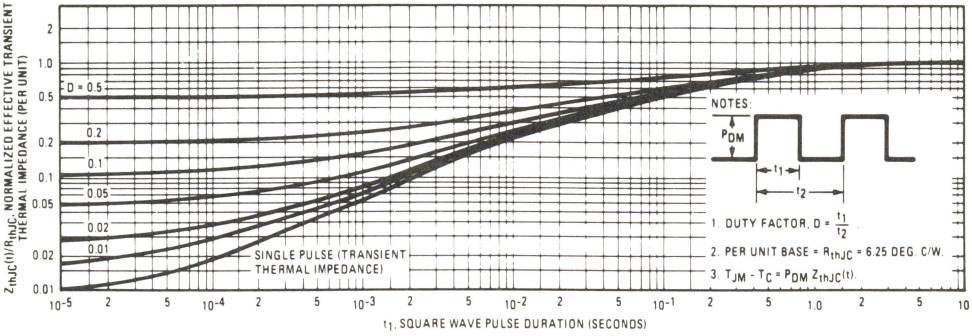


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

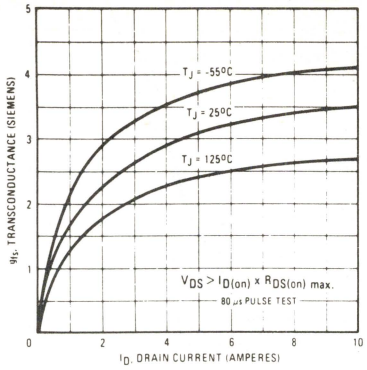


Fig. 6 - Typical transconductance vs. drain current.

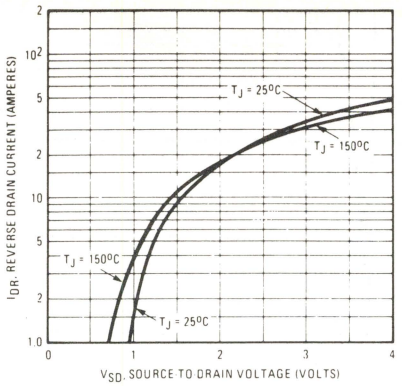


Fig. 7 - Typical source-drain diode forward voltage.

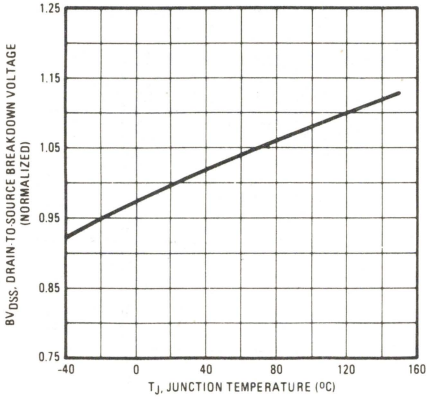


Fig. 8 - Breakdown voltage vs. temperature.

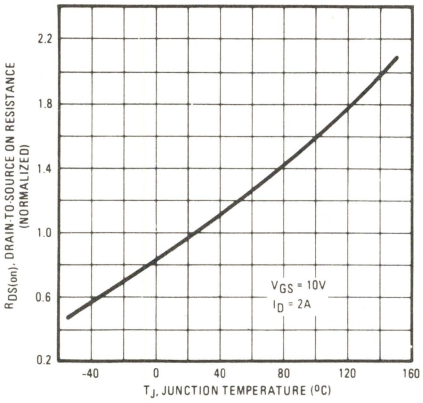


Fig. 9 - Normalized on-resistance vs. temperature.

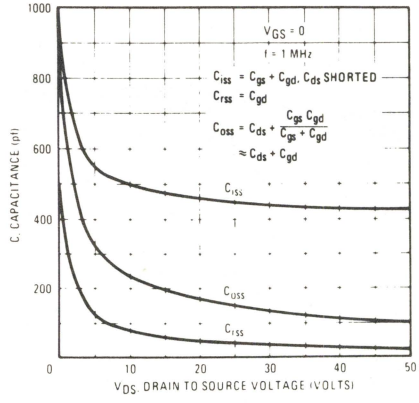


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

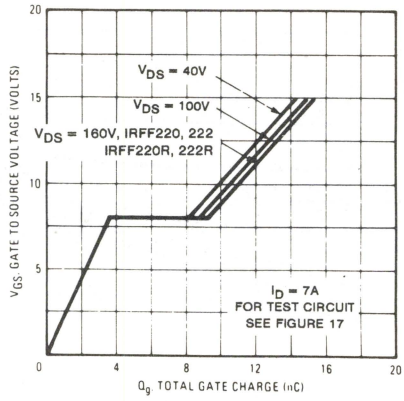


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

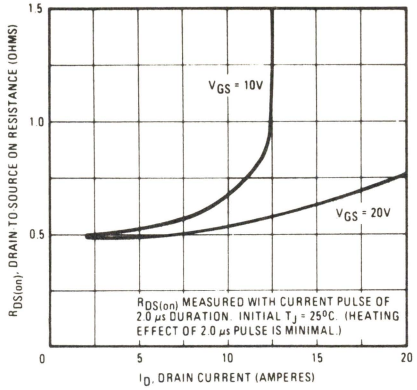


Figure 12 - Typical On-Resistance Vs. Drain Current

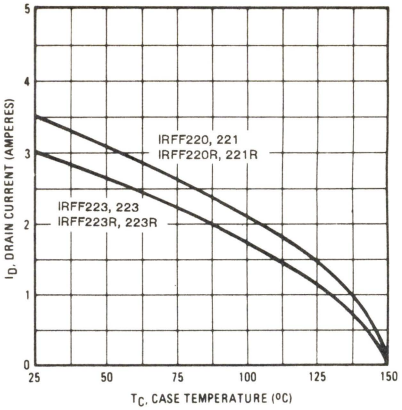


Fig. 13 - Maximum Drain Current Vs. Case Temperature

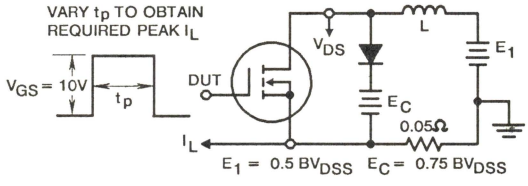


Fig. 14a - Clamped Inductive Test Circuit

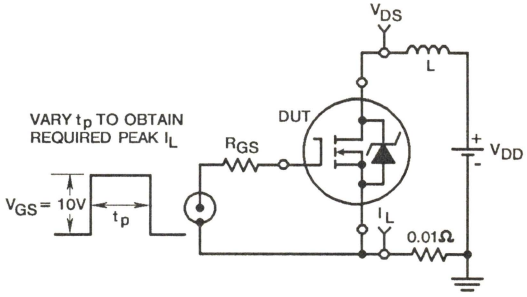


Fig. 15a - Unclamped Energy Test Circuit

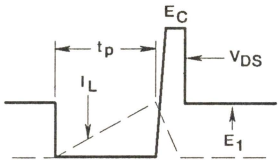


Fig. 14b - Clamped Inductive Waveforms

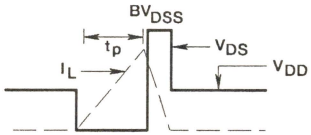


Fig. 15b - Unclamped Energy Waveforms

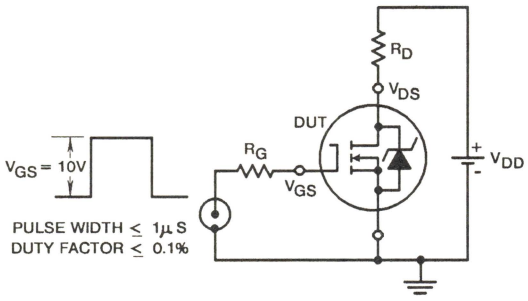


Fig. 16 - Switching Time Test Circuit

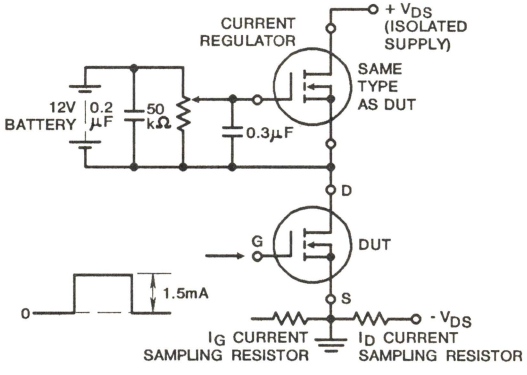


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFF230/231/232/233
IRFF230R/231R/232R/233R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 4.5A and 5.5A, 150V - 200V
- $r_{DS(on)}$ = 0.4Ω and 0.6Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

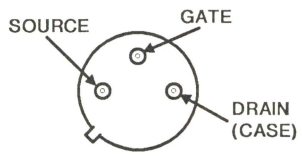
Description

The IRFF230, IRFF231, IRFF232, and IRFF233 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF230R, IRFF231R, IRFF232R, and IRFF233R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

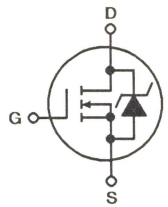
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF230 IRFF230R	IRFF231 IRFF231R	IRFF232 IRFF232R	IRFF233 IRFF233R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current T_C = +25°C ..... I_D	5.5	5.5	4.5	4.5	A
Pulsed Drain Current (3) ..... I_{DM}	22	22	18	18	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	22	22	18	18	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	85	85	85	85	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 20V, starting T_J = +25°C, L = 8.9mH, R_{GS} = 50Ω, I_{PEAK} = 5.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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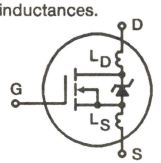
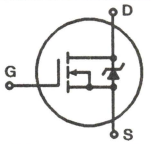
File Number **1892.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF230/232, IRFF230R/232R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	–	–	V
IRFF231/233, IRFF231R/233R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF230/231, IRFF230R/231R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	5.5	–	–	A
IRFF232/233, IRFF232R/233R			4.5	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF230/231, IRFF230R/231R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.0A	–	0.25	0.4	Ω
IRFF232/233, IRFF232R/233R			–	0.4	0.6	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 3.0A	2.5	4.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	250	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 5.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	30	ns
Rise Time	t_r		–	–	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	50	ns
Fall Time	t_f		–	–	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 5.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	19	30	nC
Gate-Source Charge	Q_{gs}		–	10	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	9.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	5.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	22	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 5.5A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 5.5A, dI_F/dt = 100A/μs	–	450	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 5.5A, dI_F/dt = 100A/μs	–	3.0	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 20V, starting T_J = +25°C, L = 8.9mH, R_{GS} = 50Ω, I_{PEAK} = 5.5A. (See Figure 15.)

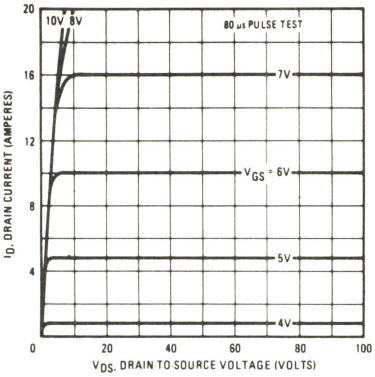


Fig. 1 - Typical output characteristics.

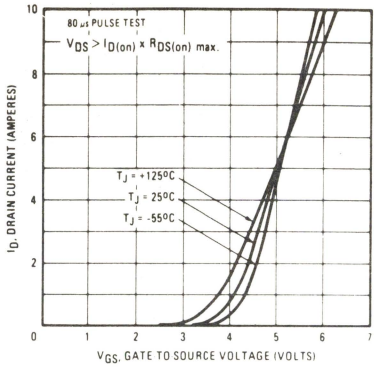


Fig. 2 - Typical transfer characteristics.

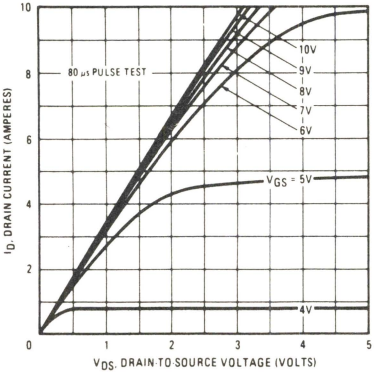


Fig. 3 - Typical saturation characteristics.

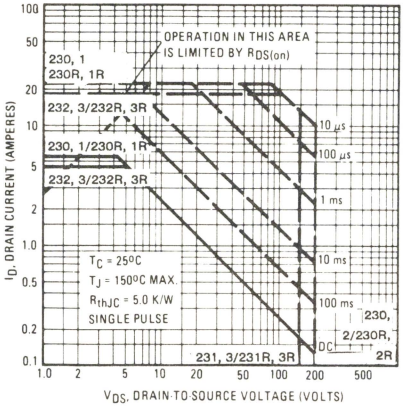


Fig. 4 - Maximum safe operating area.

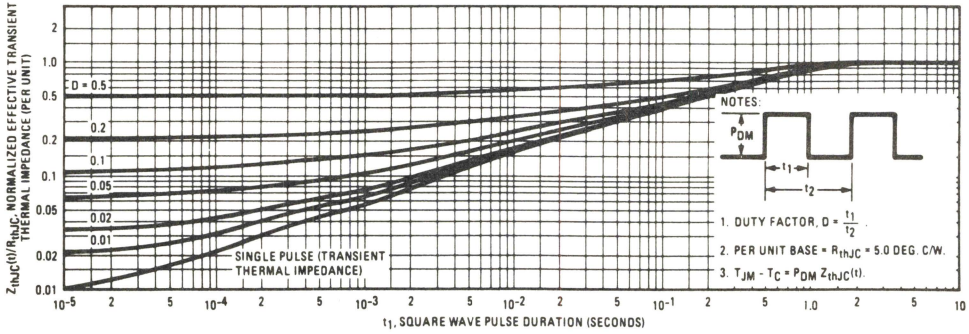


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

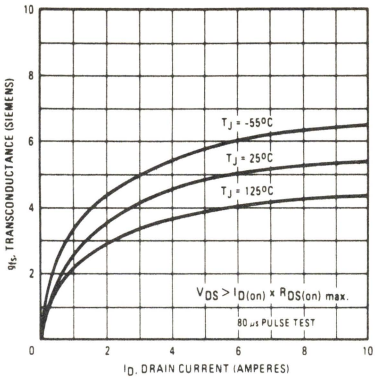


Fig. 6 - Typical transconductance vs. drain current.

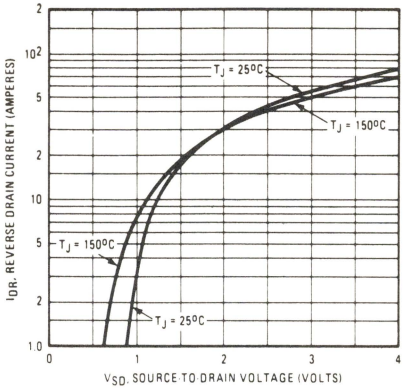


Fig. 7 - Typical source-drain diode forward voltage.

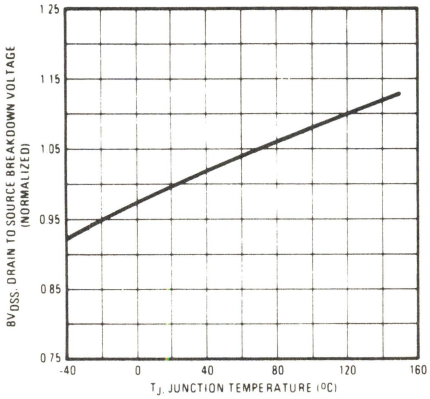


Fig. 8 - Breakdown voltage vs. temperature.

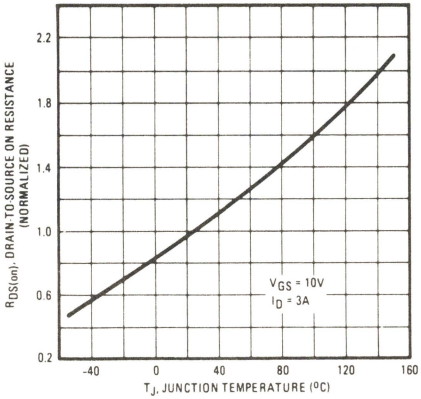


Fig. 9 - Normalized on-resistance vs. temperature.

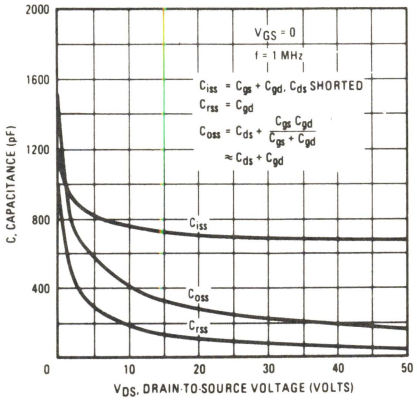


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

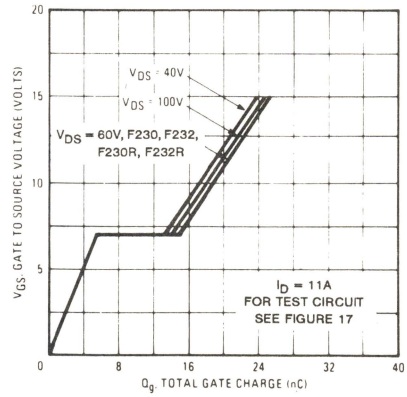


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

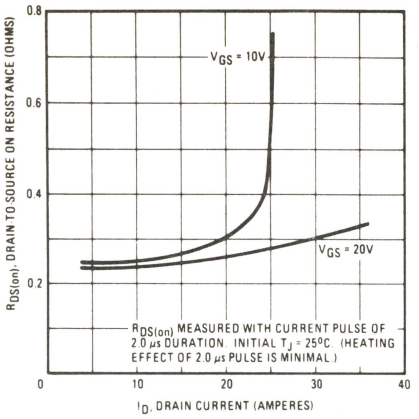


Figure 12 – Typical On-Resistance Vs. Drain Current

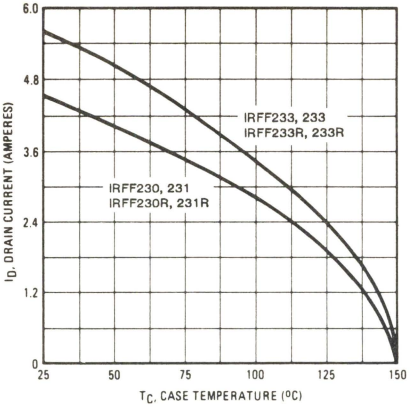


Fig. 13 – Maximum Drain Current Vs. Case Temperature

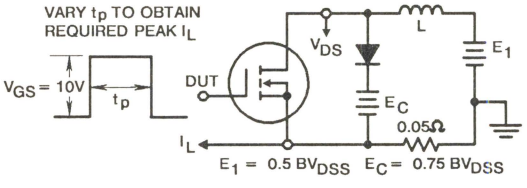


Fig. 14a – Clamped Inductive Test Circuit

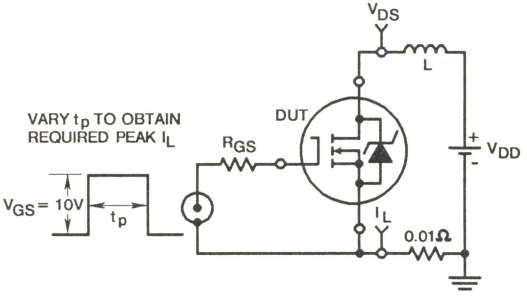


Fig. 15a – Unclamped Energy Test Circuit

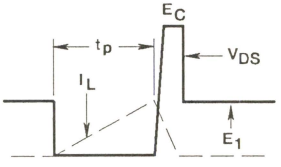


Fig. 14b – Clamped Inductive Waveforms

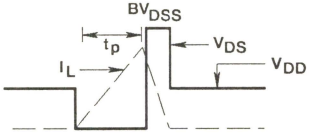


Fig. 15b – Unclamped Energy Waveforms

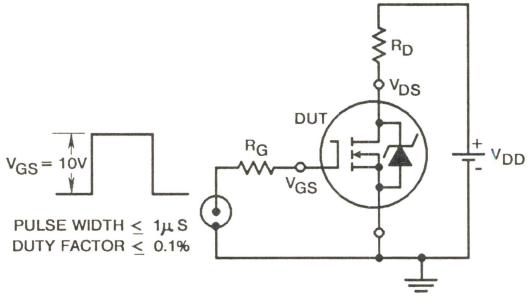


Fig. 16 – Switching Time Test Circuit

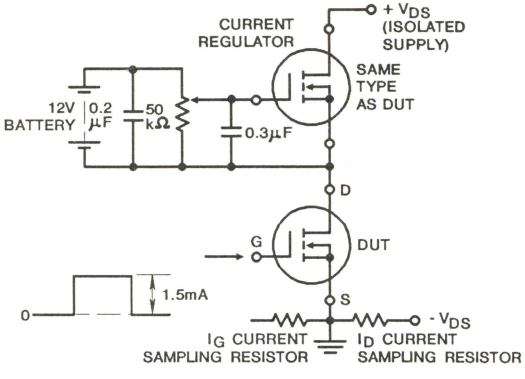


Fig. 17 – Gate Charge Test Circuit

IRFF310/311/312/313
IRFF310R/311R/312R/313R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 1.35A and 1.15A, 350V - 400V
- $r_{DS(on)}$ = 3.6Ω and 5.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

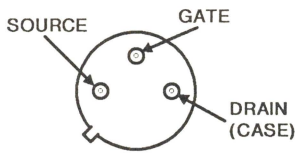
Description

The IRFF310, IRFF311, IRFF312, and IRFF313 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF310R, IRFF311R, IRFF312R, and IRFF313R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

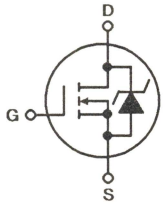
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF310 IRFF310R	IRFF311 IRFF311R	IRFF312 IRFF312R	IRFF313 IRFF313R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	1.35	1.35	1.15	1.15	A
Pulsed Drain Current (3) ..... I_{DM}	5.5	5.5	4.5	4.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	15	15	15	15	W
Linear Derating Factor	0.12	0.12	0.12	0.12	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	5.5	5.5	4.5	4.5	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	150	150	150	150	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.35A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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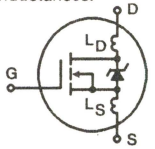
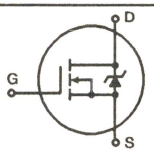
File Number **1888.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF310/312, IRFF310R/312R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRFF311/313, IRFF311R/313R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFF310/311, IRFF310R/311R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	1.35	–	–	A
IRFF312/313, IRFF312R/313R			1.15	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF310/311, IRFF310R/311R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.8A	–	3.3	3.6	Ω
IRFF312/313, IRFF312R/313R			–	3.6	5.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.8A	0.5	1.2	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	135	–	pF
Output Capacitance	C_{OSS}		–	35	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	8.0	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.35A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	3.0	10	ns
Rise Time	t_r		–	10	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	5.0	10	ns
Fall Time	t_f		–	8.0	15	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.35A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	6.0	7.5	nC
Gate-Source Charge	Q_{gs}		–	3.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	3.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	8.33	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	1.35	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	5.5	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.35A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.35A, dI_F/dt = 100A/µs	–	380	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.35A, dI_F/dt = 100A/µs	–	2.7	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 40V, starting T_J = +25°C, L = 44.89mH, R_{GS} = 50Ω, I_{PEAK} = 1.35A. (See Figure 15.)

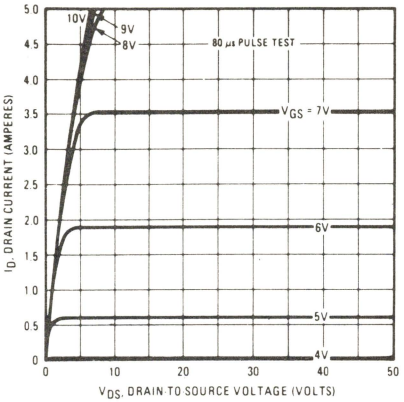


Fig. 1 - Typical output characteristics.

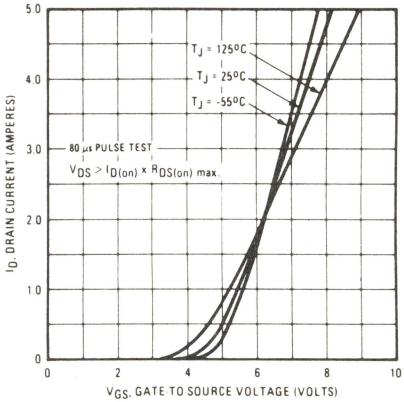


Fig. 2 - Typical transfer characteristics.

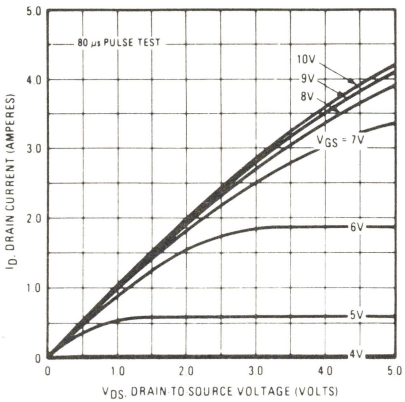


Fig. 3 - Typical saturation characteristics.

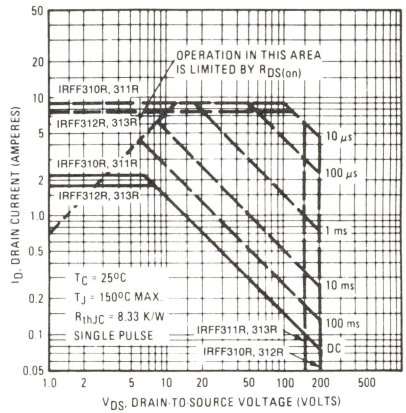


Fig. 4 - Maximum safe operating area.

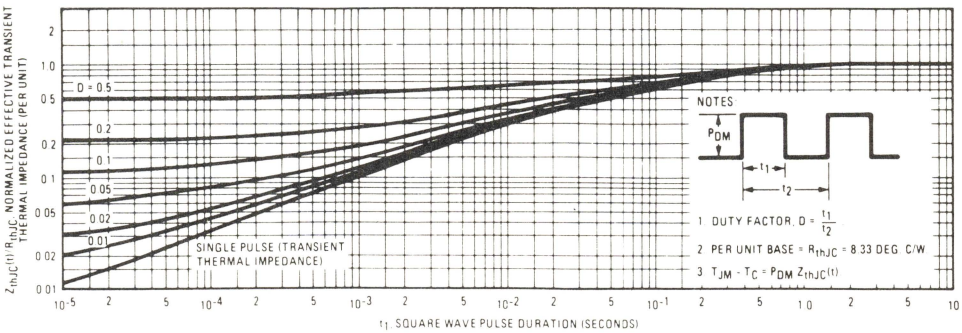


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

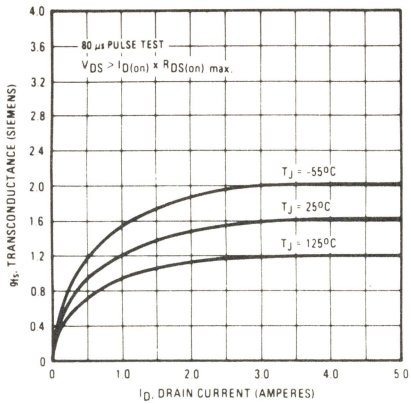


Fig. 6 - Typical transconductance vs. drain current.

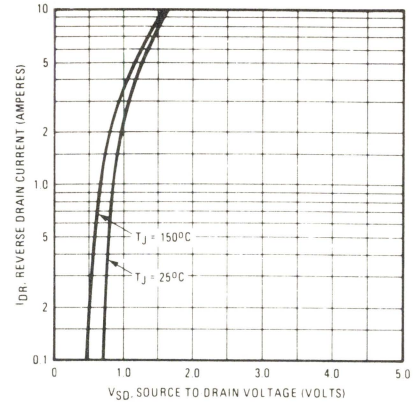


Fig. 7 - Typical source-drain diode forward voltage.

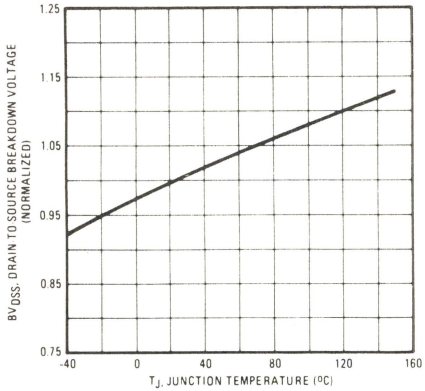


Fig. 8 - Breakdown voltage vs. temperature.

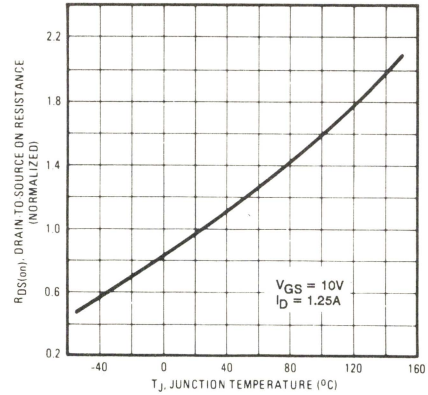


Fig. 9 - Normalized on-resistance vs. temperature.

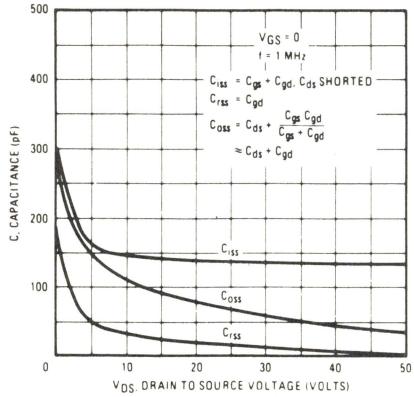


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

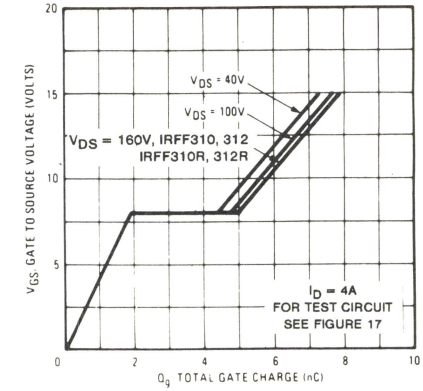


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

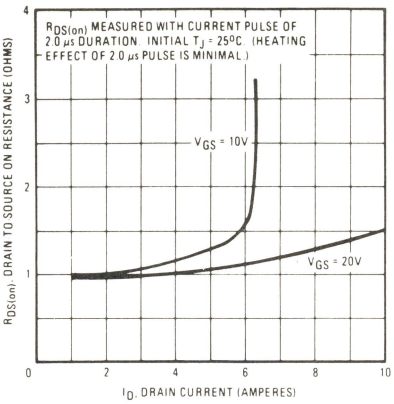


Figure 12 - Typical On-Resistance Vs. Drain Current

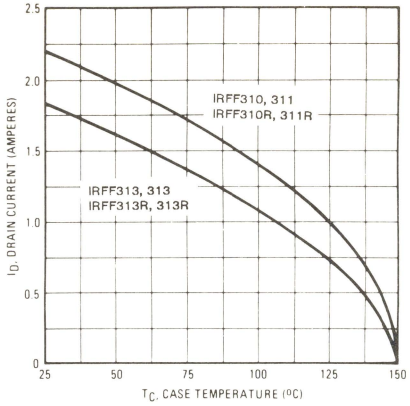


Fig. 13 - Maximum Drain Current Vs. Case Temperature

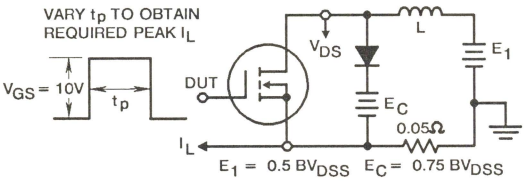


Fig. 14a - Clamped Inductive Test Circuit

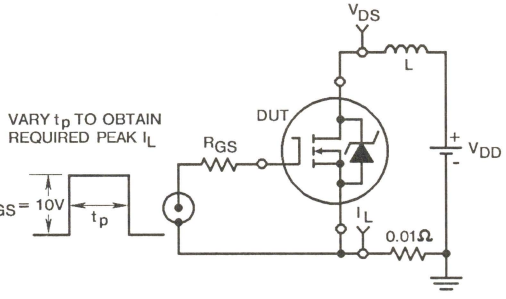


Fig. 15a - Unclamped Energy Test Circuit

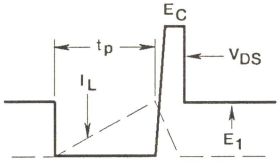


Fig. 14b - Clamped Inductive Waveforms

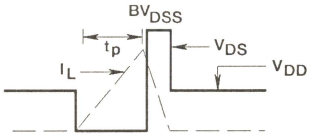


Fig. 15b - Unclamped Energy Waveforms

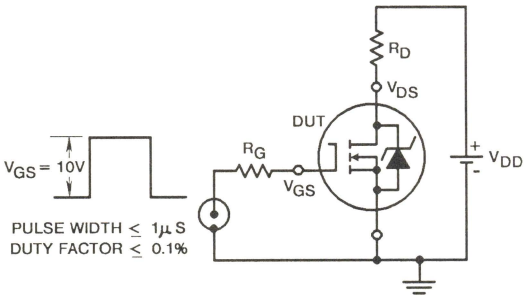


Fig. 16 - Switching Time Test Circuit

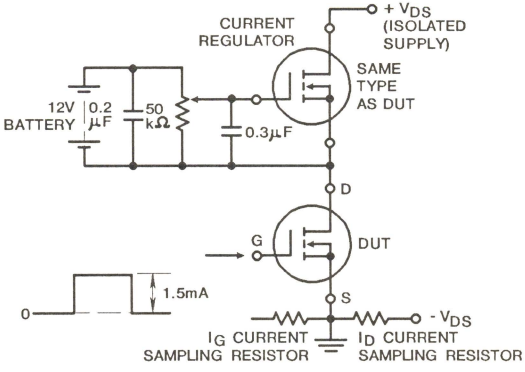


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFF320/321/322/323
IRFF320R/321R/322R/323R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.0A and 2.5A, 350V - 400V
- $r_{DS(on)}$ = 1.8Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

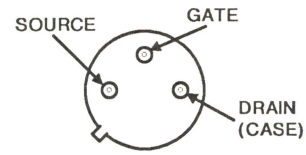
Description

The IRFF320, IRFF321, IRFF322, and IRFF323 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF320R, IRFF321R, IRFF322R, and IRFF323R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

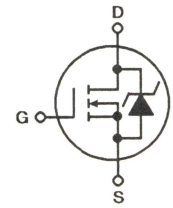
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF320 IRFF320R	IRFF321 IRFF321R	IRFF322 IRFF322R	IRFF323 IRFF323R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	2.5	2.5	2.0	2.0	A
Pulsed Drain Current (3) ..... I_{DM}	10	10	8.0	8.0	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	10	10	8.0	8.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	100	100	100	100	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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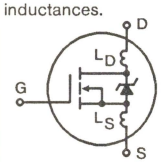
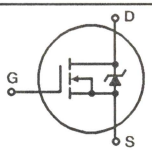
File Number **1890.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF320/322, IRFF320R/322R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
IRFF321/323, IRFF321R/323R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF320/321, IRFF320R/321R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	2.5	–	–	A
IRFF322/323, IRFF322R/323R			2.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF320/321, IRFF320R/321R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.25A	–	1.5	1.8	Ω
IRFF322/323, IRFF322R/323R			–	1.8	2.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.25A	1.0	2.0	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	450	–	pF
Output Capacitance	C_{OSS}		–	100	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 2.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	20	40	ns
Rise Time	t_r		–	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	25	50	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	12	15	nC
Gate-Source Charge	Q_{gs}		–	6.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	10	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.5A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.5A, dI_F/dt = 100A/μs	–	450	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.5A, dI_F/dt = 100A/μs	–	3.1	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 40V, starting T_J = +25°C, L = 29.09mH, R_{GS} = 50Ω, I_{PEAK} = 2.5A. (See Figure 15.)

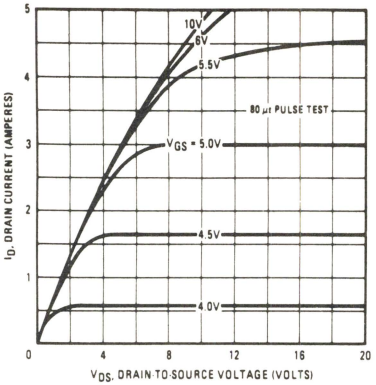


Fig. 1 - Typical output characteristics.

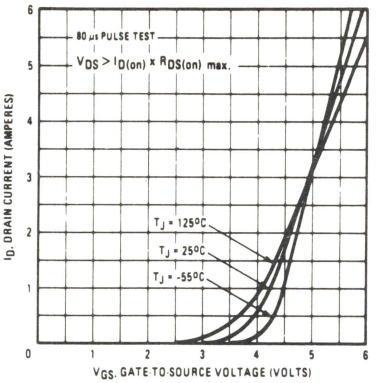


Fig. 2 - Typical transfer characteristics.

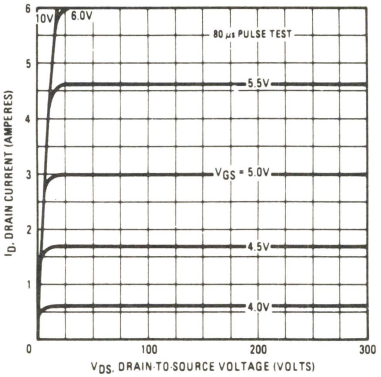


Fig. 3 - Typical saturation characteristics.

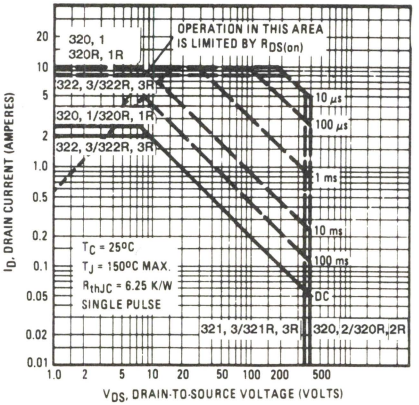


Fig. 4 - Maximum safe operating area.

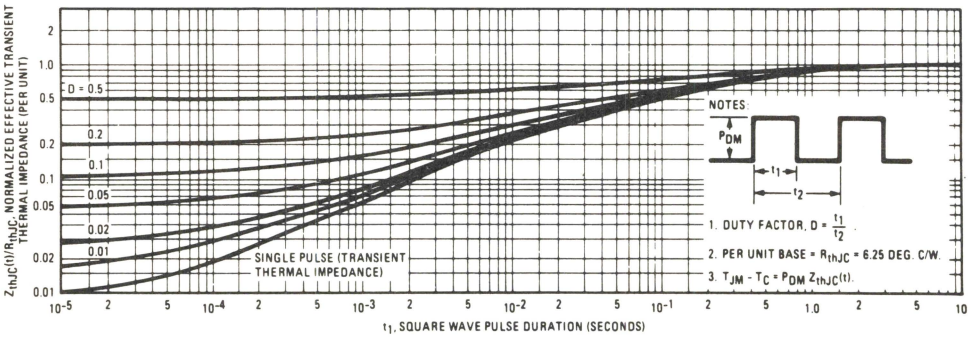


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

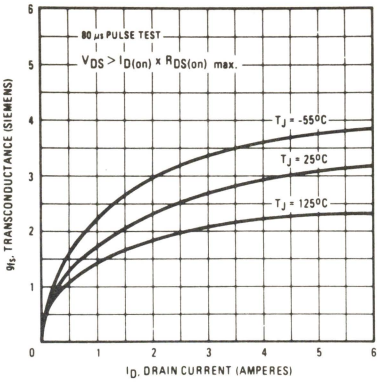


Fig. 6 - Typical transconductance vs. drain current.

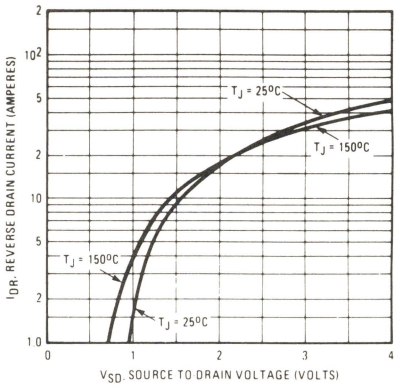


Fig. 7 - Typical source-drain diode forward voltage.

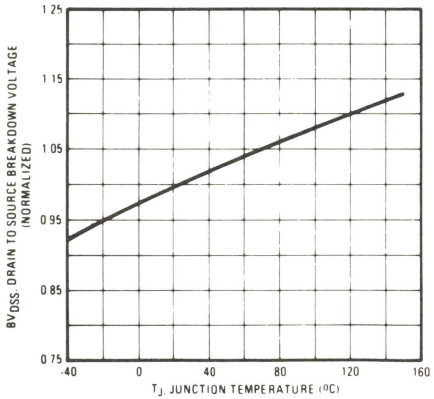


Fig. 8 - Breakdown voltage vs. temperature.

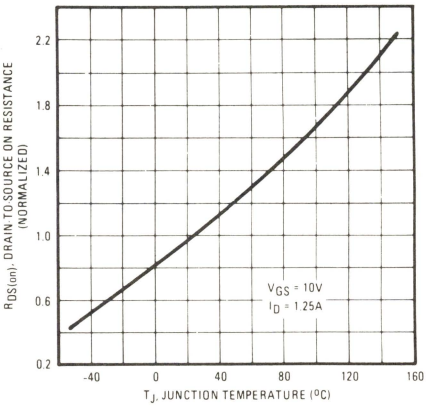


Fig. 9 - Normalized on-resistance vs. temperature.

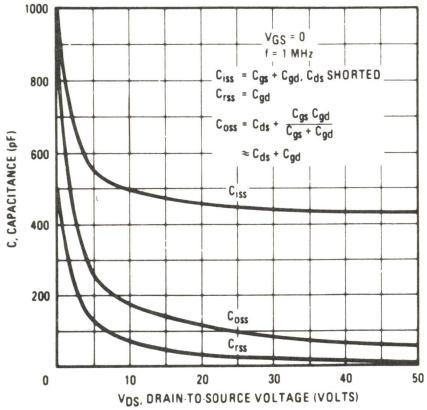


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

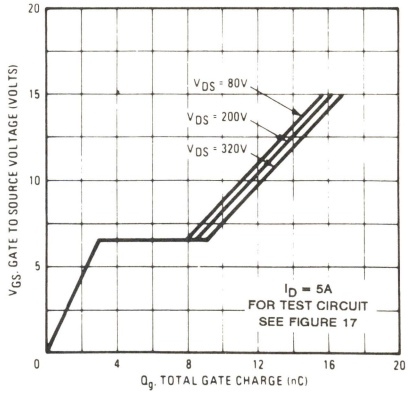


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

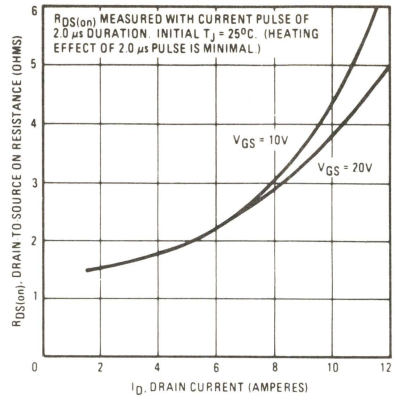


Figure 12 - Typical On-Resistance Vs. Drain Current

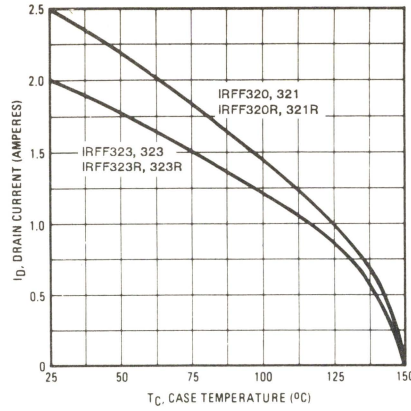


Fig. 13 - Maximum Drain Current Vs. Case Temperature

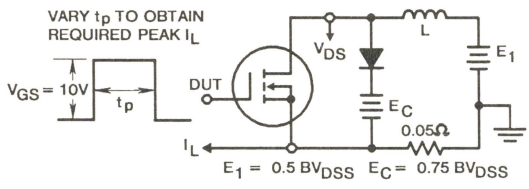


Fig. 14a - Clamped Inductive Test Circuit

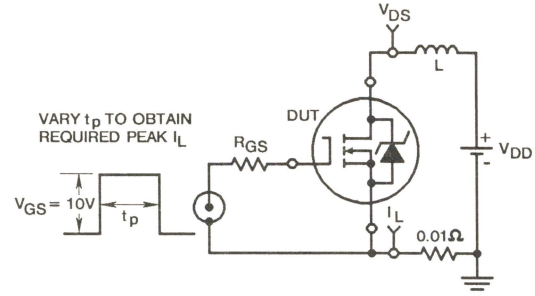


Fig. 15a - Unclamped Energy Test Circuit

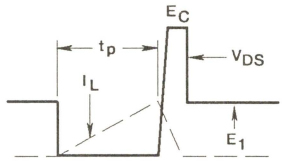


Fig. 14b - Clamped Inductive Waveforms

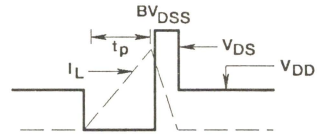


Fig. 15b - Unclamped Energy Waveforms

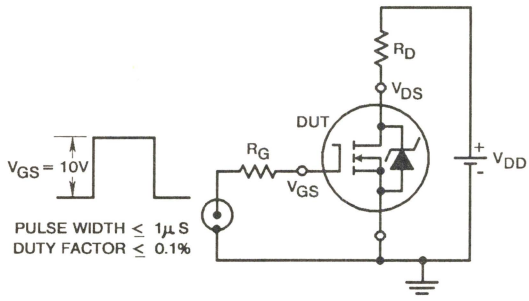


Fig. 16 - Switching Time Test Circuit

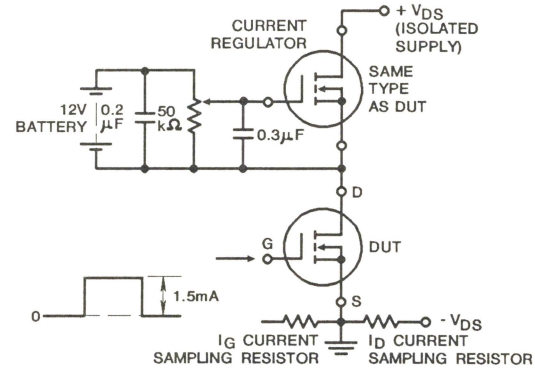


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFF330/331/332/333
IRFF330R/331R/332R/333R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 3.0A and 3.5A, 350V - 400V
- $r_{DS(on)}$ = 1.0Ω and 1.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

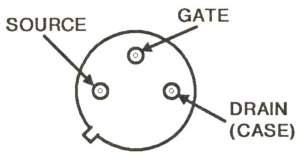
Description

The IRFF330, IRFF331, IRFF332, and IRFF333 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF330R, IRFF331R, IRFF332R, and IRFF333R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

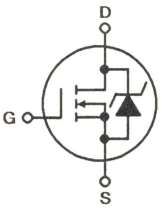
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF330 IRFF330R	IRFF331 IRFF331R	IRFF332 IRFF332R	IRFF333 IRFF333R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current T_C = +25°C ..... I_D	3.5	3.5	3.0	3.0	A
Pulsed Drain Current (3) ..... I_{DM}	14	14	12	12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	14	14	12	12	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	300	300	300	300	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 42.85mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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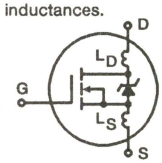
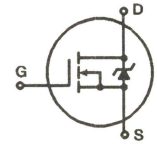
File Number 1893.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF330/332, IRFF330R/332R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
IRFF331/333, IRFF331R/333R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFF330/331, IRFF330R/331R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	3.5	–	–	A
IRFF332/333, IRFF332R/333R			3.0	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF330/331, IRFF330R/331R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.0A	–	0.8	1.0	Ω
IRFF332/333, IRFF332R/333R			–	1.0	1.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 2.0A	2.0	3.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	700	–	pF
Output Capacitance	C_{OSS}		–	150	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq$ 175V, I_D = 3.5A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	30	ns
Rise Time	t_r		–	–	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	55	ns
Fall Time	t_f		–	–	35	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 3.5A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	18	30	nC
Gate-Source Charge	Q_{gs}		–	11	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	7.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 3.5A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/μs	–	600	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 3.5A, dI_F/dt = 100A/μs	–	4.0	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 50V, starting T_J = +25°C, L = 42.85mH, R_{GS} = 25Ω, I_{PEAK} = 3.5A. (See Figure 15.)

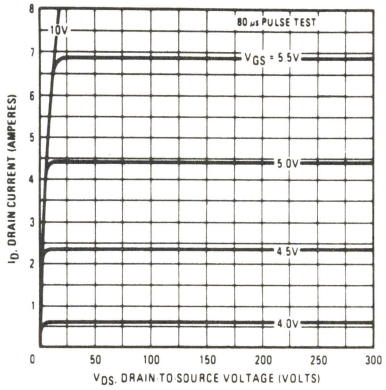


Fig. 1 - Typical output characteristics.

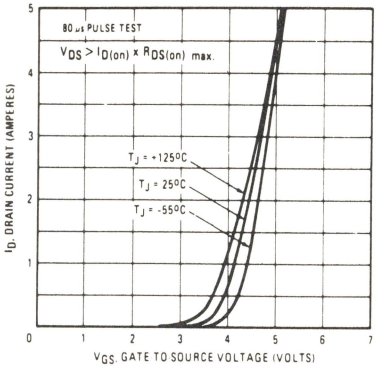


Fig. 2 - Typical transfer characteristics.

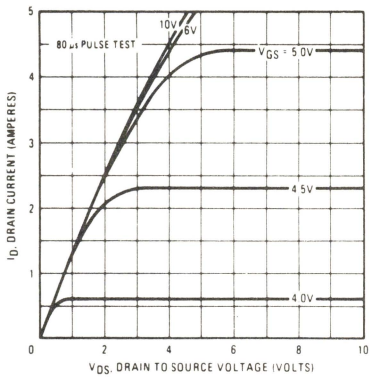


Fig. 3 - Typical saturation characteristics.

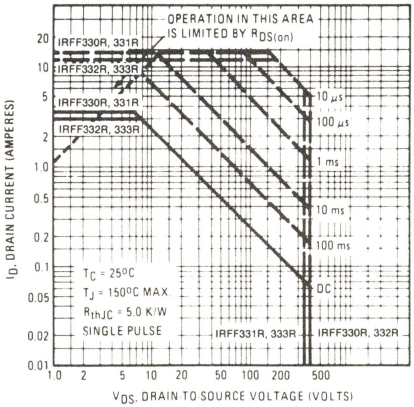


Fig. 4 - Maximum safe operating area.

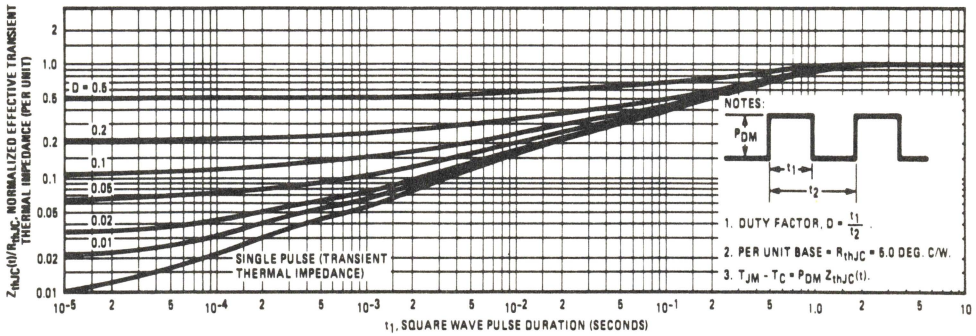


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

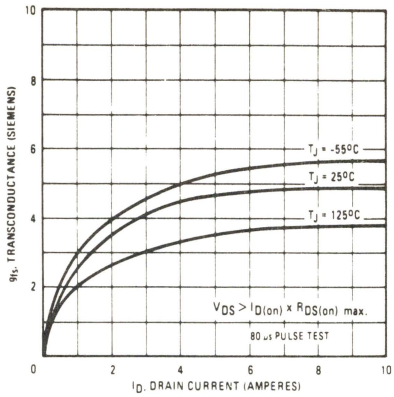


Fig. 6 - Typical transconductance vs. drain current.

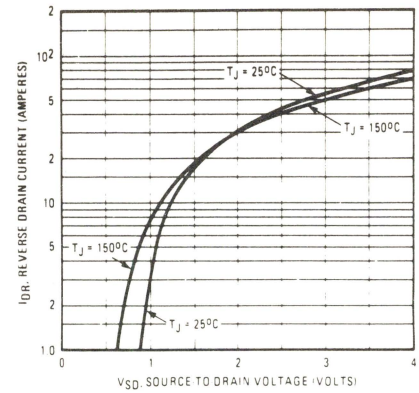


Fig. 7 - Typical source-drain diode forward voltage.

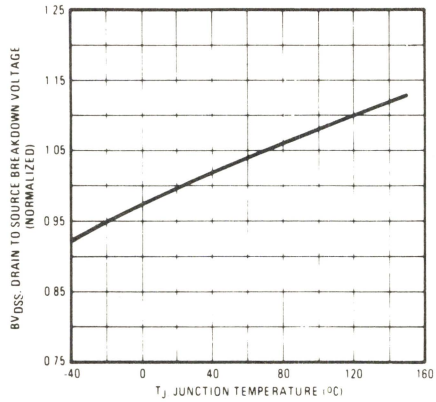


Fig. 8 - Breakdown voltage vs. temperature.

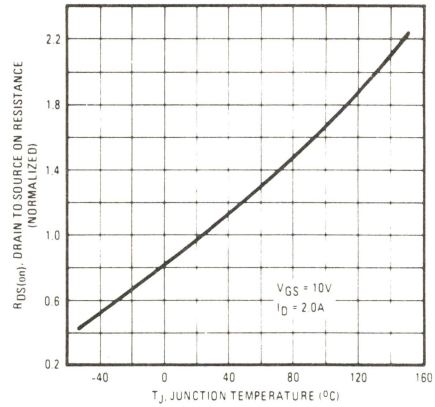


Fig. 9 - Normalized on-resistance vs. temperature.

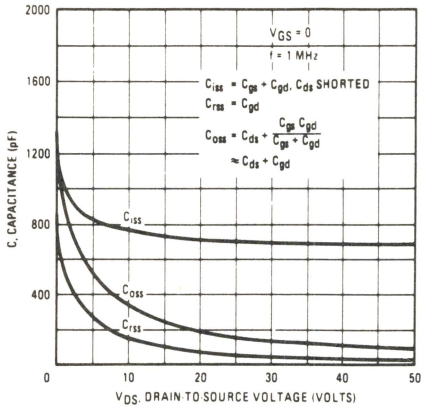


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

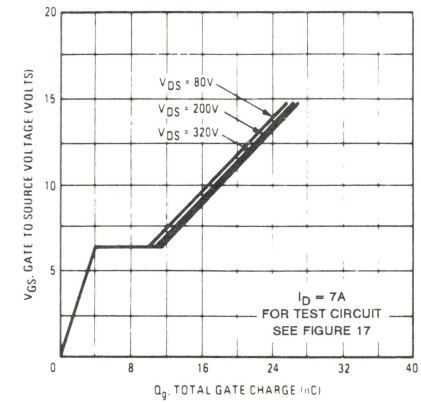


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

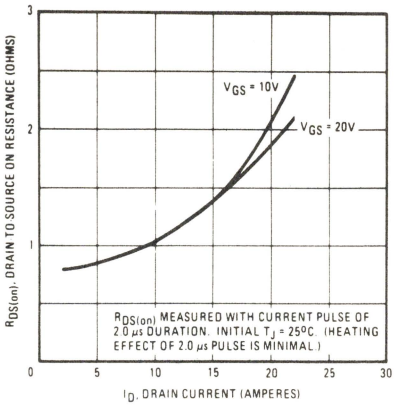


Figure 12 - Typical On-Resistance Vs. Drain Current

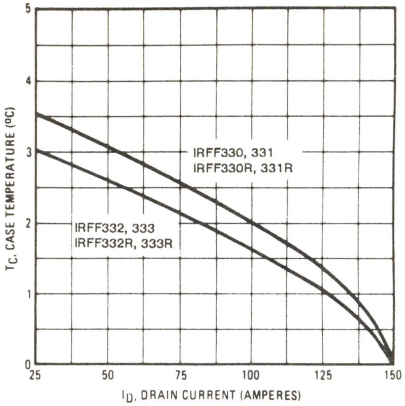


Fig. 13 - Maximum Drain Current Vs. Case Temperature

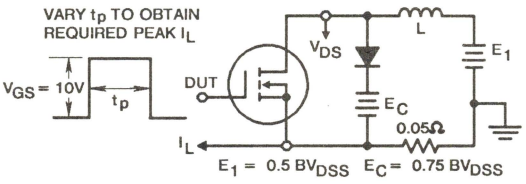


Fig. 14a - Clamped Inductive Test Circuit

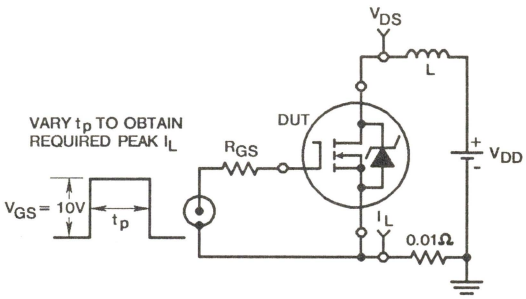


Fig. 15a - Unclamped Energy Test Circuit

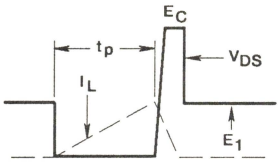


Fig. 14b - Clamped Inductive Waveforms

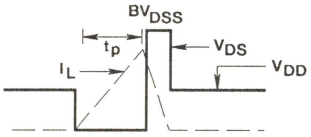


Fig. 15b - Unclamped Energy Waveforms

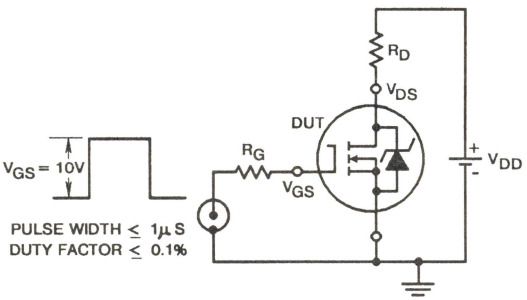


Fig. 16 - Switching Time Test Circuit

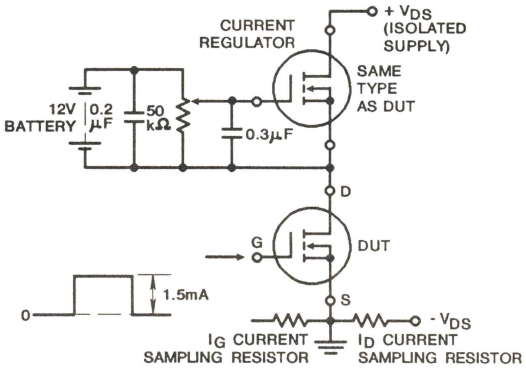


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFF420/421/422/423
IRFF420R/421R/422R/423R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 1.4A and 1.6A, 450V - 500V
- $r_{DS(on)}$ = 3.0Ω and 4.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

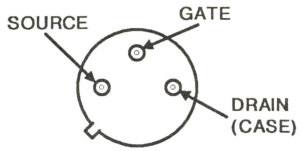
Description

The IRFF420, IRFF421, IRFF422, and IRFF423 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF420R, IRFF421R, IRFF422R, and IRFF423R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

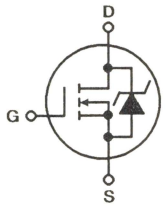
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF420 IRFF420R	IRFF421 IRFF421R	IRFF422 IRFF422R	IRFF423 IRFF423R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current T_C = +25°C ..... I_D	1.6	1.6	1.4	1.4	A
Pulsed Drain Current (3) ..... I_{DM}	6.5	6.5	5.5	5.5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	20	20	20	20	W
Linear Derating Factor	0.16	0.16	0.16	0.16	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	6.5	6.5	5.5	5.5	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	210	210	210	210	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 143.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.6A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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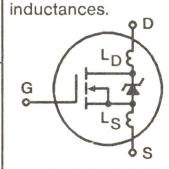
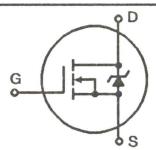
File Number **1891.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF420/422, IRFF420R/422R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRFF421/423, IRFF421R/423R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFF420/421, IRFF420R/421R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	1.6	–	–	A
IRFF422/423, IRFF422R/423R			1.4	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF420/421, IRFF420R/421R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.0A	–	2.5	3.0	Ω
IRFF422/423, IRFF422R/423R			–	3.0	4.0	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.0A	1.0	1.75	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	300	–	pF
Output Capacitance	C_{OSS}		–	75	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	20	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.6A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	30	60	ns
Rise Time	t_r		–	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	30	60	ns
Fall Time	t_f		–	15	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	11	15	nC
Gate-Source Charge	Q_{gs}		–	5.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	6.0	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	1.6	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	6.5	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.6A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/µs	–	600	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.6A, dI_F/dt = 100A/µs	–	3.5	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 50V, starting T_J = +25°C, L = 143.5mH, R_{GS} = 25Ω, I_{PEAK} = 1.6A. (See Figure 15.)

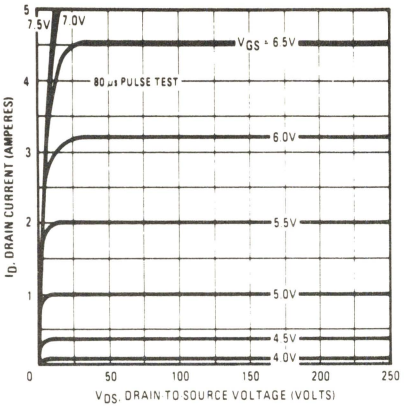


Fig. 1 - Typical output characteristics.

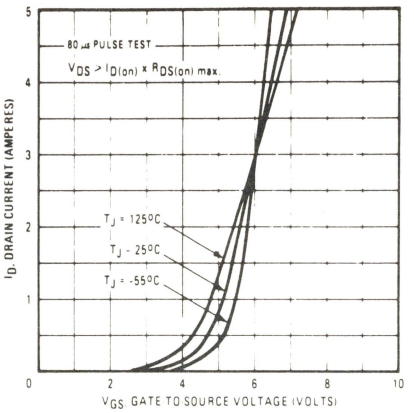


Fig. 2 - Typical transfer characteristics.

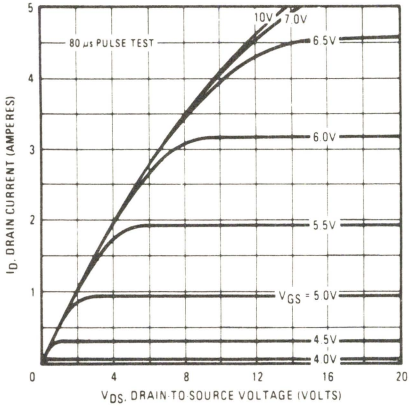


Fig. 3 - Typical saturation characteristics.

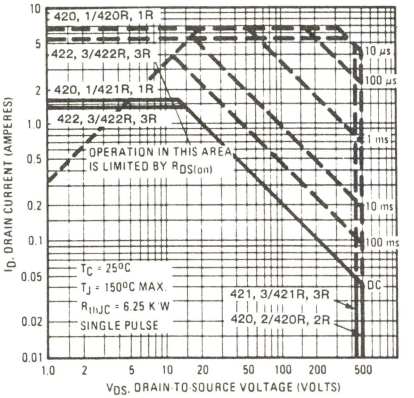


Fig. 4 - Maximum safe operating area.

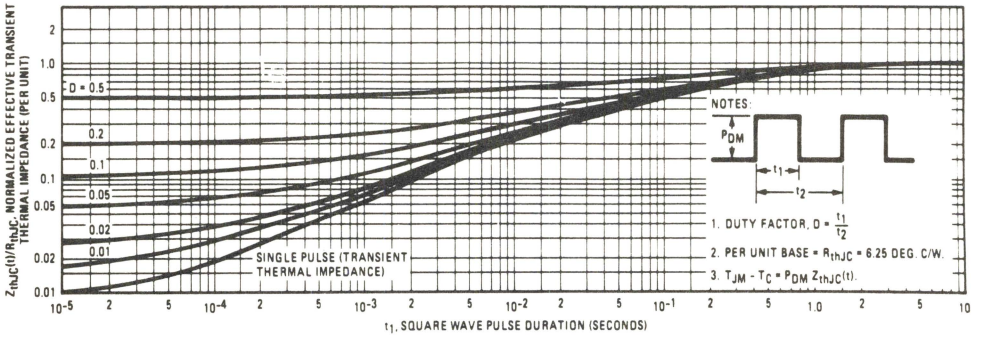


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

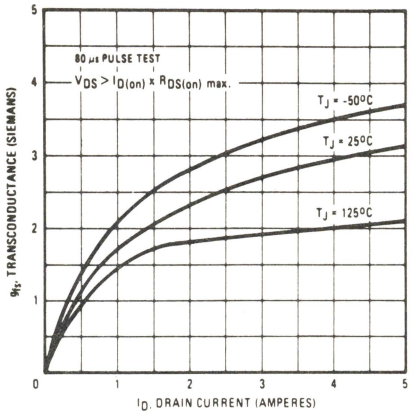


Fig. 6 - Typical transconductance vs. drain current.

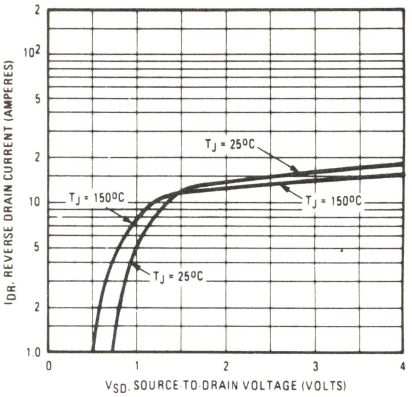


Fig. 7 - Typical source-drain diode forward voltage.

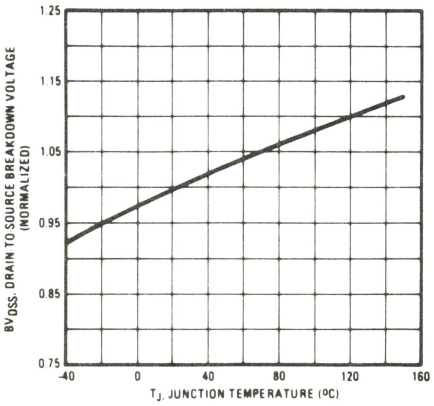


Fig. 8 - Breakdown voltage vs. temperature.

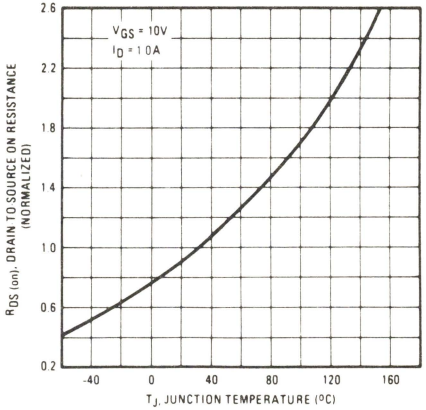


Fig. 9 - Normalized on-resistance vs. temperature.

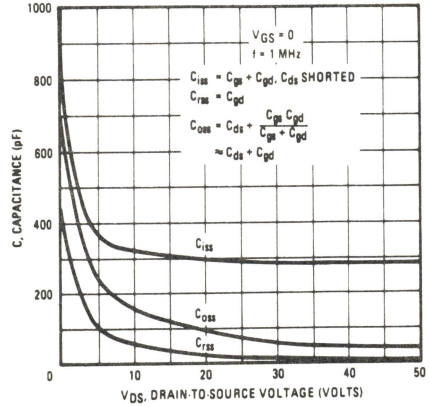


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

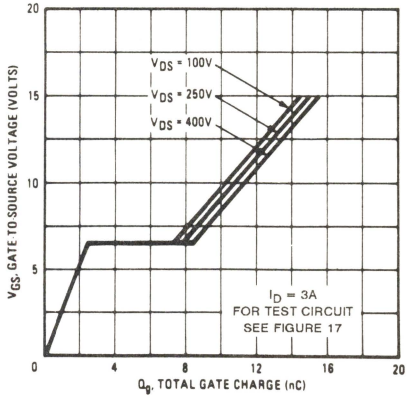


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

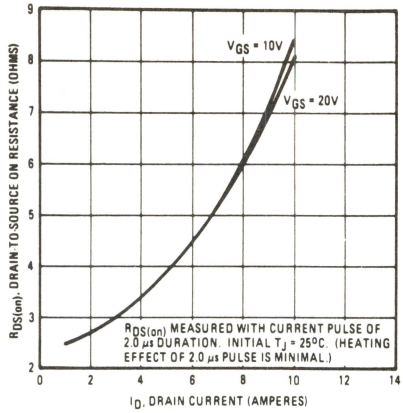


Figure 12 – Typical On-Resistance Vs. Drain Current

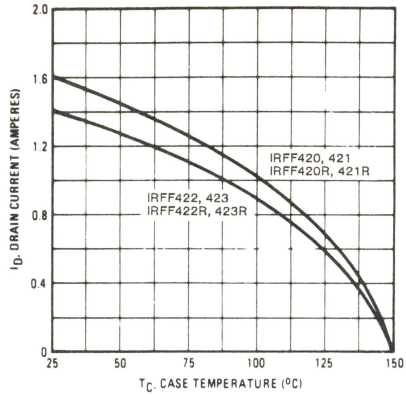


Fig. 13 – Maximum Drain Current Vs. Case Temperature

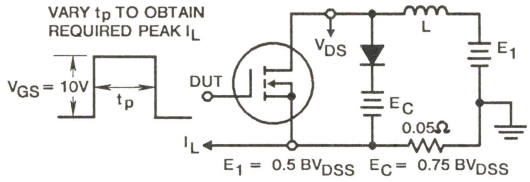


Fig. 14a – Clamped Inductive Test Circuit

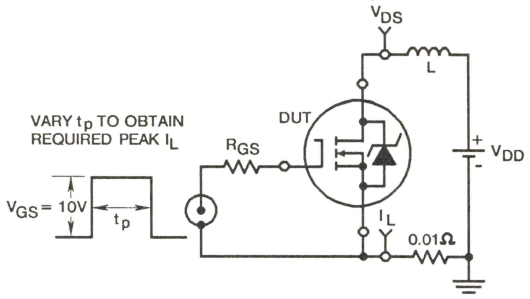


Fig. 15a – Unclamped Energy Test Circuit

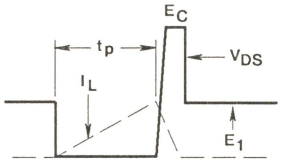


Fig. 14b – Clamped Inductive Waveforms

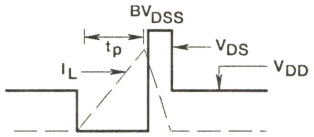


Fig. 15b – Unclamped Energy Waveforms

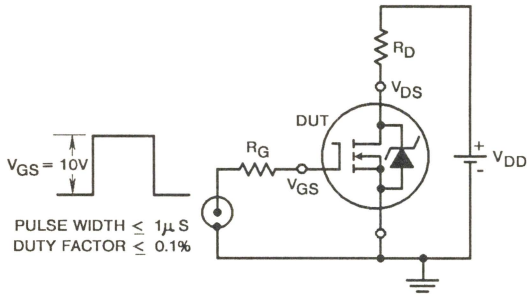


Fig. 16 – Switching Time Test Circuit

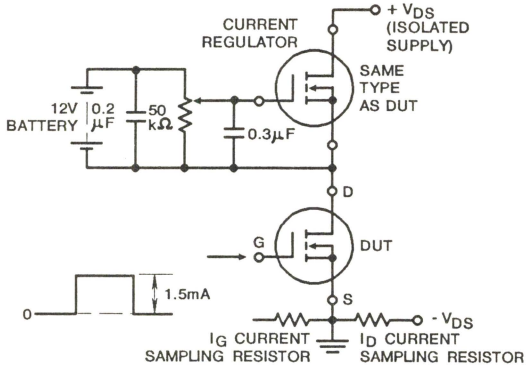


Fig. 17 – Gate Charge Test Circuit

HARRIS

IRFF430/431/432/433
IRFF430R/431R/432R/433R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 2.25A and 2.75A, 450V - 500V
- $r_{DS(on)}$ = 1.5Ω and 2.0Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

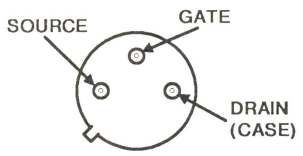
Description

The IRFF430, IRFF431, IRFF432, and IRFF433 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFF430R, IRFF431R, IRFF432R, and IRFF433R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

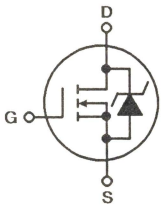
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFF430 IRFF430R	IRFF431 IRFF431R	IRFF432 IRFF432R	IRFF433 IRFF433R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current T_C = +25°C ..... I_D	2.75	2.75	2.25	2.25	A
Pulsed Drain Current (3) ..... I_{DM}	11	11	9.0	9.0	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C ..... P_D	25	25	25	25	W
Linear Derating Factor	0.2	0.2	0.2	0.2	W/°C
Inductive Current, Clamped (See Figure 14, L = 100μH) ..... I_{LM}	11	11	9.0	9.0	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	300	300	300	300	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 69.42, R_{GS} = 50Ω, I_{PEAK} = 2.75A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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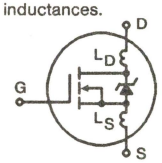
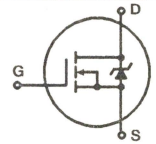
File Number 1894.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF430/432, IRFF430R/432R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRFF431/433, IRFF431R/433R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFF430/431, IRFF430R/431R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	2.75	–	–	A
IRFF432/433, IRFF432R/433R			2.25	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF430/431, IRFF430R/431R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 1.5A	–	1.3	1.5	Ω
IRFF432/433, IRFF432R/433R			–	1.5	2.0	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = 1.5A	1.5	2.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	600	–	pF
Output Capacitance	C_{OSS}		–	100	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	30	–	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq$ 225V, I_D = 2.75A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	–	30	ns
Rise Time	t_r		–	–	30	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	–	55	ns
Fall Time	t_f		–	–	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 2.75A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	22	30	nC
Gate-Source Charge	Q_{gs}		–	11	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	11	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5.0mm (0.2 in.) from header to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5.0mm (0.2") from header to source bonding pad.	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	2.75	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	11	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 2.75A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 2.75A, dI_F/dt = 100A/µs	–	800	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 2.75A, dI_F/dt = 100A/µs	–	4.6	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

4. V_{DD} = 50V, starting T_J = +25°C, L = 69.42mH, R_{GS} = 50Ω, I_{PEAK} = 2.75A. (See Figure 15.)

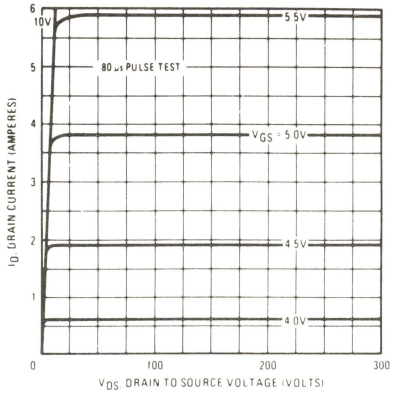


Fig. 1 - Typical output characteristics.

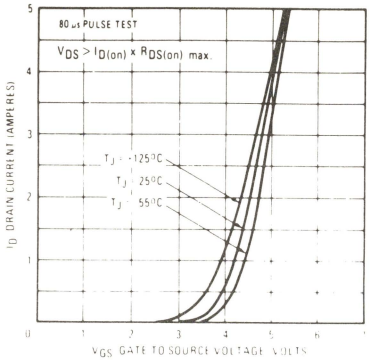


Fig. 2 - Typical transfer characteristics.

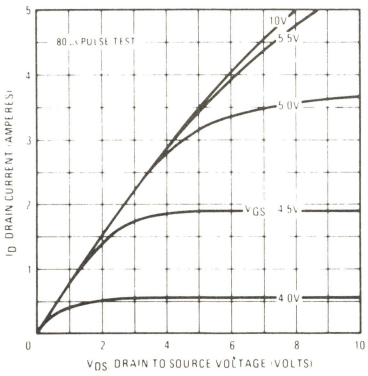


Fig. 3 - Typical saturation characteristics.

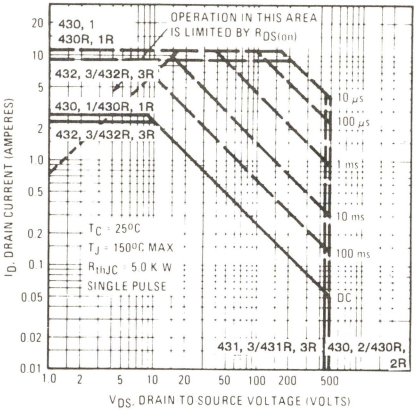


Fig. 4 - Maximum safe operating area.

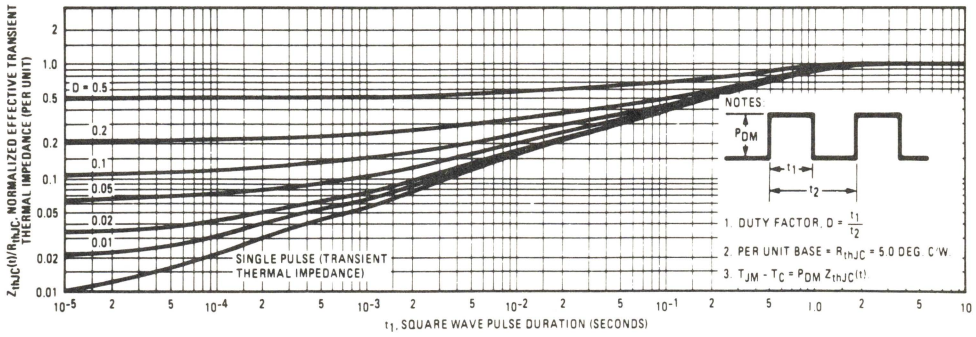


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

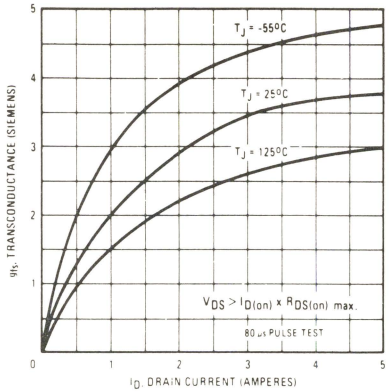


Fig. 6 - Typical transconductance vs. drain current.

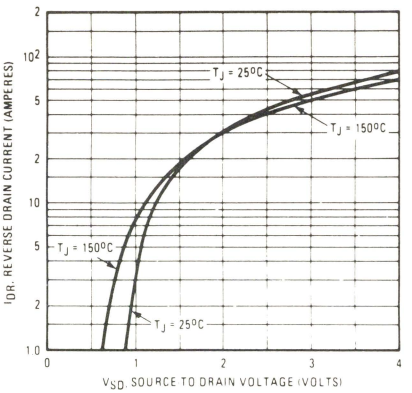


Fig. 7 - Typical source-drain diode forward voltage.

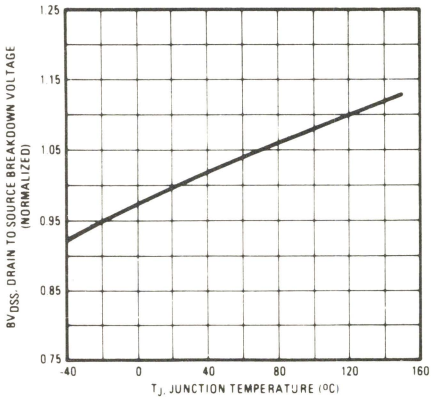


Fig. 8 - Breakdown voltage vs. temperature.

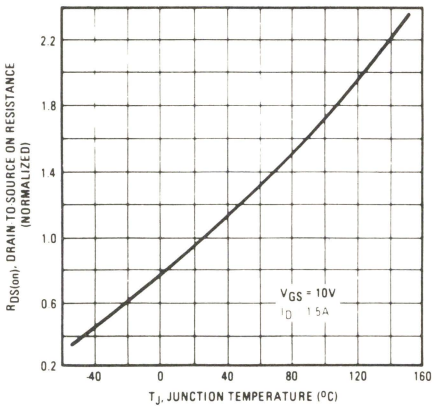


Fig. 9 - Normalized on-resistance vs. temperature.

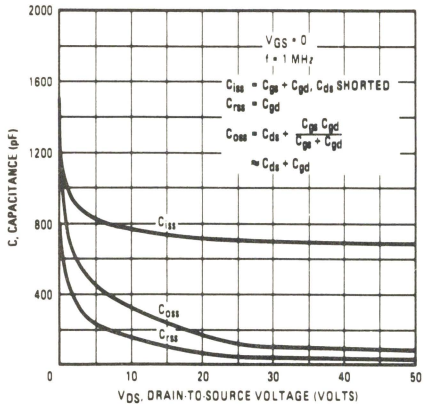


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

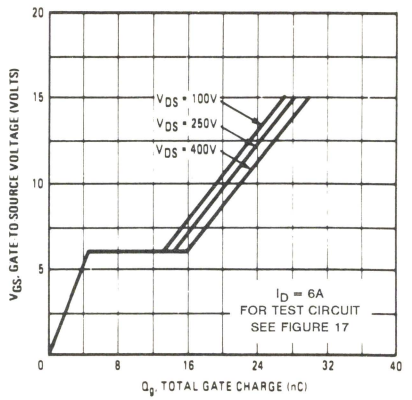


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

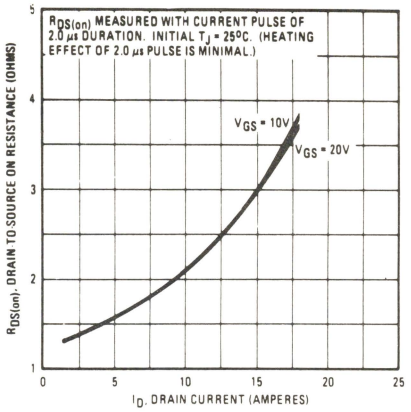


Figure 12 - Typical On-Resistance Vs. Drain Current

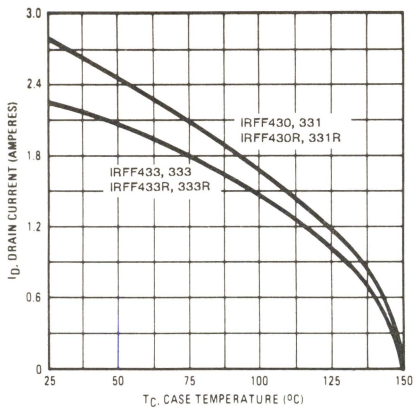


Fig. 13 - Maximum Drain Current Vs. Case Temperature

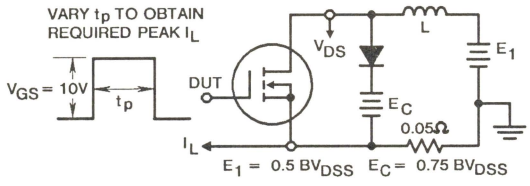


Fig. 14a - Clamped Inductive Test Circuit

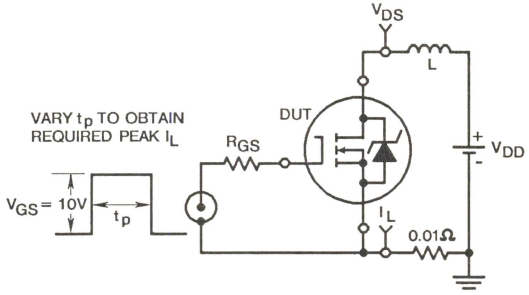


Fig. 15a - Unclamped Energy Test Circuit

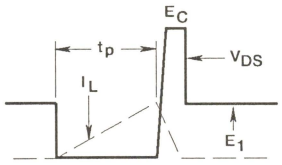


Fig. 14b - Clamped Inductive Waveforms

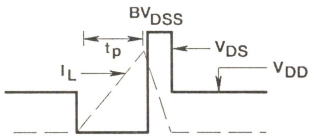


Fig. 15b - Unclamped Energy Waveforms

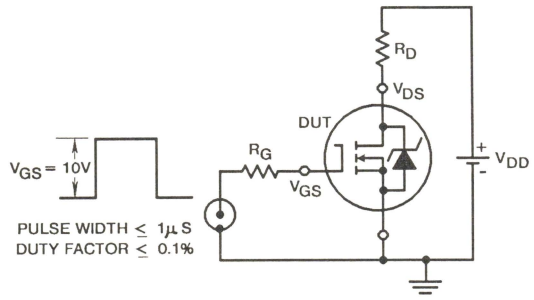


Fig. 16 - Switching Time Test Circuit

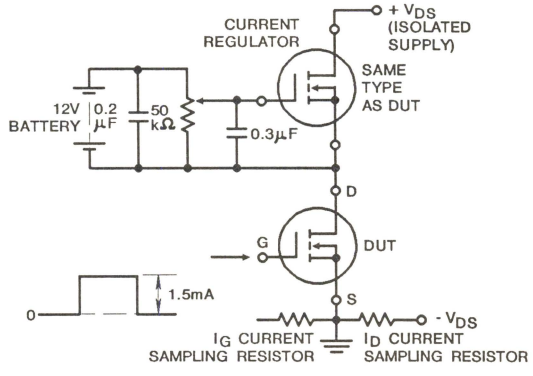


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFP140R, IRFP141R IRFP142R, IRFP143R

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 27A and 31A, 80V - 100V
- $r_{DS(on)}$ = 0.077Ω and 0.099Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

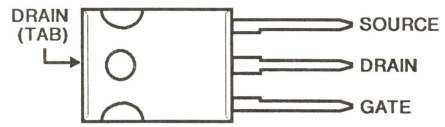
Description

The IRFP140R, IRFP141R, IRFP142R, and IRFP143R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

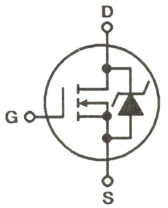
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP140R	IRFP141R	IRFP142R	IRFP143R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current					
T_C = +25°C ..... I_D	31	31	27	27	A
T_C = +100°C ..... I_D	22	22	19	19	A
Pulsed Drain Current (3) ..... I_{DM}	120	120	110	110	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	100	100	100	100	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +175	-55 to +175	-55 to +175	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 25V, starting T_J = +25°C, L = 160μH, R_{GS} = 50Ω, I_{PEAK} = 31A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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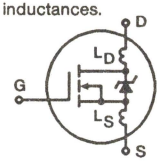
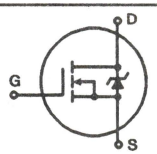
File Number **2086.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP140R, IRFP142R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100	-	-	V
IRFP141R, IRFP143R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFP140R, IRFP141R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	31	-	-	A
IRFP142R, IRFP143R			27	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP140R, IRFP141R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 19A	-	0.055	0.077	Ω
IRFP142R, IRFP143R			-	0.077	0.099	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 19A	9.3	14	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1275	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D ≈ 28A, R_G = 9.1Ω, RD = 1.8Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	15	23	ns
Rise Time	t_r		-	72	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	60	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	59	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	21	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	31	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	120	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 31A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/μs	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 28A, dI_F/dt = 100A/μs	0.44	0.91	1.9	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 160μH, R_{GS} = 50Ω, I_{PEAK} = 31A. (See Figures 14 & 15)

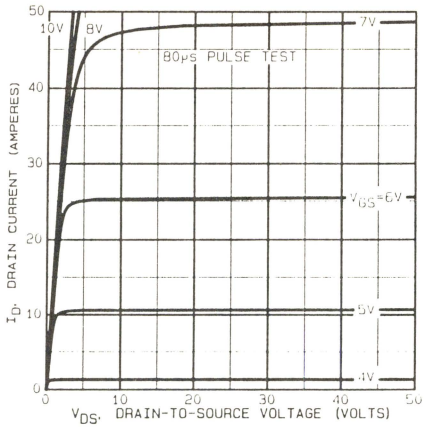


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

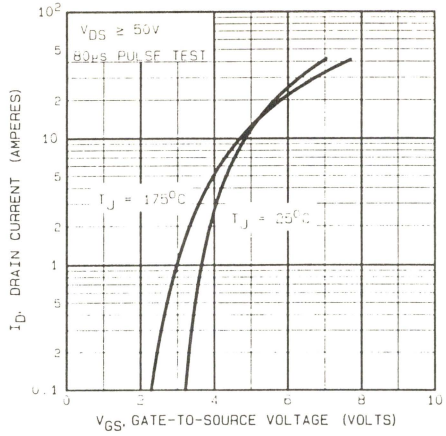


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

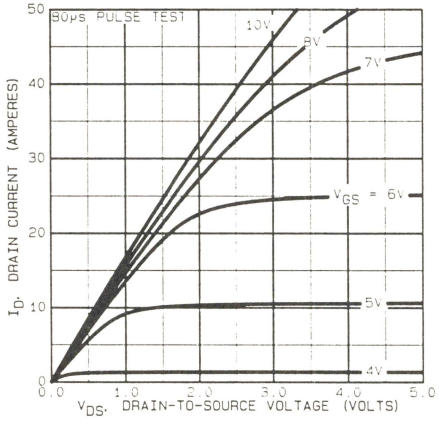


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

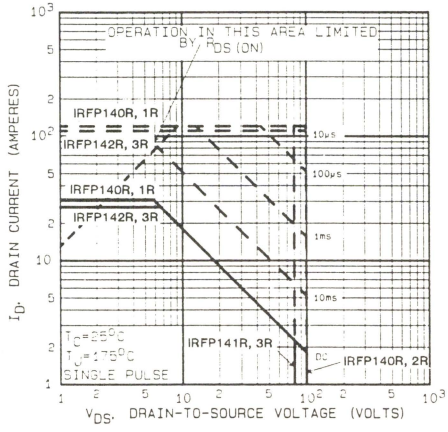


FIGURE 4. MAXIMUM SAFE OPERATING AREA

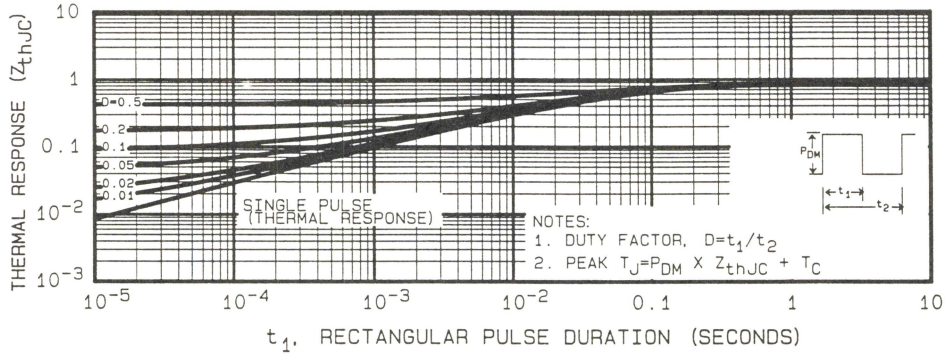


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

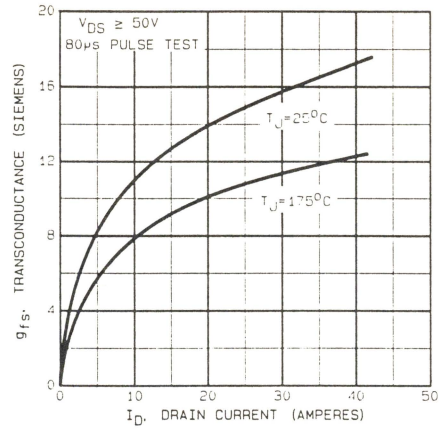


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

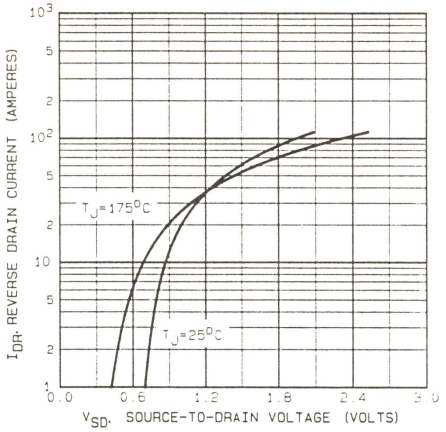


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

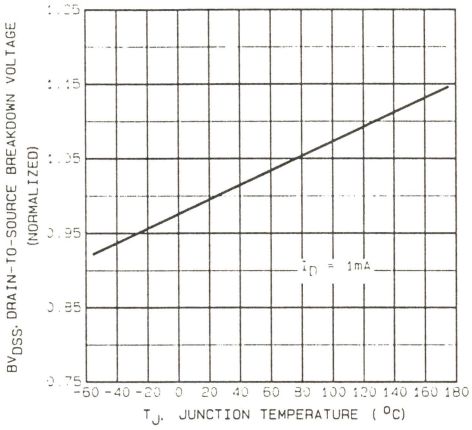


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

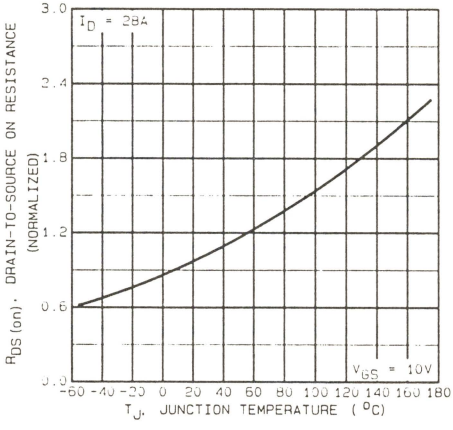


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

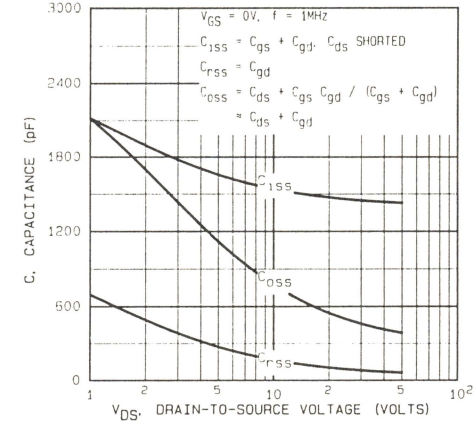


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

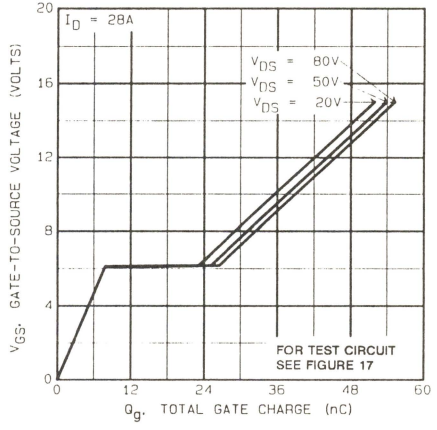


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

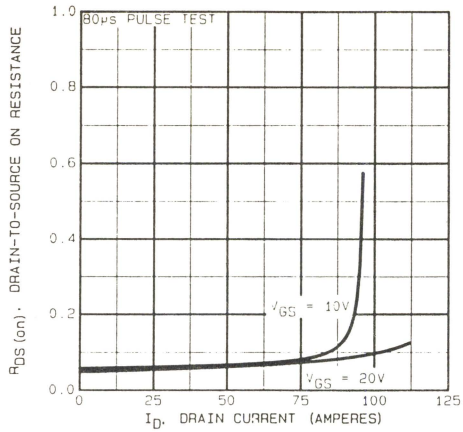


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

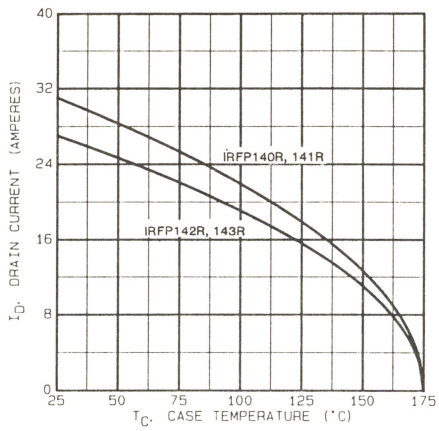


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

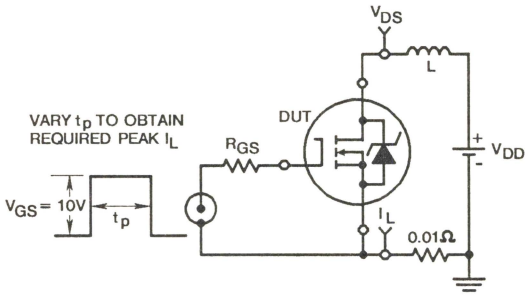


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

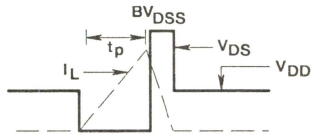


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

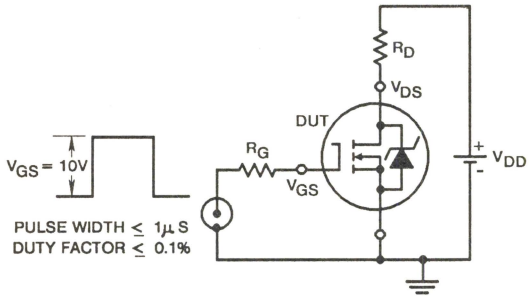


FIGURE 16. SWITCHING TIME TEST CIRCUIT

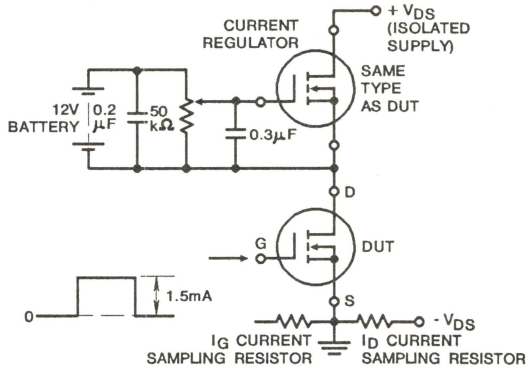


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRFP150/151/152/153
IRFP150R/151R/152R/153R

N-Channel Power MOSFETs
Avalanche Energy Rated*

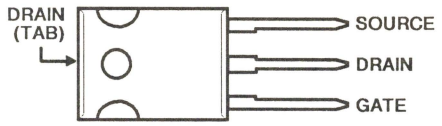
August 1991

Features

- 34A and 40A, 60V - 100V
- $r_{DS(on)}$ = 0.055Ω and 0.08Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



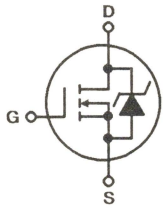
Description

The IRFP150, IRFP151, IRFP152, and IRFP153 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP150R, IRFP151R, IRFP152R, and IRFP153R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP150 IRFP150R	IRFP151 IRFP151R	IRFP152 IRFP152R	IRFP153 IRFP153R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	60	100	60	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	60	100	60	V
Continuous Drain Current					
T_C = +25°C ..... I_D	40	40	34	34	A
T_C = +100°C ..... I_D	26	26	22	22	A
Pulsed Drain Current (3) ..... I_{DM}	160	160	140	140	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	170	170	140	140	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	150	150	150	150	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 10V, starting T_J = +25°C, L = 170μH, R_{GS} = 50Ω, I_{PEAK} = 40A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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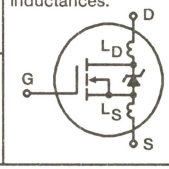
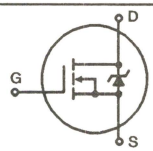
File Number **2318.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP150/152, IRFP150R/152R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	–	–	V
IRFP151/153, IRFP151R/153R			60	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP150/151, IRFP150R/151R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	40	–	–	A
IRFP152/153, IRFP152R/153R			34	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP150/151, IRFP150R/151R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 22A	–	0.045	0.055	Ω
IRFP152/153, IRFP152R/153R			–	0.06	0.08	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x VGS, I_D = 20A	13	20	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	1000	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	350	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 40A, R_G = 6.8Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	15	24	ns
Rise Time	t_r		–	140	210	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	60	89	ns
Fall Time	t_f		–	90	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 40A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	70	110	nC
Gate-Source Charge	Q_{gs}		–	20	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	30	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	40	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	170	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 40A, V_{GS} = 0V	–	–	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 40A, dI_F/dt = 100A/µs	98	–	530	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 40A, dI_F/dt = 100A/µs	0.41	–	2.5	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 10V, Start T_J = +25°C, L = 170µH, R_{GS} = 50Ω, I_{PEAK} = 40A (See Figure 15)

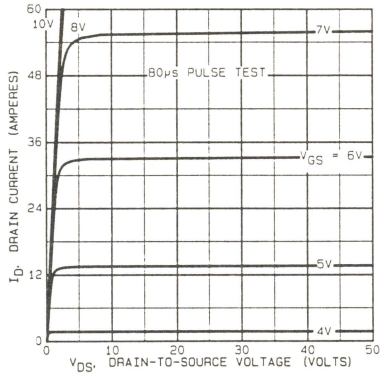


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

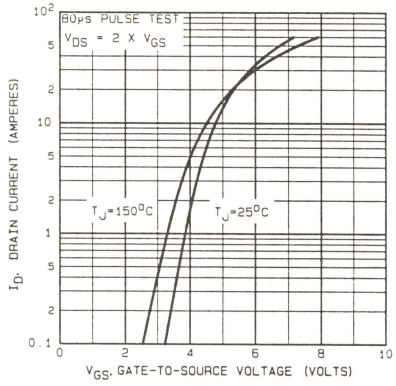


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

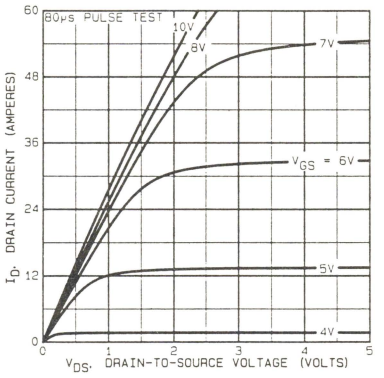


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

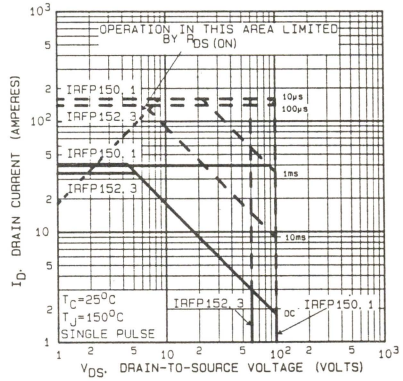


FIGURE 4. MAXIMUM SAFE OPERATING AREA

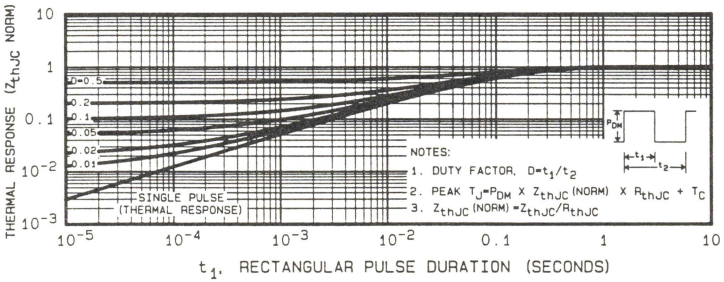


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

4 N-CHANNEL POWER MOSFETs

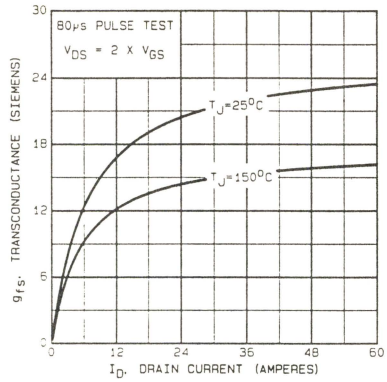


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

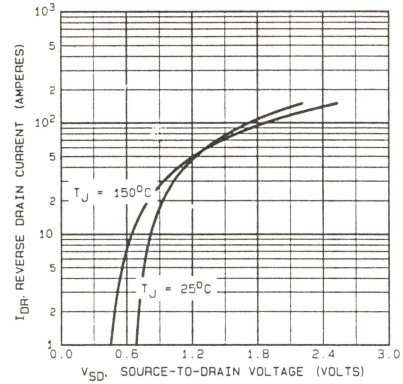


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

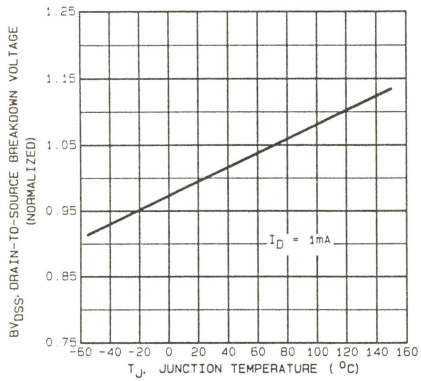


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

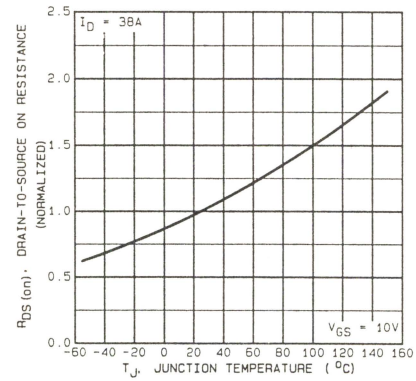


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

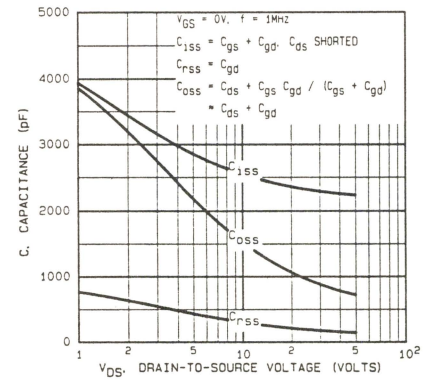


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

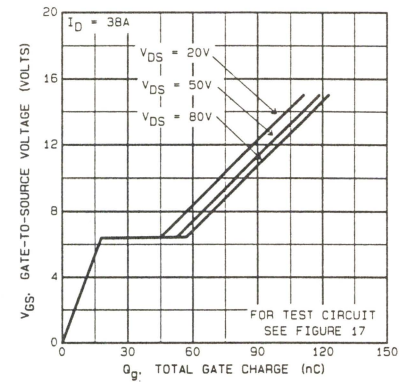


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

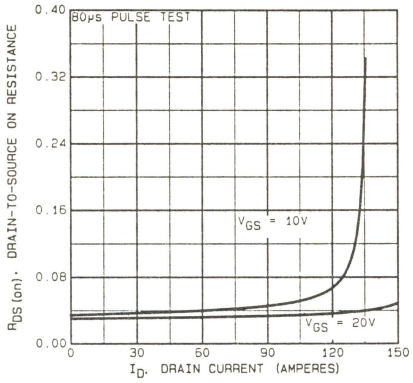


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

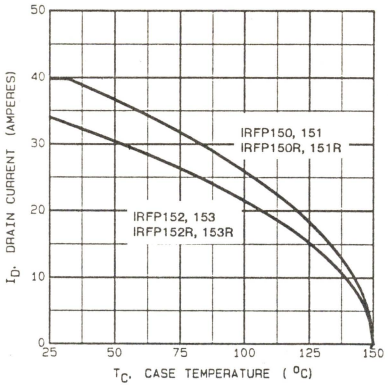


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

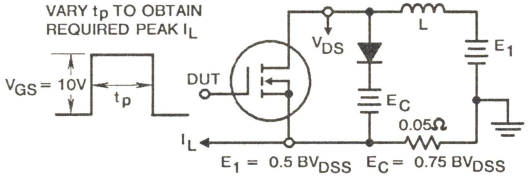


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

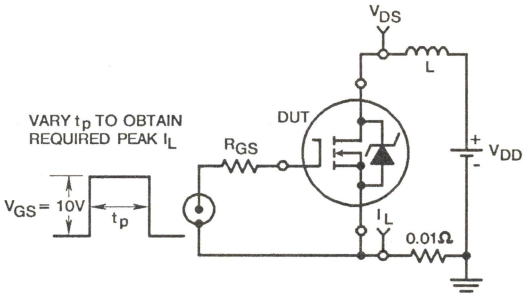


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

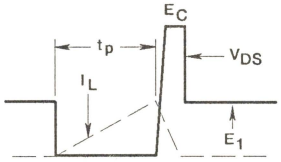


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

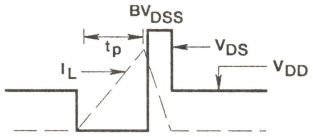


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

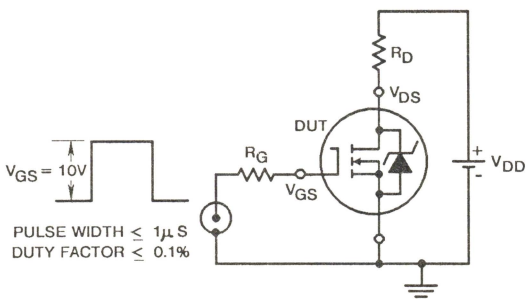


FIGURE 16. SWITCHING TIME TEST CIRCUIT

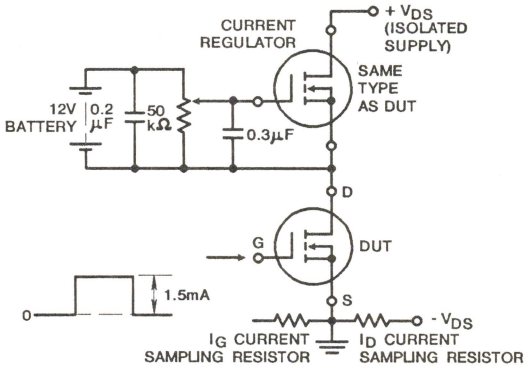


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRFP240R, IRFP241R IRFP242R, IRFP243R

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 18A and 20A, 200V - 150V
- $r_{DS(on)}$ = 0.18Ω and 0.22Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

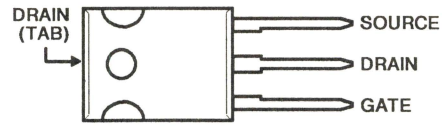
Description

The IRFP240R, IRFP241R, IRFP242R, and IRFP243R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

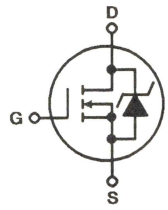
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP240R	IRFP241R	IRFP242R	IRFP243R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	120	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	20	20	18	18	A
T_C = +100°C ..... I_D	12	12	11	11	A
Pulsed Drain Current (3) ..... I_{DM}	80	80	72	72	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	510	510	510	510	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 1.9mH, R_{GS} = 50Ω, I_{PEAK} = 20A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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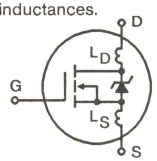
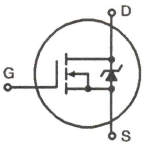
File Number **2087.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP240R, IRFP242R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	200	-	-	V
IRFP241R, IRFP243R			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFP240R, IRFP241R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 11V	20	-	-	A
IRFP242R, IRFP243R			18	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP240R, IRFP241R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	-	0.14	0.18	Ω
IRFP242R, IRFP243R			-	0.20	0.22	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 11A	7.3	11	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	1275	-	pF
Output Capacitance	C_{OSS}		-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 18A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	14	21	ns
Rise Time	t_r		-	51	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	45	68	ns
Fall Time	t_f		-	36	54	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	43	60	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	32	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	20	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	80	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 18A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 18A, dI_F/dt = 100A/μs	120	250	530	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 18A, dI_F/dt = 100A/μs	1.3	2.6	5.6	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 1.9mH, R_{GS} = 50Ω, I_{PEAK} = 20A. (See Figures 14 & 15)

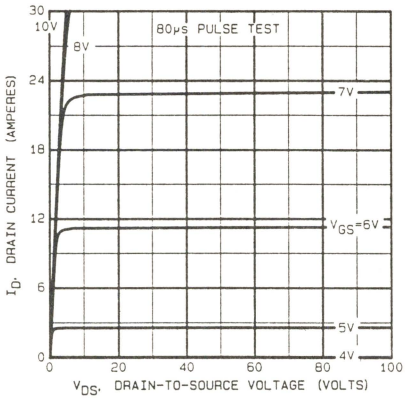


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

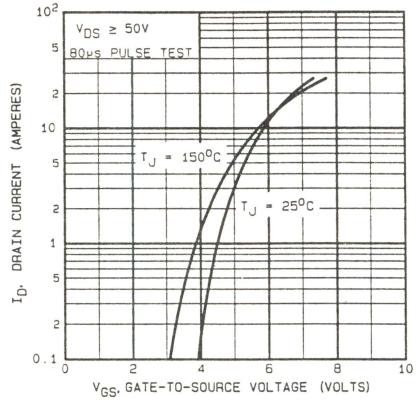


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

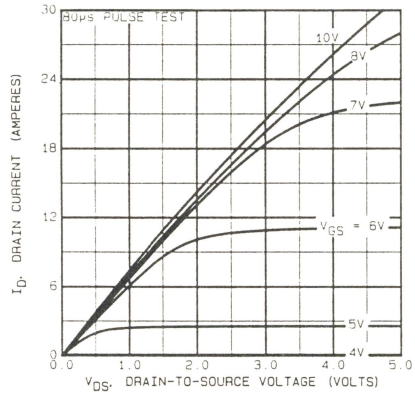


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

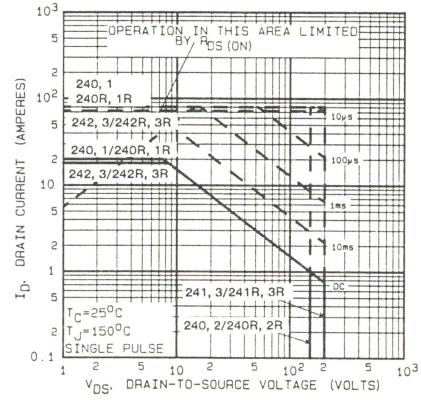


FIGURE 4. MAXIMUM SAFE OPERATING AREA

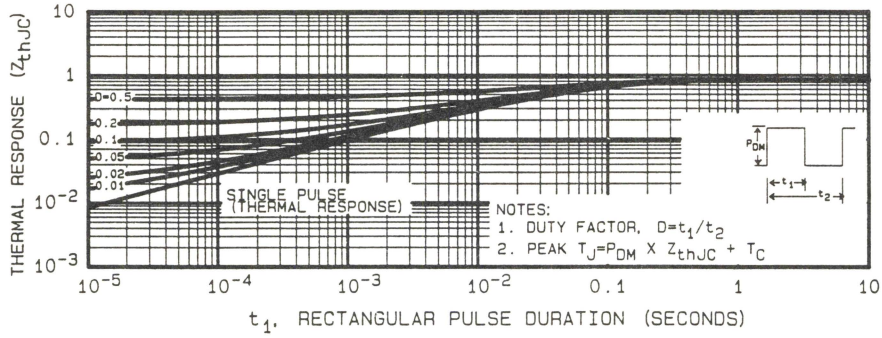


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

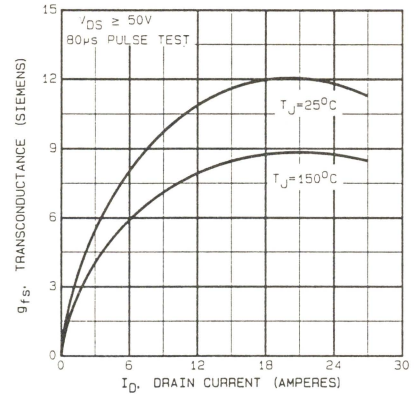


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

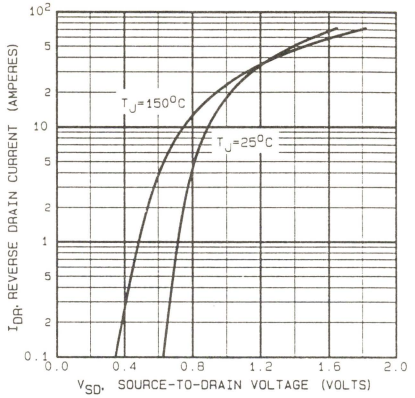


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

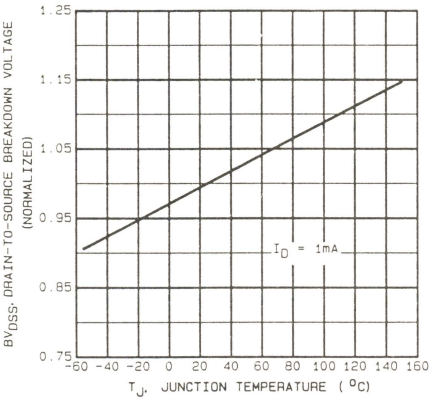


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

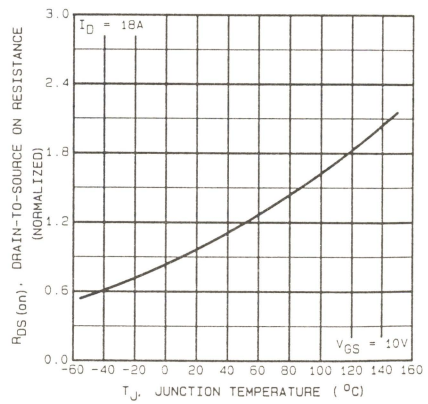


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

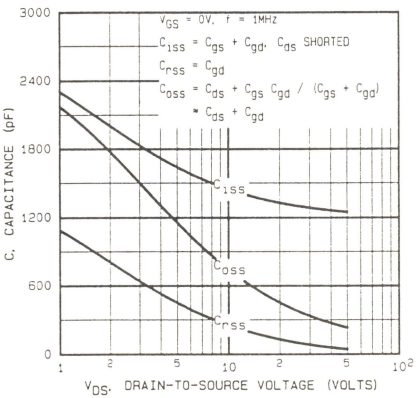


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

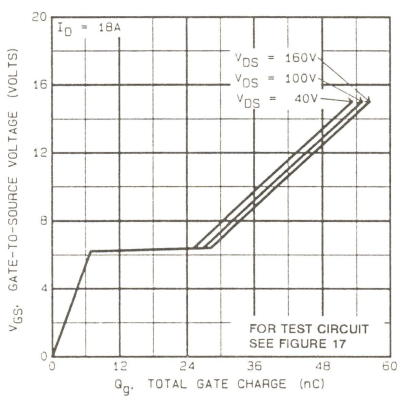


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

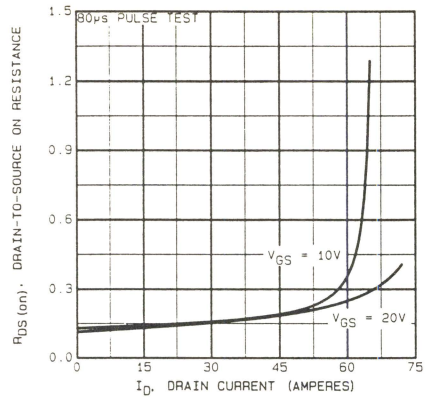


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

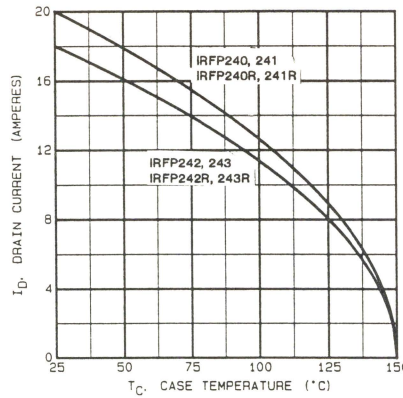


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

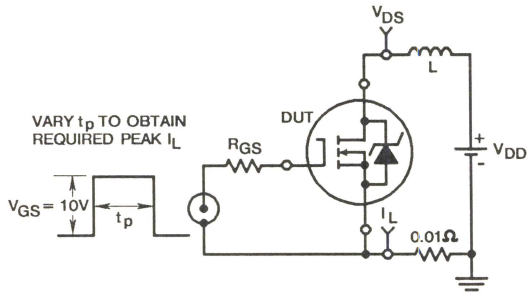


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

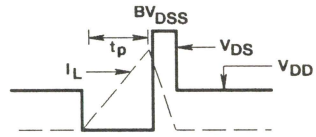


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

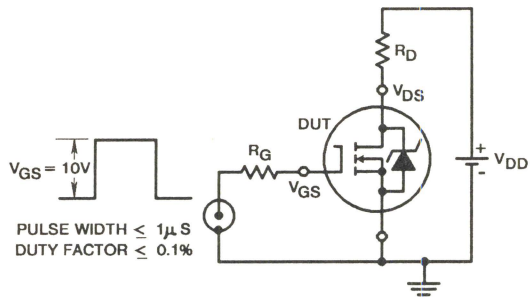


FIGURE 16. SWITCHING TIME TEST CIRCUIT

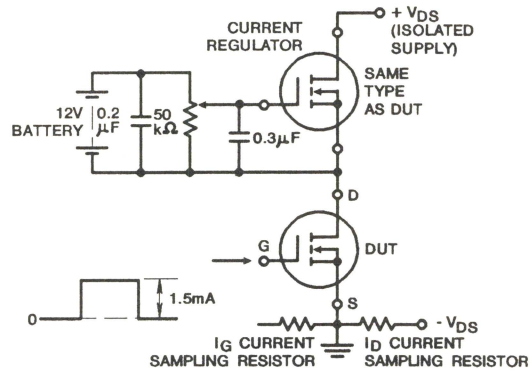


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP244, IRFP245 IRFP246, IRFP247

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 15A and 14A, 275V - 250V
- $r_{DS(on)}$ = 0.28Ω and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275V, 250V DC Rated - 120V AC Line System Operation

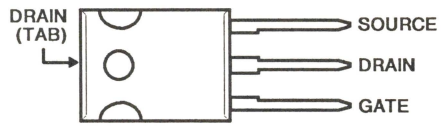
Description

The IRFP244, IRFP245, IRFP246, and IRFP247 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

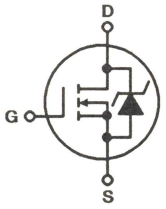
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP244	IRFP245	IRFP246	IRFP247	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	15	14	15	14	A
T_C = +100°C	I_D	9.7	8.8	9.7	8.8	A
Pulsed Drain Current (3)	I_{DM}	60	56	60	56	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	150	150	150	150	W
Linear Derating Factor		1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	550	550	550	550	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, I_{PEAK} = 15A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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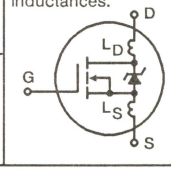
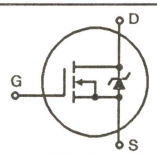
File Number 2211.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP244, IRFP245	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	–	–	V
IRFP246, IRFP247			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFP244, IRFP246	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	15	–	–	A
IRFP245, IRFP247			14	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP244, IRFP246	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 10A	–	0.20	0.28	Ω
IRFP245, IRFP247			–	0.24	0.34	V
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 10A	6.7	11	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1300	–	pF
Output Capacitance	C_{OSS}		–	320	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	69	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 15A, R_G = 9.1Ω, See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	24	ns
Rise Time	t_r		–	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	53	80	ns
Fall Time	t_f		–	49	74	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 15A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	39	59	nC
Gate-Source Charge	Q_{gs}		–	6.6	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	20	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	15	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	60	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 15A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	150	300	640	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 14A, dI_F/dt = 100A/μs	1.6	3.4	7.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, I_{PEAK} = 15A. (See Figures 14 & 15)

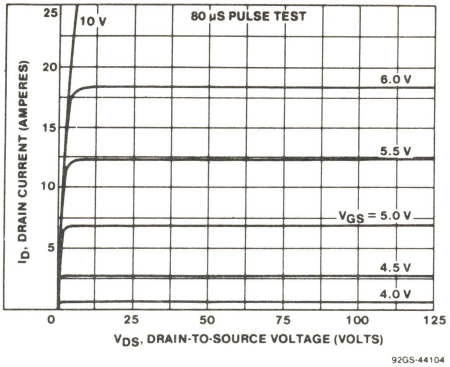


Fig. 1 - Typical output characteristics.

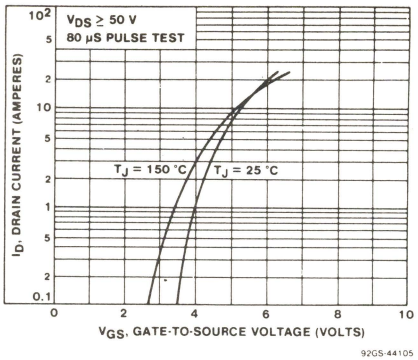


Fig. 2 - Typical transfer characteristics.

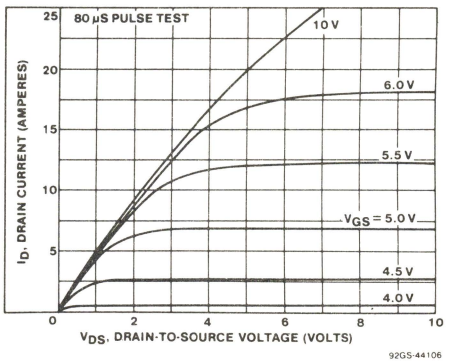


Fig. 3 - Typical saturation characteristics.

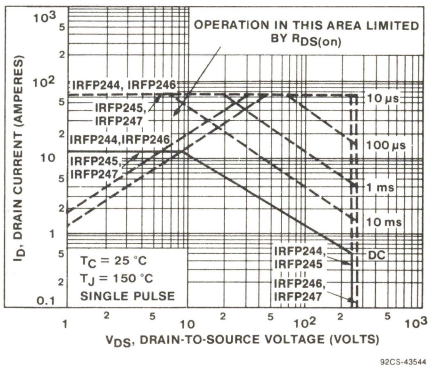


Fig. 4 - Maximum safe operating area.

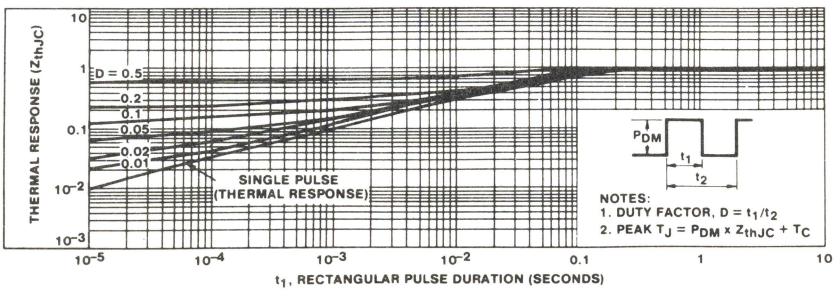


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

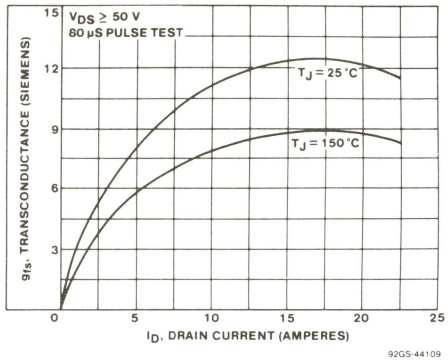


Fig. 6 - Typical transconductance vs. drain current.

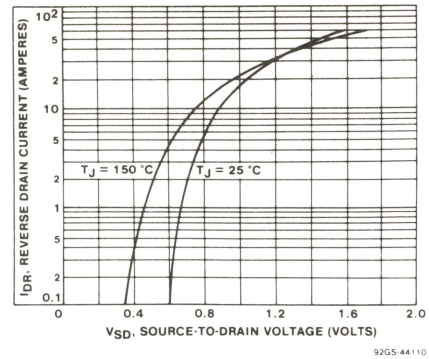


Fig. 7 - Typical source-drain diode forward voltage.

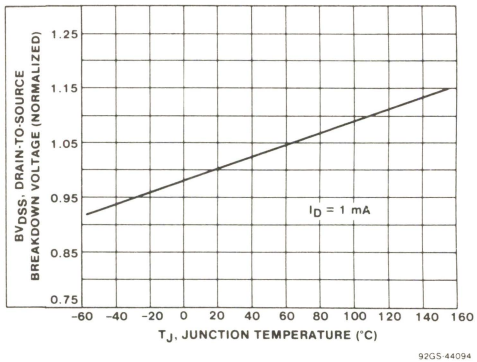


Fig. 8 - Breakdown voltage vs. temperature.

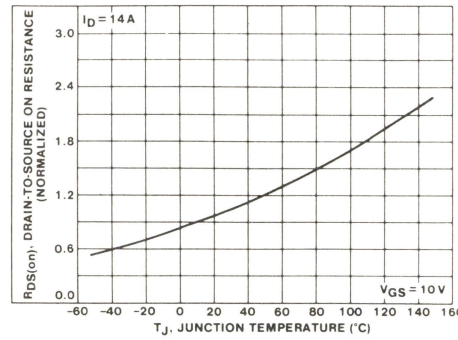


Fig. 9 - Normalized on-resistance vs. temperature.

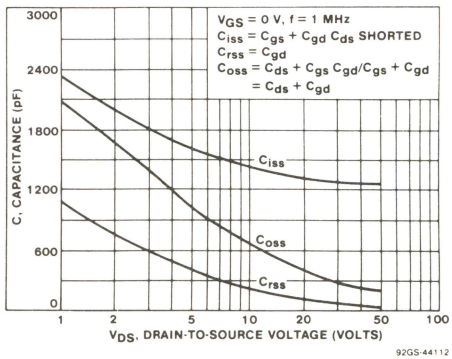


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

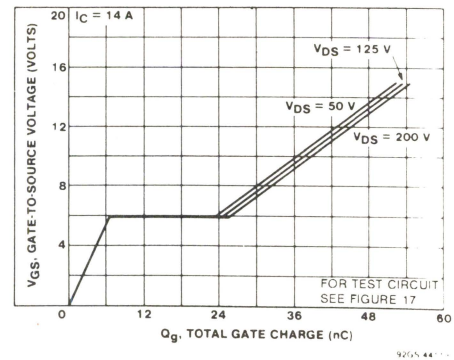


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

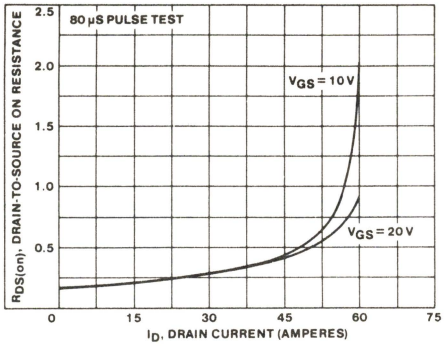


Fig. 12 - Typical on-resistance vs. drain current.

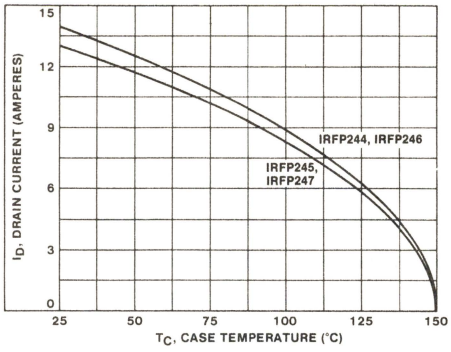


Fig. 13 - Maximum drain current vs case temperature.

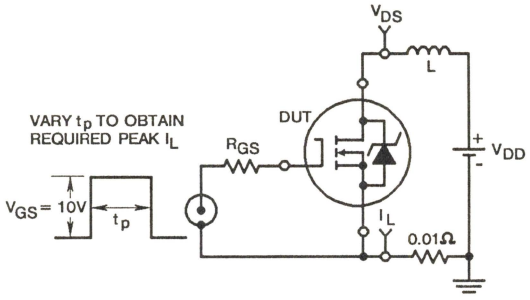


Fig. 14 - Unclamped energy test circuit.

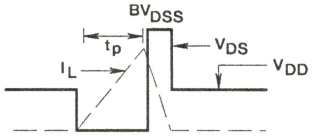


Fig. 15 - Unclamped energy waveforms.

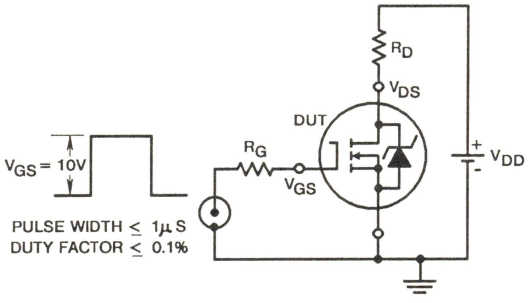


Fig. 16 - Switching time test circuit.

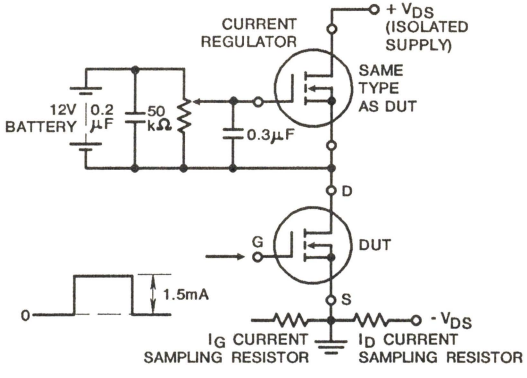


Fig. 17 - Gate charge test circuit.

HARRIS

IRFP250/251/252/253
IRFP250R/251R/252R/253R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 27A and 33A, 150V - 200V
- $r_{DS(on)}$ = 0.085Ω and 0.120Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

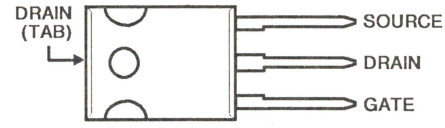
Description

The IRFP250, IRFP251, IRFP252, and IRFP253 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP250R, IRFP251R, IRFP252R, and IRFP253R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

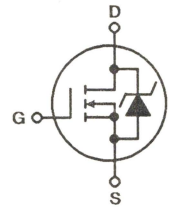
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP250 IRFP250R	IRFP251 IRFP251R	IRFP252 IRFP252R	IRFP253 IRFP253R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	200	150	200	150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	200	150	200	150	V
Continuous Drain Current					
T_C = +25°C ..... I_D	33	33	27	27	A
T_C = +100°C ..... I_D	21	21	17	17	A
Pulsed Drain Current (3) ..... I_{DM}	130	130	110	110	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	120	120	100	100	A
Single Pulse Avalanche Energy Rating (4) ..... E_{as}*	810	810	810	810	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 1.1mH, R_{GS} = 50Ω, I_{PEAK} = 33A. See Figure 15.

* R Suffix Types Only

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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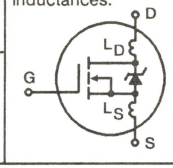
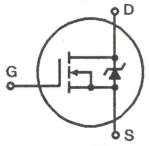
File Number **2330.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP250/252, IRFP250R/252R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	200	–	–	V
IRFP251/253, IRFP251R/253R			150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP250/251, IRFP250R/251R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	33	–	–	A
IRFP252/253, IRFP252R/253R			27	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP250/251, IRFP250R/251R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 17A	–	0.07	0.085	Ω
IRFP252/253, IRFP252R/253R			–	0.09	0.120	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 17A	13	19	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	800	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	300	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, I_D = 30A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	18	30	ns
Rise Time	t_r		–	125	180	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	70	100	ns
Fall Time	t_f		–	80	120	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 30A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	79	120	nC
Gate-Source Charge	Q_{gs}		–	12	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	33	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	130	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 33A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/µs	140	–	630	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 30A, dI_F/dt = 100A/µs	1.8	–	8.1	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 1.1mH, R_{GS} = 50Ω, I_{PEAK} = 33A (See Figure 15)

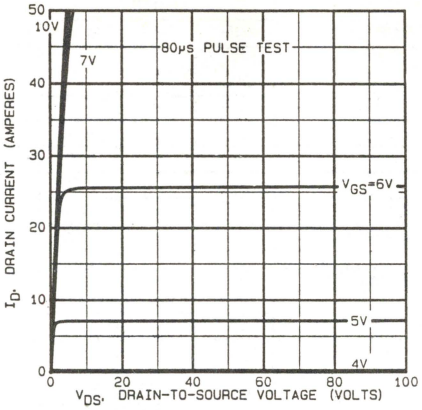


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

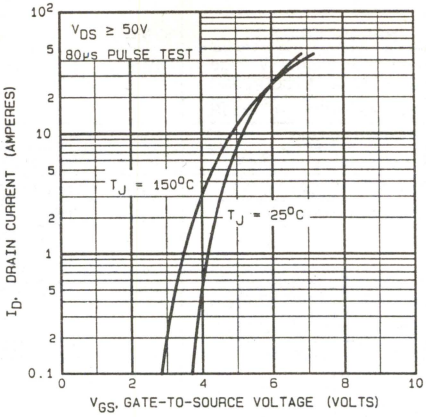


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

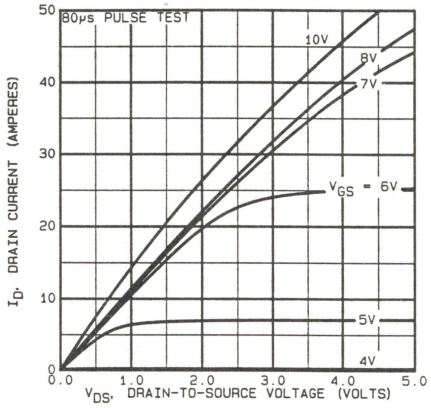


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

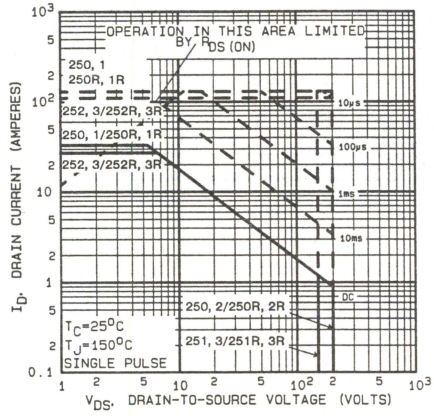


FIGURE 4. MAXIMUM SAFE OPERATING AREA

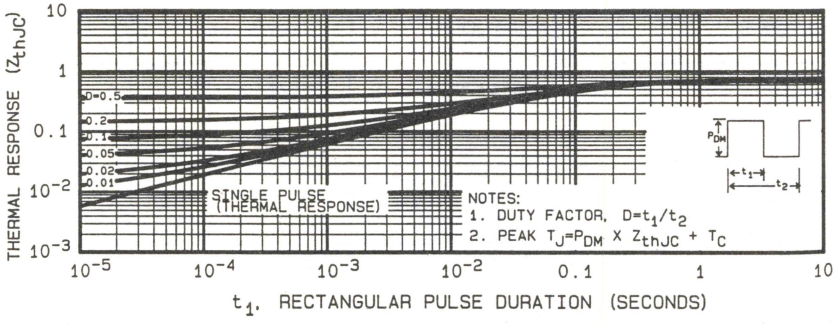


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

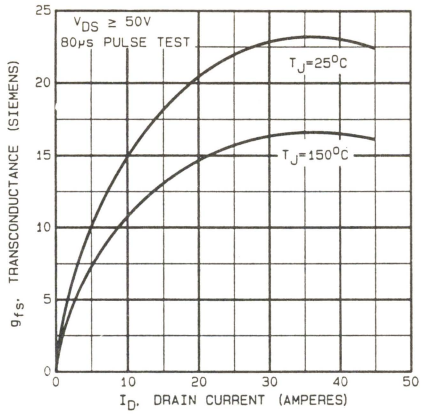


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

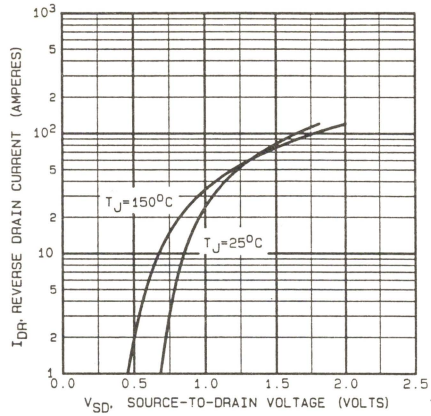


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

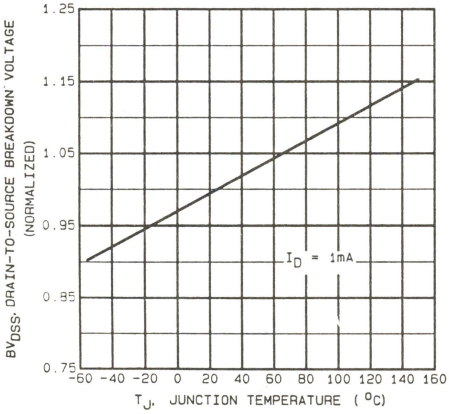


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

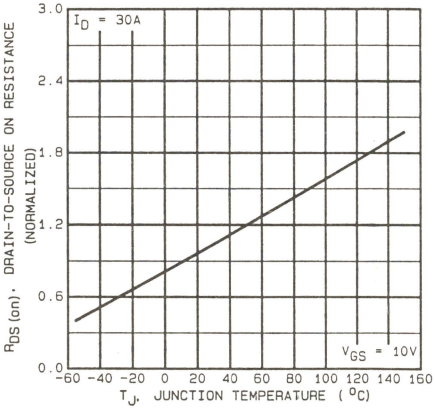


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

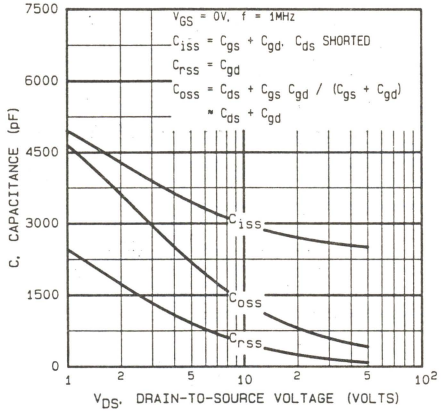


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

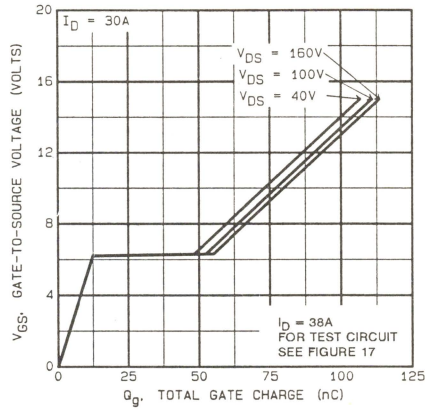


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

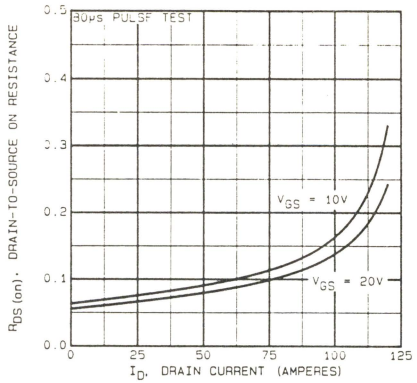


FIGURE 12. TYPICAL ON RESISTANCE vs DRAIN CURRENT

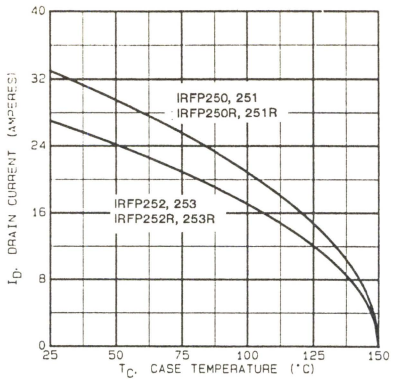


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

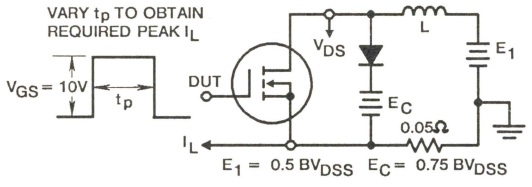


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

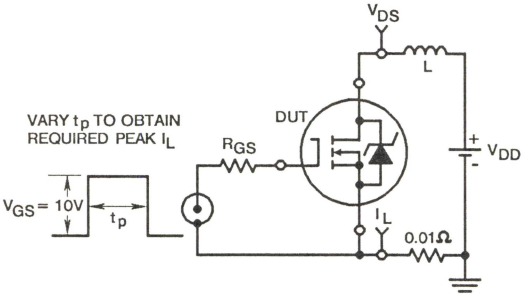


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

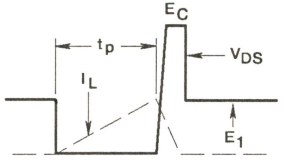


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

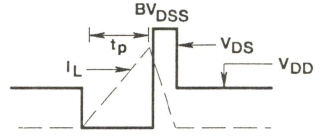


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

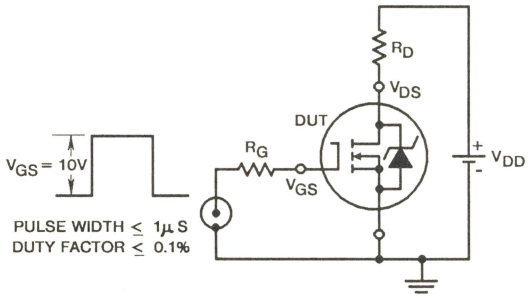


FIGURE 16. SWITCHING TIME TEST CIRCUIT

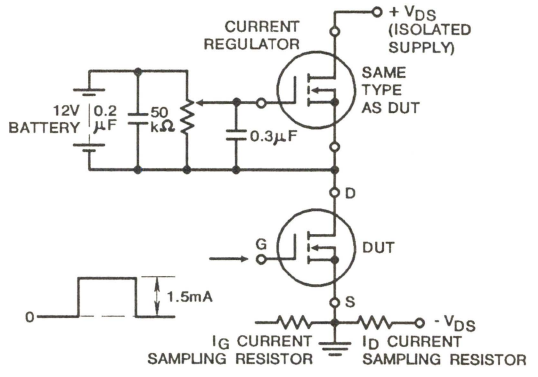


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP254, IRFP255 IRFP256, IRFP257

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 21A and 23A, 250V and 275V
- $r_{DS(on)} = 0.14\Omega$ and 0.17Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 250V, 275V DC Rated - 120V AC Line System Operation

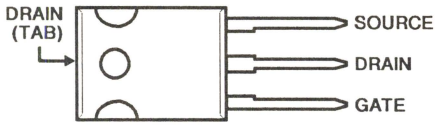
Description

The IRFP254, IRFP255, IRFP256, and IRFP257 are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

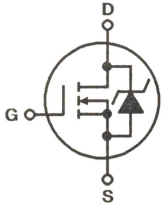
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP254	IRFP255	IRFP256	IRFP257	UNITS
Drain-Source Voltage (1)	V_{DS}	250	250	275	275	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current						
T_C = +25°C	I_D	23	21	23	21	A
T_C = +100°C	I_D	15	13	15	13	A
Pulsed Drain Current (3)	I_{DM}	92	84	92	84	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation						
T_C = +25°C	P_D	180	180	180	180	W
Linear Derating Factor		1.44	1.44	1.44	1.44	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	1000	1000	1000	1000	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 3.1mH, R_{GS} = 25Ω, I_{PEAK} = 23A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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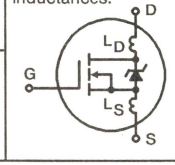
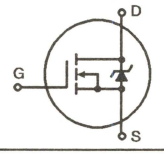
File Number **2289.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP254, IRFP255	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	250	–	–	V
IRFP256, IRFP257			275	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFP254, IRFP256	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	23	–	–	A
IRFP255, IRFP257			21	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP254, IRFP256	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 13A	–	0.11	0.14	V
IRFP255, IRFP257			–	0.14	0.17	V
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > 50V, I_D = 13A	11	17	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2700	–	pF
Output Capacitance	C_{OSS}		–	580	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	130	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 23A, R_G = 6.2Ω, See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	19	29	ns
Rise Time	t_r		–	84	130	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	75	110	ns
Fall Time	t_f		–	65	98	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 23A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	87	130	nC
Gate-Source Charge	Q_{gs}		–	14	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	73	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	23	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	92	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 23A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/μs	150	310	650	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 22A, dI_F/dt = 100A/μs	1.9	4	8.4	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 3.1mH, R_{GS} = 25Ω, I_{PEAK} = 23A. (See Figures 14 & 15)

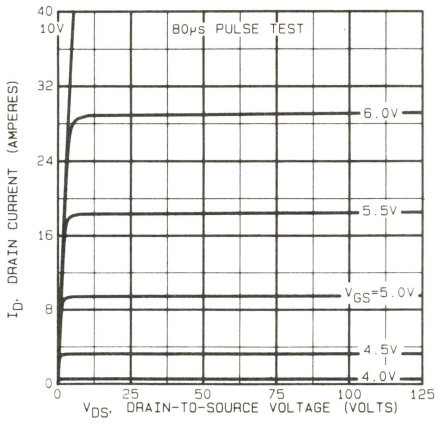


Fig. 1 - Typical output characteristics.

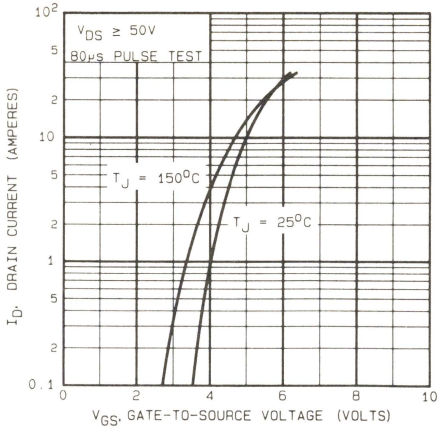


Fig. 2 - Typical transfer characteristics.

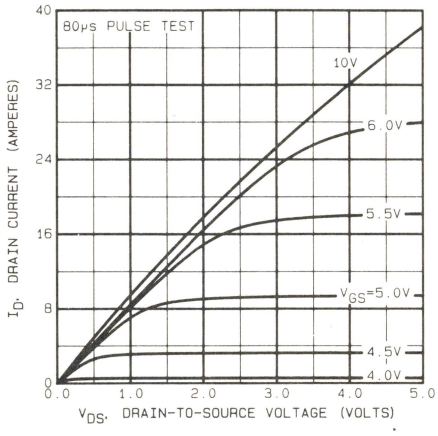


Fig. 3 - Typical saturation characteristics.

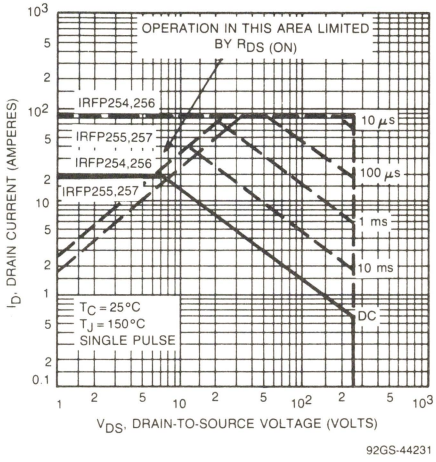


Fig. 4 - Maximum safe operating area.

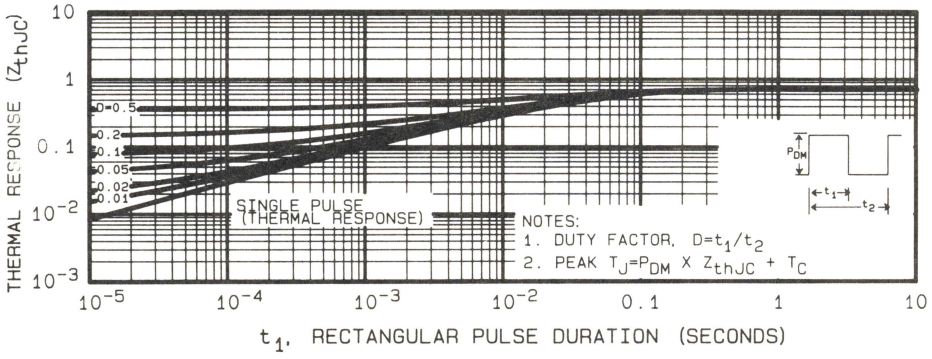


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

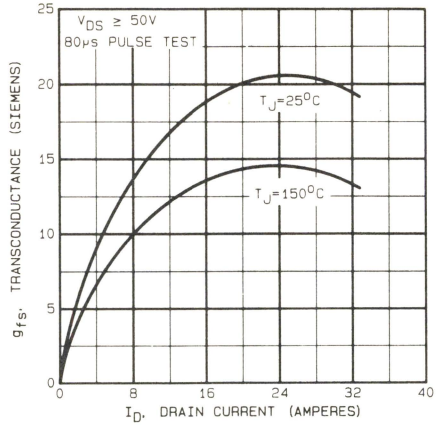


Fig. 6 - Typical transconductance vs. drain current.

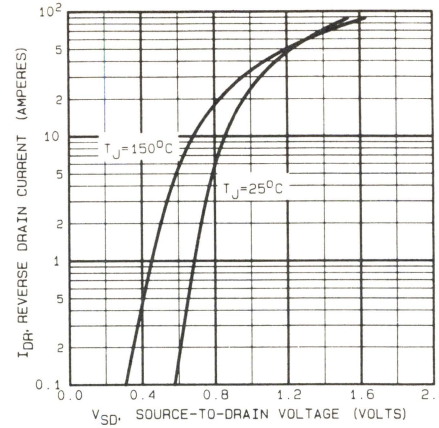


Fig. 7 - Typical source-drain diode forward voltage.

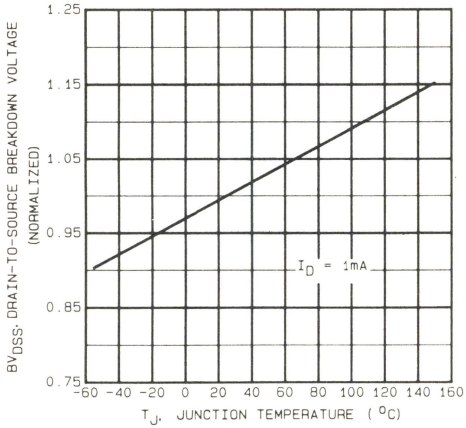


Fig. 8 - Breakdown voltage vs. temperature.

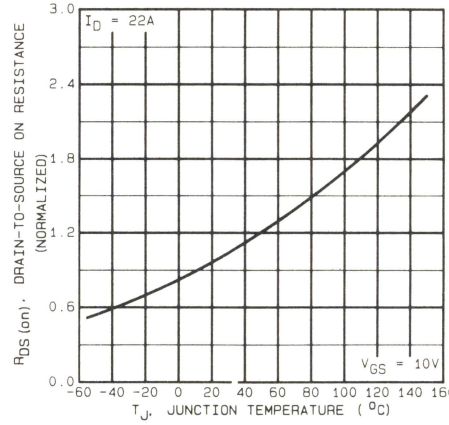


Fig. 9 - Normalized on-resistance vs. temperature.

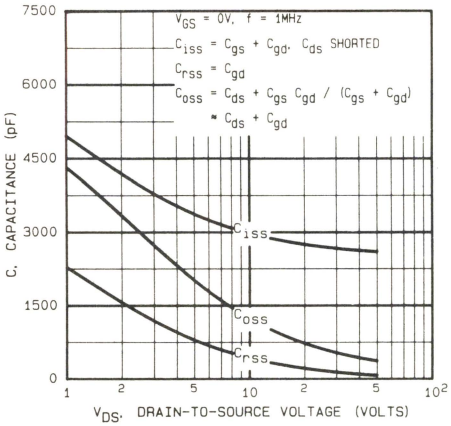


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

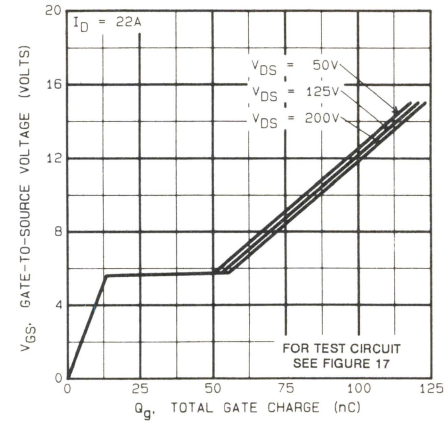


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

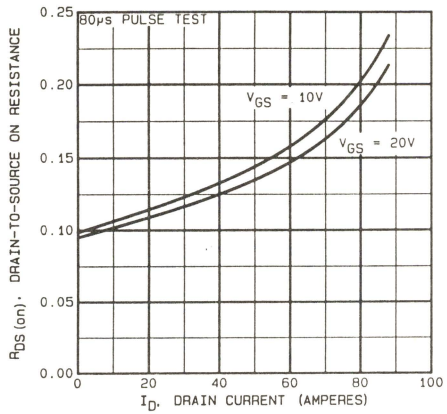


Fig. 12 – Typical on-resistance vs. drain current.

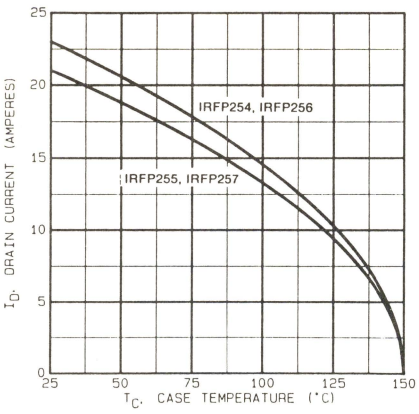


Fig. 13 – Maximum drain current vs case temperature.

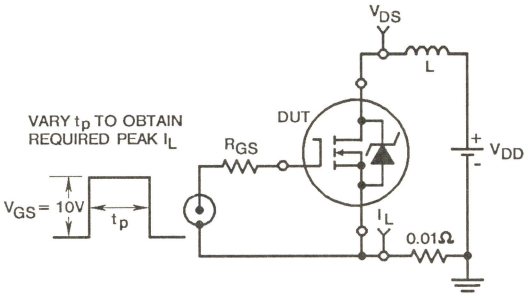


Fig. 14 – Unclamped energy test circuit.

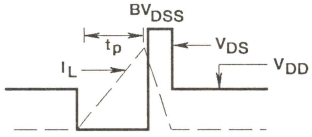


Fig. 15 – Unclamped energy waveforms.

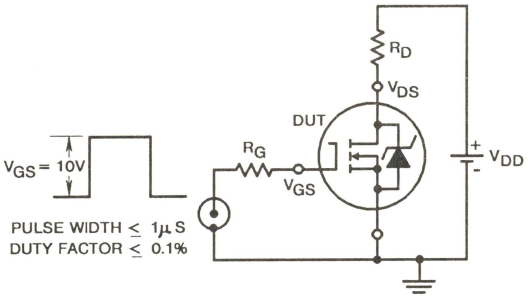


Fig. 16 – Switching time test circuit.

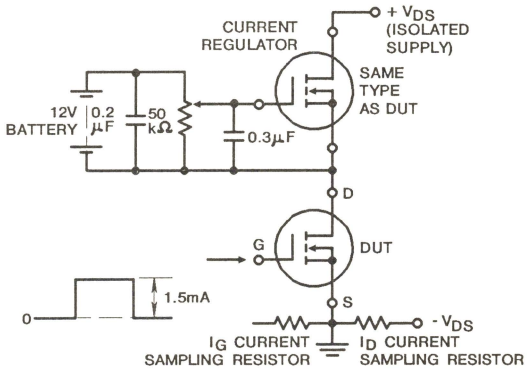


Fig. 17 – Gate charge test circuit.

HARRIS

IRFP340R, IRFP341R IRFP342R, IRFP343R

N-Channel Power MOSFETs Avalanche Energy Rated

August 1991

Features

- 11A and 8.7A, 350V and 400V
- $r_{DS(on)}$ = 0.55Ω and 0.80Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

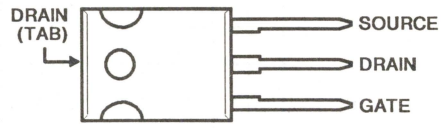
Description

The IRFP340R, IRFP341R, IRFP342R, and IRFP343R are advanced power MOSFETs designed, tested and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

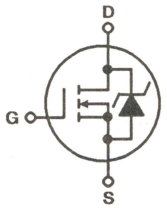
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP340R	IRFP341R	IRFP342R	IRFP343R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	11	11	8.7	8.7	A
T_C = +100°C ..... I_D	6.8	6.8	5.5	5.5	A
Pulsed Drain Current (3) ..... I_{DM}	44	44	35	35	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	480	480	480	480	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 7.0mH, R_{GS} = 50Ω, I_{PEAK} = 11A. See Figures 14 and 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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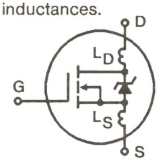
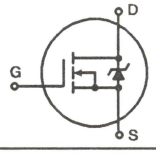
File Number **2088.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP340R, IRFP342R	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	–	–	V
IRFP341R, IRFP343R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 2) IRFP340R, IRFP341R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	11	–	–	A
IRFP342R, IRFP343R			8.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP340R, IRFP341R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 5.5A	–	0.47	0.55	Ω
IRFP342R, IRFP343R			–	0.68	0.80	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 5.5A	6.1	9.1	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1250	–	pF
Output Capacitance	C_{OSS}		–	300	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	80	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} ≃ 200V, I_D = 11A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	14	21	ns
Rise Time	t_r		–	27	41	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	75	ns
Fall Time	t_f		–	24	36	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	41	63	nC
Gate-Source Charge	Q_{gs}		–	6.0	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	23	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	11	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	44	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 11A, V_{GS} = 0V	–	–	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	170	370	790	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 10A, dI_F/dt = 100A/μs	1.6	3.8	8.2	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 7.0mH, R_{GS} = 50Ω, I_{PEAK} = 11A. (See Figures 14 & 15)

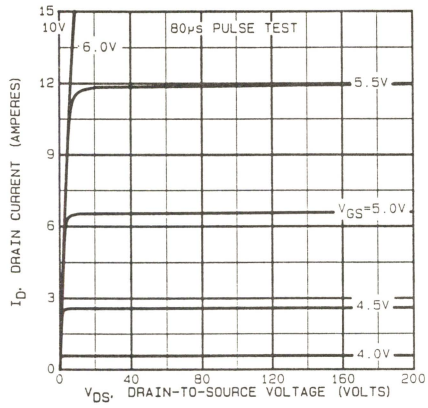


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

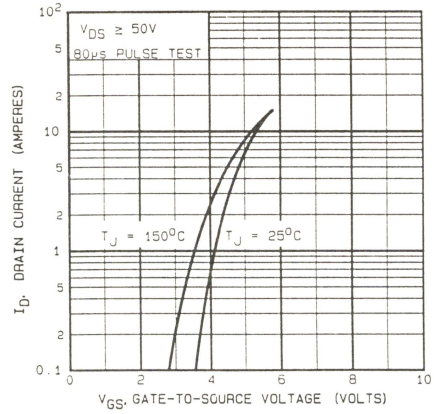


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

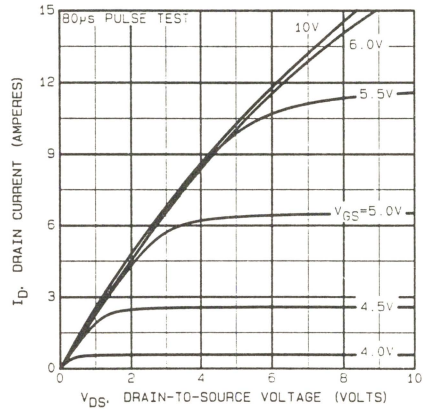


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

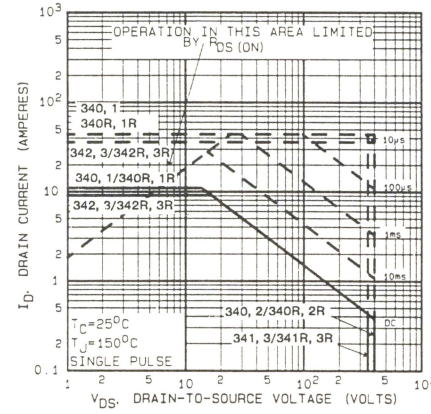


FIGURE 4. MAXIMUM SAFE OPERATING AREA

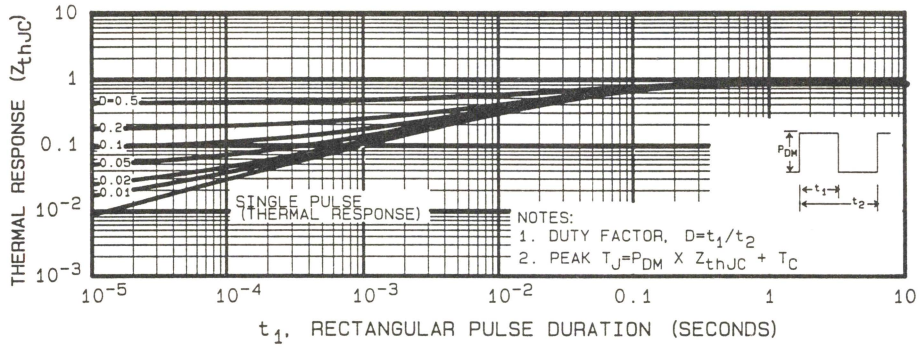


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

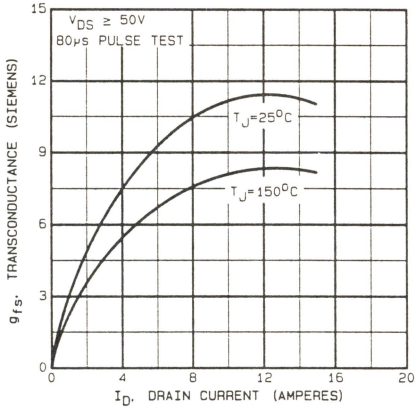


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

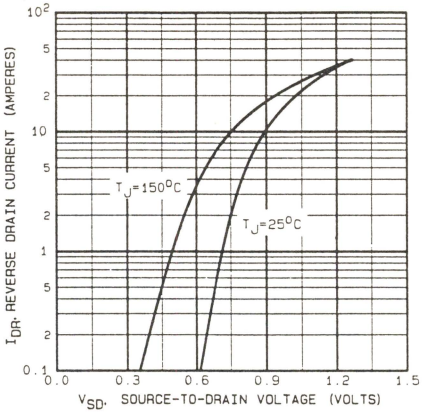


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

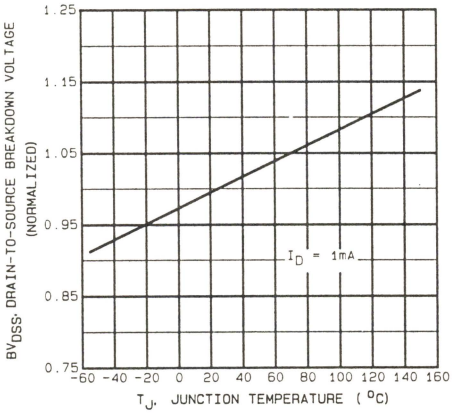


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

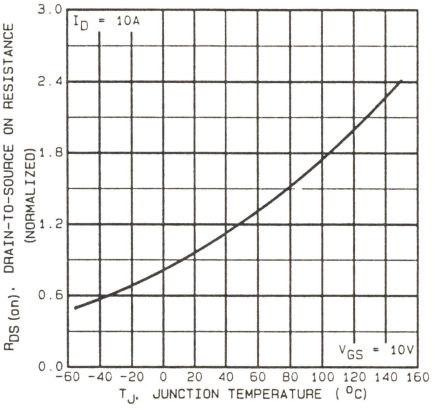


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

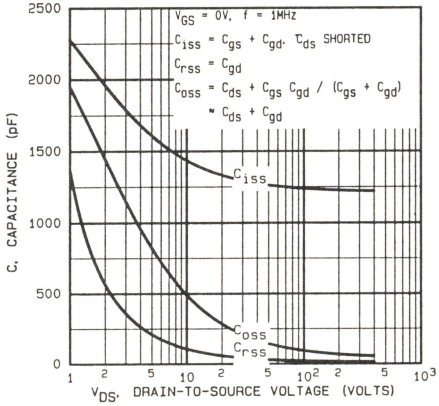


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

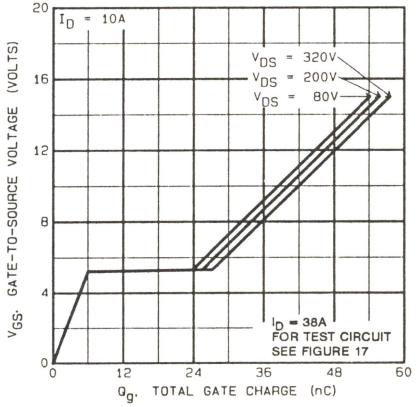


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

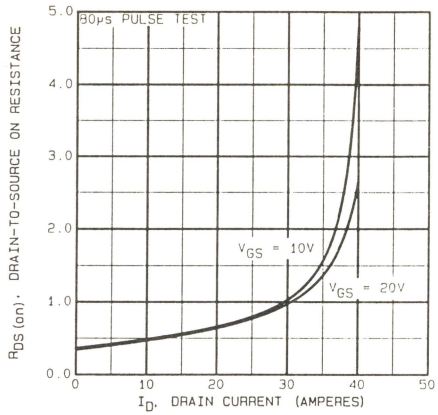


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

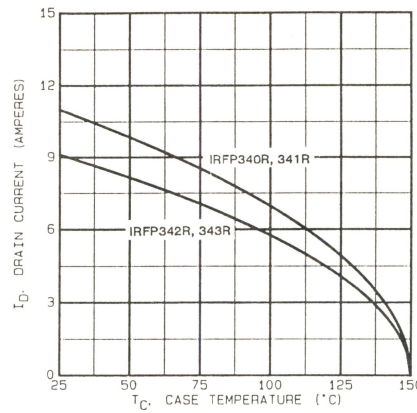


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

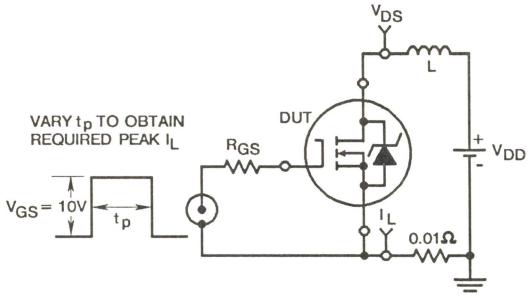


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

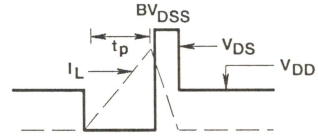


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

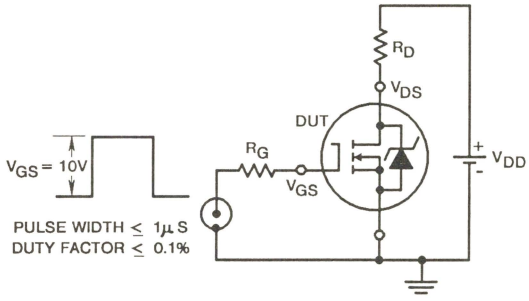


FIGURE 16. SWITCHING TIME TEST CIRCUIT

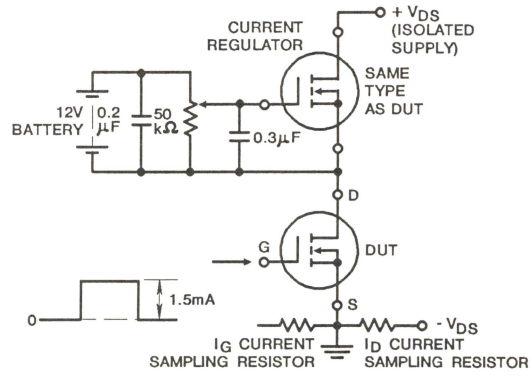


FIGURE 17. GATE CHARGE TEST CIRCUIT

IRFP350/351/352/353
IRFP350R/351R/352R/353R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1993

Features

- 14A and 16A, 350V - 400V
- $r_{DS}(on)$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

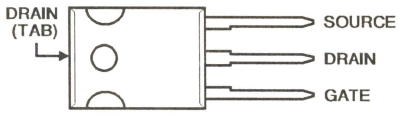
Description

The IRFP350, IRFP351, IRFP352, and IRFP353 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP350R, IRFP351R, IRFP352R and IRFP353R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the TO-247 plastic style package.

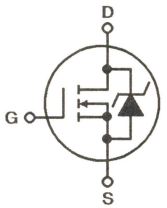
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP350 IRFP350R	IRFP351 IRFP351R	IRFP352 IRFP352R	IRFP353 IRFP353R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	400	350	400	350	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	400	350	400	350	V
Continuous Drain Current					
T_C = +25°C ..... I_D	16	16	14	14	A
T_C = +100°C ..... I_D	10	10	8.9	8.9	A
Pulsed Drain Current (3) ..... I_{DM}	64	64	56	56	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	64	64	56	56	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	700	700	700	700	mj
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 40V, starting T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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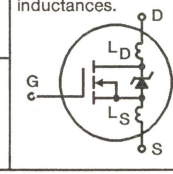
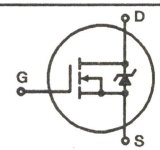
File Number **2319.2**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP350/352, IRFP350R/352R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	400	–	–	V
IRFP351/353, IRFP351R/353R			350	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP350/351, IRFP350R/351R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	16	–	–	A
IRFP352/353, IRFP352R/353R			14	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP350/351, IRFP350R/351R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 8.9A	–	0.25	0.3	Ω
IRFP352/353, IRFP352R/353R			–	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} = 2 x V_{GS}, I_D = 8.0A	8.0	10	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 16A, R_G = 6.2Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	12	18	ns
Rise Time	t_r		–	51	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	75	110	ns
Fall Time	t_f		–	47	71	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	87	130	nC
Gate-Source Charge	Q_{gs}		–	10	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	33	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	16	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	64	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 16A, V_{GS} = 0V	–	–	1.6	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/µs	270	–	1300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 15A, dI_F/dt = 100A/µs	1.7	–	8.1	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 40V, Start T_J = +25°C, L = 5.66mH, R_{GS} = 50Ω, I_{PEAK} = 15A (See Figure 15)

Performance Curves

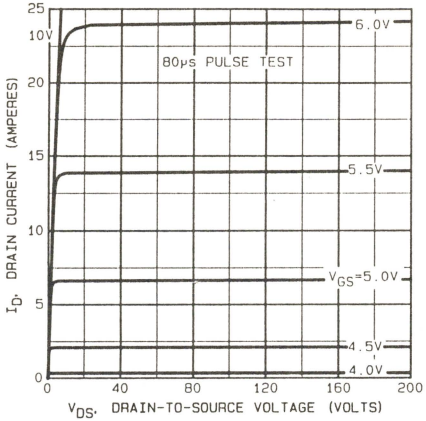


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

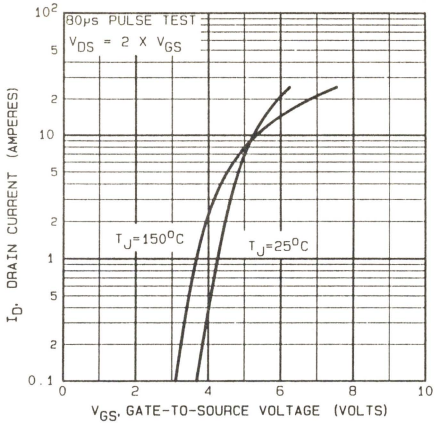


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

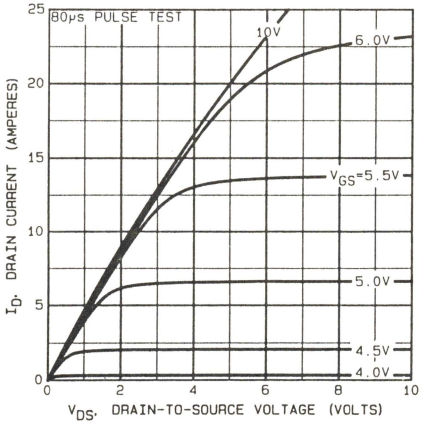


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

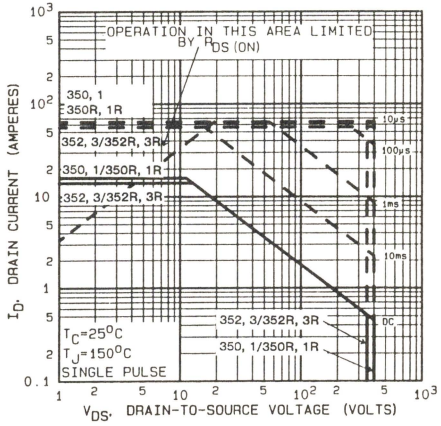


FIGURE 4. MAXIMUM SAFE OPERATING AREA

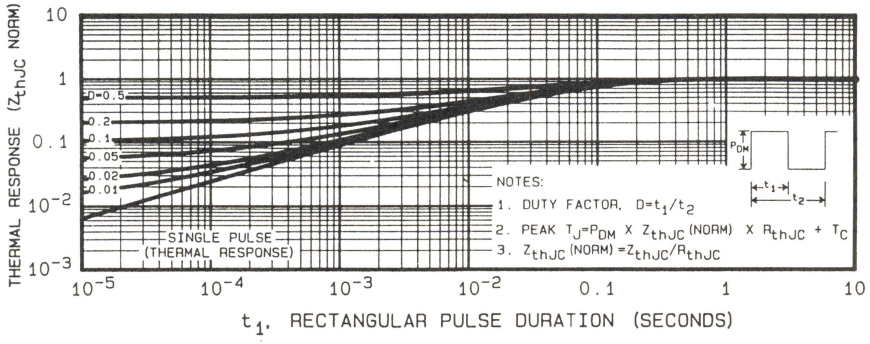


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

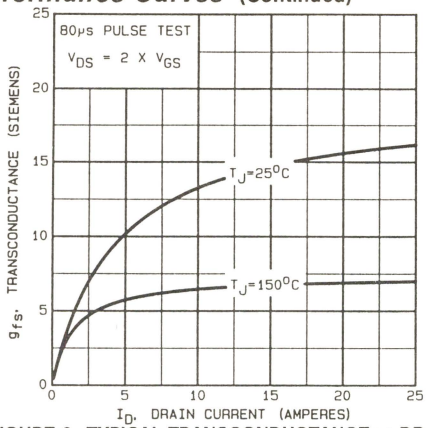


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

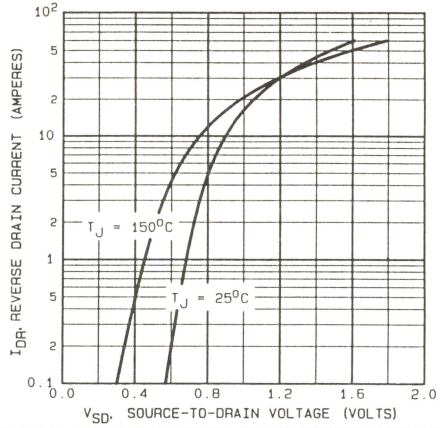


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

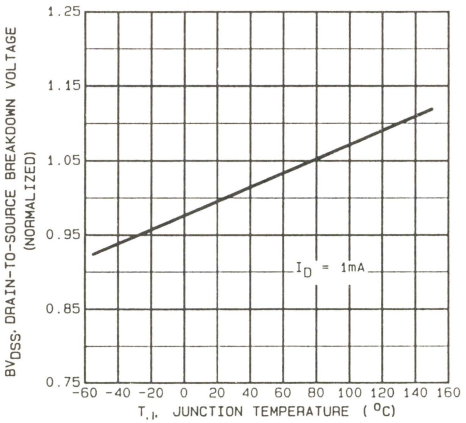


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

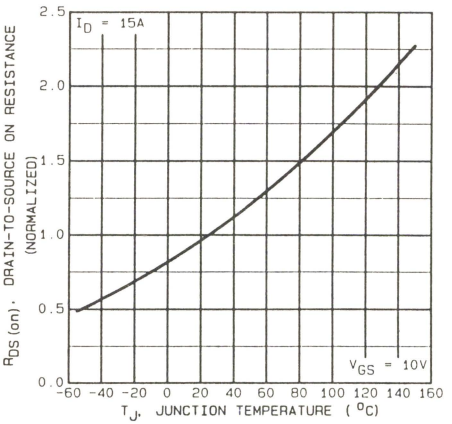


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

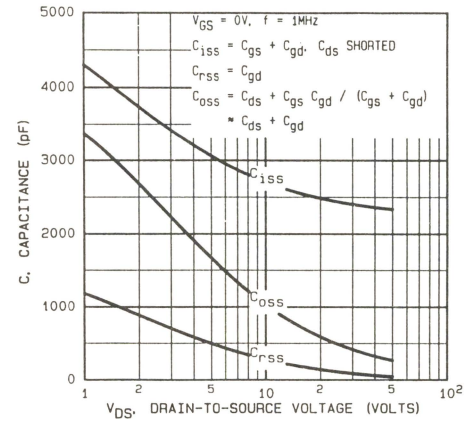


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

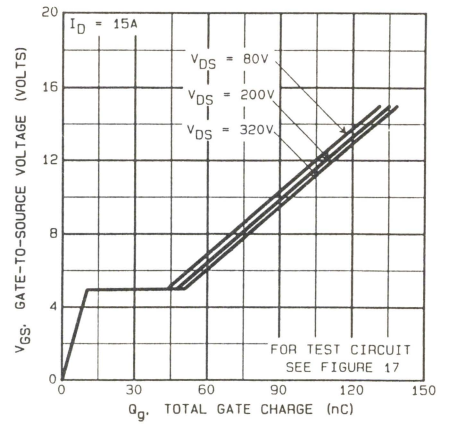


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

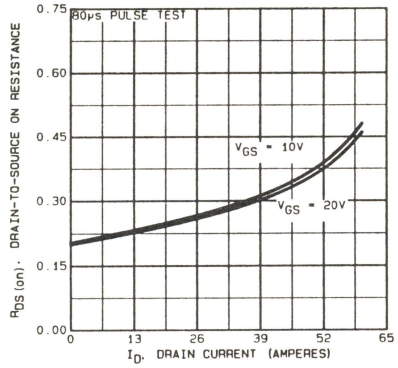


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

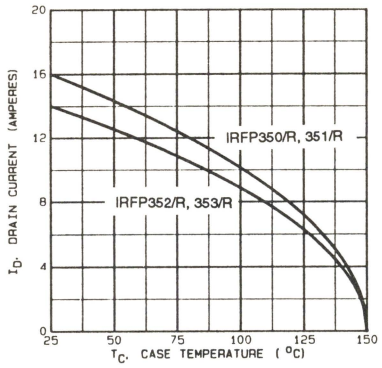


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

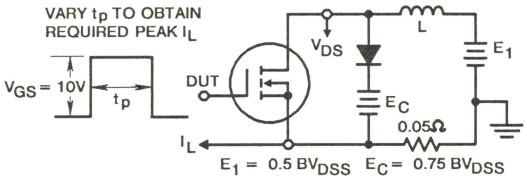


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

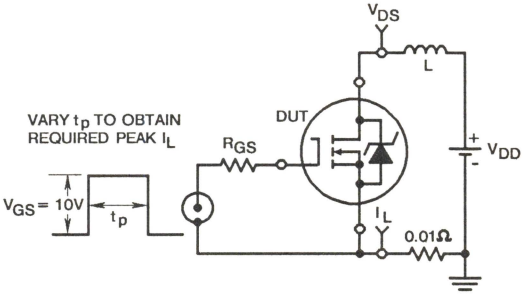


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

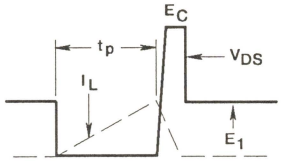


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

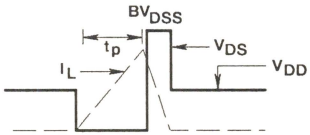


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

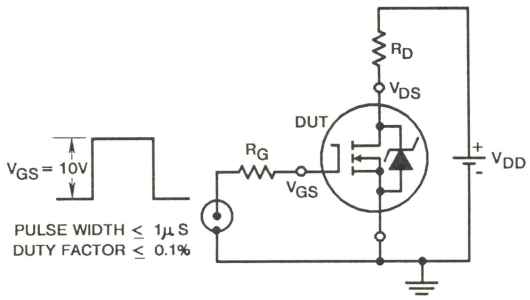


FIGURE 16. SWITCHING TIME TEST CIRCUIT

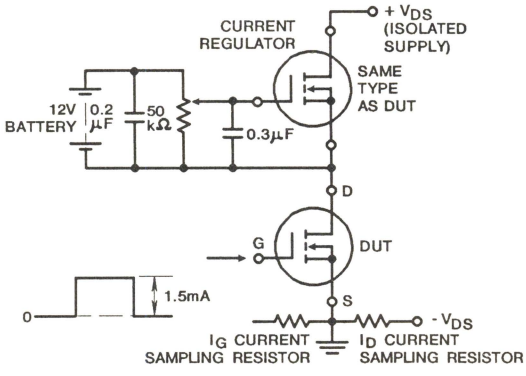


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP360
IRFP362

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 20A and 23A, 400V
- $r_{DS}(on)$ = 0.20Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

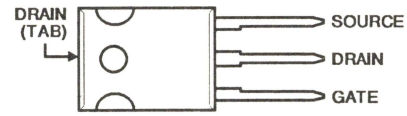
Description

The IRFP360 and IRFP362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

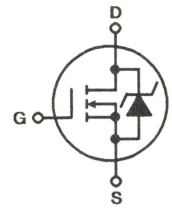
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP360	IRFP362	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	23	20	A
T_C = +100°C	I_D	14	13	A
Pulsed Drain Current (1)	I_{DM}	92	80	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	250	250	W
Linear Derating Factor		2.0	2.0	W/°C
Single Pulse Avalanche Energy Rating (2) See Figure 14	E_{AS}	1200	1200	mj
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.0mH, R_{GS} = 25Ω, Peak I_L = 23A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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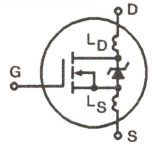
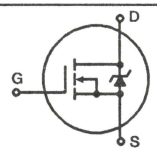
File Number **2290.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 3) IRFP360	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	23	-	-	A
IRFP362			20	-	-	A
Static Drain-Source On-State Resistance (Note 3) IRFP360	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 13A	-	0.18	0.20	Ω
IRFP362			-	0.20	0.25	Ω
Forward Transconductance (Note 3)	g_{fs}	$V_{DS} \geq$ 50V, I_{DS} > 13A	14	21	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	4000	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	97	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 25A, R_G = 4.3Ω R_D = 7.5Ω. (MOSFET switching times are essentially independent of operating temperature)	-	22	33	ns
Rise Time	t_r		-	94	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	66	99	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 25A, V_{DS} = 0.8V x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	68	100	nC
Gate-Source Charge	Q_{gs}		-	17	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	24	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.50	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	23	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	92	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 23A, V_{GS} = 0V	-	-	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	200	460	1000	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	3.1	7.1	16	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:
1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 50V, Start T_J = +25°C, L = 4.0mH, R_G = 25Ω, I_{PEAK} = 23A (See Figure 14)
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

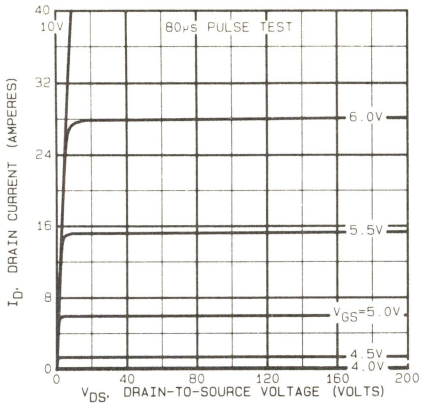


Fig. 1 - Typical output characteristics.

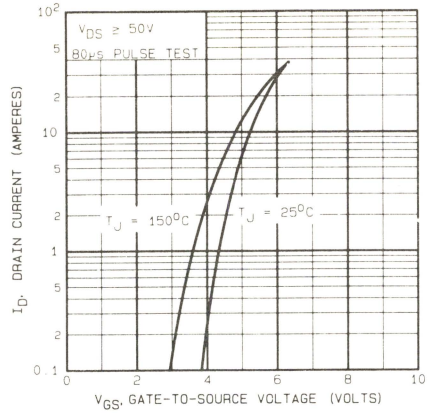


Fig. 2 - Typical transfer characteristics.

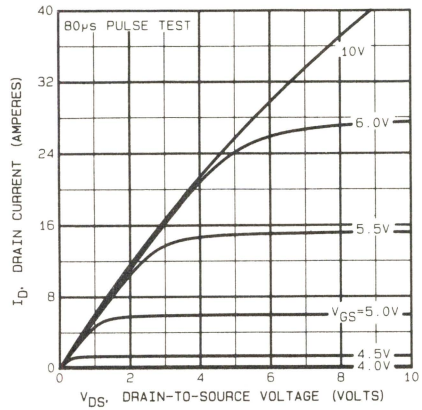


Fig. 3 - Typical saturation characteristics.

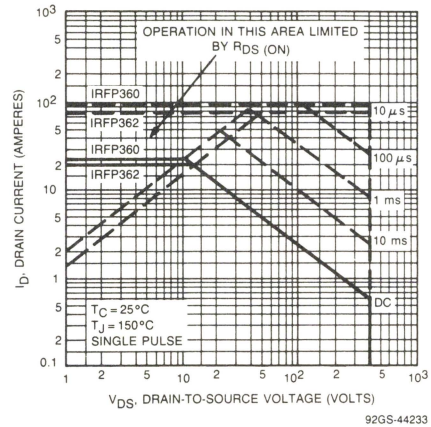


Fig. 4 - Maximum safe operating area.

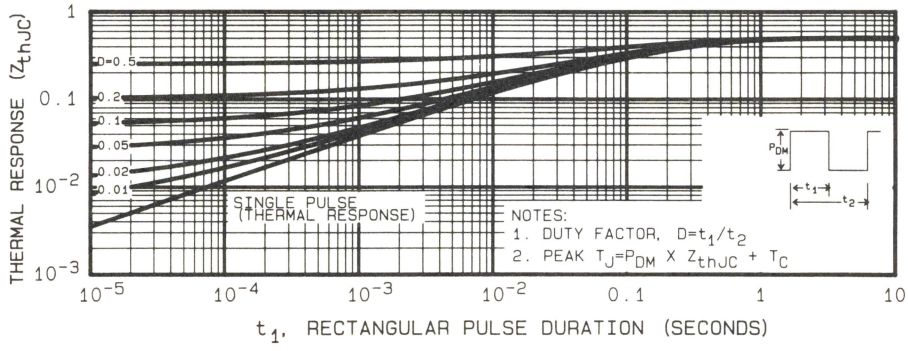


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

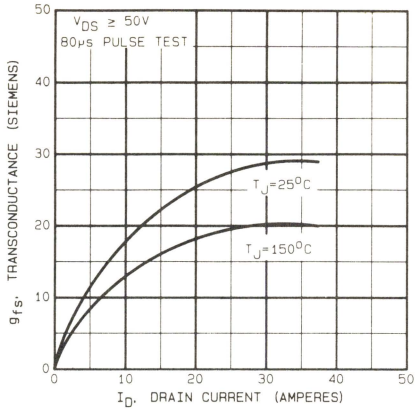


Fig. 6 - Typical transconductance vs. drain current.

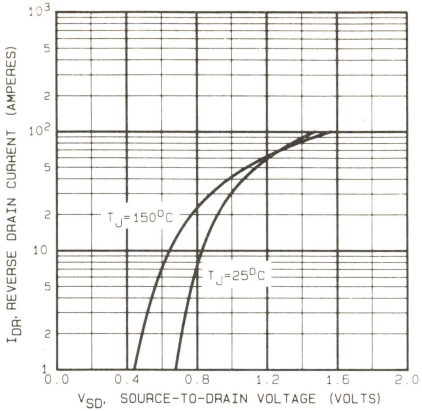


Fig. 7 - Typical source-drain diode forward voltage.

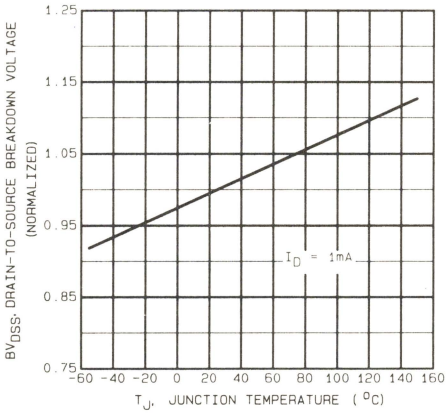


Fig. 8 - Breakdown voltage vs. temperature.

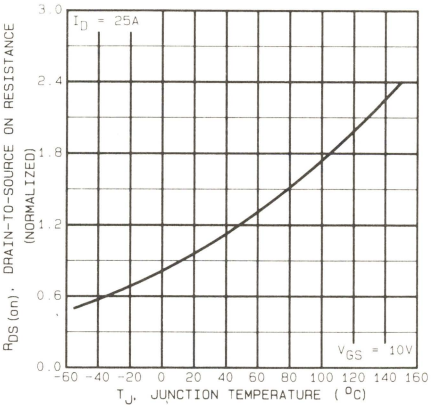


Fig. 9 - Normalized on-resistance vs. temperature.

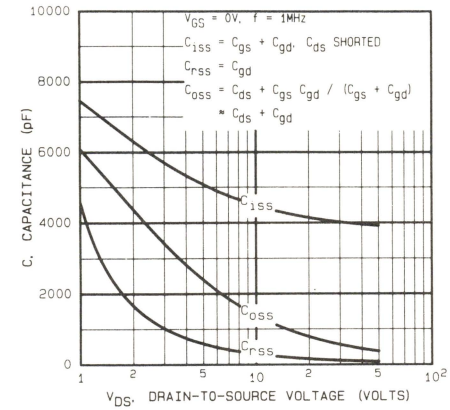


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

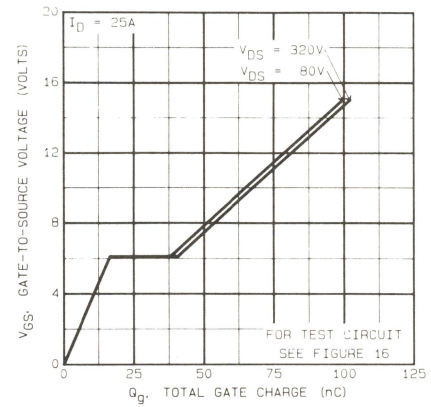


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

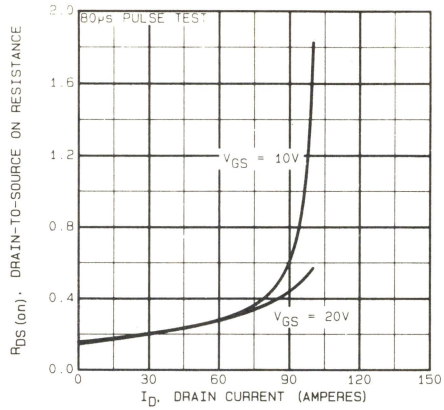


Fig. 12 - Typical on-resistance vs. drain current.

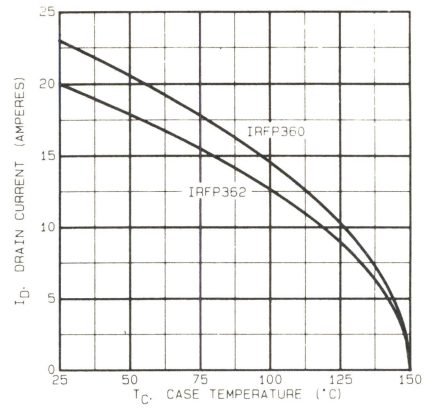


Fig. 13 - Maximum drain current vs. case temperature.

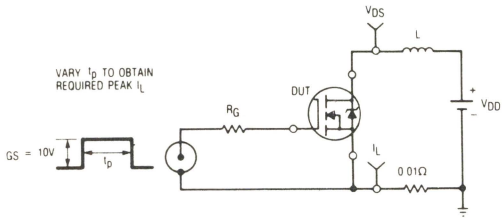


Fig. 14a - Unclamped inductive test circuit.

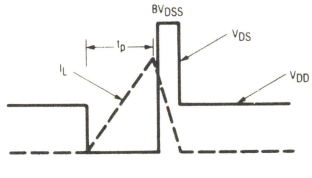


Fig. 14b - Unclamped inductive waveforms.

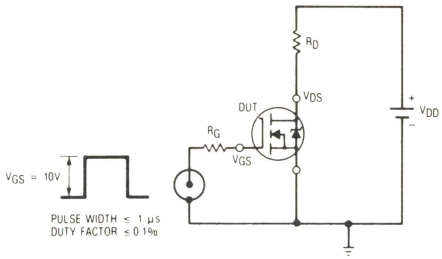


Fig. 15a - Switching time test circuit.

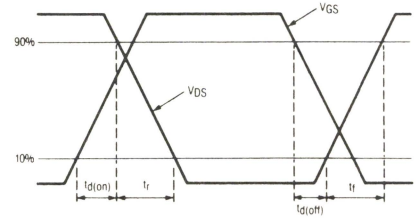


Fig. 15b - Switching time waveforms.

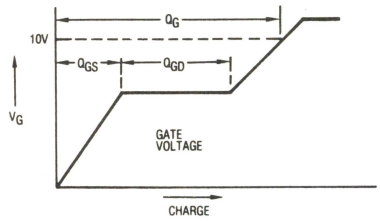


Fig. 16a - Basic gate charge waveform.

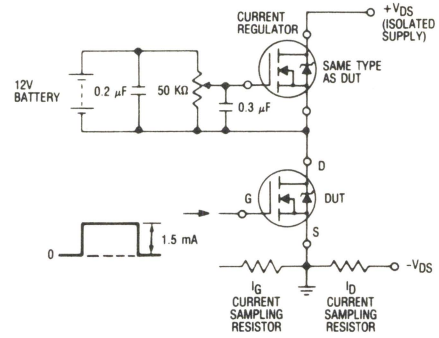


Fig. 16b - Gate charge test circuit.

HARRIS

IRFP440R, IRFP441R IRFP442R, IRFP443R

N-Channel Power MOSFETs Avalanche-Energy Rated

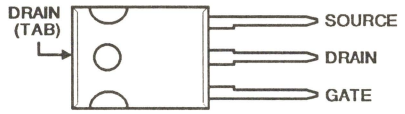
August 1991

Features

- 7.7A and 8.8A, 400V - 500V
- $r_{DS}(on)$ = 0.85Ω and 1.1Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Package

TO-247
TOP VIEW



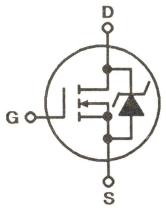
Description

The IRFP440R, IRFP441R, IRFP442R, and IRFP443R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP440R	IRFP441R	IRFP442R	IRFP443R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	8.8	8.8	7.7	7.7	A
T_C = +100°C ..... I_D	5.6	5.6	4.9	4.9	A
Pulsed Drain Current (3) ..... I_{DM}	35	35	31	31	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	150	150	150	150	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}	480	480	480	480	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
4. V_{DD} = 50V, starting T_J = +25°C, L = 11mH, R_{GS} = 50Ω, I_{PEAK} = 8.8A. See Figures 14 & 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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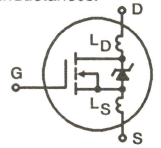
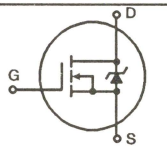
File Number 2089.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP440R, IRFP442R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRFP441R, IRFP443R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP440R, IRFP441R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = 10V	8.8	–	–	A
IRFP442R, IRFP443R			7.7	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP440R, IRFP441R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 4.9A	–	0.8	0.85	Ω
IRFP442R, IRFP443R			–	1.0	1.1	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq$ 50V, I_D = 4.9A	5.3	8.2	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1225	–	pF
Output Capacitance	C_{OSS}		–	200	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	85	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 8A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	17	21	ns
Rise Time	t_r		–	23	35	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	42	74	ns
Fall Time	t_f		–	18	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 8A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	42	63	nC
Gate-Source Charge	Q_{gs}		–	7	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	22	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.1	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	8.8	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	35	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 8.8A, V_{GS} = 0V	–	–	1.8	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	210	460	970	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 8.0A, dI_F/dt = 100A/µs	2	4.2	8.9	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 11mH, R_{GS} = 50Ω, I_{PEAK} = 8.8A (See Figures 14 & 15)

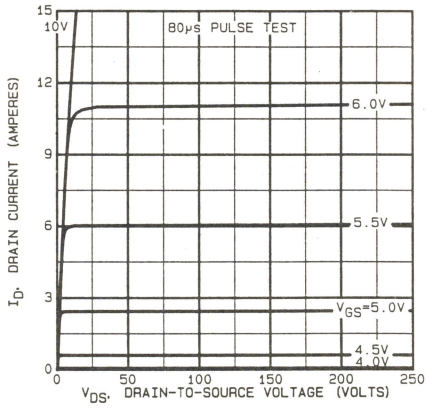


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

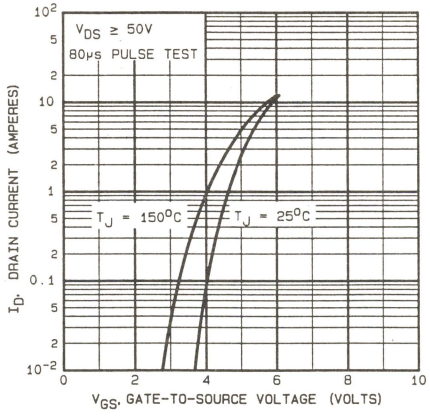


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

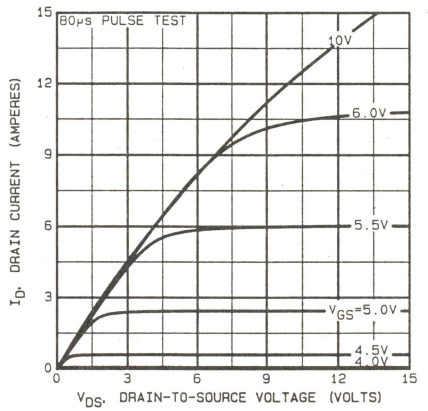


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

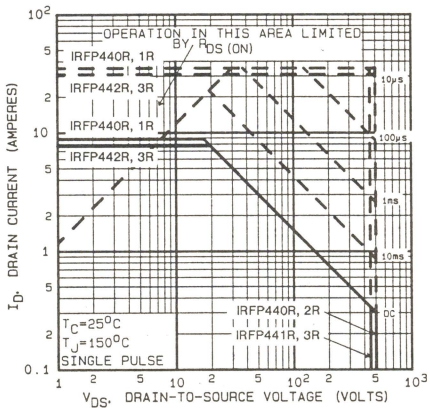


FIGURE 4. MAXIMUM SAFE OPERATING AREA

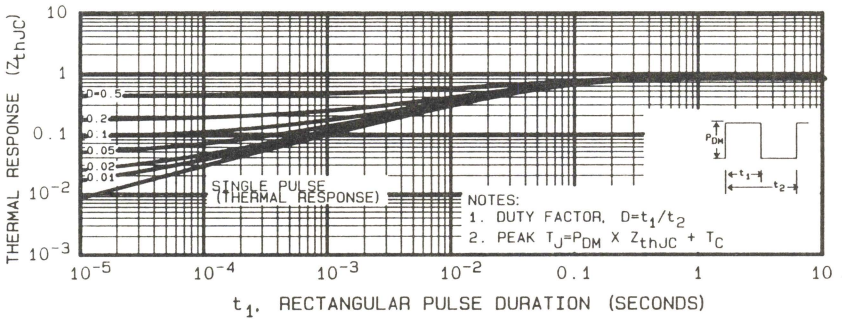


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

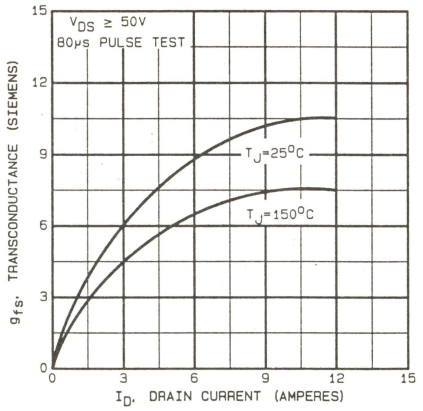


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

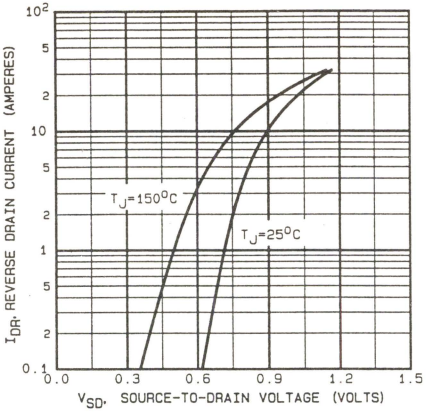


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

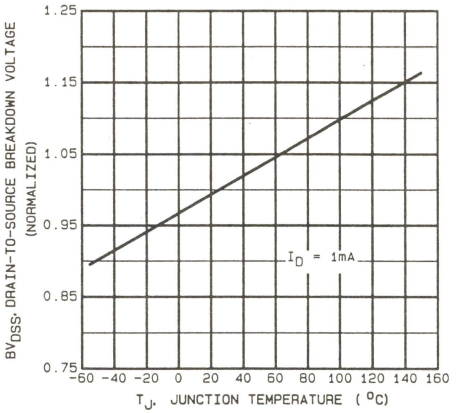


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

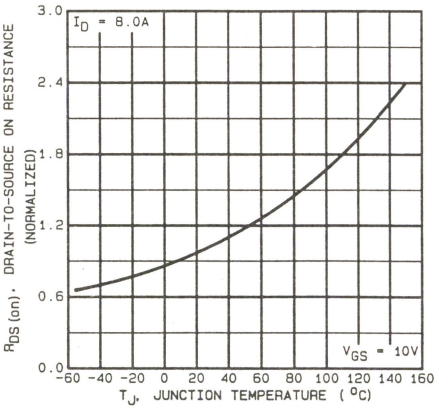


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

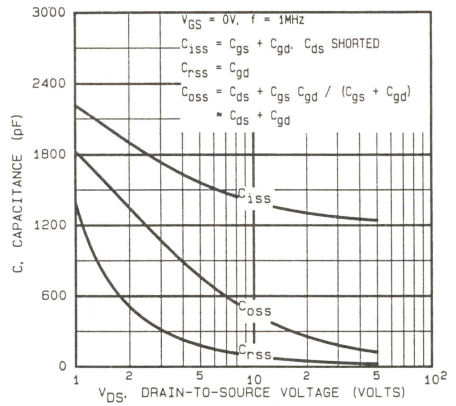


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

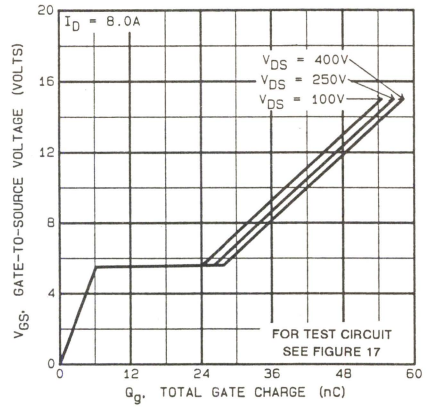


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

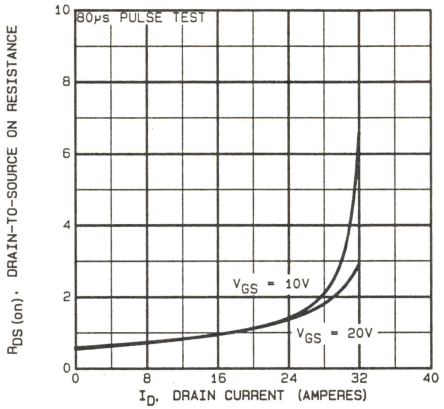


FIGURE 12. TYPICAL ON-RESISTANCE VS DRAIN CURRENT

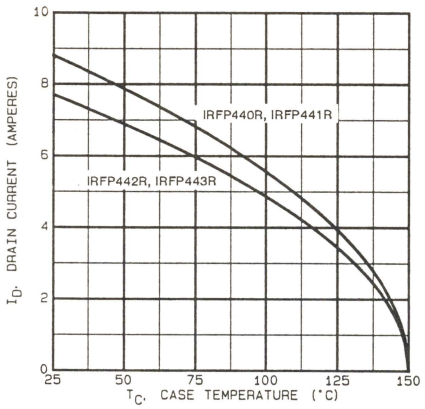


FIGURE 13. MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

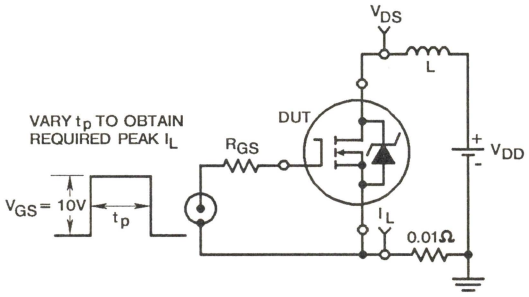


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

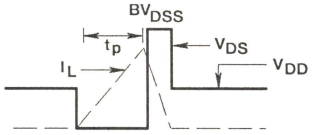


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

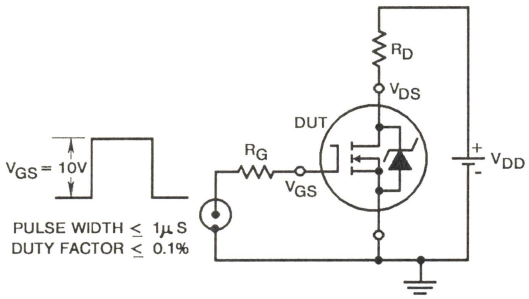


FIGURE 16. SWITCHING TIME TEST CIRCUIT

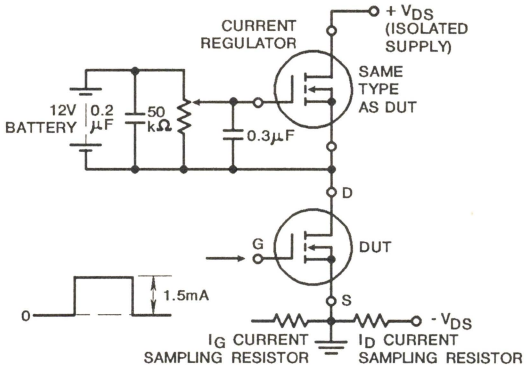


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP450/451/452/453
IRFP450R/451R/452R/453R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 12A and 14A, 450V - 500V
- $r_{DS}(on)$ = 0.4Ω and 0.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

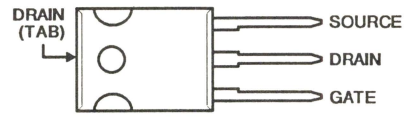
Description

The IRFP450, IRFP451, IRFP452, and IRFP453 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP450R, IRFP451R, IRFP452R and IRFP453R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

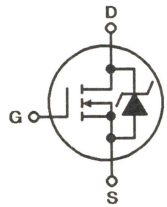
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP450 IRFP450R	IRFP451 IRFP451R	IRFP452 IRFP452R	IRFP453 IRFP453R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	14	12	12	A
T_C = +100°C ..... I_D	8.8	8.8	7.9	7.9	A
Pulsed Drain Current (3) ..... I_{DM}	56	56	48	48	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	52	52	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	860	860	860	860	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 7.9mH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figure 15.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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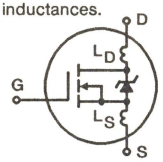
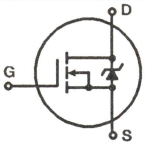
File Number **2331.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP450/452, IRFP450R/452R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	–	–	V
IRFP451/453, IRFP451R/453R			450	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	µA
On-State Drain Current (Note 2) IRFP450/451, IRFP450R/451R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\ Max}$, V_{GS} = 10V	14	–	–	A
IRFP452/453, IRFP452R/453R			12	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFP450/451, IRFP450R/451R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 7.9A	–	0.3	0.4	Ω
IRFP452/453, IRFP452R/453R			–	0.4	0.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 7.9A	9.3	13.8	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	2000	–	pF
Output Capacitance	C_{OSS}		–	400	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	100	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 14A, R_G = 6.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	–	16	27	ns
Rise Time	t_r		–	45	66	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	68	100	ns
Fall Time	t_f		–	41	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	82	130	nC
Gate-Source Charge	Q_{gs}		–	12	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	42	–	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	–	–	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 13A, dI_F/dt = 100A/µs	–	1300	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 13A, dI_F/dt = 100A/µs	–	7.4	–	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 7.9mH, R_{GS} = 25Ω, I_{PEAK} = 14A (See Figure 15)

Performance Curves

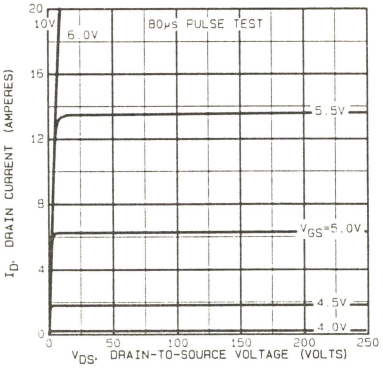


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

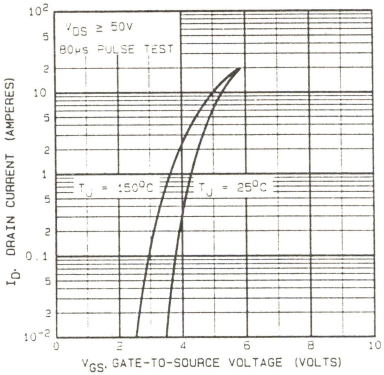


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

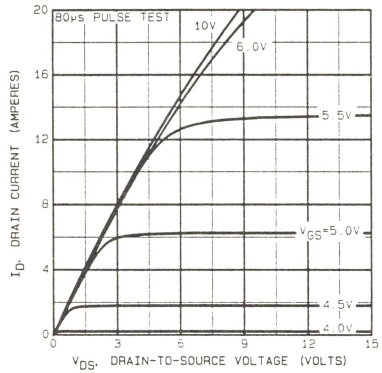


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

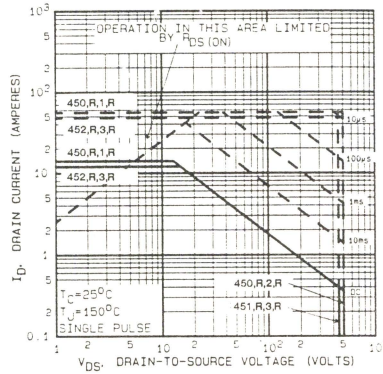


FIGURE 4. MAXIMUM SAFE OPERATING AREA

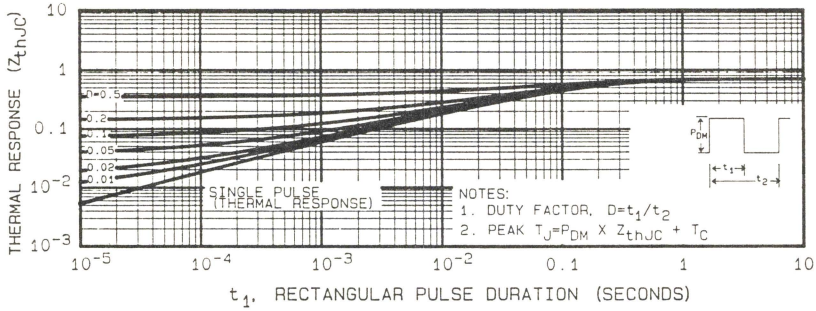


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

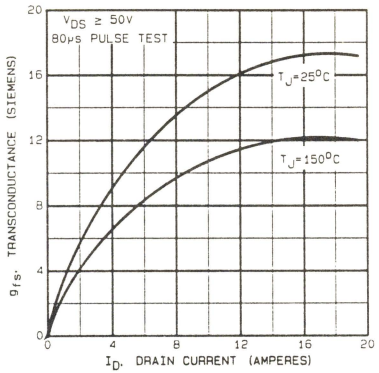


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

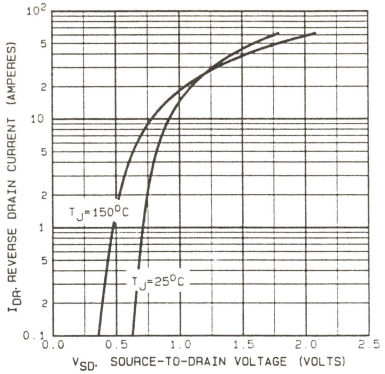


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

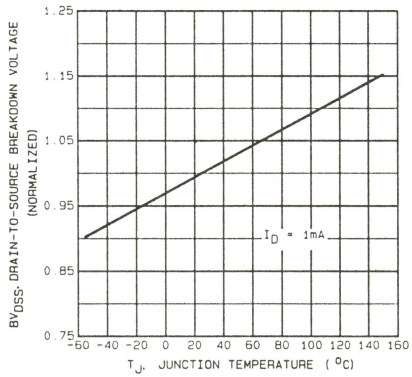


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

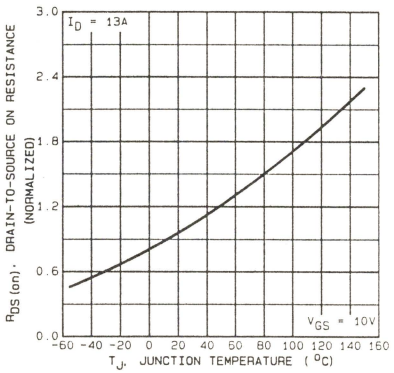


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

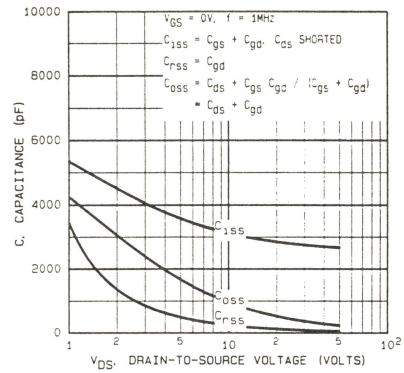


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

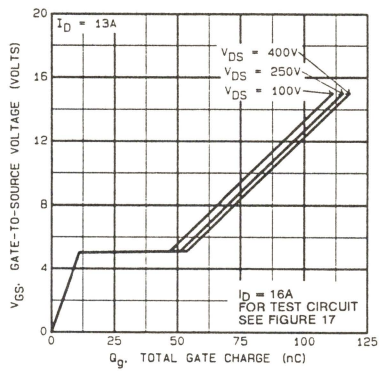


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

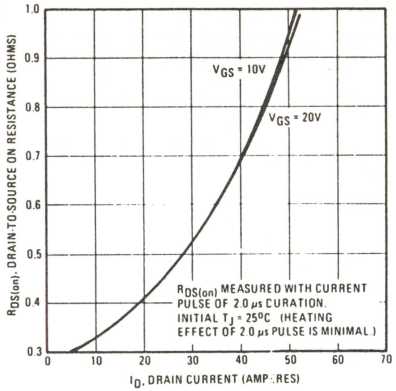


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

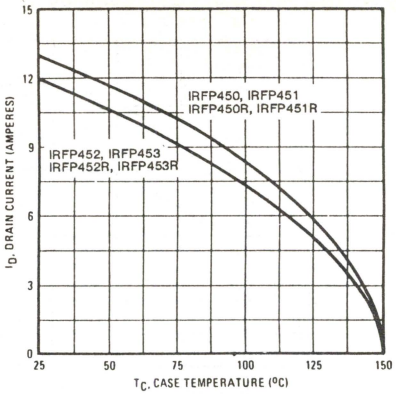


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

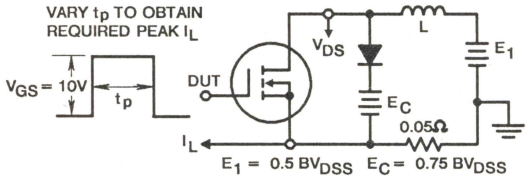


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

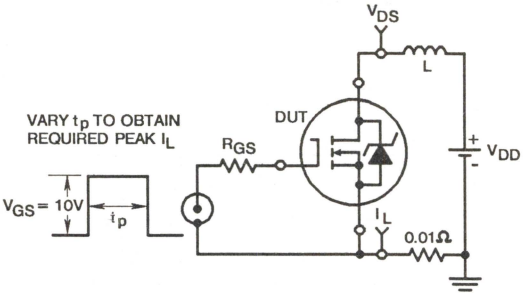


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

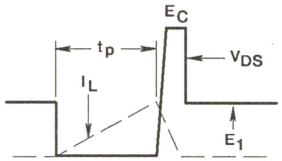


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

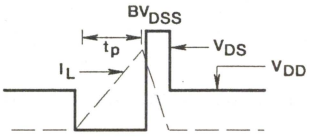


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

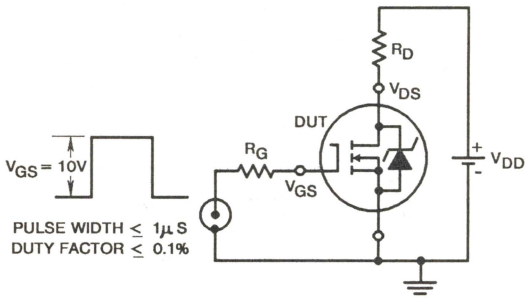


FIGURE 16. SWITCHING TIME TEST CIRCUIT

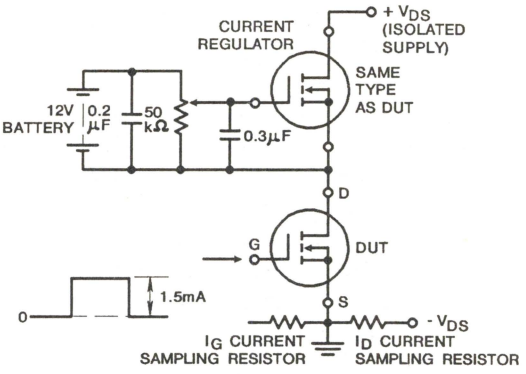


FIGURE 17. GATE CHARGE TEST CIRCUIT

HARRIS

IRFP460
IRFP462

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 20A and 17A, 500V
- $r_{DS}(on)$ = 0.27Ω and 0.35Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

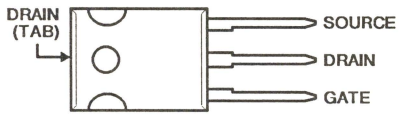
Description

The IRFP460 and IRFP462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

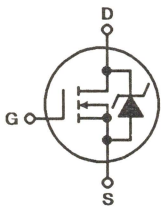
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP460	IRFP462	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	20	17	A
T_C = +100°C	I_D	12	11	A
Pulsed Drain Current (1)	I_{DM}	80	68	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	250	250	W
Linear Derating Factor		2.0	2.0	W/°C
Single Pulse Avalanche Energy Rating (2) See Figure 14	E_{AS}	960	960	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.3mH, R_{GS} = 25Ω, Peak I_L = 20A. See Fig. 14.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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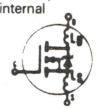
File Number **2291.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25°C Unless Otherwise Specified*

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFP460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 11A
		IRFP462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRFP460	20	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max. V_{GS} = 10V
		IRFP462	17				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	13	19	–	S (℧)	V_{DS} = ≥ 50V, I_{DS} = 11A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = −20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gs}	Gate-to-Source Charge	ALL	–	18	—	nC	
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	—	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D ≈ 21A, R_G = 4.3Ω
t_r	Rise Time	ALL	–	81	120	ns	R_D = 12Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	See Fig. 15
t_f	Fall Time	ALL	–	65	98	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	–	480	–	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	–	–	0.50	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.10	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free air operation
	Mounting Torque	ALL	–	–	10	in. • lbs	Standard 6-32 screw

Modified MOSFET symbol showing the internal inductances



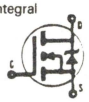
① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.3 mH, R_G = 25Ω, Peak I_L = 20A. See Fig. 14.

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	–	–	20	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	80	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D				



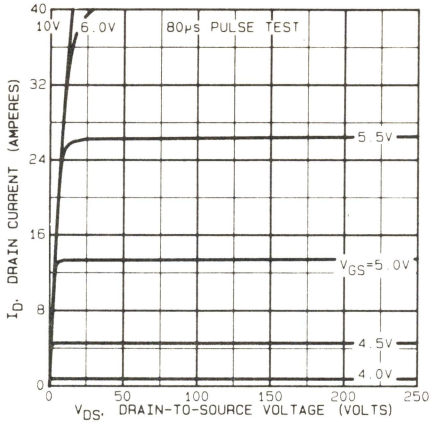


Fig. 1 - Typical output characteristics.

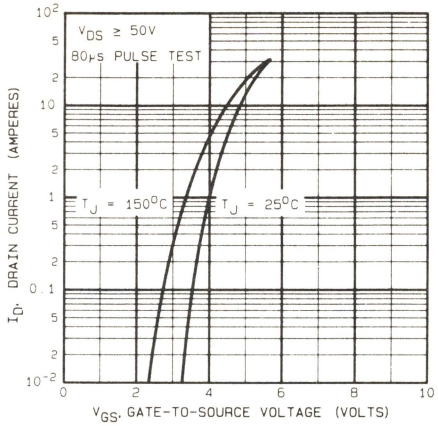


Fig. 2 - Typical transfer characteristics.

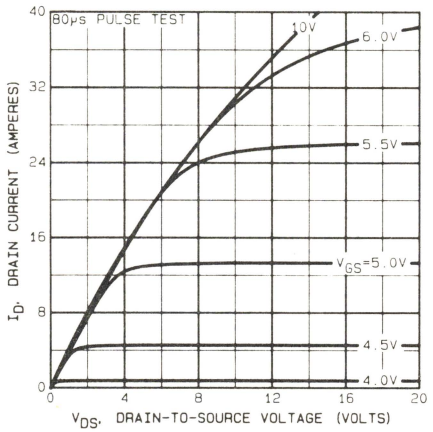


Fig. 3 - Typical saturation characteristics.

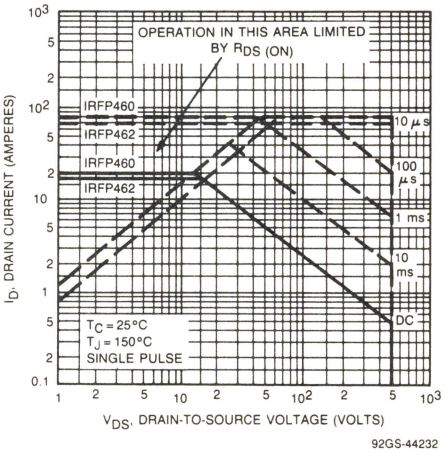


Fig. 4 - Maximum safe operating area.

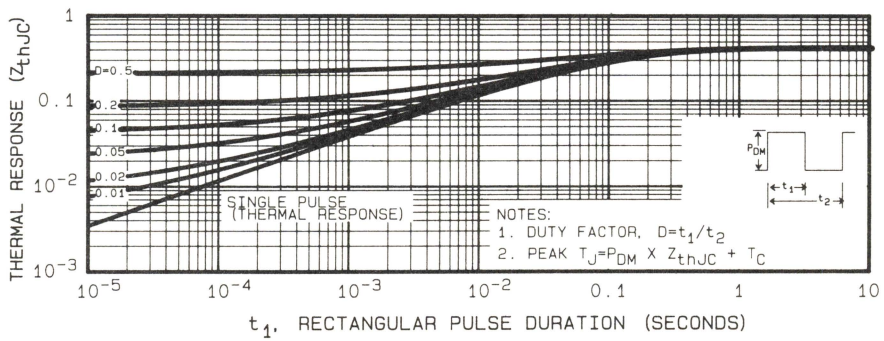


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

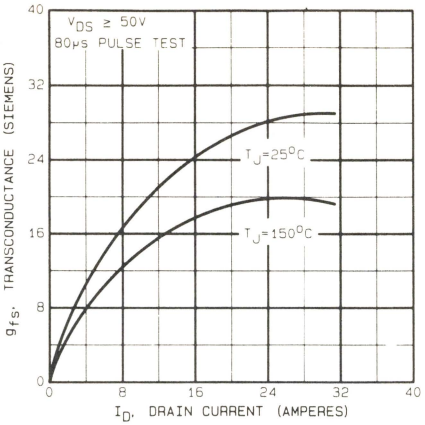


Fig. 6 - Typical transconductance vs. drain current.

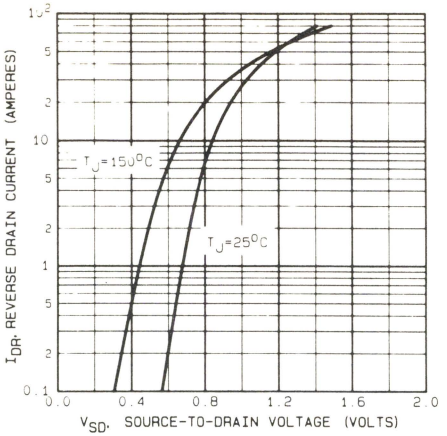


Fig. 7 - Typical source-drain diode forward voltage.

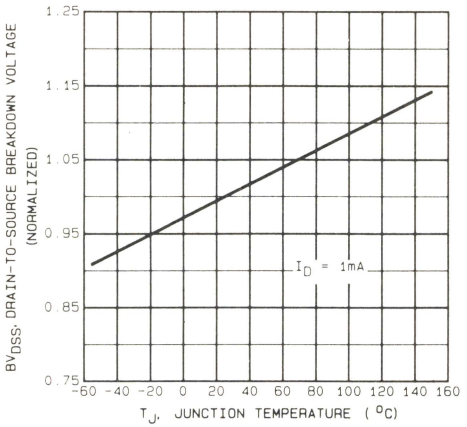


Fig. 8 - Breakdown voltage vs. temperature.

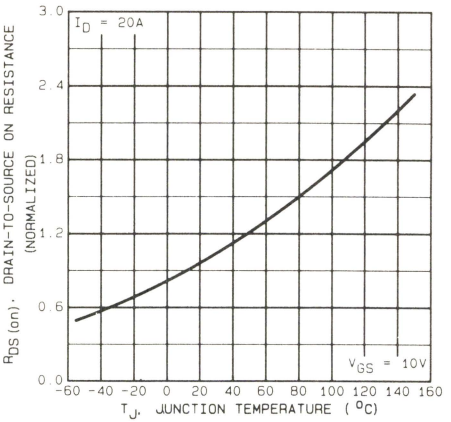


Fig. 9 - Normalized on-resistance vs. temperature.

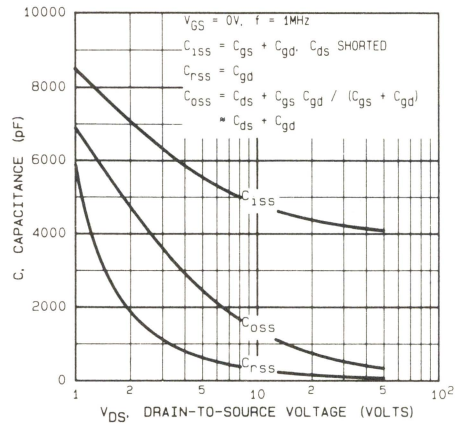


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

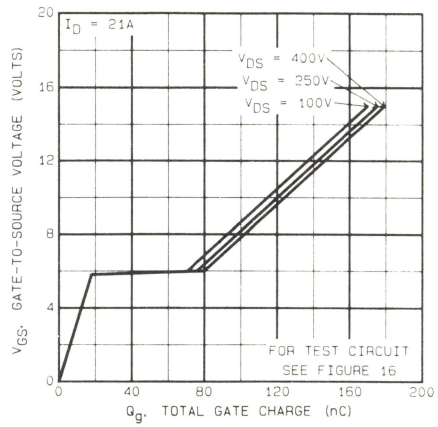


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

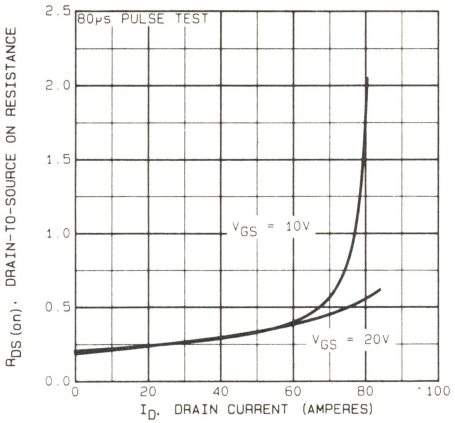


Fig. 12 - Typical on-resistance vs. drain current.

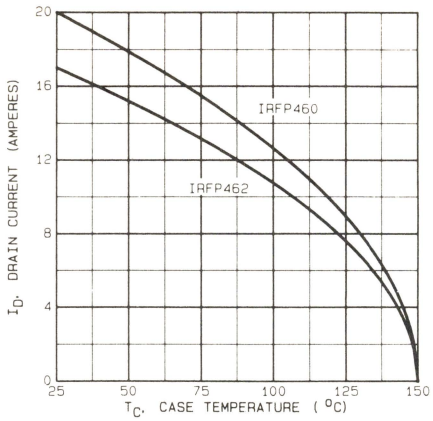


Fig. 13 - Maximum drain current vs. case temperature.

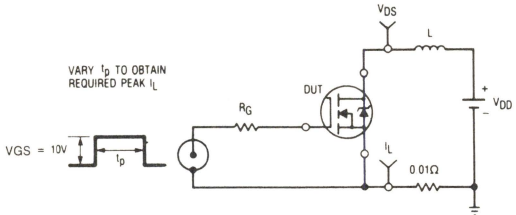


Fig. 14a - Unclamped inductive test circuit.

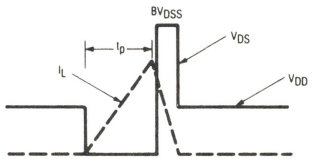


Fig. 14b - Unclamped inductive waveforms.

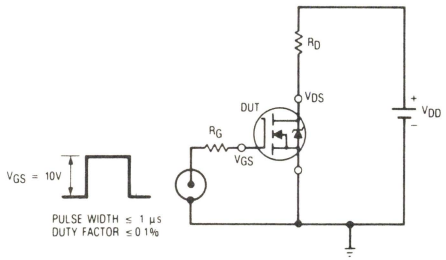


Fig. 15a - Switching time test circuit.

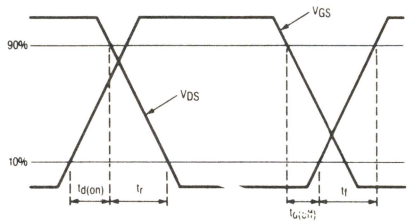


Fig. 15b - Switching time waveforms.

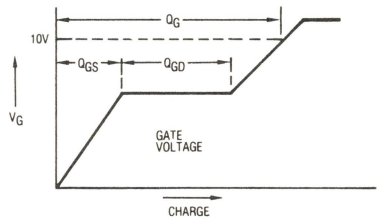


Fig. 16a - Basic gate charge waveform.

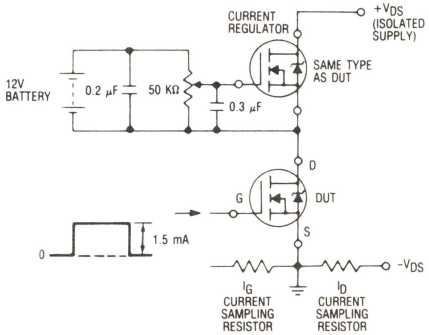


Fig. 16b - Gate charge test circuit.

HARRIS

IRFPC40R
IRFPC42R

N-Channel Power MOSFETs
Avalanche-Energy-Rated

May 1992

Features

- 6.8A, 5.9A and 600V
- $r_{DS(ON)}$ = 1.2Ω and 1.6Ω
- Isolated Central Mounting Hole
- Repetitive Avalanche Ratings
- Simple Drive Requirements
- Ease of Paralleling

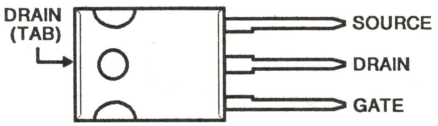
Description

The IRFPC40R and IRFPC42R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFPC types are supplied in the JEDEC TO-247 plastic package.

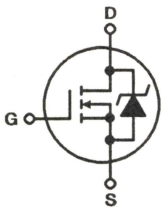
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFPC40R	IRFPC42R	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	6.8	5.9	A
T_C = +100°C	I_D	4.3	3.7	A
Pulsed Drain Current (2)	I_{DM}	27	24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	410	410	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 50V, Start T_J = +25°C, L = 16mH, R_G = 25Ω, Peak I_L = 6.8A

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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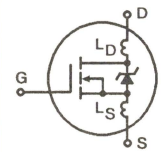
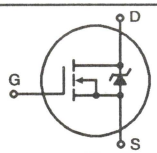
File Number **2158.1**

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	600	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	–	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	–	–	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	–	–	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	–	–	1000	μA
On-State Drain Current (Note 1) IRFPC40R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	6.8	–	–	A
IRFPC42R			5.9	–	–	A
Static Drain-Source On-State Resistance (Note 1) IRFPC40R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 3.7A	–	0.97	1.2	Ω
IRFPC42R			–	1.2	1.6	Ω
Forward Transconductance (Note 1)	g_{fs}	I_{DS} = 3.7A, V_{DS} ≥ 100V	4.9	7.3	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	–	1300	–	pF
Output Capacitance	C_{OSS}		–	160	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	45	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 200V, I_D = 6.2A, R_G = 9.1Ω R_D = 47Ω. (Independent of operating temperature) See Figure 15.	–	13	20	ns
Rise Time	t_r		–	18	27	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	55	83	ns
Fall Time	t_f		–	20	30	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 6.2A, V_{DS} = 0.6V x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	40	60	nC
Gate-Source Charge	Q_{gs}		–	5.5	8.3	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	20	30	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal inductances. 	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad.	–	12.5	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	–	0.10	–	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	–	–	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	6.8	A
Pulse Source Current (Body Diode) (Note 1)	I_{SM}		–	–	27	A
Diode Forward Voltage (Note 3)	V_{SD}	T_J = +25°C, I_S = 6.2A, V_{GS} = 0V	–	–	1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 6.2A, dI_F/dt = 100A/μs	200	450	940	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 6.2A, dI_F/dt = 100A/μs	1.8	3.8	7.9	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 50V, Start T_J = +25°C, L = 16mH, R_{GS} = 25Ω, I_{PEAK} = 6.8A

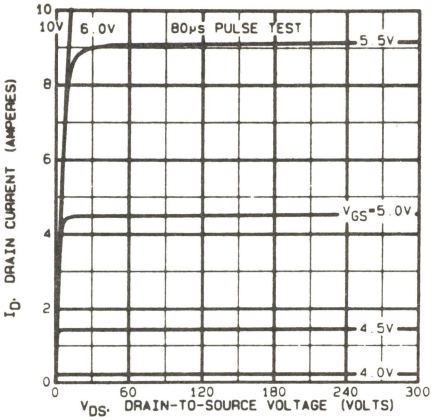


Fig. 1 - Typical Output Characteristics

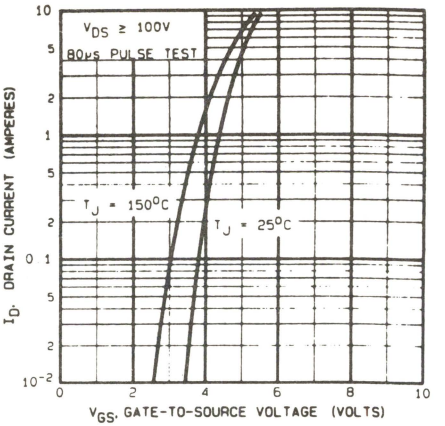


Fig. 2 - Typical Transfer Characteristics

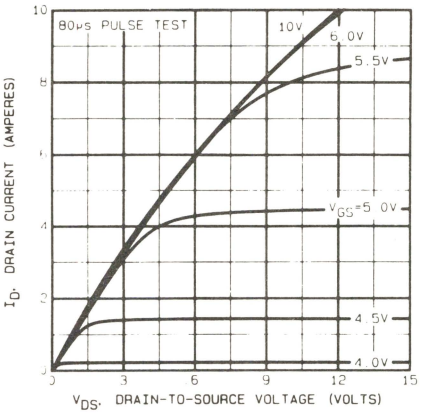


Fig. 3 - Typical Saturation Characteristics

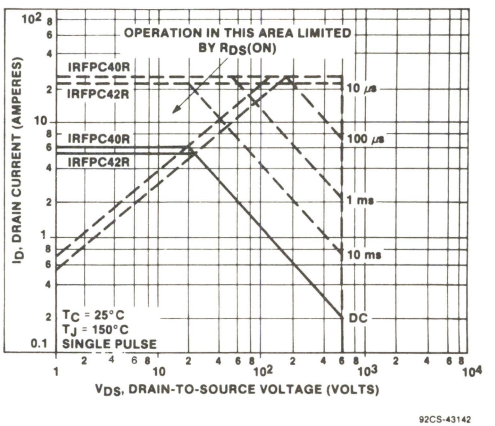


Fig. 4 - Maximum Safe Operating Area

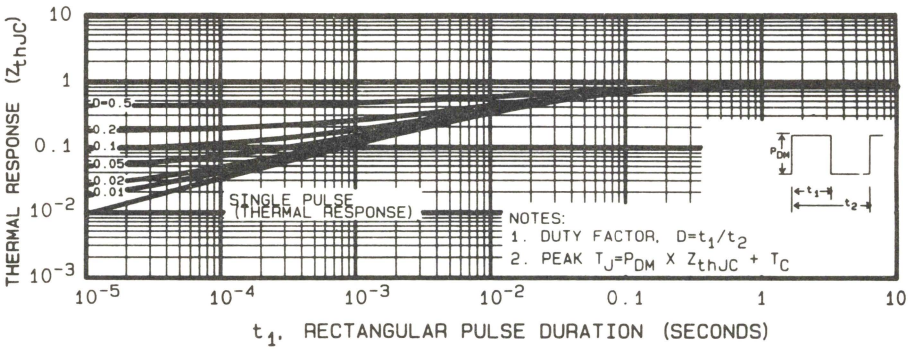


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

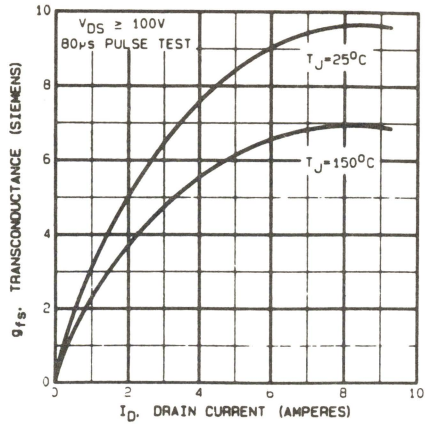


Fig. 6 - Typical Transconductance Vs. Drain Current

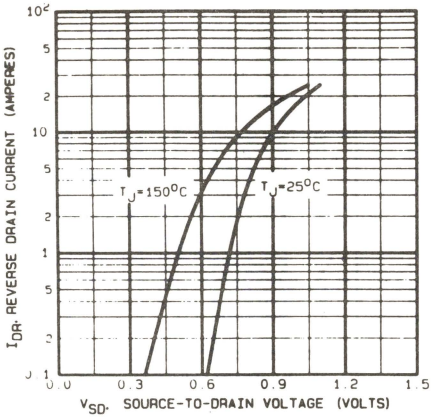


Fig. 7 - Typical Source-Drain Diode Forward Voltage

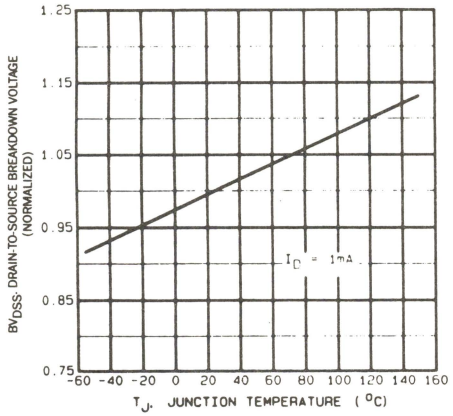


Fig. 8 - Breakdown Voltage Vs. Temperature

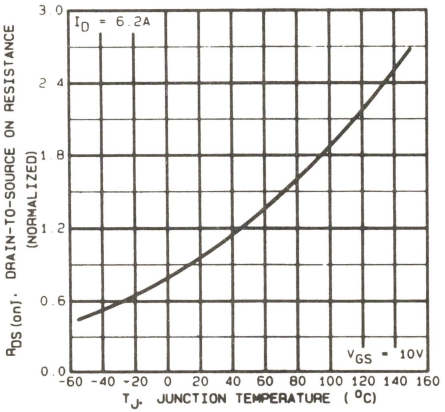


Fig. 9 - Normalized On-Resistance Vs. Temperature

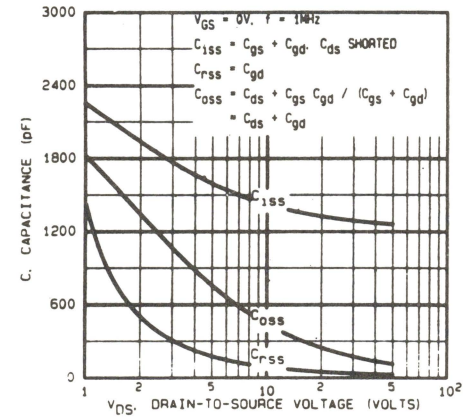


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

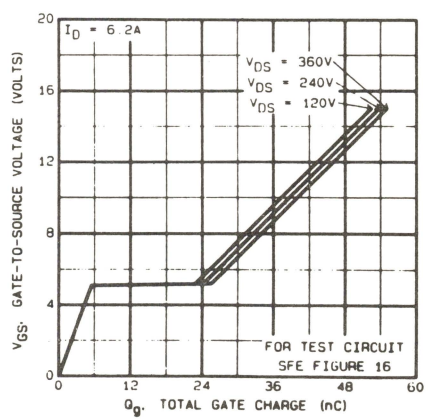


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

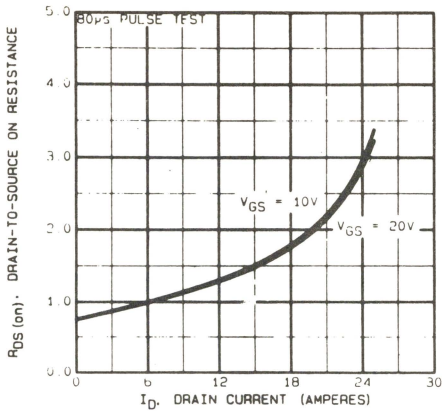


Fig. 12 - Typical On-Resistance Vs. Drain Current

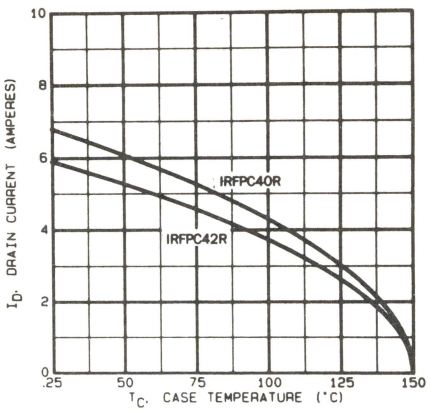


Fig. 13 - Maximum Drain Current Vs. Case Temperature

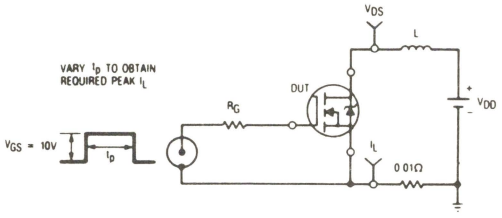


Fig. 14a - Unclamped Inductive Test Circuit

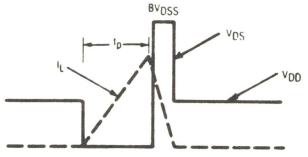


Fig. 14b - Unclamped Inductive Waveforms

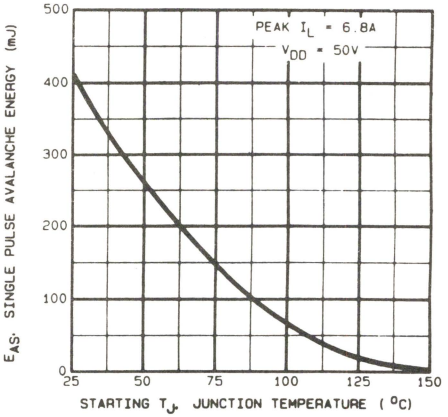


Fig. 14c - Maximum Avalanche Energy Vs. Starting Junction Temperature

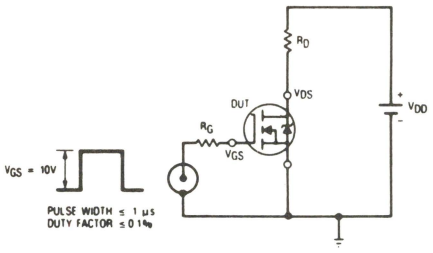


Fig. 15a - Switching Time Test Circuit

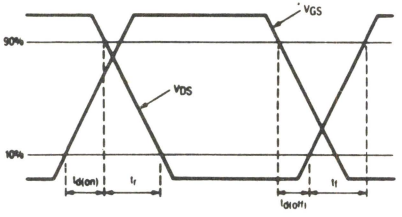


Fig. 15b - Switching Time Waveforms

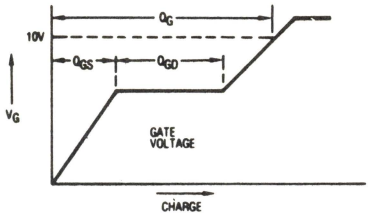
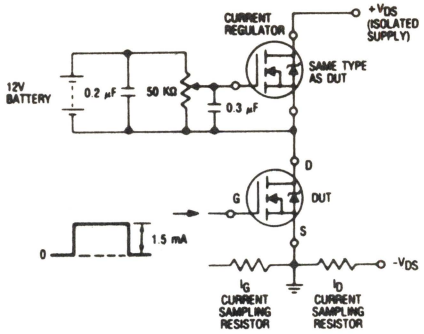


Fig. 16a - Basic Gate Charge Waveform



Fib. 16b - Gate Charge Test Circuit

HARRIS

IRFPG40
IRFPG42

High Voltage N-Channel Enhancement Mode Power Field Effect Transistor

August 1991

Features

- IRFPG40: 4.3A, 1000V, $r_{DS(ON)} = 3.5\Omega$
- IRFPG42: 3.9A, 1000V, $r_{DS(ON)} = 4.2\Omega$
- UIS SOA Rating Curve (Single Pulse)
- -55°C to 150°C Operating and Storage Temperature

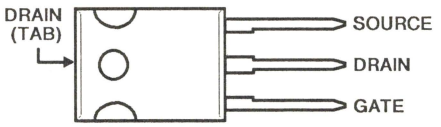
Description

The IRFPG40 and IRFPG42 are n-channel enhancement mode silicon-gate power field effect transistors. They are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFPG40 and IRFPG42 are supplied in the JEDEC TO-247 plastic package.

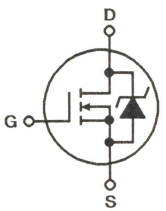
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFPG40	IRFPG42	UNITS
Drain-Souce	V_{DSS}	1000	1000	V
Drain-Gate	V_{DGR}	1000	1000	V
Continuous Drain Current	I_D	4.3	3.9	A
Pulsed Drain Current	I_{DM}	17	16	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = 25°C	P_D	150	150	W
Derate Above T_C = 25°C		0.83	0.83	W/°C
Single Pulse Avalanche Energy Rating (See Figure 13)	E_{as}	490	490	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2879**

Electrical Characteristics (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	1000	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA	2.0	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V	–		µA
		V_{DS} = 1000V T_C = 25°C	–	250	µA
		V_{DS} = 800V T_C = 150°C	–	1000	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	–	±500	nA
On Resistance	$r_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V			
IRFPG40			–	3.5	Ω
IRFPG42			–	4.2	Ω
Forward Transconductance	g_{fs}	I_D = 2.5A, V_{DS} = 100V	3.5	–	s
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 500V, I = 3.9A	–	30	ns
Rise Time	t_r	R_G = 9.1Ω	–	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$	R_D = 120Ω	–	170	ns
Fall Time	t_f	See Figure 14	–	50	ns
Total Gate Charge	Q_g	I_D = 3.9A, V_{DS} = 800V, V_{GS} = 10V	–	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		–	0.83	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		–	40	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 4.3A	–	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 3.9A, d_{IF}/dT = 100 A/µs	–	1000	ns

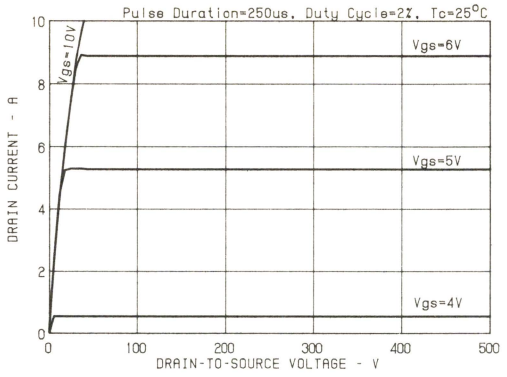


Figure 1 – Typical output characteristics.

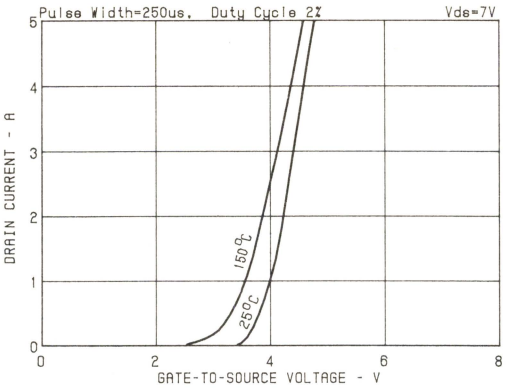


Figure 2 – Typical transfer characteristics.

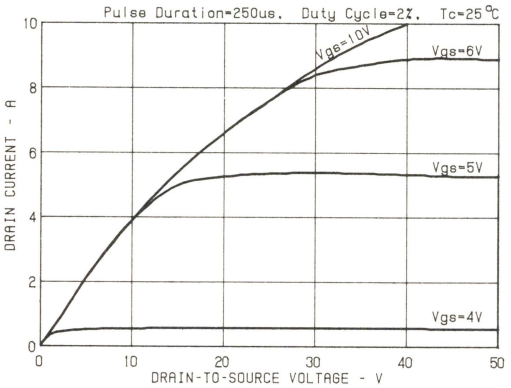


Figure 3 – Typical saturation characteristics.

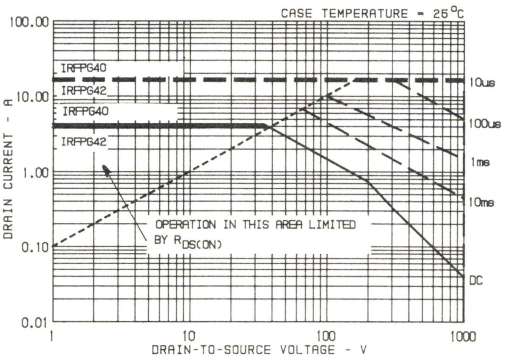


Figure 4 – Maximum safe operating area.

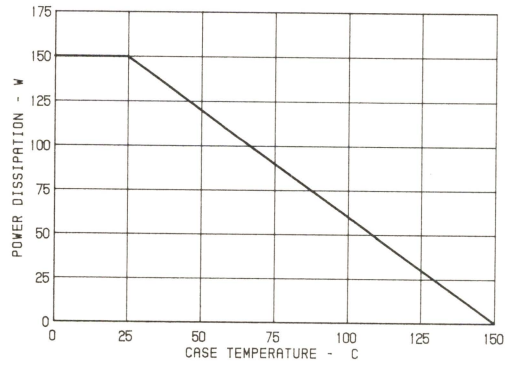


Figure 5 – Power vs. temperature derating curve.

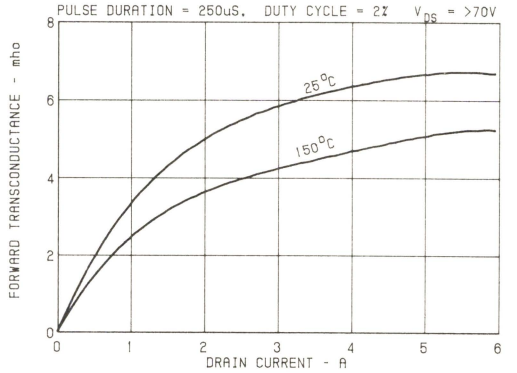


Figure 6 – Typical forward transconductance.

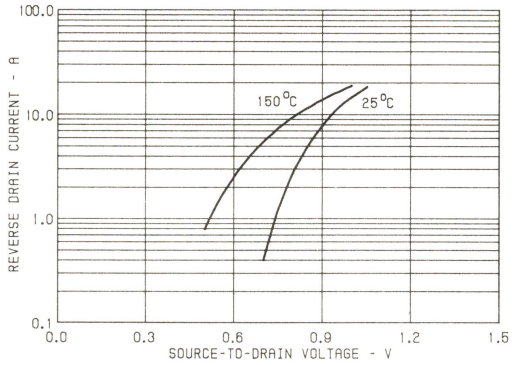


Figure 7 – Typical source-to-drain diode forward voltage.

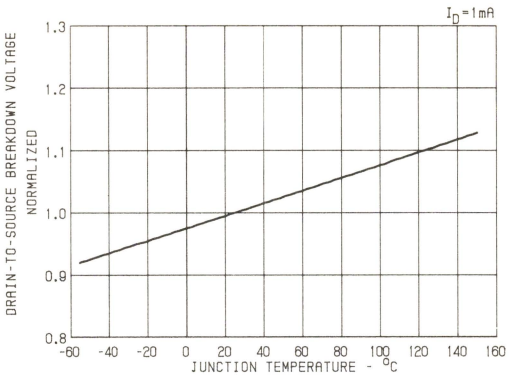


Figure 8 – Breakdown voltage vs. temperature.

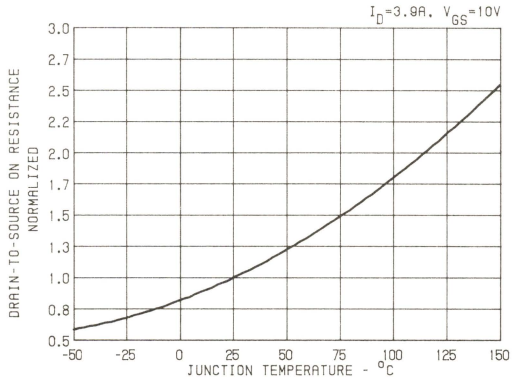


Figure 9 – Normalized drain-to-source on resistance.

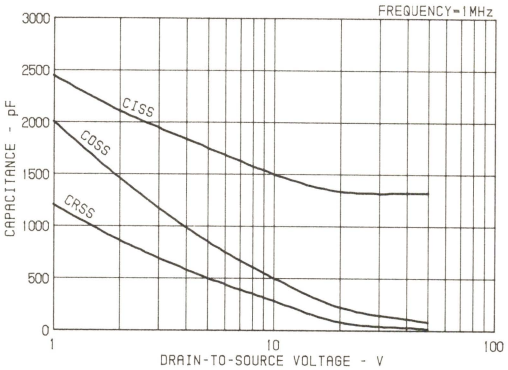


Figure 10 – Typical capacitance vs. voltage.

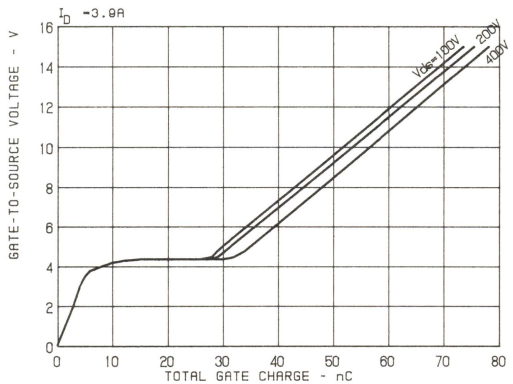


Figure 11 – Typical gate charge.

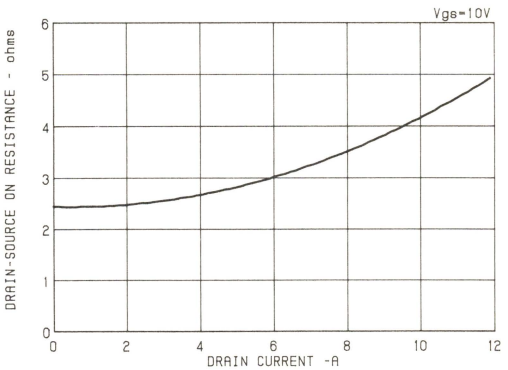


Figure 12 – Typical drain-source on resistance.

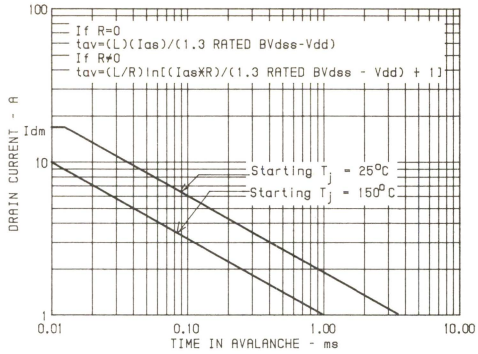


Figure 13 – Unclamped inductive switching SOA.

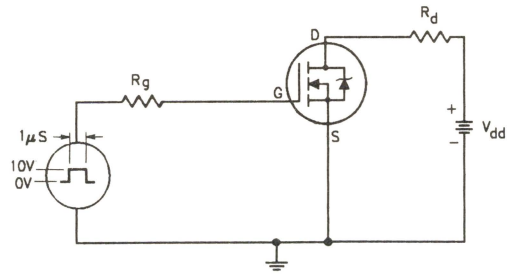


Figure 14 – Switching time test circuit.

IRFR110
IRFU110

N-Channel Power MOSFETs
Avalanche Energy Rated

January 1994

Features

- 4.7A, 100V
- $r_{DS(ON)} = 0.54\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

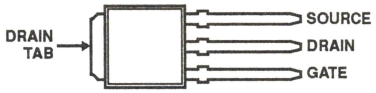
Description

The IRFR110 and IRFU110 are n-channel enhancement-mode silicon-gate power field-effect transistors designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

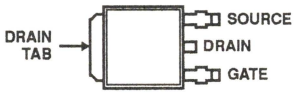
The IRFU110 is supplied in the JEDEC TO-251AA plastic package and the IRFR110 in the JEDEC TO-252AA plastic package.

Packages

JEDEC TO-251AA
TOP VIEW



JEDEC TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings ($T_C = +25°C$), Unless Otherwise Specified

		IRFR110, IRFU110	UNITS
Drain-Source Voltage (1)	V_{DS}	100	V
Drain-Gate Voltage	V_{DGR}	100	V
Continuous Drain Current			
$T_C = +25°C$	I_D	4.7	A
$T_C = +100°C$	I_D	3.3	A
Pulsed Drain Current (2)	I_{DM}	17	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	30	W
Linear Derating Factor		0.2	W/°C
Single Pulse Avalanche Rating (3) (See Fig. 14)	E_{as}	19	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

1. $T_J = +25°C$ to $+150°C$.
2. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Figure 5)
3. $V_{DD} = 25V$, Starting $T_J = +25°C$, $L = 1.3mH$, $R_G = 25\Omega$, Peak $I_L = 4.7A$.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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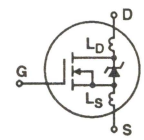
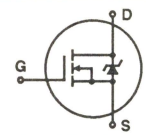
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	-	-	250	μA
		V_{DS} = 80V, V_{GS} = 0V, T_J = +150°C	-	-	1000	μA
On-State Drain Current	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)Max}$, V_{GS} = 10V	4.7	-	-	A
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 3.3A, V_{GS} = 10V	-	0.41	0.54	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = ≥ 50V, I_{DS} = 3.3A	1.3	2.0	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	180	-	pF
Output Capacitance	C_{OSS}		-	82	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	15	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 5.6A, R_G = 24Ω, R_D = 9.1Ω, See Figure 15 (MOSFET switching times are essentially independent of operating temperature)	-	7.6	11	ns
Rise Time	t_r		-	24	36	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	14	21	ns
Fall Time	t_f		-	14	21	ns
Total Gate Charge	Q_g	V_{GS} = 10V, I_D = 5.6A, V_{DS} = 0.8 x Max Rating. See Figure 16 (Gate charge is essentially independent of operating temperature)	-	5.2	7.7	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	2.2	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad. 	-	7.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	5.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.7	-	°C/W
Junction to Ambient	$R_{\theta JA}$	Free air operation	-	-	110	°C/W

Source-Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	-	-	4.7	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}		-	-	17	A
Diode Forward Voltage (Note 1)	V_{SD}	T_J = +25°C, I_S = 4.7A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_S = 5.6A, dI_F/dt = 100A/μs	46	96	200	ns
Reverse Recovery Charge	Q_{RR}	T_J = +25°C, I_S = 5.6A, dI_F/dt = 100A/μs	0.17	0.38	0.83	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

NOTES: 1. Pulse Test: Pulse width ≤ 300μs. Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5).

Performance Curves

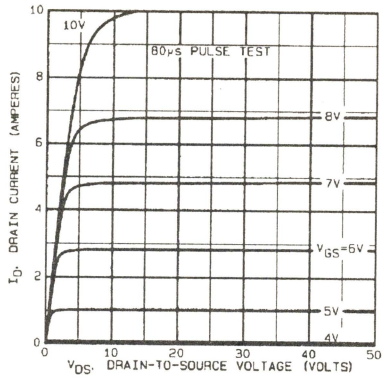


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

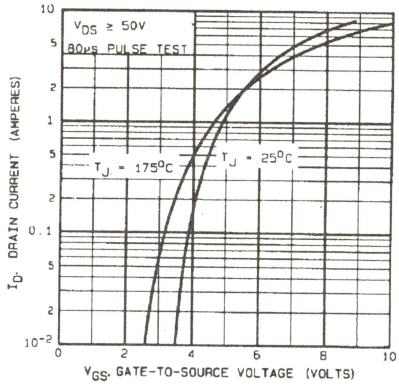


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

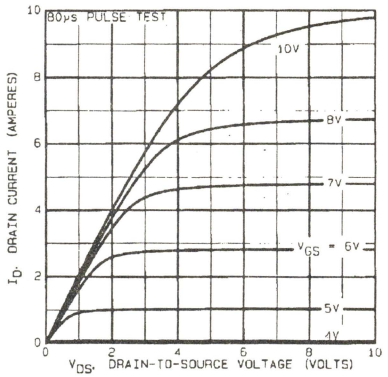


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

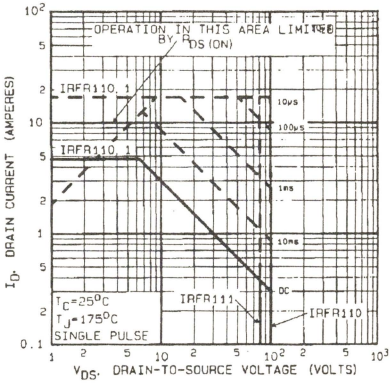


FIGURE 4. MAXIMUM SAFE OPERATING AREA

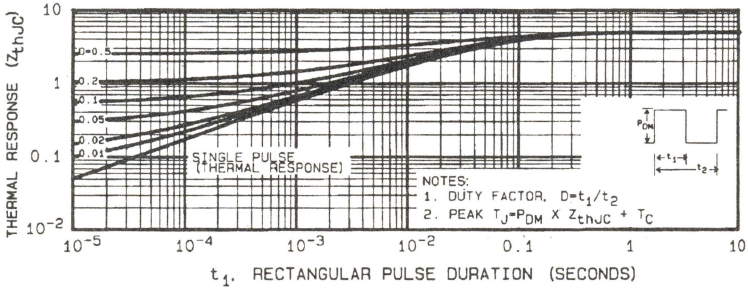


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

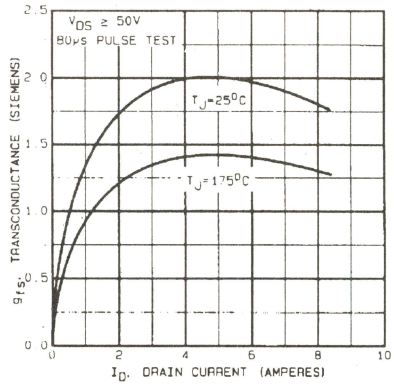


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

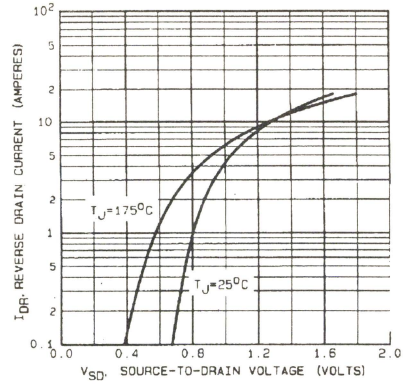


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

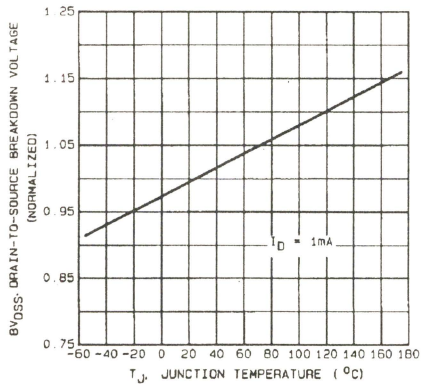


FIGURE 8 BREAKDOWN vs TEMPERATURE

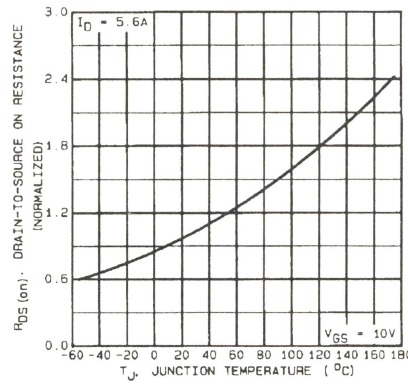


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

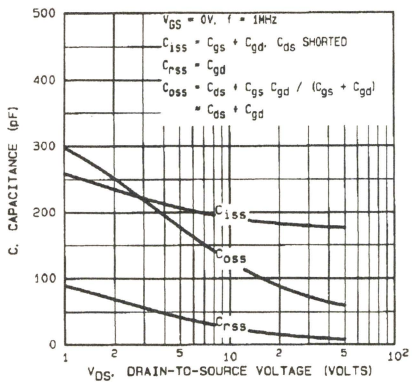


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

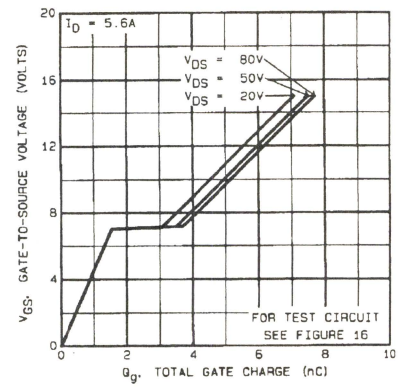


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

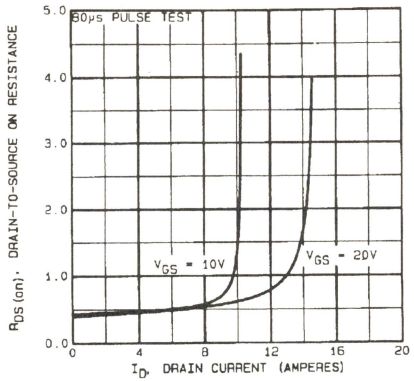


FIGURE 12. TYPICAL ON-RESISTANCE vs DRAIN CURRENT

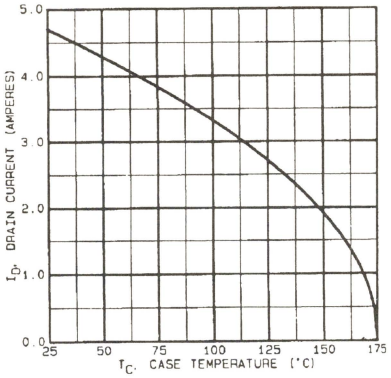


FIGURE 13. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

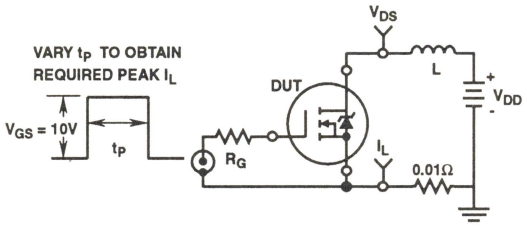


FIGURE 14a. UNCLAMPED INDUCTIVE TEST CIRCUIT

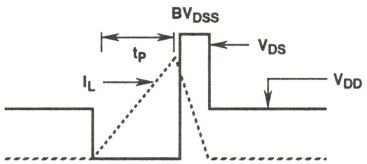


FIGURE 14b. UNCLAMPED INDUCTIVE WAVEFORMS

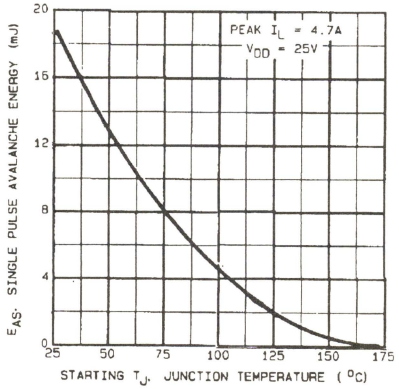


FIGURE 14c. MAXIMUM AVALANCHE vs STARTING JUNCTION TEMPERATURE

Performance Curves (Continued)

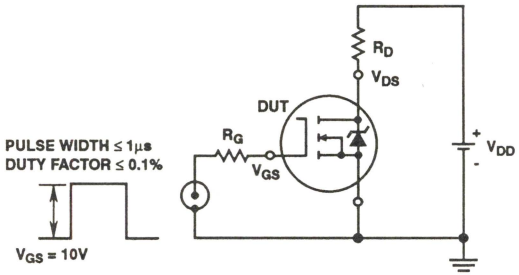


FIGURE 15a. SWITCHING TIME TEST CIRCUIT

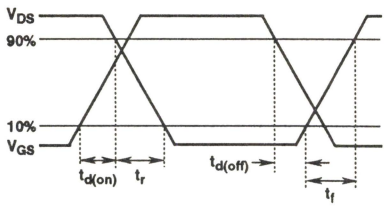


FIGURE 15b. SWITCHING TIME WAVEFORMS

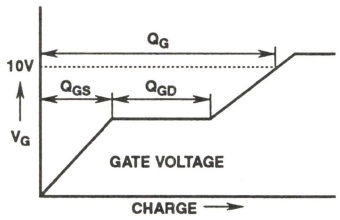


FIGURE 16a. BASIC GATE CHARGE WAVEFORMS

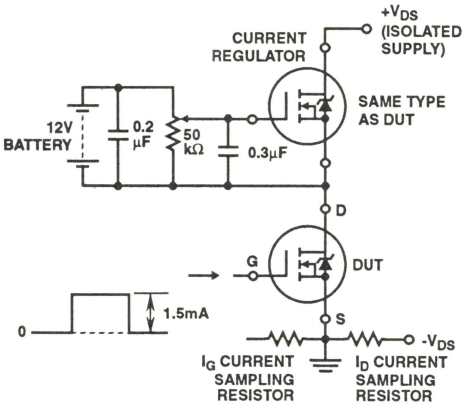


FIGURE 16. GATE CHARGE TEST CIRCUIT

HARRIS

IRFR120/IRFR121
IRFU120/IRFU121

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 8.4A, 80V and 100V
- $r_{DS(on)} = 0.27\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

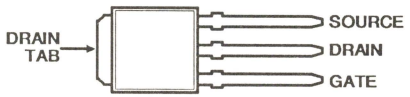
The IRFR120, IRFR121, IRFU120, IRFU121 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

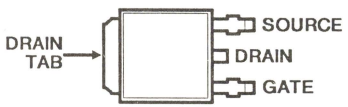
Because of space limitations branding (marking) on type IRFR120 is IRF120, IRFR121 is IFR121, IRFU120 is IFU120 and IRFU121 is IFU121.

Packages

TO-251AA
TOP VIEW

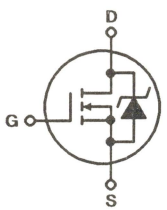


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

Gate-Source Voltage, V_{GS}	±20V
Continuous Drain Current, I_D	
$T_C = 25^oC$	8.4A
$T_C = 100^oC$	5.9A
Pulsed Drain Current (1), I_{DM}	34A
Single-Pulse Avalanche Energy Rating (2), E_{AS} (See Figure 14)	36mJ
Maximum Power Dissipation, P_D	50W
Linear Derating Factor	0.4W/^{o}C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175^{o}C
Maximum Lead Temperature for Soldering, T_L (0.063" (1.6mm) from case for 10s)	300^{o}C

NOTES:

1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 25V, Start T_J = +25^{o}C, L = 770µH, R_G = 25Ω, Peak I_L = 8.4A (See Figures 14 and 15)
3. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
4. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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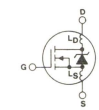
File Number **2414**

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

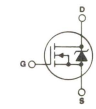
	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR120 IRFU120	100	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR121 IRFU121	80				
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ③	ALL	—	0.25	0.27	Ω	V_{GS} = 10 V, I_D = 5.9 A
$I_D(on)$	On-State Drain Current ③	ALL	8.4	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max. V_{GS} = 10 V
$V_{GS}(th)$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	2.8	4.2	—	S(℧)	$V_{DS} \geq 50$ V, I_{DS} = 5.9 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 150°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	9.7	15	nC	V_{GS} = 10 V, I_D = 8.4 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.2	3.3		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	2.3	3.4		See Fig. 16. (Independent of operating temperature)
$t_d(on)$	Turn-On Delay Time	ALL	—	8.8	13	ns	V_{DD} = 50 V, $I_D \approx$ 8.4 A, R_G = 18 Ω
t_r	Rise Time	ALL	—	30	45		R_D = 5.1 Ω
$t_d(off)$	Turn-Off Delay Time	ALL	—	19	29		See Fig. 15
t_f	Fall Time	ALL	—	20	30		(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	130	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	24	—		See Fig. 10

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	8.4	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	—	—	34		
V_{SD}	Diode Forward Voltage ③	ALL	—	—	2.5	V	T_J = 25°C, I_S = 8.4 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	55	110	240	ns	T_J = 25°C, I_F = 8.4 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.25	0.53	1.1	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	3.0	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ④
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see Fig. 5).

② At V_{DD} = 25 V, Starting T_J = 25°C, L = 770 μH, R_G = 25 Ω, Peak I_L = 8.4 A.

③ Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

④ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

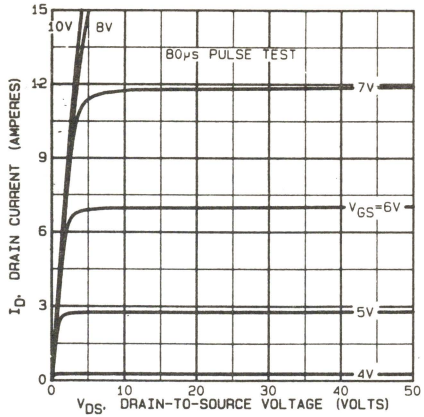


Fig. 1 - Typical output characteristics.

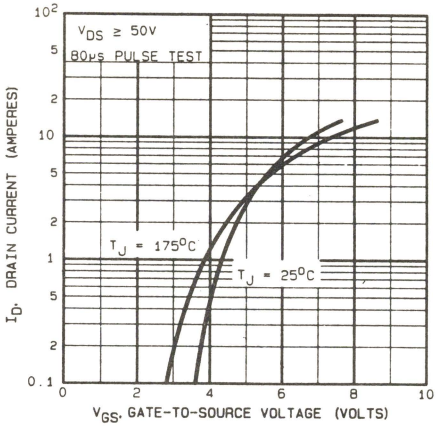


Fig. 2 - Typical transfer characteristics.

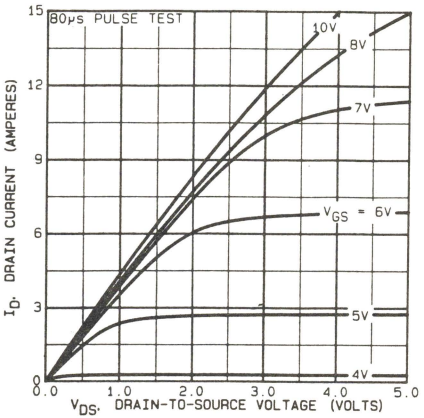


Fig. 3 - Typical saturation characteristics.

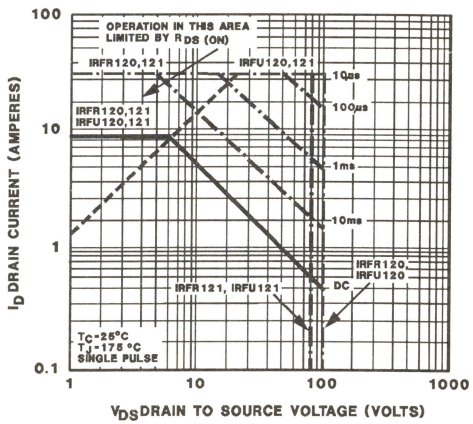


Fig. 4 - Maximum safe operating area.

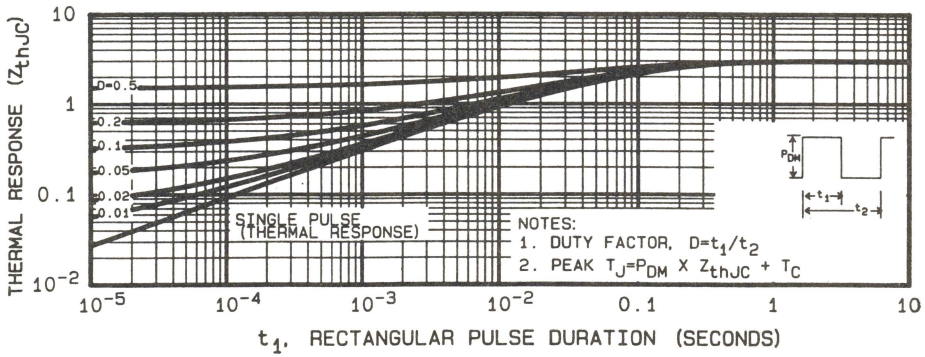


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

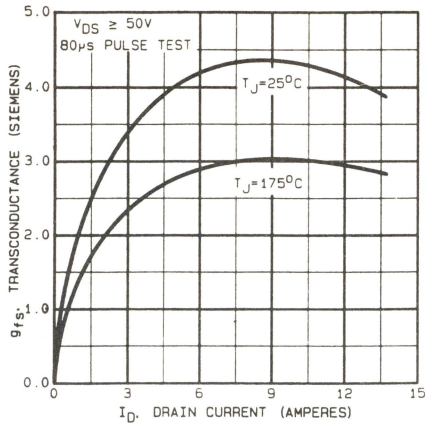


Fig. 6 - Typical transconductance vs. drain current.

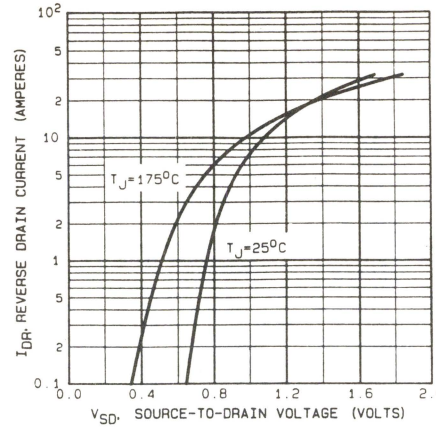


Fig. 7 - Typical source-drain diode forward voltage.

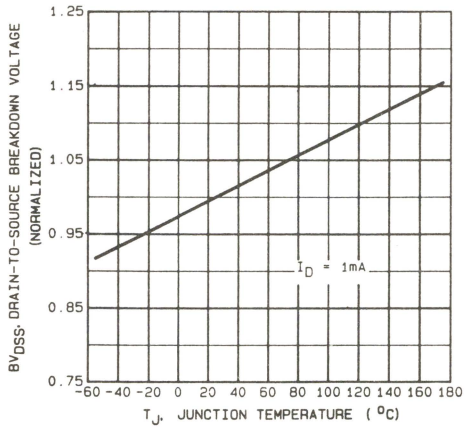


Fig. 8 - Breakdown voltage vs. temperature.

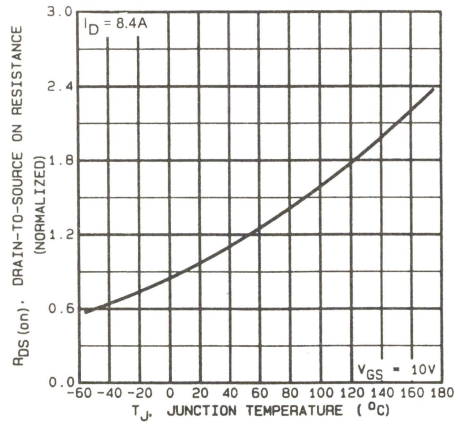


Fig. 9 - Normalized on-resistance vs. temperature.

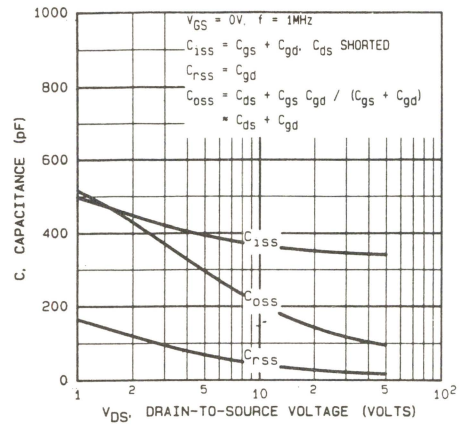


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

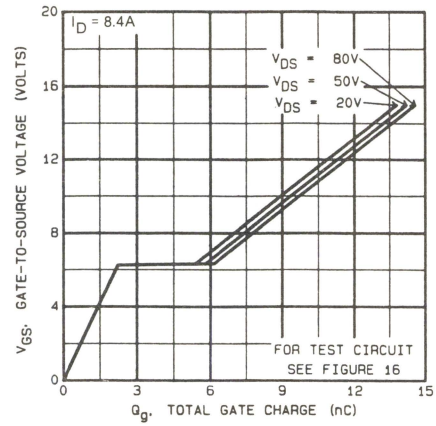


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

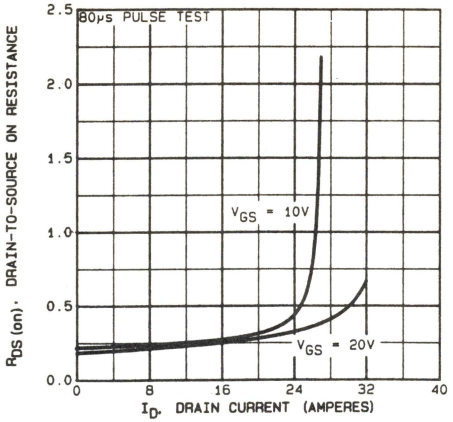


Fig. 12 — Typical on-resistance vs. drain current

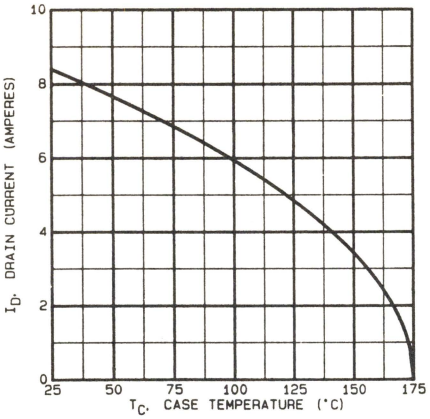


Fig. 13 — Maximum drain current vs. case temperature

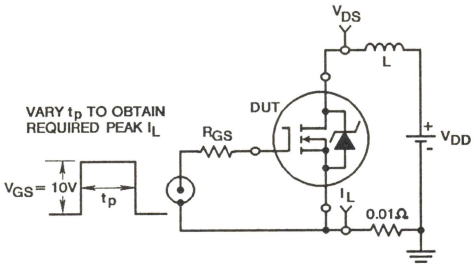


Fig. 14a — unclamped inductive test circuit

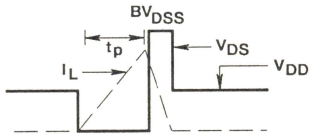


Fig. 14b — unclamped inductive waveforms

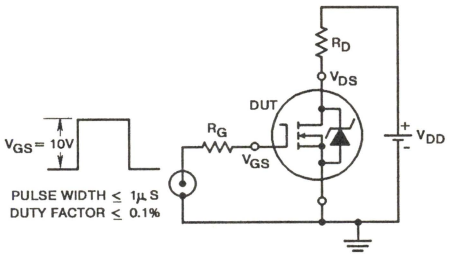


Fig. 15a — switching time test circuit

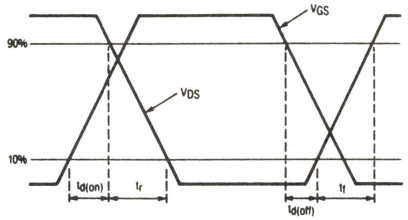


Fig. 15b — switching time waveforms

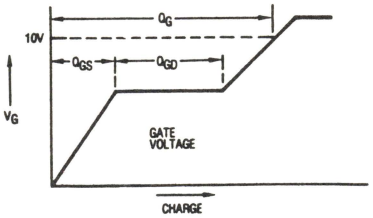


Fig. 16a — Basic gate charge waveform

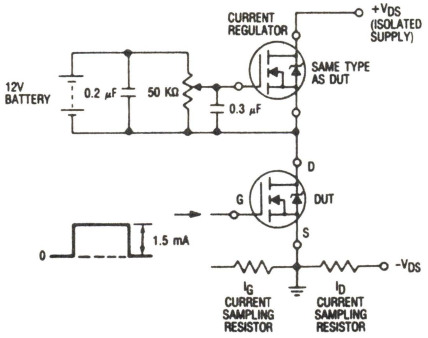


Fig. 16b — Gate charge test circuit

HARRIS SEMICONDUCTOR

IRFR214
IRFU214

N-Channel Power MOSFETs
Avalanche Energy Rated

March 1994

Features

- 2.2A, 250V
- $r_{DS(on)} = 2.0\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- High Input Impedance
- +150°C Operating Temperature

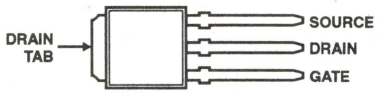
Description

The IRFR214 and IRFU214 (TA17443) are n-channel enhancement-mode silicon-gate power field-effect transistors designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

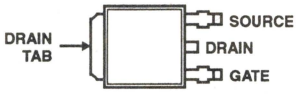
The IRFU214 is supplied in the JEDEC TO-251AA plastic package and the IRFR214 in the JEDEC TO-252AA plastic package.

Package

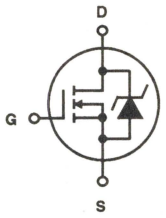
TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFR214, IRFU214	UNITS
Drain-Source Voltage (1)	V_{DS}	250	V
Drain Gate Voltage	V_{DGR}	250	V
Continuous Drain Current			
T_C = +25°C	I_D	2.2	A
T_C = +100°C	I_D	1.4	A
Pulsed Drain Current (2)	I_{DM}	8.8	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	25	W
Linear Derating Factor		0.20	W/°C
Single Pulse Avalanche Rating (3) (See Fig. 12)	E_{AS}	61	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve.
3. V_{DD} = 50V, Starting T_J = +25°C, L = 21mH, R_G = 25Ω, Peak I_L = 2.2A

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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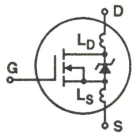
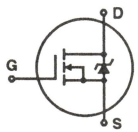
File Number **3274**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	250	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250V, V_{GS} = 0V	-	-	250	μA
		V_{DS} = 200V, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 1.3A, V_{GS} = 10V	-	1.6	2.0	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = 50V, I_{DS} = 1.3A	1.1	-	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	140	-	pF
Output Capacitance	C_{OSS}		-	42	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	9.6	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 125V, I_D = 2.7A, R_G = 24Ω, R_D = 45Ω, See Figure 15 (MOSFET switching times are essentially independent of operating temperature)	-	7.0	-	ns
Rise Time	t_r		-	7.6	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	16	-	ns
Fall Time	t_f		-	7.0	-	ns
Total Gate Charge	Q_{g10}	V_{GS} = 10V, I_D = 2.7A V_{DS} = 0.8 x Max Rating. See Figure 16 for test circuit (Gate charge is essentially independent of operating temperature)	-	-	10	nC
Gate-Source Charge	Q_{gs}		-	-	1.8	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	-	5.5	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad. 	-	7.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	5.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.7	-	°C/W
Junction to Ambient	$R_{\theta JA}$	Free air operation	-	-	110	°C/W

Source-Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	-	-	2.2	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}		-	-	8.8	A
Diode Forward Voltage (Note 1)	V_{SD}	T_J = +25°C, I_{SD} = 2.2A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_{SD} = 2.7A, dI_{SD}/dt = 100A/μs	97	-	390	ns
Reverse Recovery Charge	Q_{RR}	T_J = +25°C, I_{SD} = 2.7A, dI_{SD}/dt = 100A/μs	0.32	-	1.3	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

NOTES: 1. Pulse Test: Pulse width ≤ 300μs. Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 11).

Performance Curves

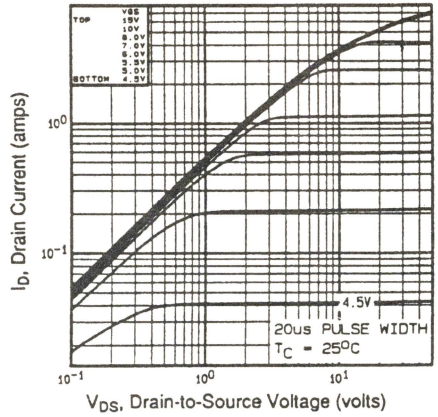


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS (T_C = +25°C)

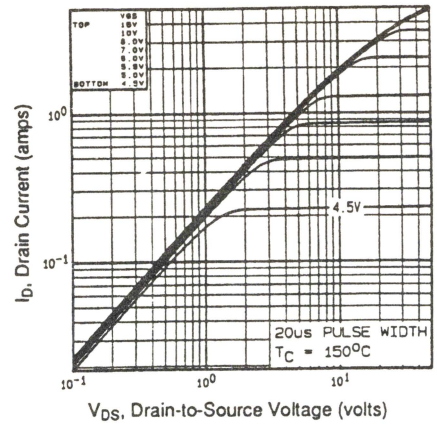


FIGURE 2. TYPICAL OUTPUT CHARACTERISTICS (T_C = +150°C)

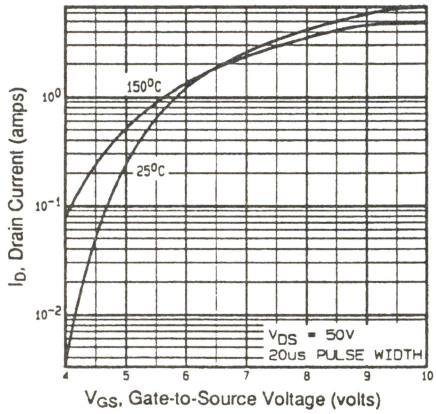


FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS

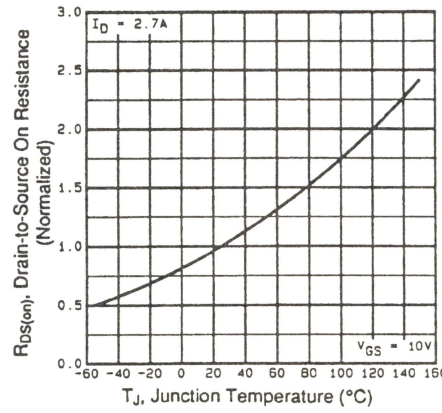


FIGURE 4. NORMALIZED ON-RESISTANCE vs TEMPERATURE

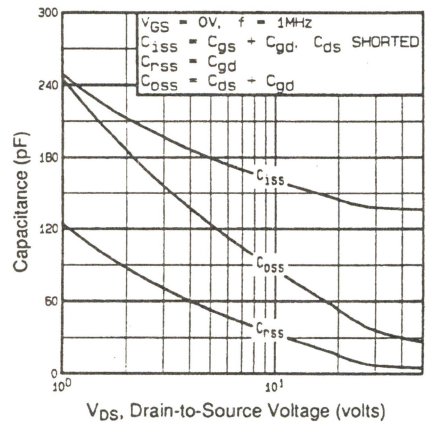


FIGURE 5. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

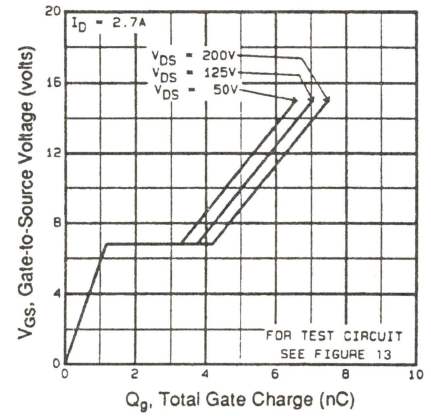


FIGURE 6. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

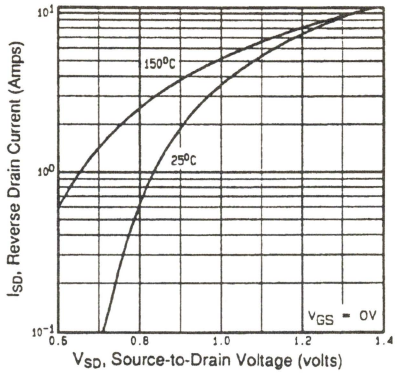


FIGURE 7. TYPICAL SOURCE DRAIN DIODE FORWARD VOLTAGE

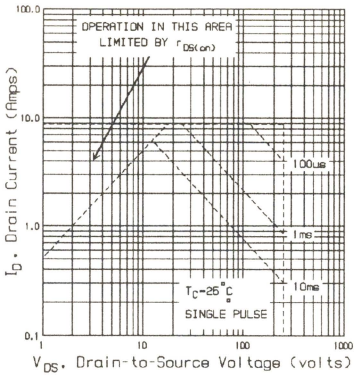


FIGURE 8. MAXIMUM SAFE OPERATING AREA

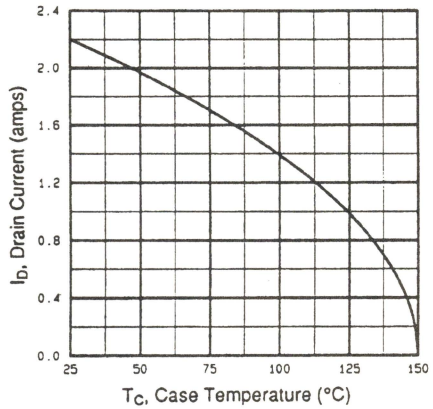


FIGURE 9. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

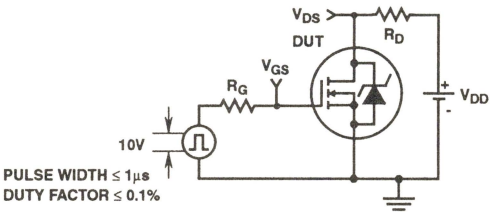


FIGURE 10a. SWITCHING TIME TEST CIRCUIT

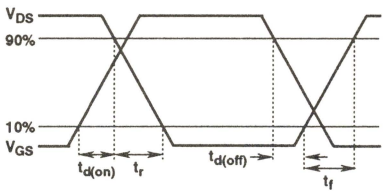


FIGURE 10b. SWITCHING THE WAVEFORMS

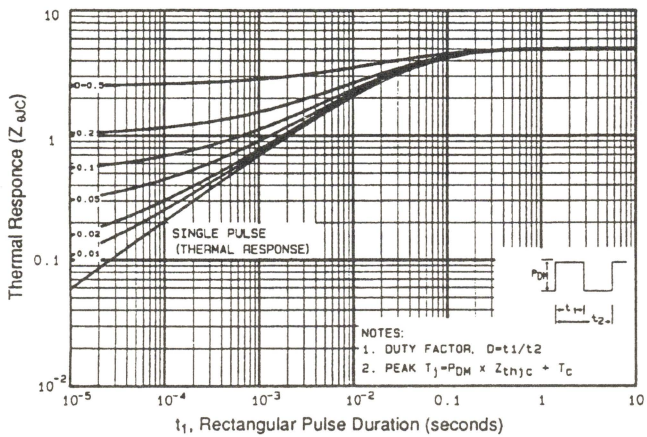


FIGURE 11. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

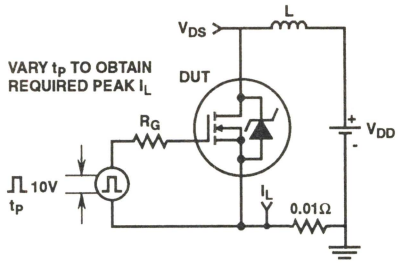


FIGURE 12a. UNCLAMPED INDUCTIVE TEST CIRCUIT

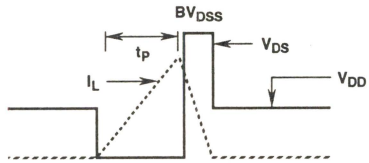


FIGURE 12b. UNCLAMPED INDUCTIVE WAVEFORMS

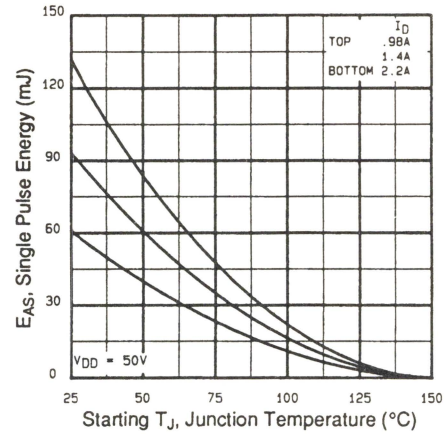


FIGURE 12c. MAX. AVALANCHE ENERGY vs DRAIN CURRENT

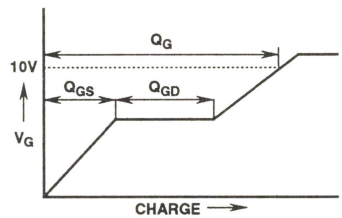


FIGURE 13a. BASIC GATE CHARGE WAVEFORM

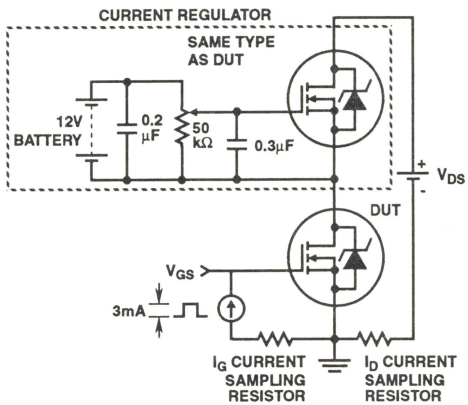


FIGURE 13b. GATE CHARGE TEST CIRCUIT

HARRIS

IRFR220/221/222
IRFU220/221/222

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 3.8A and 4.6A, 150V and 200V
- $r_{DS(on)}$ = 0.80Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

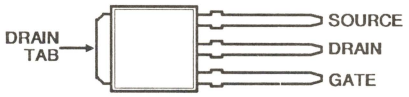
The IRFR220, IRFR221, IRFR222, IRFU220, IRFU221 and IRFU222 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

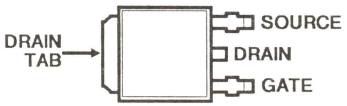
Because of space limitations branding (marking) on type IRFR220 is IRF220, IRFR221 is IFR221, IRFR222 is IRF222, IRFU220 is IFU220 and IRFU221 is IFU221, IRFU222 is IFU222.

Packages

TO-251AA
TOP VIEW

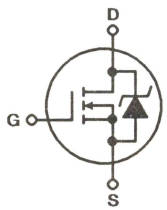


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFR220/221 IRFU220/221	IRFR222 IRFU222	UNITS
Continuous Drain Current			
T_C = 25°C ..... I_D	4.6	3.8	A
T_C = 100°C ..... I_D	2.9	2.4	A
Pulsed Drain Current ..... I_{DM}	18	15	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = 25°C ..... P_D	50	50	W
Linear Derating Factor	0.4	0.4	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS}	85	85	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. V_{DD} = 10V, Start T_J = +25°C, L = 6.18mH, R_G = 50Ω, Peak I_L = 4.6A
3. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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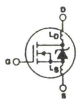
File Number **2410**

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

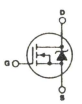
	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR221, IRFU221	150	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR220, IRFR222, IRFU220, IRFU222	200	—	—		
R_{DS}(on)	Static Drain-to-Source On-State Resistance ①	IRFR220, IRFR221, IRFU220, IRFU221	—	0.47	0.80	Ω	V_{GS} = 10 V, I_D = 2.4 A
		IRFR222, IRFU222	—	0.80	1.2		
I_D(on)	On-State Drain Current ①	IRFR220, IRFR221, IRFU220, IRFU221	4.6	—	—	A	V_{DS} > I_D(on) x R_{DS}(on) Max. V_{GS} = 10 V
		IRFR222, IRFU222	3.8				
V_{GS}(th)	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ①	ALL	1.7	2.6	—	S (℧)	V_{DS} ≥ 50 V, I_{DS} = 2.4 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{SSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	12	18	nC	V_{GS} = 10 V, I_D = 4.6 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.3	3.4		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	4.5	6.8		See Fig. 16. (Independent of operating temperature)
t_d(on)	Turn-On Delay Time	ALL	—	8.8	13	ns	V_{DD} = 100 V, I_D ≈ 4.6 A, R_G = 18 Ω
t_r	Rise Time	ALL	—	27	41		R_D = 18 Ω
t_d(off)	Turn-Off Delay Time	ALL	—	21	32		See Fig. 15
t_f	Fall Time	ALL	—	14	21		(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	330	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	120	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	41	—		See Fig. 10

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC	TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	4.6	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode)	ALL	—	—	18		
V_{SD}	Diode Forward Voltage ①	ALL	—	—	1.8	V	T_J = 25°C, I_S = 4.6 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	69	170	400	ns	T_J = 25°C, I_F = 4.6 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.30	0.72	1.8	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	2.5	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ③
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

② V_{DD} = 10 V, Starting T_J = 25°C, L = 6.18 mH, R_G = 50 Ω, Peak I_L = 4.6 A.

③ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

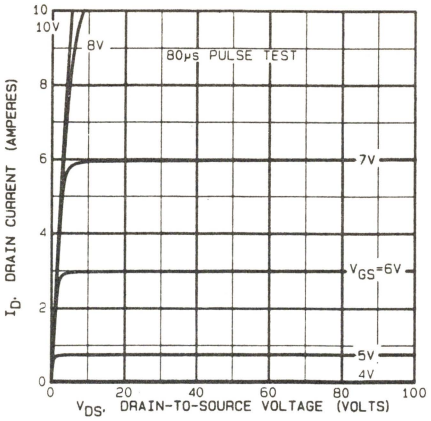


Fig. 1 - Typical output characteristics.

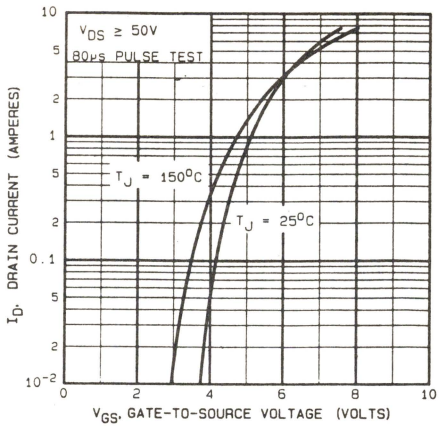


Fig. 2 - Typical transfer characteristics.

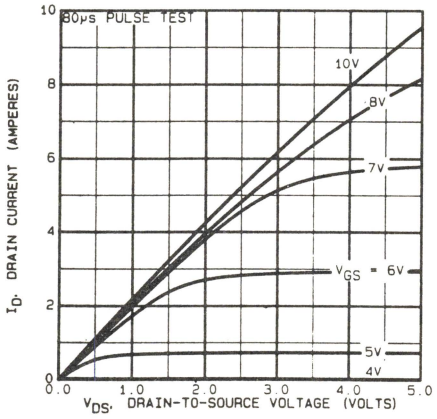


Fig. 3 - Typical saturation characteristics.

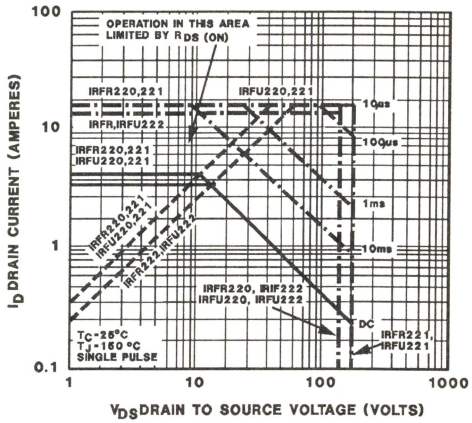


Fig. 4 - Maximum safe operating area.

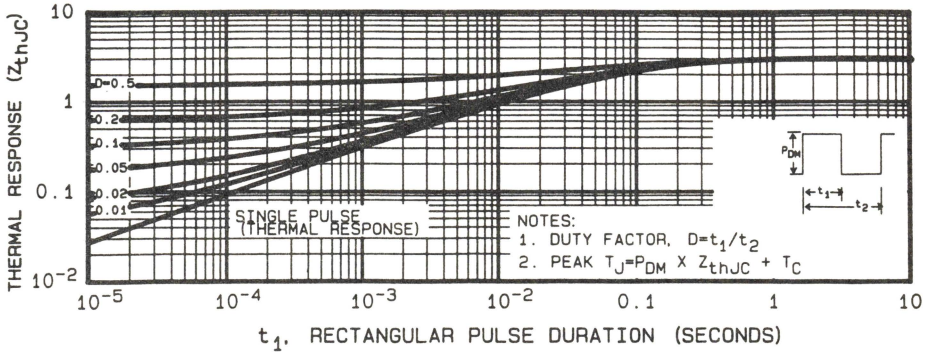


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

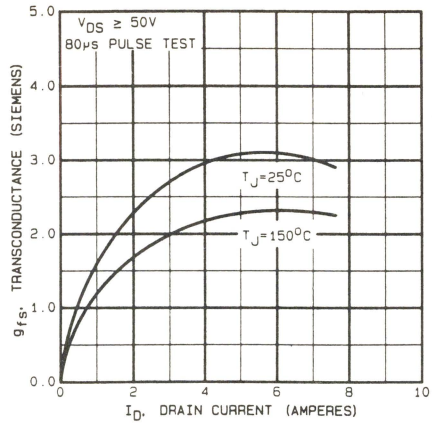


Fig. 6 - Typical transconductance vs. drain current.

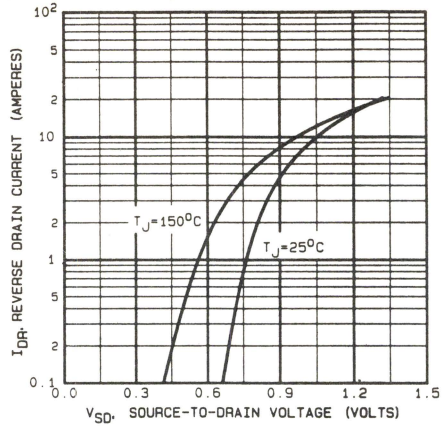


Fig. 7 - Typical source-drain diode forward voltage.

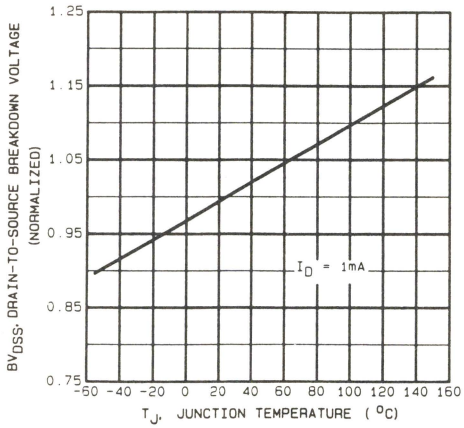


Fig. 8 - Breakdown voltage vs. temperature.

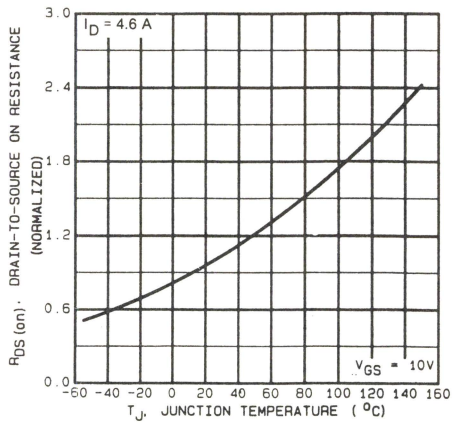


Fig. 9 - Normalized on-resistance vs. temperature.

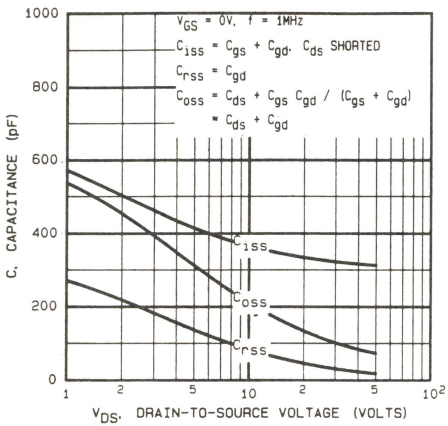


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

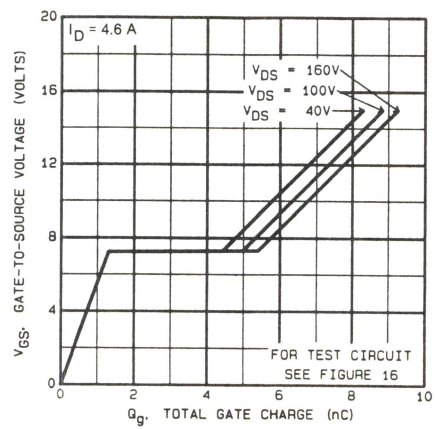


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

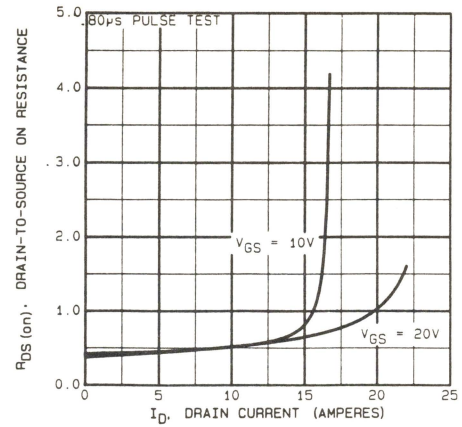


Fig. 12 — Typical on-resistance vs. drain current

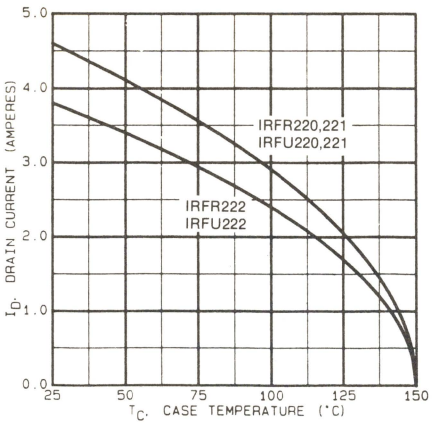


Fig. 13 — Maximum drain current vs. case temperature

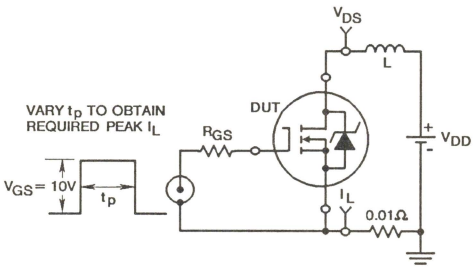


Fig. 14a — unclamped inductive test circuit

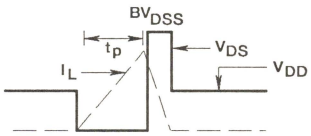


Fig. 14b — unclamped inductive waveforms

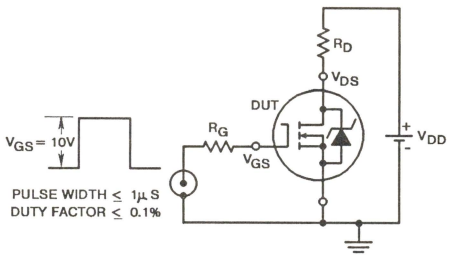


Fig. 15a — switching time test circuit

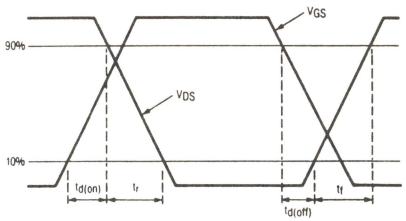


Fig. 15b — switching time waveforms

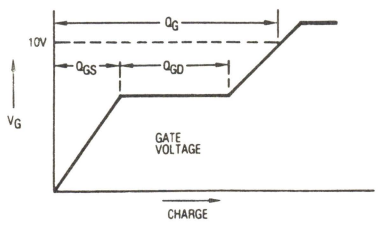


Fig. 16a — Basic gate charge waveform

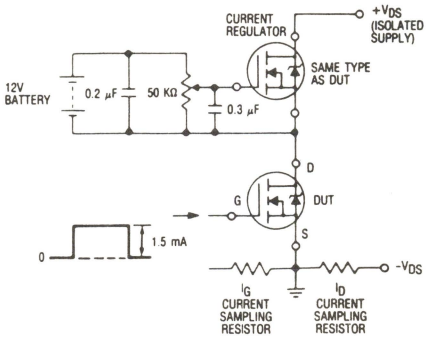


Fig. 16b — Gate charge test circuit

HARRIS

IRFR320/321/322
IRFU320/321/322

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 2.6A and 3.1A, 350V and 400V
- $r_{DS(on)}$ = 1.80Ω and 2.5Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

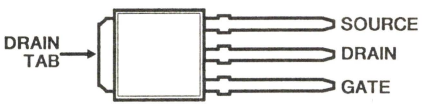
The IRFR320, IRFR321, IRFR322, IRFU320, IRFU321 and IRFU322 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

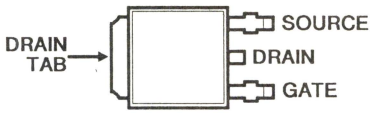
Because of space limitations branding (marking) on type IRFR320 is IRF320, IRFR321 is IFR321, IRFR322 is IRF322, IRFU320 is IFU320 and IRFU321 is IFU321, IRFU322 is IFU322.

Packages

IRFU320/321/322 TO-251AA
TOP VIEW

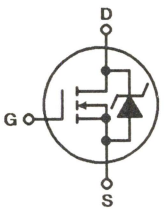


IRFR320/321/322 TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

	IRFU320/321 IRFR320/321	IRFU322 IRFR322	UNITS
Continuous Drain Current			
T_C = 25°C ..... I_D	3.1	2.6	A
T_C = 100°C ..... I_D	2.0	1.7	A
Pulsed Drain Current ..... I_{DM}	12	10	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = 25°C ..... P_D	50	50	W
Linear Derating Factor	0.4	0.4	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS}	190	190	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. V_{DD} = 50V, Start T_J = +25°C, L = 3.1mH, R_G = 25Ω, Peak I_L = 3.1A
3. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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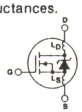
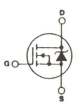
File Number 2412

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR321 IRFU321	350	—	—	V	V_{GS} = 0 V, I_D = 250 μs
		IRFR320 IRFU322 IRFR320 IRFU322	400	—	—		
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ①	IRFR320 IRFR321 IRFU320 IRFU321	—	1.6	1.8	Ω	V_{GS} = 10 V, I_D = 1.7 A
		IRFR322 IRFU322	—	1.6	2.5		
$I_D(on)$	On-State Drain Current ①	IRFR320 IRFU320 IRFR321 IRFU321	3.1	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max. V_{GS} = 10 V
		IRFR322 IRFU322	2.6				
$V_{GS}(th)$	Gate Threshold Voltage ①	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance	ALL	1.7	2.6	—	S (℧)	$V_{DS} \geq$ 50 V, I_{DS} = 1.7 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	13	20	nC	V_{GS} = 10 V, I_D = 3.1 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.2	3.3		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	7.2	11		See Fig. 16. (Independent of operating temperature)
$t_d(on)$	Turn-On Delay Time	ALL	—	10	15	ns	V_{DD} = 200 V, $I_D \approx$ 3.1 A, R_G = 18 Ω
t_r	Rise Time	ALL	—	14	21		R_D = 56 Ω
$t_d(off)$	Turn-Off Delay Time	ALL	—	30	45		See Fig. 15
t_f	Fall Time	ALL	—	13	20		(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
							Modified MOSFET symbol showing the internal inductances. 
C_{iss}	Input Capacitance	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	64	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	8.1	—		See Fig. 10

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	3.1	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I_{SM}	Pulsed Source Current (Body Diode)	ALL	—	—	12		
V_{SD}	Diode Forward Voltage ①	ALL	—	—	1.6	V	T_J = 25°C, I_S = 3.1 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	120	270	600	ns	T_J = 25°C, I_F = 3.1 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.64	1.4	3.0	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	2.5	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ③
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%. ② V_{DD} = 50 V, Starting T_J = 25°C, L = 3.1 mH, R_G = 25 Ω, Peak I_L = 3.1 A. ③ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

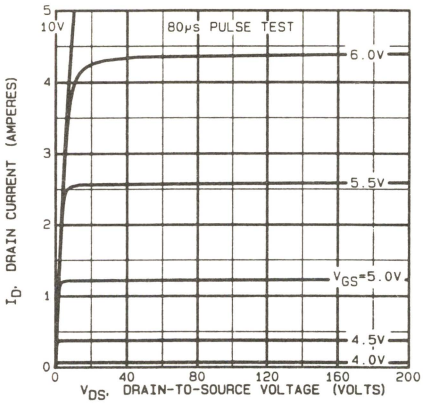


Fig. 1 - Typical output characteristics.

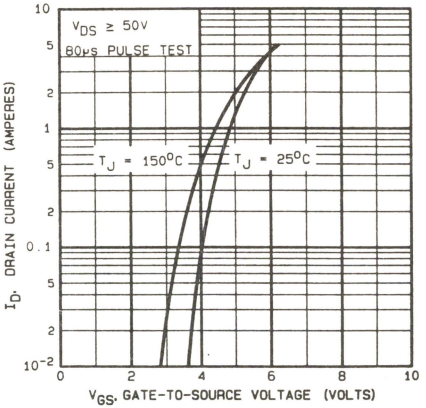


Fig. 2 - Typical transfer characteristics.

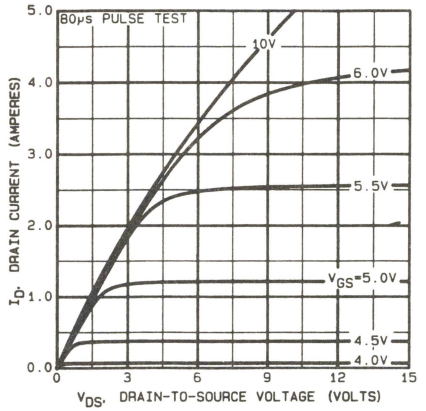


Fig. 3 - Typical saturation characteristics.

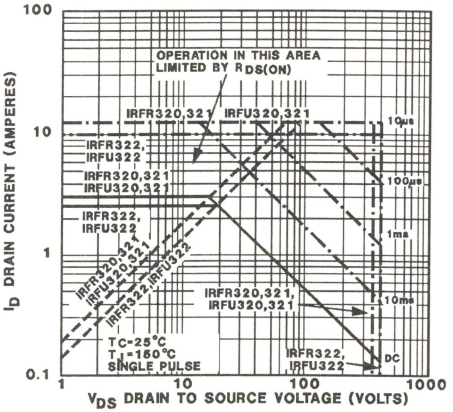


Fig. 4 - Maximum safe operating area.

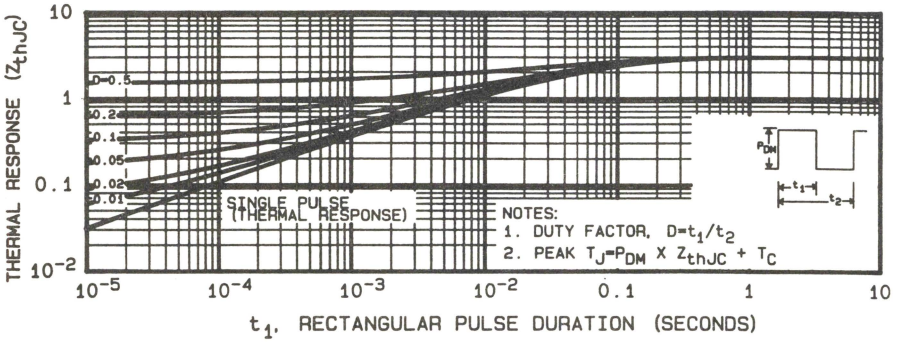


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

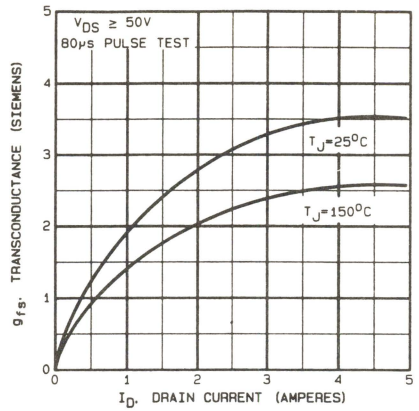


Fig. 6 - Typical transconductance vs. drain current.

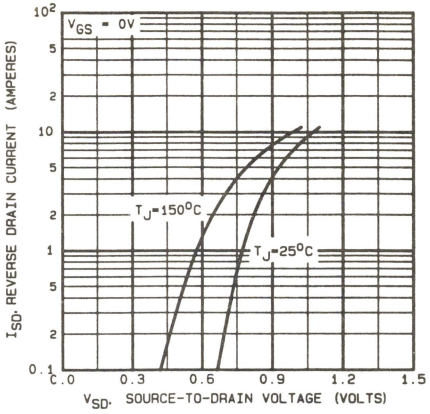


Fig. 7 - Typical source-drain diode forward voltage.

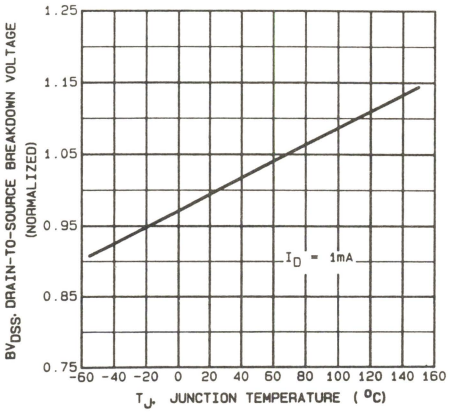


Fig. 8 - Breakdown voltage vs. temperature.

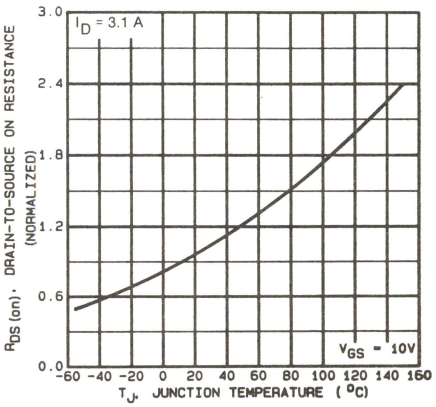


Fig. 9 - Normalized on-resistance vs. temperature.

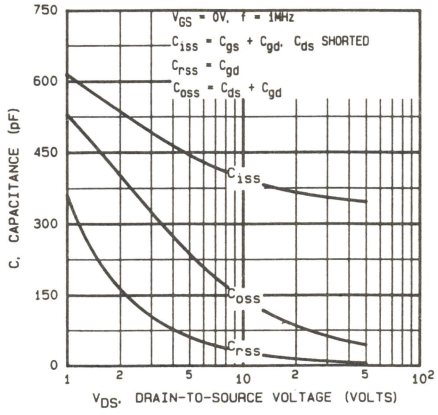


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

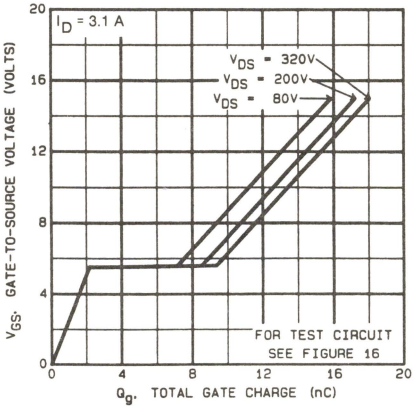


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

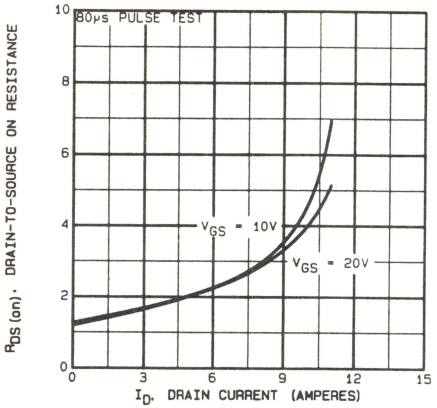


Fig. 12 — Typical on-resistance vs. drain current

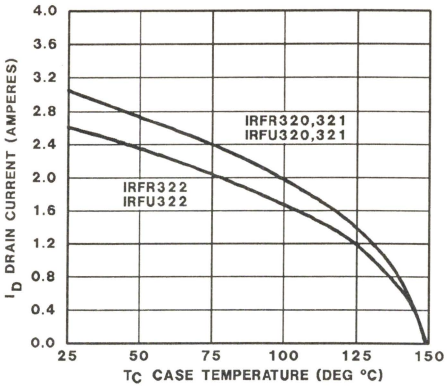


Fig. 13 — Maximum drain current vs. case temperature

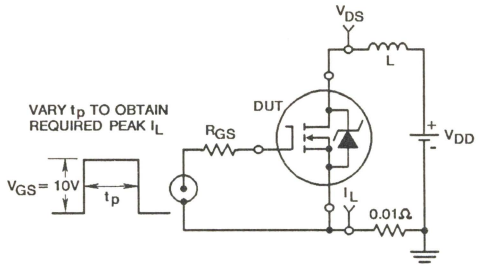


Fig. 14a — unclamped inductive test circuit

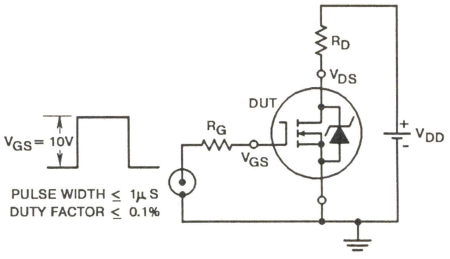


Fig. 15a — switching time test circuit

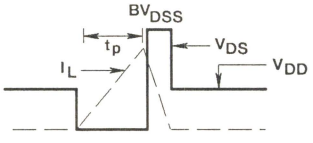


Fig. 14b — unclamped inductive waveforms

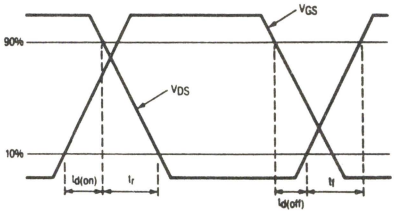


Fig. 15b — switching time waveforms

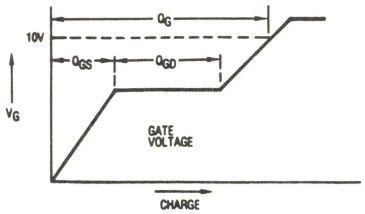


Fig. 16a — Basic gate charge waveform

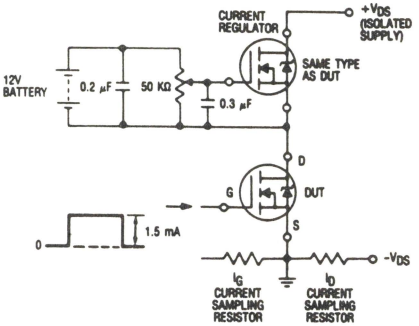


Fig. 16b — Gate charge test circuit

HARRIS SEMICONDUCTOR

IRFR410
IRFU410

1.5A, 500V Avalanche Energy Rated N-Channel Enhancement Mode Power MOSFETs

September 1992

Features

- 1.5A, 500V
- $r_{DS(ON)}$ = 7.0Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- High Input Impedance
- +150°C Operating Temperature

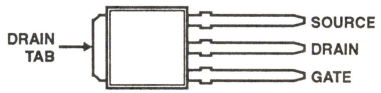
Description

The IRFR410 and IRFU410 are n-channel enhancement-mode silicon-gate power field-effect transistors designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These advanced power MOSFETs are designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

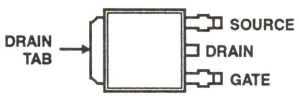
The IRFR410 is supplied in the JEDEC TO-252AA plastic package and the IRFU410 in the JEDEC TO-251AA plastic package.

Packages

TO-251AA
TOP VIEW

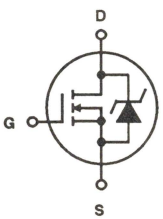


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFR410, IRFU410	UNITS
Drain-Source Voltage (1)	V_{DS}	500	V
Continuous Drain Current			
T_C = +25°C	I_D	1.5	A
T_C = +100°C	I_D	1.2	A
Pulsed Drain Current (2)	I_{DM}	3.0	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	42	W
Linear Derating Factor		0.33	W/°C
Single Pulse Avalanche Rating (3) (See Fig. 13)	E_{AS}	45	mj
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

1. T_J = +25°C to +150°C.
2. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Figure 11)
3. V_{DD} = 50V, Starting T_J = +25°C, L = 40mH, R_G = 25Ω, Peak I_L = 1.5A.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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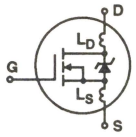
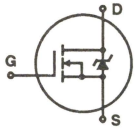
File Number 3372

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	500	-	-	V
Temperature Coeffecient of Breakdown Voltage	$\Delta BV_{DSS}/\Delta T_J$	Reference to +25°C, I_D = 250μA	-	0.61	-	V/°C
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	2	-	4	V
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500V, V_{GS} = 0V	-	-	10	μA
		V_{DS} = 500V, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 1.5A, V_{GS} = 10V	-	-	7.0	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = 50V, I_{DS} = 0.75A	0.5	-	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 5	-	210	-	pF
Output Capacitance	C_{OSS}		-	30	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	7	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 1.5A, R_{GS} = 24Ω, R_L = 167Ω, See Figures 10 and 12 (MOSFET switching times are essentially independent of operating temperature) (Note 1)	-	7	-	ns
Rise Time	t_r		-	10	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	24	-	ns
Fall Time	t_f		-	15	-	ns
Total Gate Charge	Q_{g10}	V_{GS} = 10V, I_D = 1.5A, V_{DS} = 0.8 x BV_{DSS}. See Figure 6 (Gate charge is essentially independent of operating temperature) (Note 1)	-	9	12	nC
Gate-Source Charge	Q_{gs}		-	1.1	1.4	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	5	7	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 6mm (0.25") from package to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from package to source bonding pad. 	-	7.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	3.0	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.7	-	°C/W
Junction to Ambient	$R_{\theta JA}$	Free air operation	-	-	110	°C/W

Source-Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 	-	-	1.5	A
Pulse Source Current (Body Diode) (Note 2)	I_{SM}		-	-	3.0	A
Diode Forward Voltage (Note 1)	V_{SD}	T_J = +25°C, I_{SD} = 1.5A, V_{GS} = 0V	-	-	2.0	V
Reverse Recovery Time (Note 1)	t_{rr}	T_J = +25°C, I_{SD} = 1.5A, dI_{SD}/dt = 100A/μs	130	-	520	ns
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

NOTES: 1. Pulse Test: Pulse width ≤ 300μs. Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 11).

Performance Curves

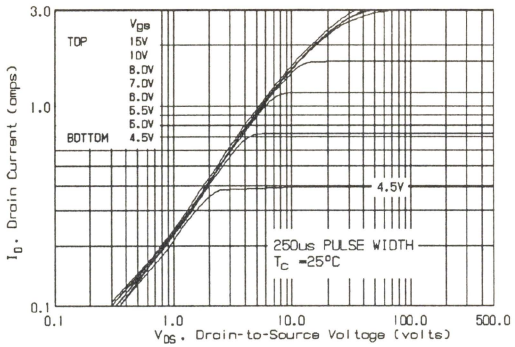


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS, T_C = +25°C

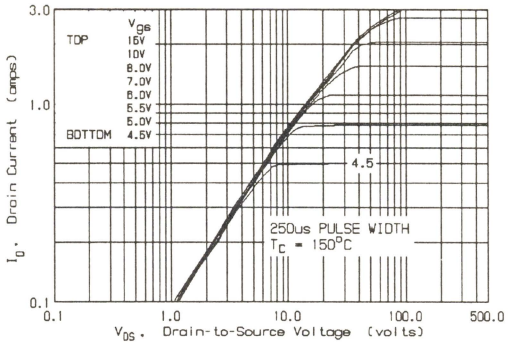


FIGURE 2. TYPICAL OUTPUT CHARACTERISTICS, T_C = +150°C

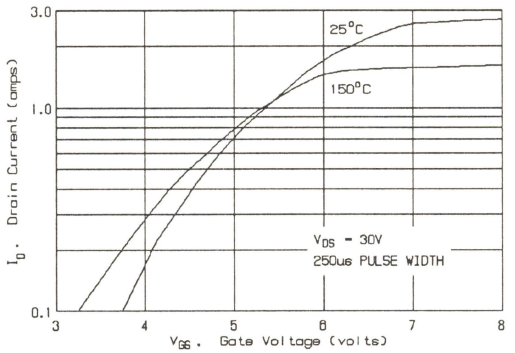


FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS

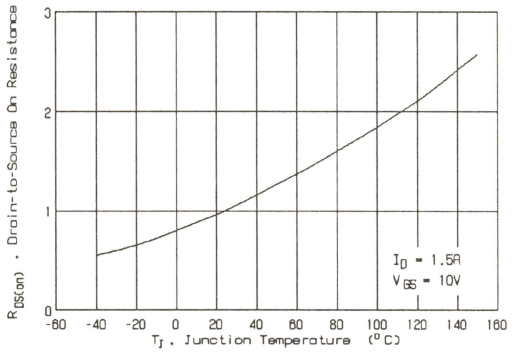


FIGURE 4. NORMALIZED ON-RESISTANCE vs TEMPERATURE

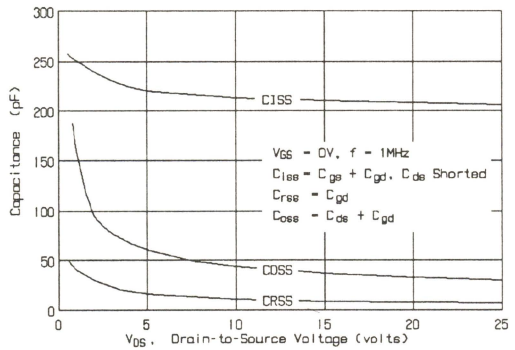


FIGURE 5. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

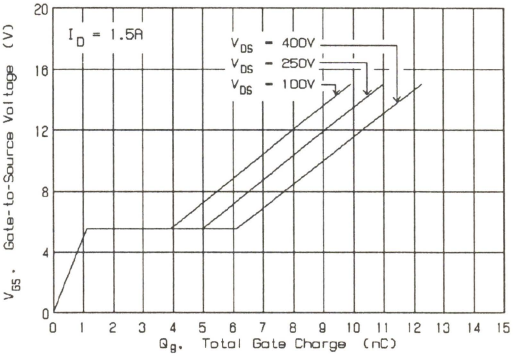


FIGURE 6. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

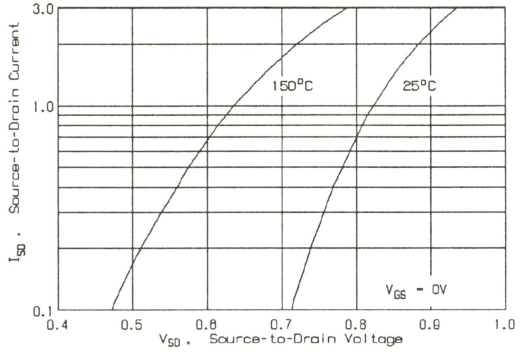


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

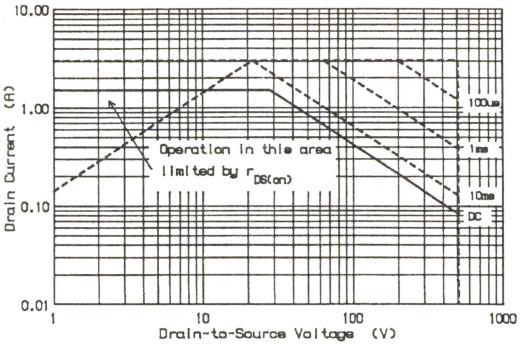


FIGURE 8. MAXIMUM SAFE OPERATING AREA

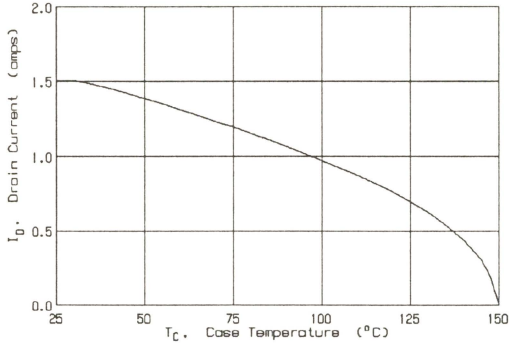


FIGURE 9. MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

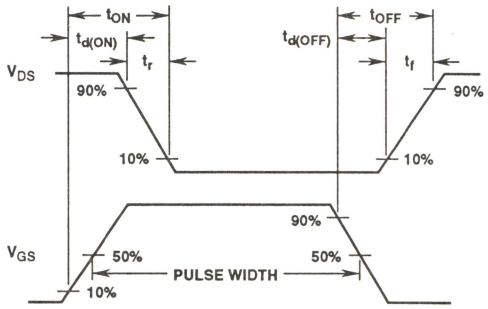


FIGURE 10. SWITCHING TIME WAVEFORMS

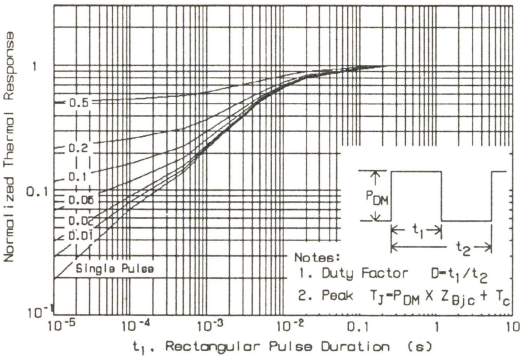


FIGURE 11. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE

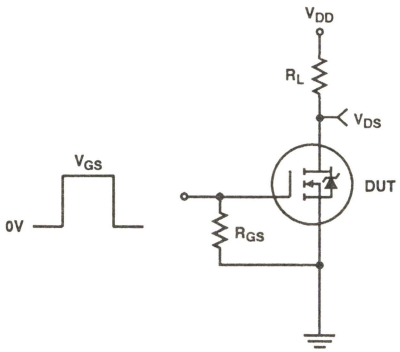


FIGURE 12. SWITCHING TIME TEST CIRCUIT

Performance Curves (Continued)

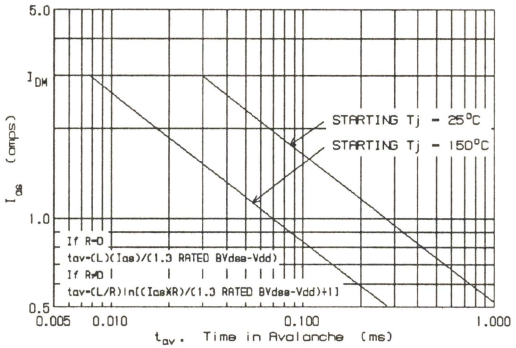


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

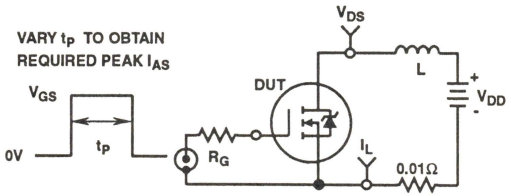


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING CIRCUIT

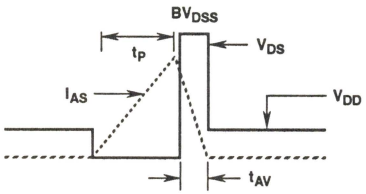


FIGURE 15. UNCLAMPED INDUCTIVE SWITCHING WAVEFORMS

HARRIS

IRFR420/421/422
IRFU420/421/422

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 2.2A and 2.5A, 450V and 500V
- $r_{DS(on)}$ = 3.0Ω and 4.0Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

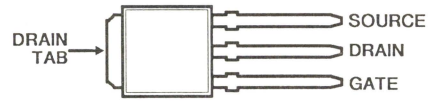
The IRFR420, IRFR421, IRFR422, IRFU420, IRFU421 and IRFU422 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are N-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

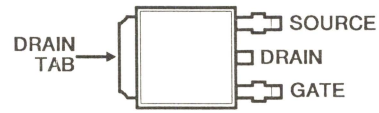
Because of space limitations branding (marking) on type IRFR420 is IFR420, IRFR421 is IFR421, IRFR422 is IFR422, IRFU420 is IFU420 and IRFU421 is IFU421, IRFU422 is IFU422.

Packages

IRFU420/421/422 TO-251AA
TOP VIEW

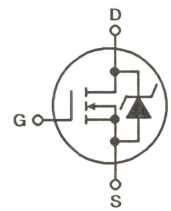


IRFR420/421/422 TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

	IRFU420/421 IRFR420/421	IRFU422 IRFR422	UNITS
Continuous Drain Current			
T_C = 25°C ..... I_D	2.5	2.2	A
T_C = 100°C ..... I_D	1.6	1.4	A
Pulsed Drain Current ..... I_{DM}	8	7	A
Gate-Source Voltage ..... V_{GS}	±20	±20	V
Maximum Power Dissipation			
T_C = 25°C ..... P_D	50	50	W
Linear Derating Factor	0.4	0.4	W/°C
Single Pulse Avalanche Energy Rating (2) ..... E_{AS}	210	210	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. V_{DD} = 50V, Start T_J = +25°C, L = 60mH, R_G = 25Ω, Peak I_L = 2.5A
3. Mounting pad must cover heatsink surface area. See Packages.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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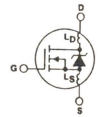
File Number **2411**

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

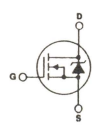
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR421 IRFU421	450	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR420 IRFR422 IRFU420 IRFU422	500	—	—		
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ①	IRFR420 IRFR421 IRFU420 IRFU421	—	2.9	3.0	Ω	V_{GS} = 10 V, I_D = 1.3 A
		IRFR422 IRFU422	—	—	4.0		
$I_D(on)$	On-State Drain Current ①	IRFR420 IRFR421 IRFU420 IRFU421	2.5	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max. V_{GS} = 10 V
		IRFR422 IRFU422	2.2				
$V_{GS}(th)$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
gf_s	Forward Transconductance ①	ALL	1.5	2.2	—	S (℧)	$V_{DS} \geq 50$ V, I_{DS} = 1.4 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	13	19	nC	V_{GS} = 10 V, I_D = 2.5 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.2	3.3		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	6.8	10		See Fig. 16. (Independent of operating temperature)
$t_d(on)$	Turn-On Delay Time	ALL	—	10	15	ns	V_{DD} = 250 V, $I_D \approx$ 2.5 A, R_G = 18 Ω
t_r	Rise Time	ALL	—	12	18		R_D = 100 Ω
$t_d(off)$	Turn-Off Delay Time	ALL	—	28	42		See Fig. 15
t_f	Fall Time	ALL	—	12	18		(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	54	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	9.6	—		See Fig. 10

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	2.5	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode)	ALL	—	—	8		
V_{SD}	Diode Forward Voltage ①	ALL	—	—	1.6	V	T_J = 25°C, I_S = 2.5 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	130	270	540	ns	T_J = 25°C, I_F = 2.5 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.57	1.2	2.3	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	2.5	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ③
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

② V_{DD} = 50 V, Starting T_J = 25°C, L = 60 mH, R_G = 25 Ω, Peak I_L = 2.5 A.

③ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

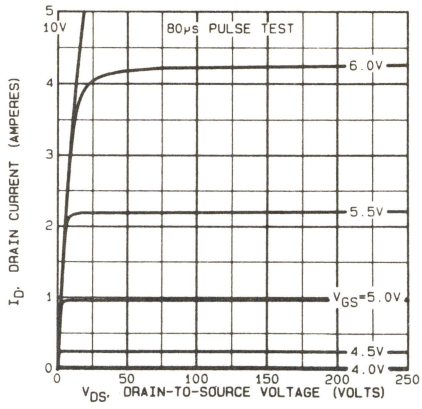


Fig. 1 - Typical output characteristics.

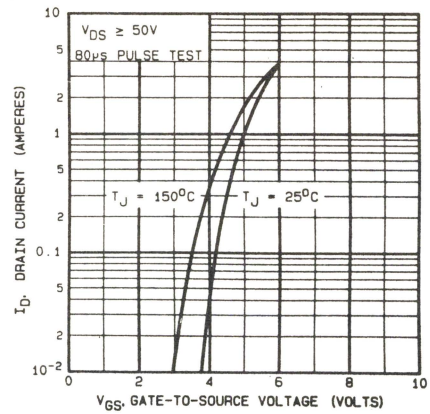


Fig. 2 - Typical transfer characteristics.

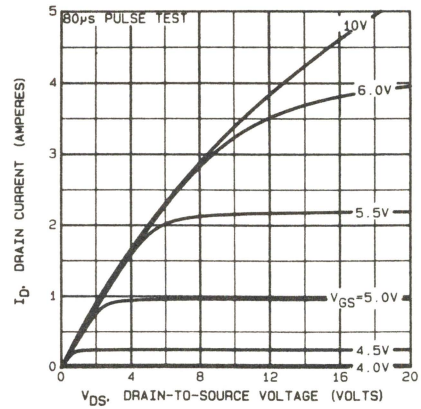


Fig. 3 - Typical saturation characteristics.

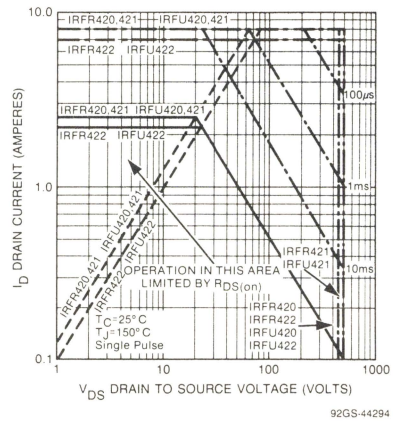


Fig. 4 - Maximum safe operating area.

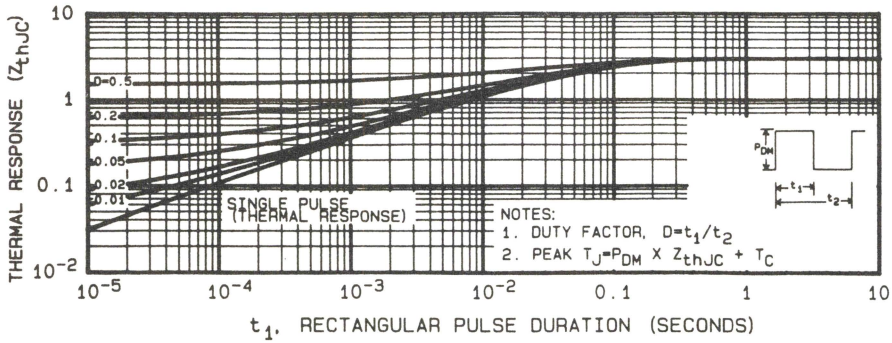


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

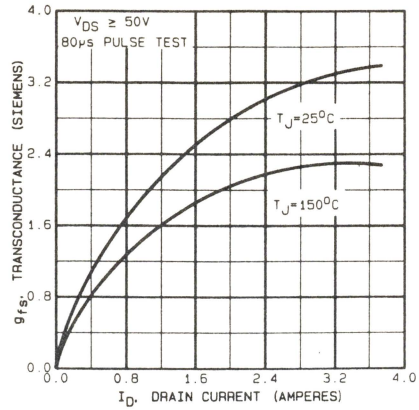


Fig. 6 - Typical transconductance vs. drain current.

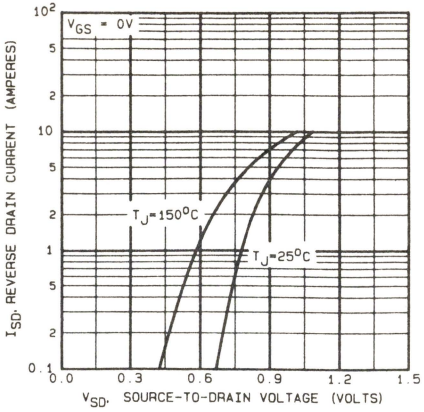


Fig. 7 - Typical source-drain diode forward voltage.

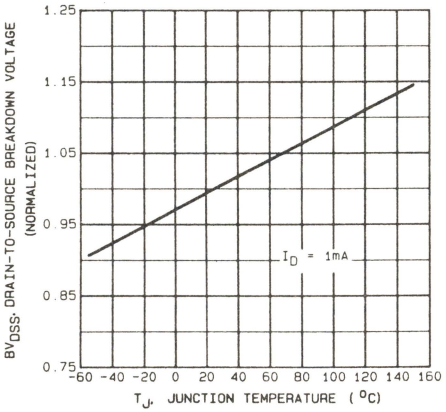


Fig. 8 - Breakdown voltage vs. temperature.

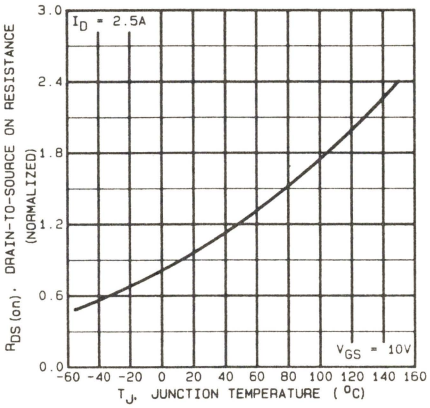


Fig. 9 - Normalized on-resistance vs. temperature.

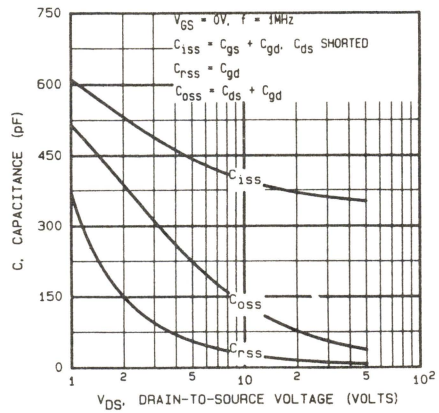


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

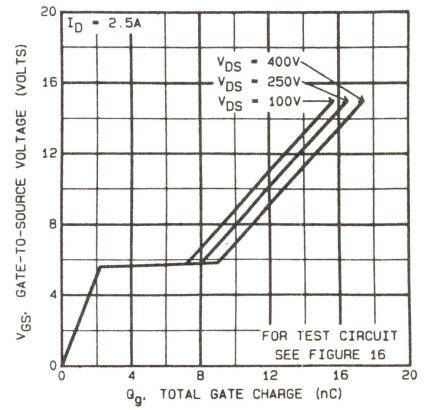


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

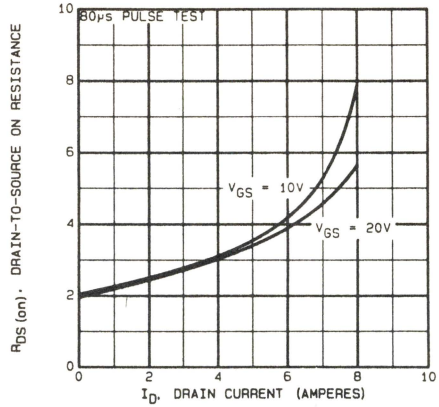


Fig. 12 — Typical on-resistance vs. drain current

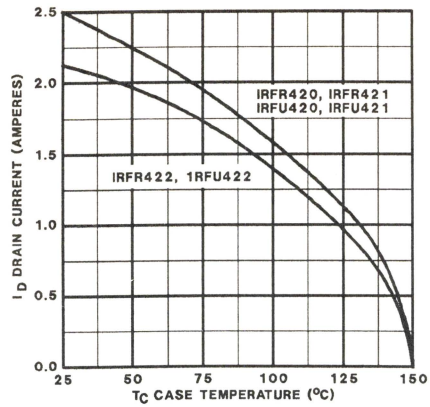


Fig. 13 — Maximum drain current vs. case temperature

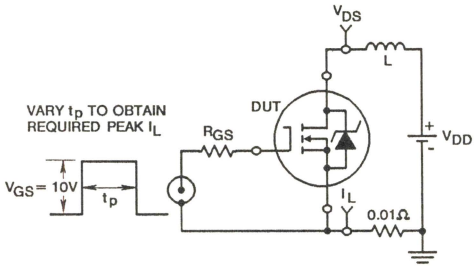


Fig. 14a — unclamped inductive test circuit

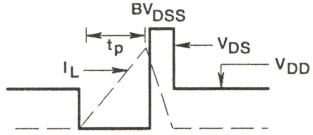


Fig. 14b — unclamped inductive waveforms

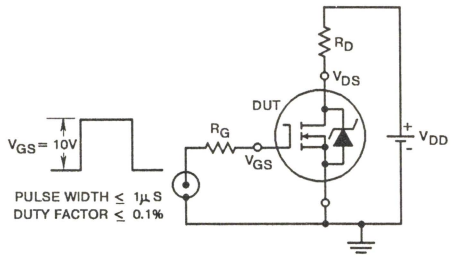


Fig. 15a — switching time test circuit

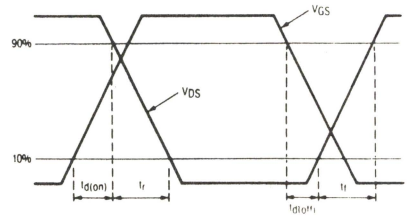


Fig. 15b — switching time waveforms

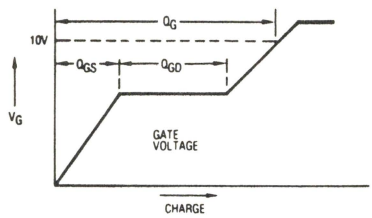


Fig. 16a — Basic gate charge waveform

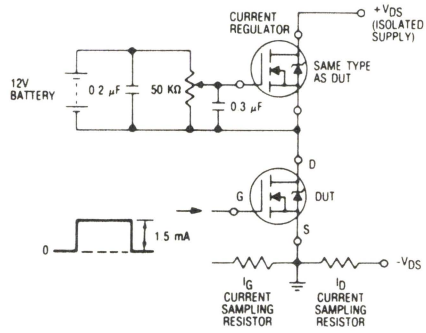


Fig. 16b — Gate charge test circuit

HARRIS

RFL1N08
RFL1N10

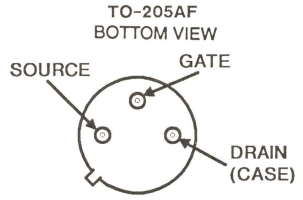
N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

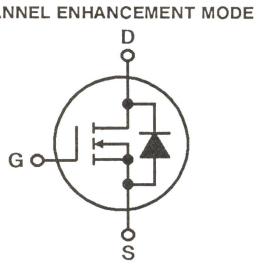
Features

- 1A, 80V and 100V
- $R_{DS(on)} = 1.2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package



Terminal Diagram



Description

The RFL1N08 and RFL1N10 are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL1N08	RFL1N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current, RMS Continuous	I_D	1	1	A
Pulsed	I_{DM}	5	5	A
Power Dissipation Total @ T_C = 25°C	P_D	8.33	8.33	W
Derating Above T_C = 25°C		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number 1385.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08		RFL1N10		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	μA
		V_{DS} = 80V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 65V	–	50	–	–	μA
		V_{DS} = 80V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.2	–	1.2	V
		I_D = 2A, V_{GS} = 10V	–	3.3	–	3.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.2	–	1.2	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08		RFL1N10		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

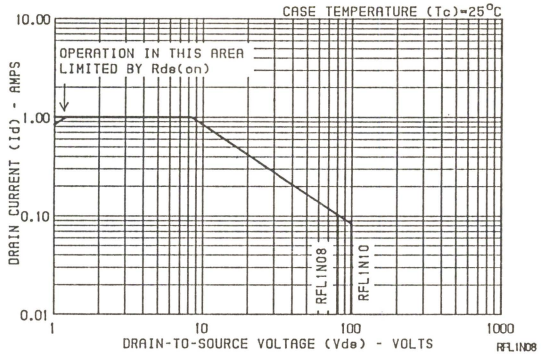


Fig. 1 - Maximum operating areas for all types.

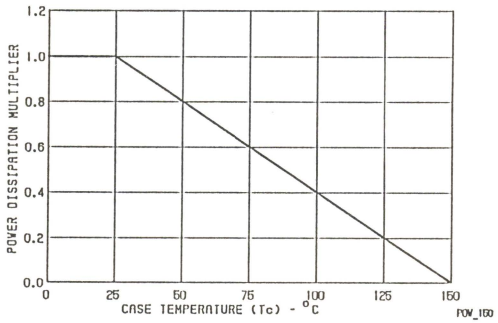


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

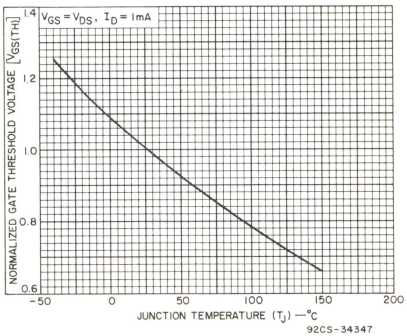


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

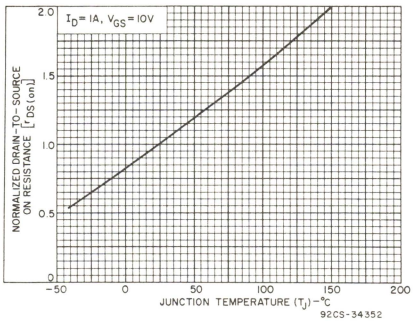


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

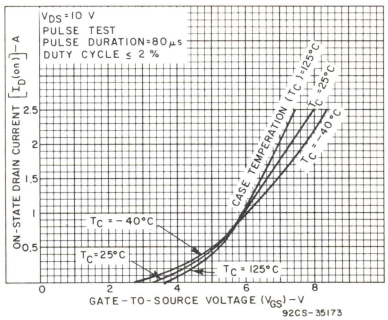


Fig. 5 - Typical transfer characteristics for all types.

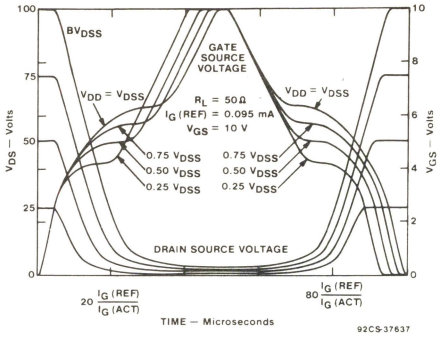


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

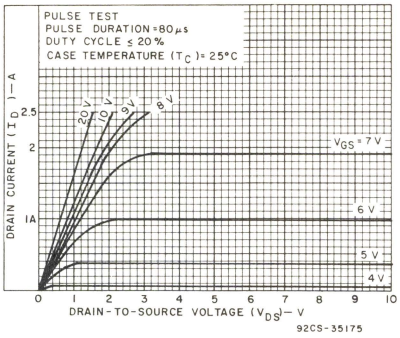


Fig. 7 - Typical saturation characteristics for all types.

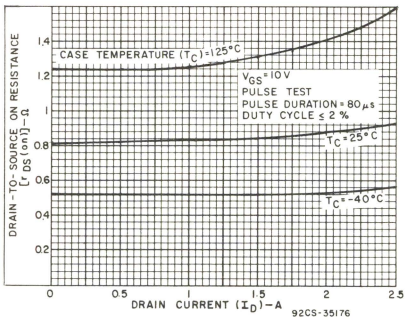


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

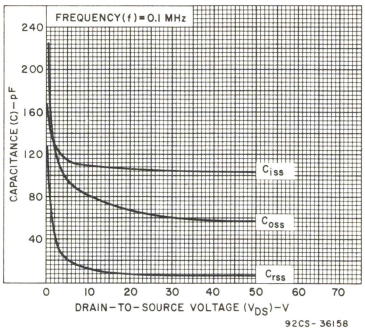


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

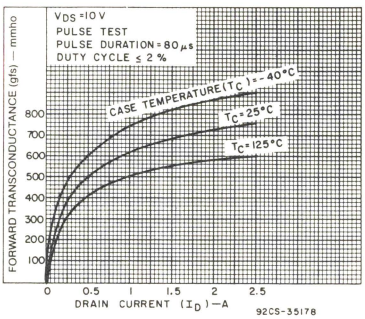


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

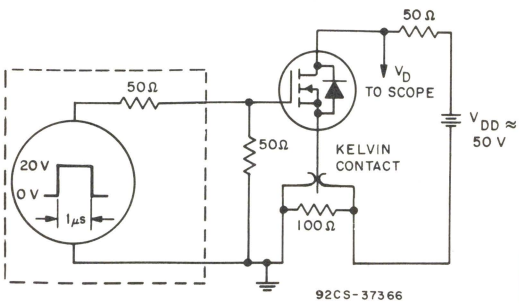


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFL1N12
RFL1N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 1A, 120V and 150V
- $r_{DS}(on) = 1.9\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

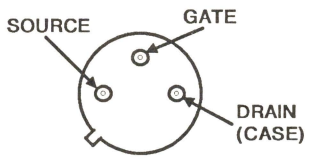
Description

The RFL1N12 and RFL1N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

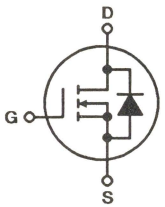
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL1N12	RFL1N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current	I_D	1A	1A	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	8.33	8.33	W
Linear Derating Factor		0.0667	0.0667	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1444.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N12		RFL1N15		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	-	120	-	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	-	1	-	-	μA
		V_{DS} = 120V	-	-	-	1	μA
		T_C = +125°C, V_{DS} = 100V	-	50	-	-	μA
		V_{DS} = 120V	-	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	100	-	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	-	1.9	-	1.9	V
		I_D = 2A, V_{GS} = 10V	-	6.3	-	6.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	-	1.9	-	1.9	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	-	400	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	200	-	200	pF
Output Capacitance	C_{OSS}		-	80	-	80	pF
Reverse-Transfer Capacitance	C_{RSS}		-	25	-	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	5	-	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N12		RFL1N15		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	-	1.4	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

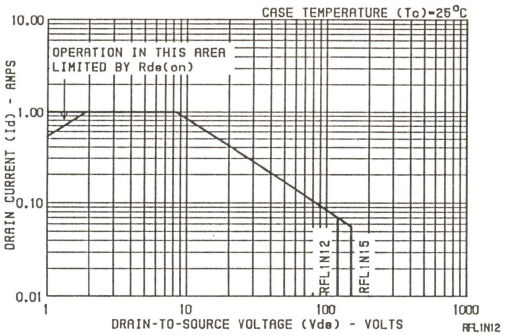


Fig. 1 — Maximum operating areas for all types.

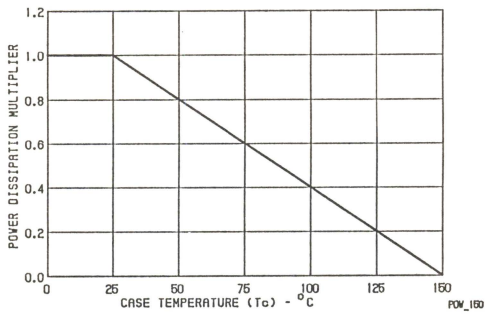


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

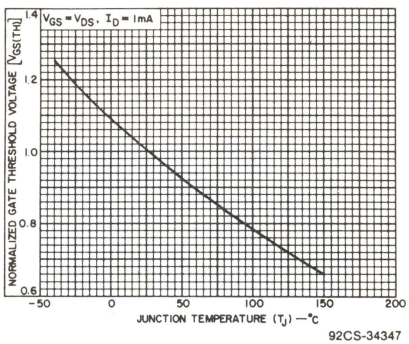


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

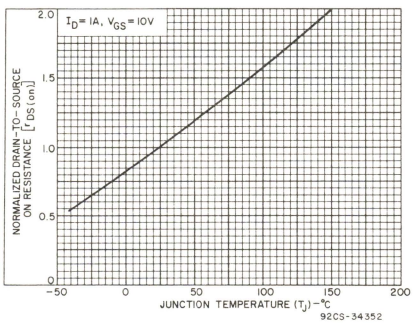


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

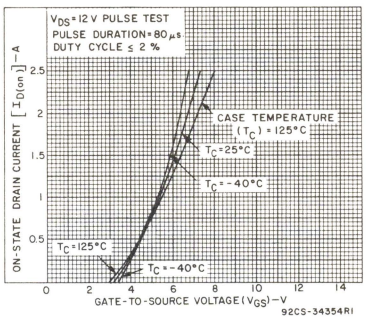


Fig. 5 — Typical transfer characteristics for all types.

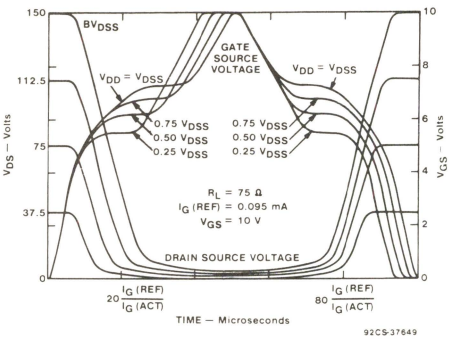


Fig. 6. Normalized switching waveforms for constant gate-current drive.

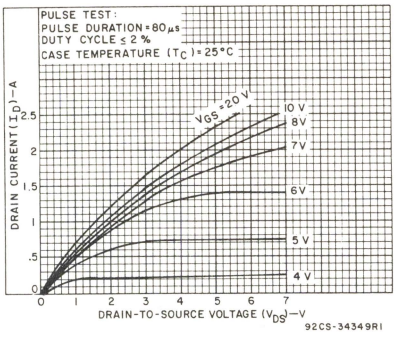


Fig. 7. Typical saturation characteristics for all types.

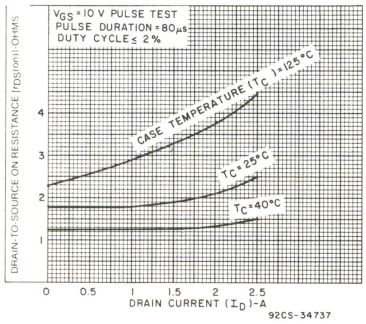


Fig. 8. Typical drain-to-source on resistance as a function of drain current for all types.

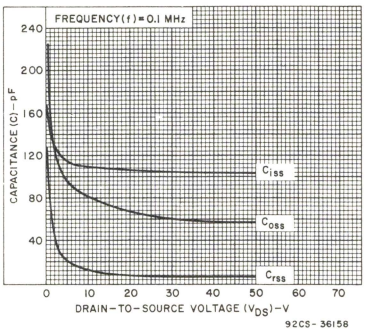


Fig. 9. Capacitance as a function of drain-to-source voltage for all types.

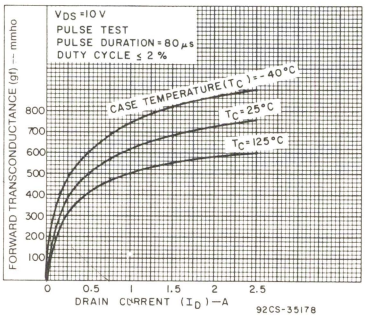


Fig. 10. Typical forward transconductance as a function of drain current for all types.

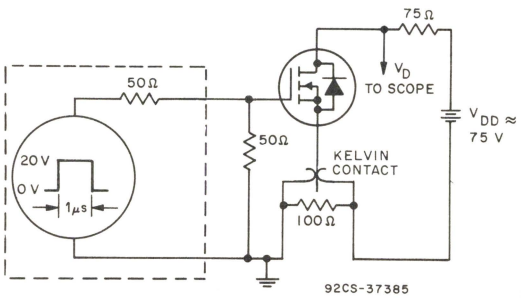


Fig. 11. Switching Time Test Circuit.

HARRIS

RFL1N18
RFL1N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 1A, 180V and 200V
- $r_{DS}(on) = 3.65\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

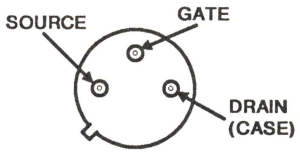
Description

The RFL1N18 and RFL1N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

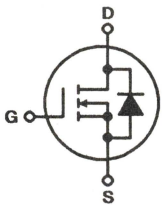
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL1N18	RFL1N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	8.33	8.33	W
Derate Above T_C = +25°C		0.0667	0.0667	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1442.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18		RFL2N20		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	–	200	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	–	1	–	–	μA
		V_{DS} = 160V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 145V	–	50	–	–	μA
		V_{DS} = 160V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.65	–	3.65	V
		I_D = 2A, V_{GS} = 10V	–	8.3	–	8.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.65	–	3.65	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	60	–	60	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	15 (typ)	25	15 (typ)	25	ns
Rise Time	t_r		20 (typ)	30	20 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18		RFL2N20		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = –1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

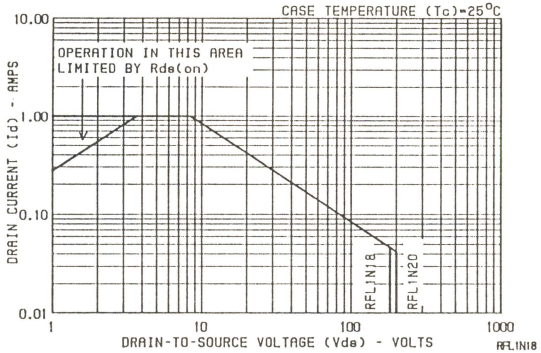


Fig. 1 - Maximum operating areas for all types.

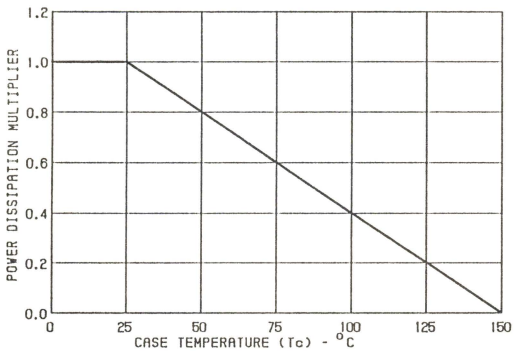


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

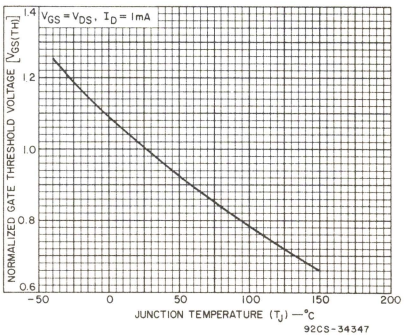


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

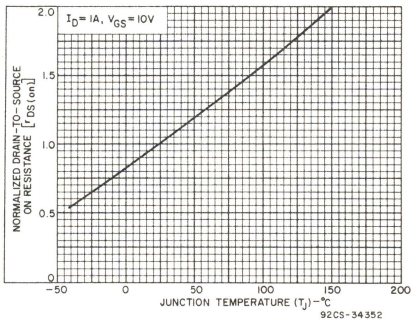


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

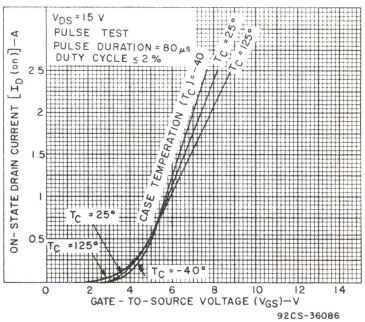


Fig. 5 - Typical transfer characteristics for all types.

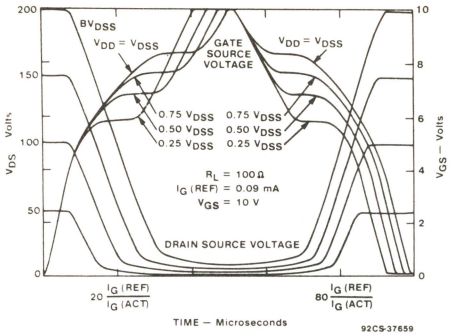


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

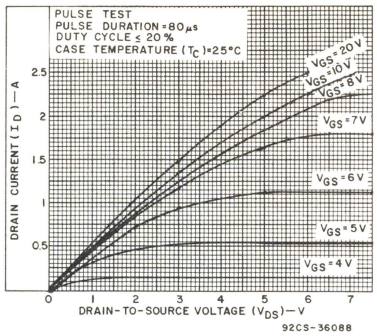


Fig. 7 - Typical saturation characteristics for all types.

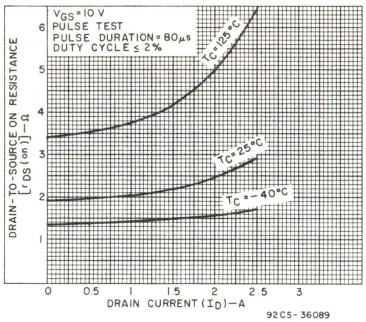


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

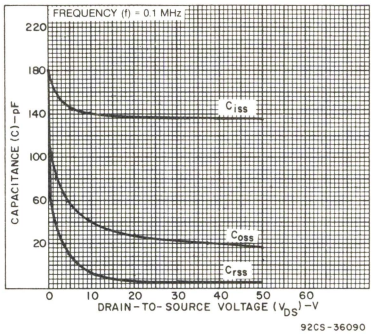


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

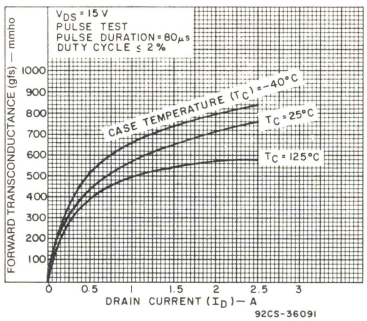


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

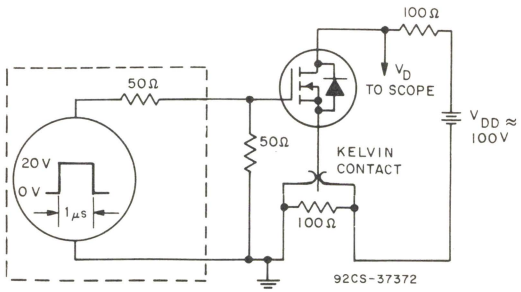


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFL2N05
RFL2N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

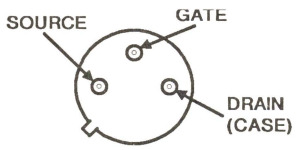
August 1991

Features

- 2A, 50V and 60V
- $R_{DS(on)} = 0.95\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

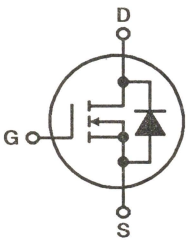
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Description

The RFL2N05 and RFL2N06 are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL2N05	RFL2N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current, RMS Continuous	I_D	2	2	A
Pulsed	I_{DM}	10	10	A
Power Dissipation Total @ T_C = 25°C	P_D	8.33	8.33	W
Derating Above T_C = 25°C		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.
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File Number 1497.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05		RFL2N06		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.95	–	0.95	V
		I_D = 2A, V_{GS} = 10V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 15V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.95	–	0.95	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	85	–	85	pF
Reverse-Transfer Capacitance	C_{RSS}		–	30	–	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	6 (typ)	15	6 (typ)	15	ns
Rise Time	t_r		14 (typ)	30	14 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		16 (typ)	30	16 (typ)	30	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05		RFL2N06		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration ≤ 300μs max., duty cycle ≤ 2%.

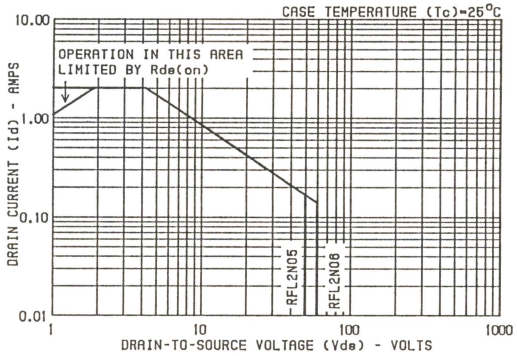


Fig. 1 — Maximum operating areas for all types.

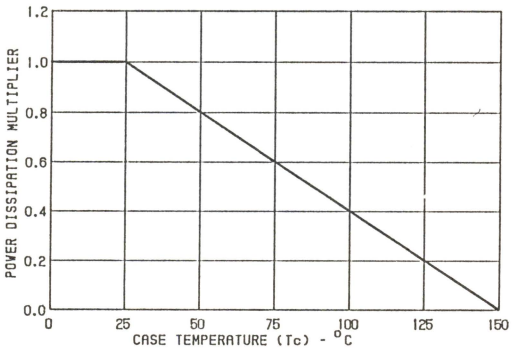


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

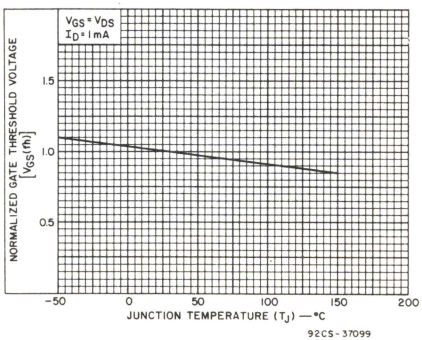


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

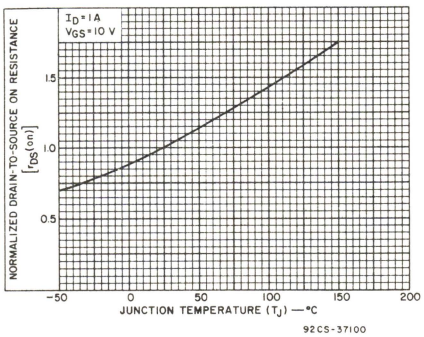


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

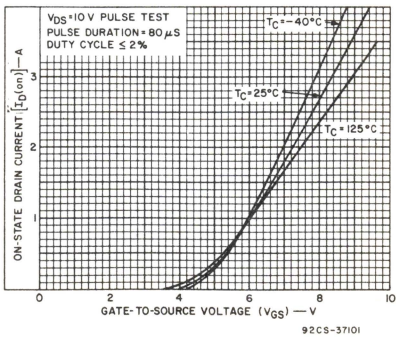


Fig. 5 — Typical transfer characteristics for all types.

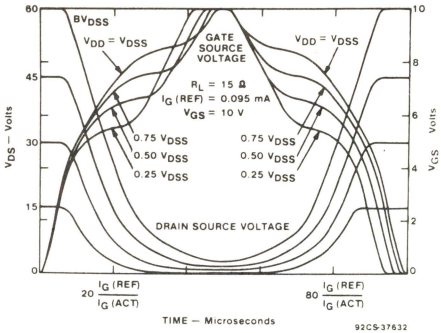


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

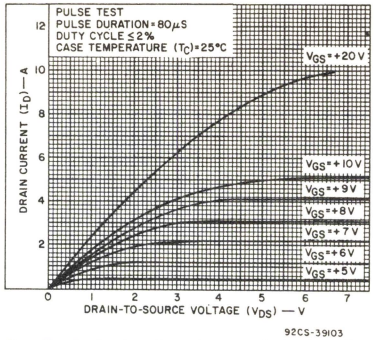


Fig. 7 — Typical saturation characteristics for all types.

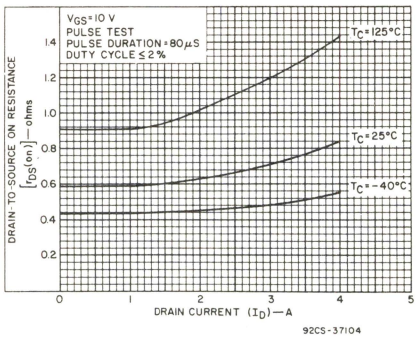


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

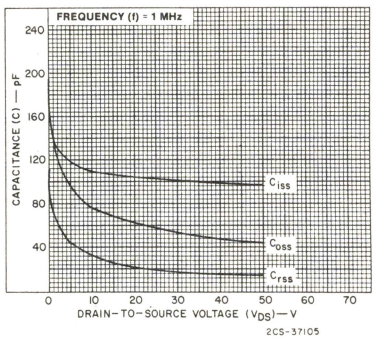


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

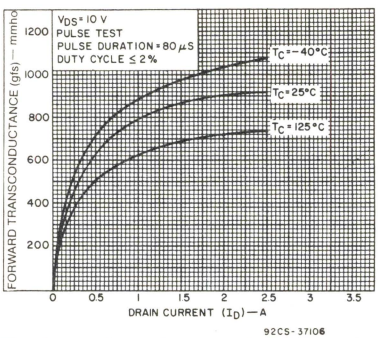


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

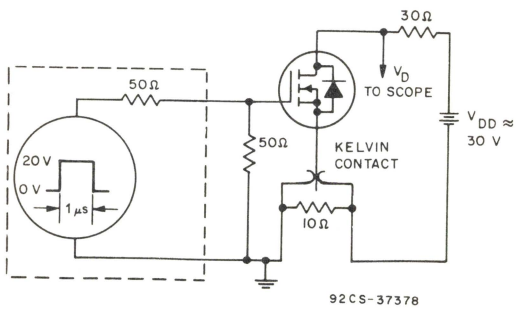


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP2N08
RFP2N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 2A, 80V and 100V
- $r_{DS}(on) = 1.05\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

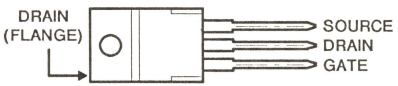
Description

The RFP2N08 and RFP2N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP-types are supplied in the JEDEC TO-220AB plastic package.

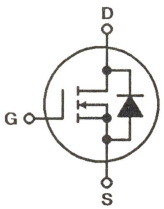
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP2N08	RFP2N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
RMS Continuous Drain Current				
T_C = +25°C	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-to-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
T_C > +25°C		0.2	0.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2883

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N08		RFP2N10		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	μA
		V_{DS} = 80V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 65V	–	50	–	–	μA
		V_{DS} = 80V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.05	–	1.05	V
		I_D = 2A, V_{GS} = 10V	–	3.0	–	3.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.05	–	1.05	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		17 (typ)	25	17 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N08		RFP2N10		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

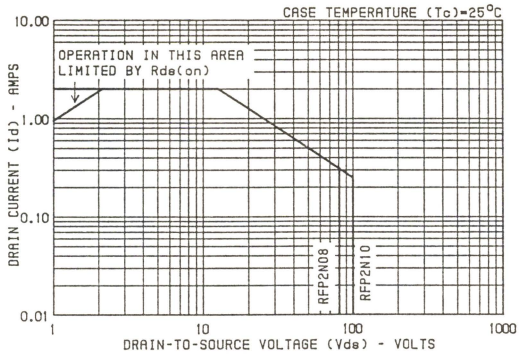


Fig. 1 - Maximum operating areas for all types.

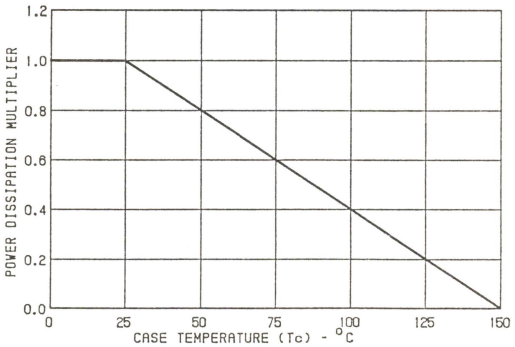


Fig. 2 - Normalized power dissipation vs. temperature derating curve

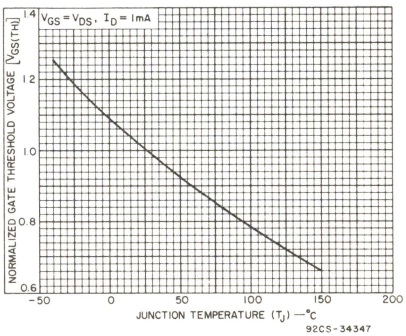


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

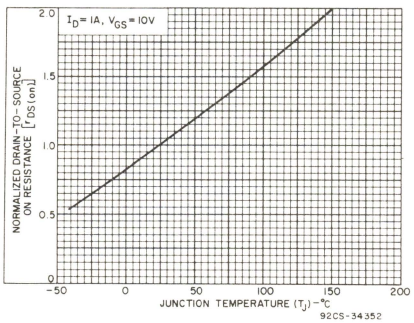


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

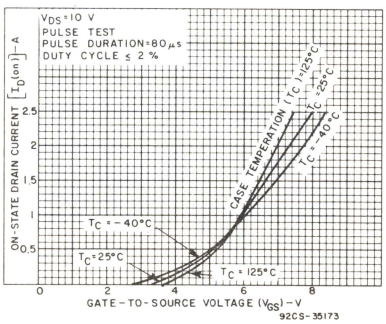


Fig. 5 - Typical transfer characteristics for all types.

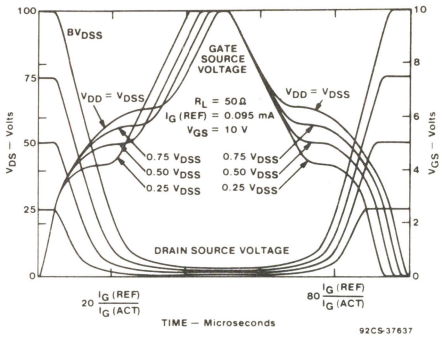


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

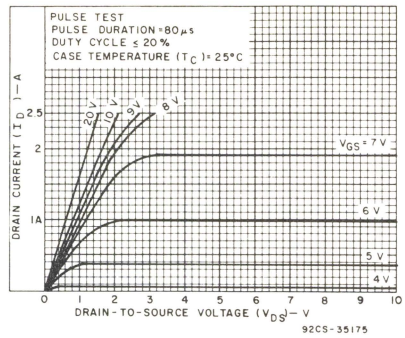


Fig. 7 - Typical saturation characteristics for all types.

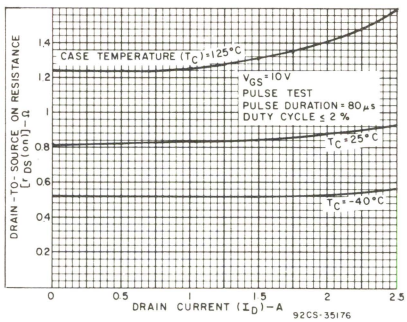


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

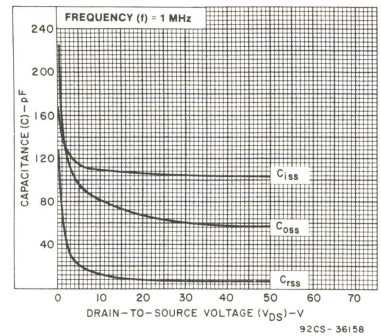


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

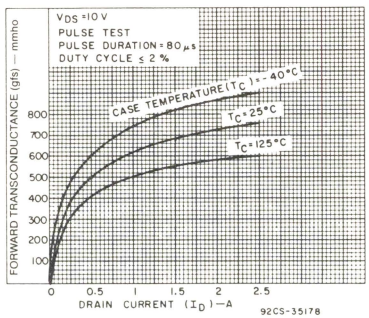


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

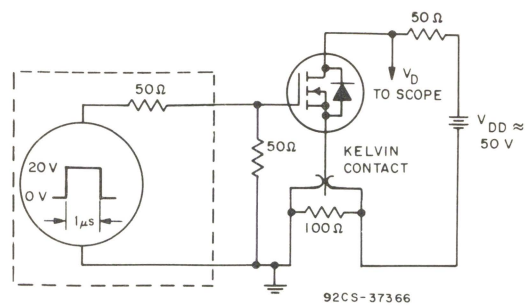


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFP2N12
RFP2N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 2A, 120V and 150V
- $r_{DS}(on)$ = 1.75Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

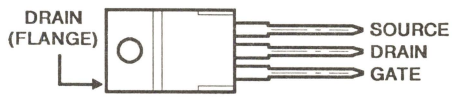
Description

The RFP2N12 and RFP2N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

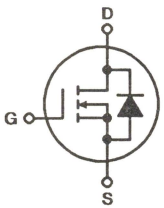
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP2N12	RFP2N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
Derate Above T_C = +25°C		0.2	0.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2882

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N12		RFP2N15		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	–	150	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	–	1	–	–	μA
		V_{DS} = 120V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 100V	–	50	–	–	μA
		V_{DS} = 120V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.75	–	1.75	V
		I_D = 2A, V_{GS} = 10V	–	6.0	–	6.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.75	–	1.75	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		17 (typ)	25	17 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N12		RFP2N15		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

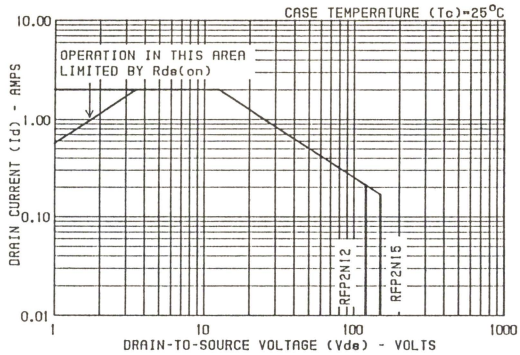


Fig. 1 — Maximum operating areas for all types.

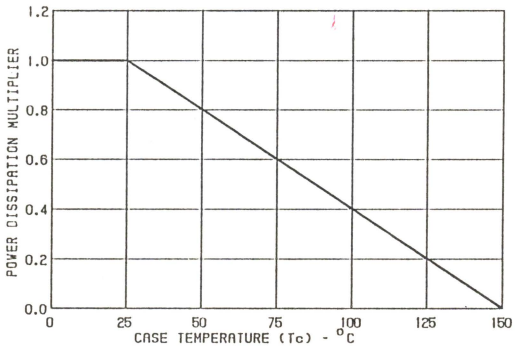


Fig. 2 - Normalized power dissipation vs temperature derating curve.

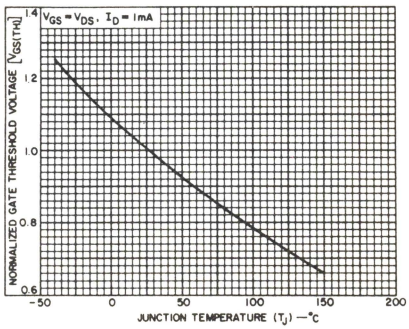


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

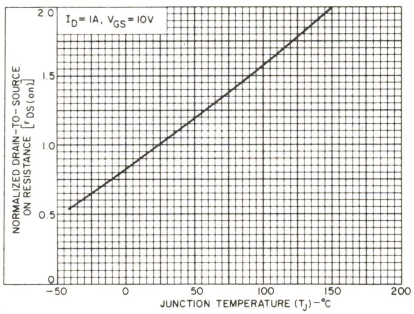


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

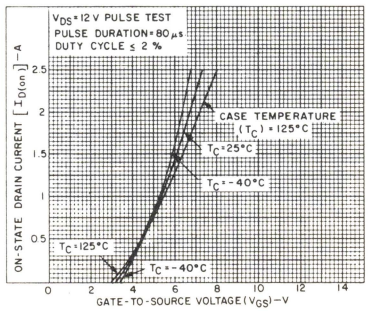


Fig. 5 — Typical transfer characteristics for all types.

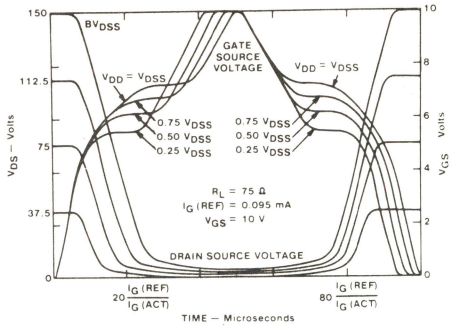


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

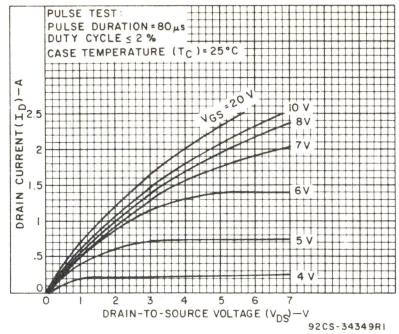


Fig. 7 — Typical saturation characteristics for all types.

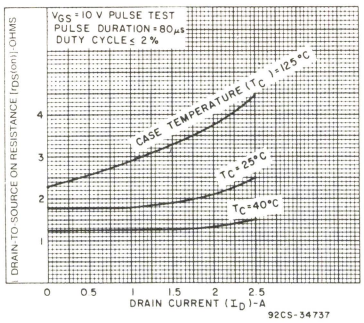


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

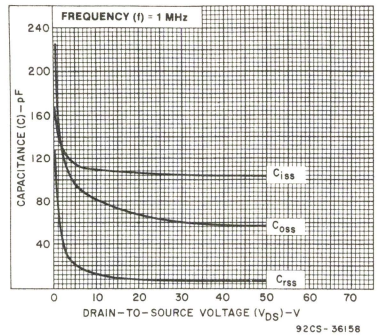


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

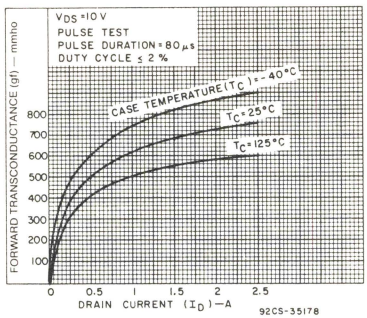


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

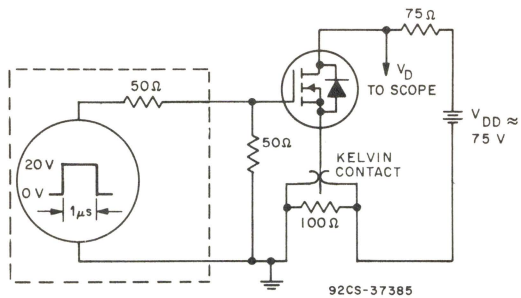


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP2N18
RFP2N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 2A, 180V and 200V
- $r_{DS}(on) = 3.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

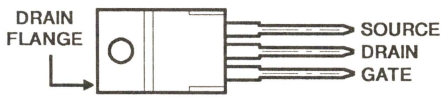
Description

The RFP2N18 and RFP2N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

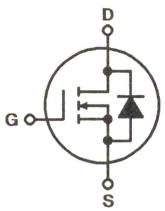
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP2N18	RFP2N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
Derate Above T_C = +25°C		0.2	0.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2881

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N18		RFP2N20		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	–	200	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	–	1	–	–	μA
		V_{DS} = 160V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 145V	–	50	–	–	μA
		V_{DS} = 160V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.5	–	3.5	V
		I_D = 2A, V_{GS} = 10V	–	8.0	–	8.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	3.5	–	3.5	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	60	–	60	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	15 (typ)	25	15 (typ)	25	ns
Rise Time	t_r		20 (typ)	30	20 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		15 (typ)	25	15 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N18		RFP2N20		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = –1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

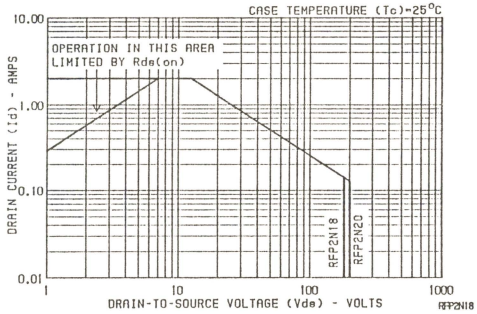


Fig. 1 - Maximum operating areas for all types.

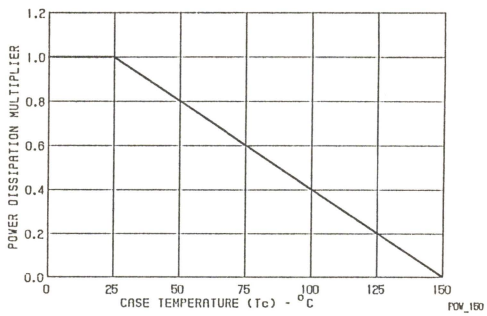


Fig. 2 – Normalized power dissipation vs temperature derating curve.

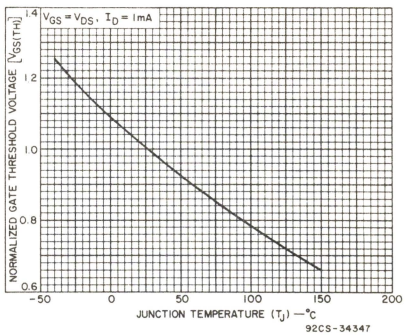


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

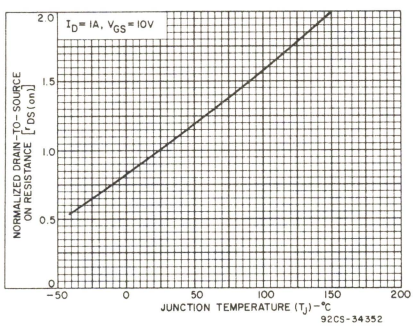


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

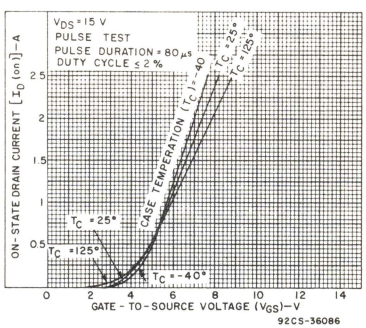


Fig. 5 - Typical transfer characteristics for all types.

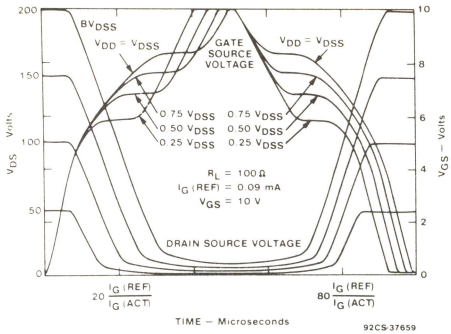


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

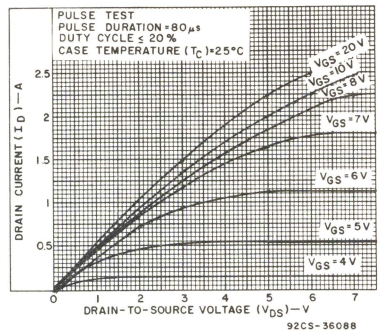


Fig. 7 - Typical saturation characteristics for all types.

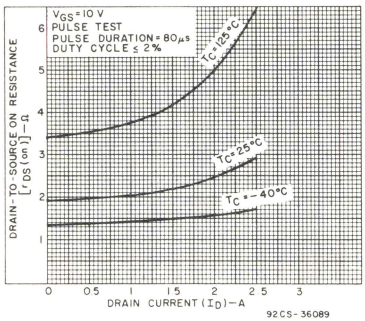


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

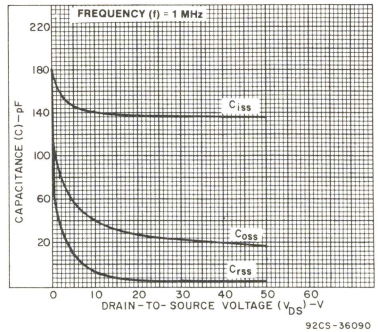


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

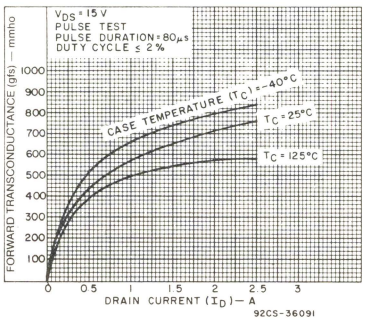


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

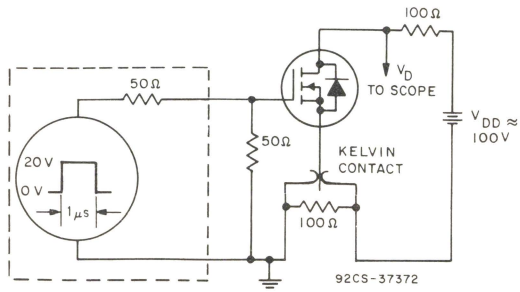


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFM3N45/3N50
RFP3N45/3N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 3A, 450V and 500V
- $r_{DS(on)} = 3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

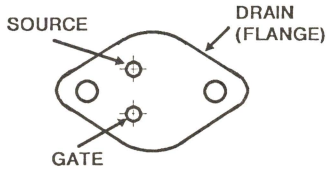
Description

The RFM3N45 and RFM3N50 and the RFP3N45 and RFP3N50 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

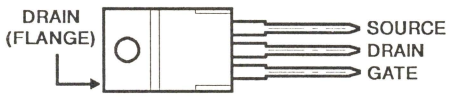
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

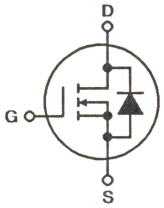


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM3N45	RFM3N50	RFP3N45	RFP3N50	UNITS
Drain-Source Voltage ..... V_{DSS}	450	500	450	500	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	450	500	450	500	V
Continuous Drain Current					
RMS Continuous ..... I_D	3	3	3	3	A
Pulsed Drain Current ..... I_{DM}	5	5	5	5	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly ..... P_D	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1384.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS}=0	450	—	500	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V	—	10	—	—	μA
		V_{DS}=400 V	—	—	—	10	
		T_C=125°C V_{DS}=360 V	—	50	—	—	
		V_{DS}=400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm$20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	4.5	—	4.5	V
		I_D=3 A V_{GS}=10 V	—	10.5	—	10.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	3	—	3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=1.5 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	750	—	750	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	150	—	150	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=250 V	30(Typ)	45	30(Typ)	45	ns
Rise Time	t_r	I_D=1.5 A	40(Typ)	60	40(Typ)	60	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	90(Typ)	135	90(Typ)	135	
Fall Time	t_f	V_{GS}=10 V	50(Typ)	75	50(Typ)	75	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM3N45, RFM3N50	—	1.67	—	1.67	°C/W
		RFP3N45, RFP3N50	—	2.083	—	2.083	

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

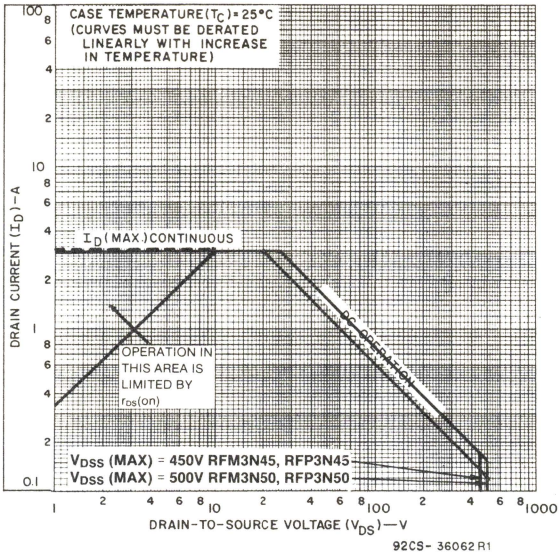


Fig. 1 - Maximum operating areas for all types.

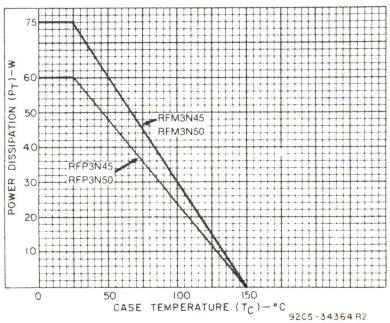


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

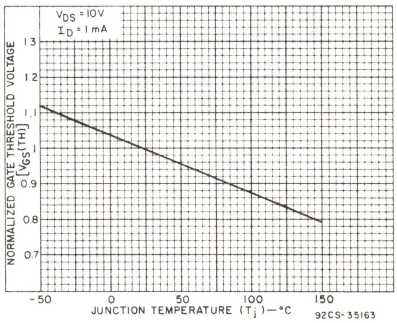


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

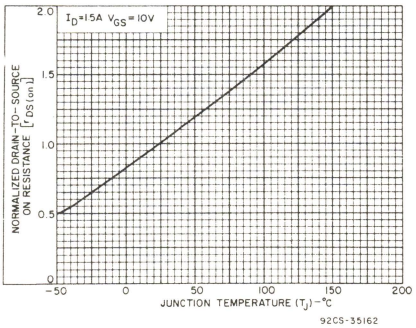


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

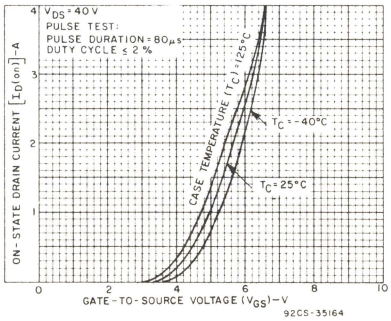


Fig. 5 - Typical transfer characteristics for all types.

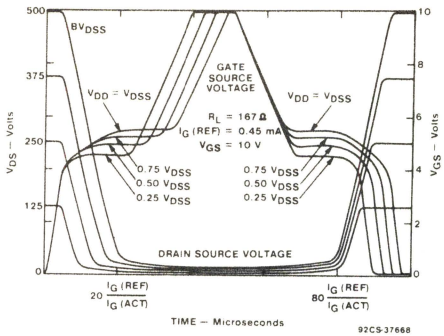


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

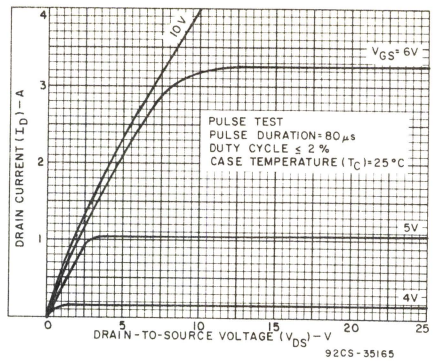


Fig. 7 - Typical saturation characteristics for all types.

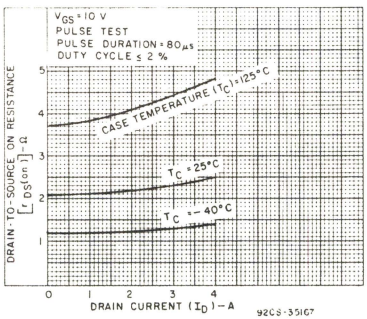


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

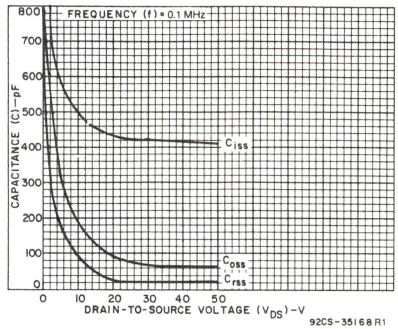


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

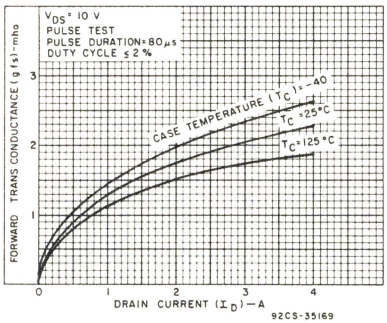


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

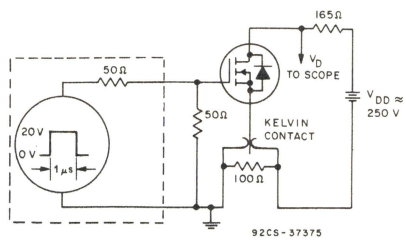


Fig. 11 — Switching Time Test Circuit

HARRIS

RFP4N05
RFP4N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4A, 50V and 60V
- $R_{DS(ON)}$ = 0.8W
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

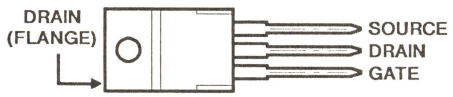
Description

The RFP4N05 and RFP4N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP-series types are supplied in the JEDEC TO-220AB plastic package.

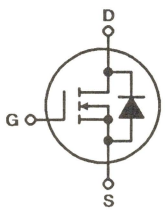
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP4N05	RFP4N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Continuous Drain Current	I_D	4	4	A
Pulsed Drain Current	I_{DM}	10	10	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	25	25	W
Linear Derating Factor		0.2	0.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2880

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP4N05		RFP4N06		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 1mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.8	–	0.8	V
		I_D = 2A, V_{GS} = 10V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 10V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	0.8	–	0.8	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	85	–	85	pF
Reverse-Transfer Capacitance	C_{RSS}		–	30	–	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, $R_{GEN} = R_{GS}$ = 50Ω, V_{GS} = 10V	6 (typ)	15	6 (typ)	15	ns
Rise Time	t_r		14 (typ)	30	14 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		16 (typ)	30	16 (typ)	30	ns
Fall Time	t_f		14 (typ)	25	14 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP4N05		RFP4N06		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration ≤ 300μs max., duty cycle ≤ 2%.

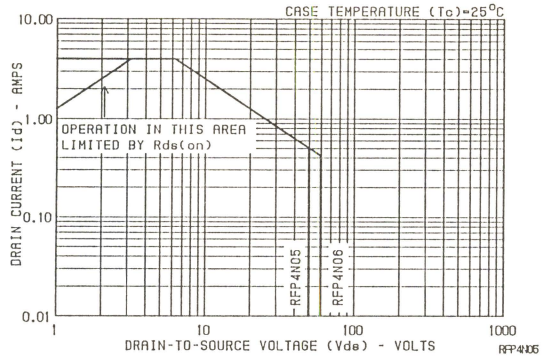


Fig. 1 — Maximum operating areas for all types.

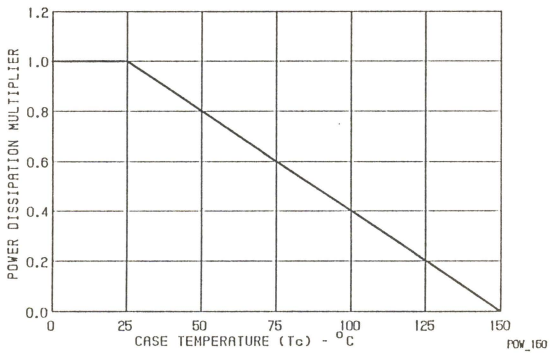


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

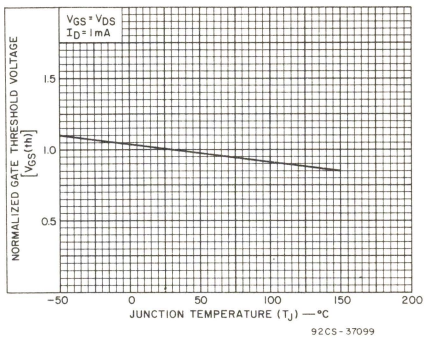


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

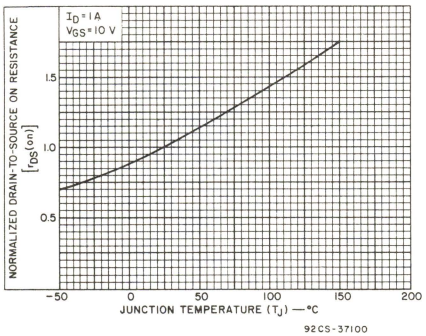


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

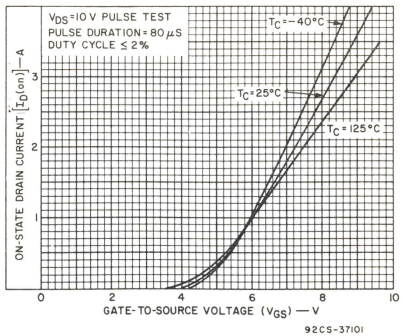


Fig. 5 — Typical transfer characteristics for all types.

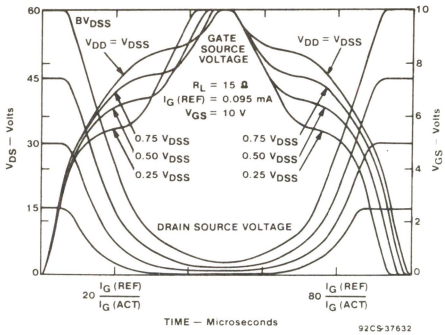


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

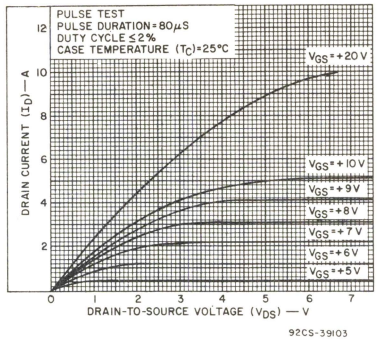


Fig. 7 — Typical saturation characteristics for all types.

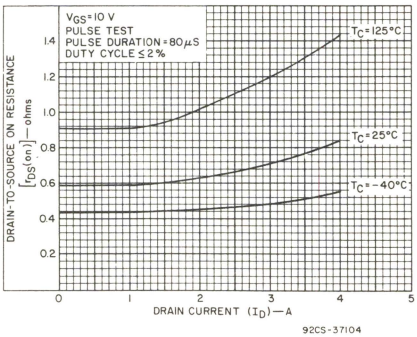


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

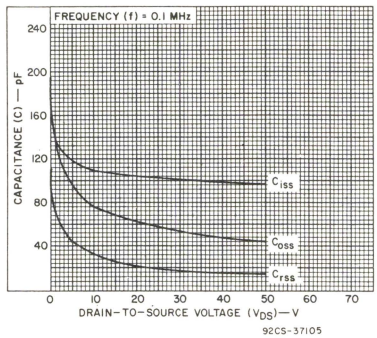


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types

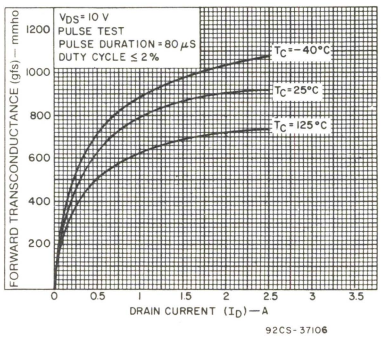


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

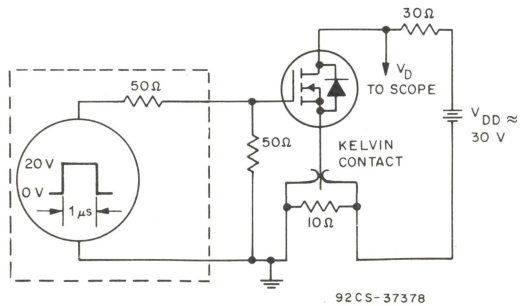


Fig. 11 — Switching Time Test Circuit

HARRIS

RFL4N12
RFL4N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

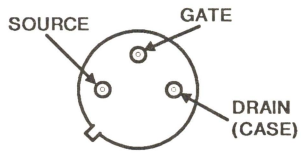
August 1991

Features

- 4A, 120V and 150V
- $r_{DS}(on) = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Package

TO-205AF
BOTTOM VIEW



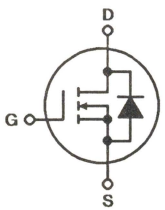
Description

The RFL4N12 and RFL4N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL4N12	RFL4N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current				
T_C = +25°C	I_D	4	4	A
Pulsed Drain Current	I_{DM}	15	15	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	8.33	8.33	W
Linear Derating Factor		0.0667	0.0667	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1462.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125°C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D=2 A V_{GS}=10 V	—	0.8	—	0.8	V
		I_D=4 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D=2 A V_{GS}=10 V	—	0.40	—	0.40	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	230	—	230	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 75 V	40(typ)	60	40(typ)	60	ns
Rise Time	t_r	I_D=2 A	165(typ)	250	165(typ)	250	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen}=R_{gs}=50 Ω	90(typ)	135	90(typ)	135	
Fall Time	t_f	V_{GS}=10 V	90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL4N12, RFL4N15	—	15	—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 2A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

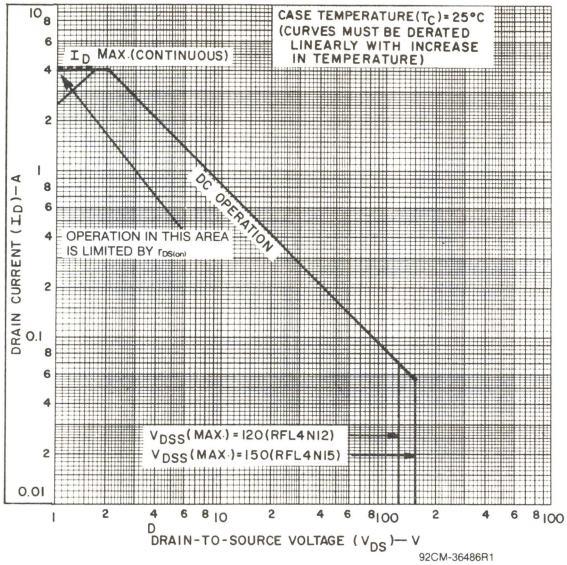


Fig. 1 - Maximum safe operating areas for all types.

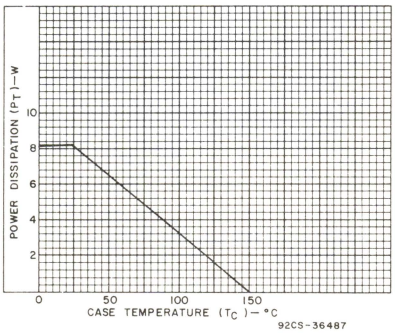


Fig. 2 - Power vs. temperature derating curve for all types.

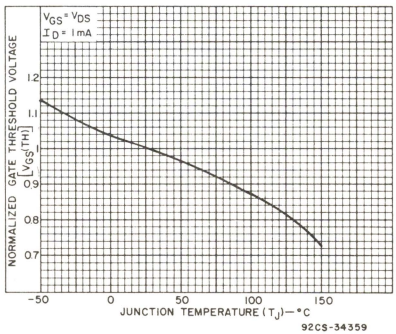


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

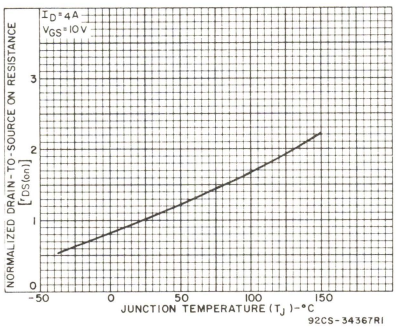


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

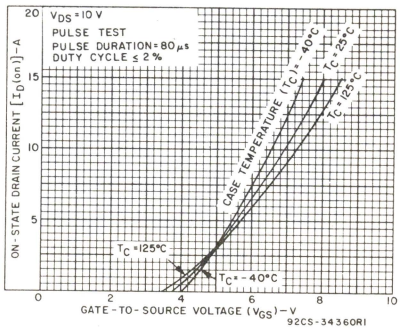


Fig. 5 - Typical transfer characteristics for all types.

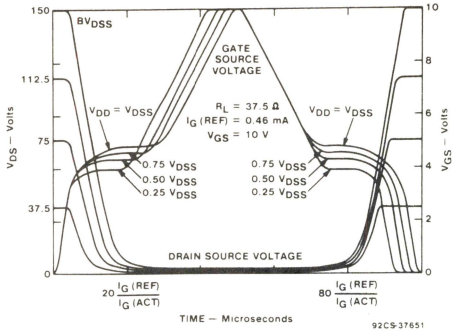


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

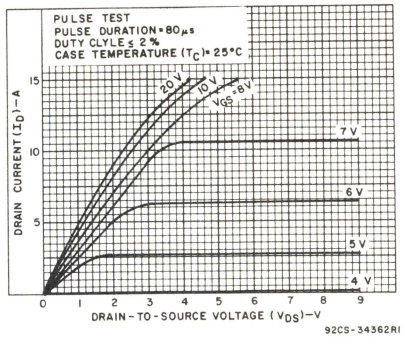


Fig. 7 - Typical saturation characteristics for all types.

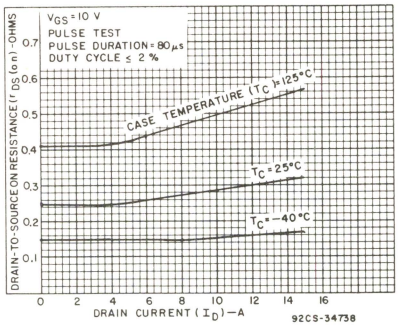


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

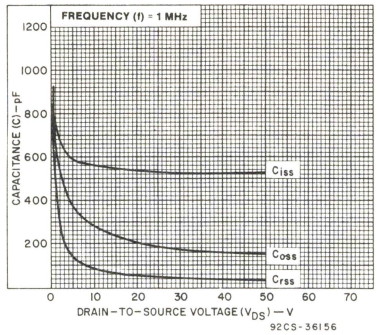


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

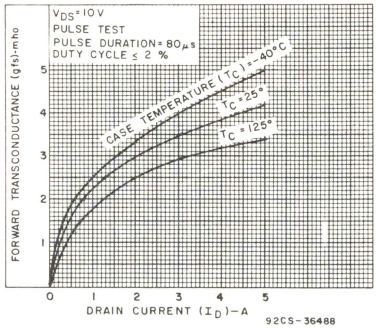


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

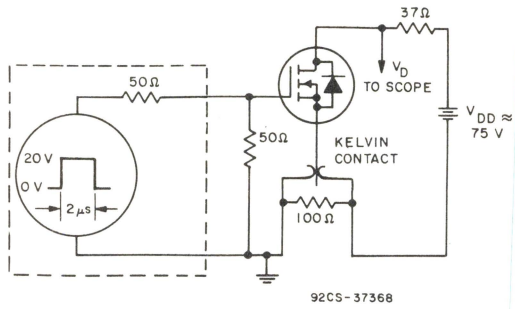


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM4N35/4N40
RFP4N35/4N40

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 4A, 350V and 400V
- $r_{DS(on)} = 2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

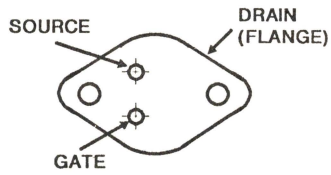
Description

The RFM4N35 and RFM4N40 and the RFP4N35 and RFP4N40 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

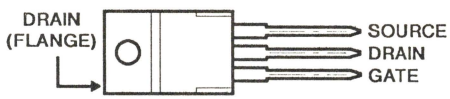
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

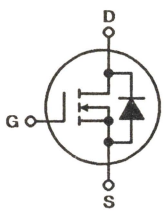


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM4N35	RFM4N40	RFP4N35	RFP4N40	UNITS
Drain-Source Voltage ..... V_{DSS}	350	400	350	400	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	350	400	350	400	V
Continuous Drain Current					
RMS Continuous ..... I_D	4	4	4	4	A
Pulsed Drain Current ..... I_{DM}	8	8	8	8	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	$W/^oC$
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1491.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) 25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V V_{DS}=320 V	— —	10 —	— —	— 10	μA
		T_C=125° C V_{DS}=280 V V_{DS}=320 V	— —	100 —	— —	— 100	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	4	—	4	V
		I_D=4 A V_{GS}=10 V	—	12	—	12	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	2	—	2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	750	—	750	pF
Output Capacitance	C_{oss}		—	150	—	150	pF
Reverse Transfer Capacitance	C_{rss}		—	100	—	100	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=200 V I_D=2 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	12(typ)	45	12(typ)	45	ns
Rise Time	t_r		42(typ)	60	42(typ)	60	ns
Turn-Off Delay Time	$t_d(off)$		130(typ)	200	130(typ)	200	ns
Fall Time	t_f		62(typ)	100	62(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM4N35, RFM4N40	—	1.67	—	1.67	°C/W
		RFP4N35, RFP4N40	—	2.083	—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD} [a]	I_{SD}=2 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

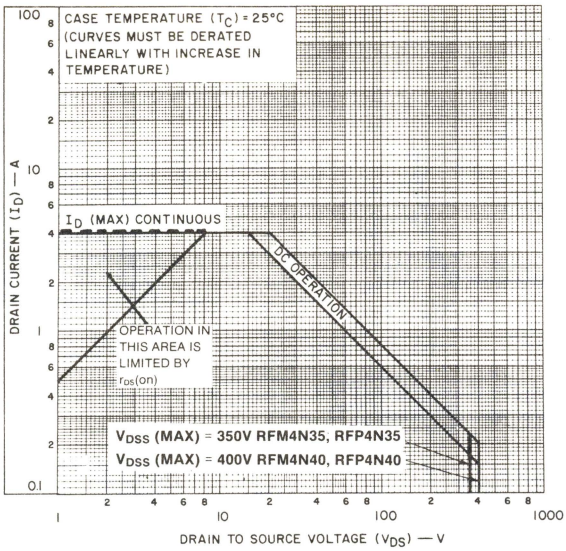


Fig. 1 — Maximum operating areas for all types.

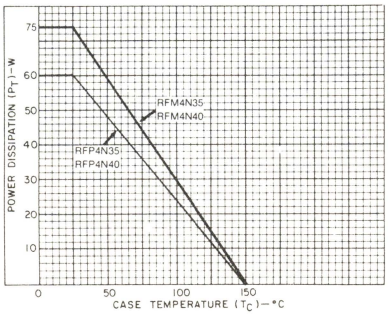


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

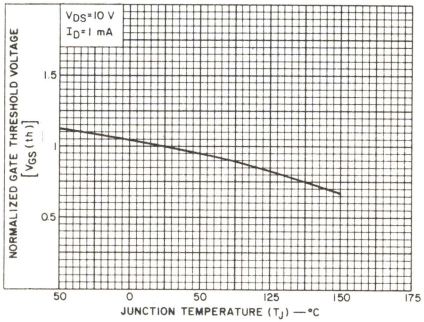


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

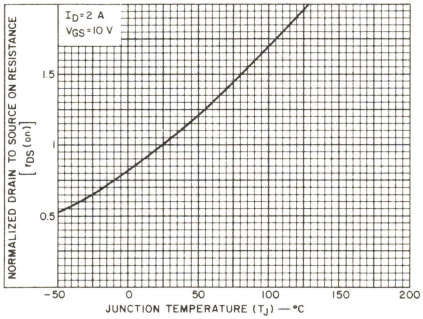


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

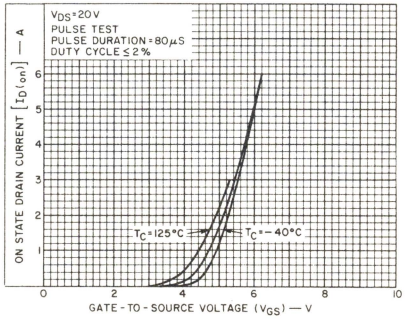


Fig. 5 — Typical transfer characteristics for all types.

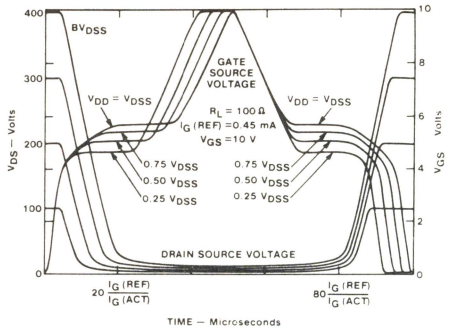


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

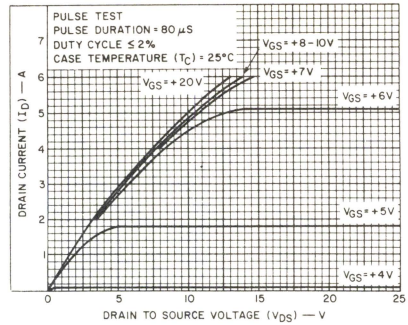


Fig. 7 — Typical saturation characteristics for all types.

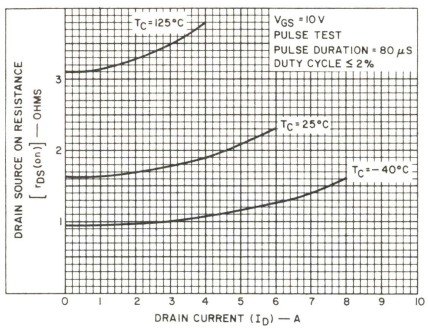


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

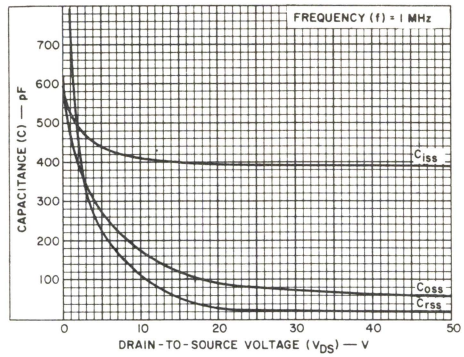


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

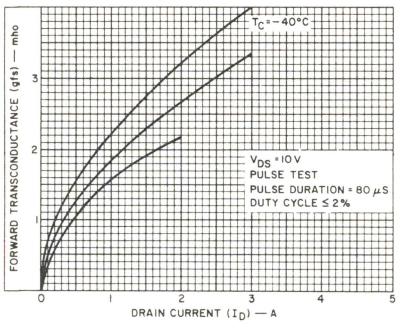


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

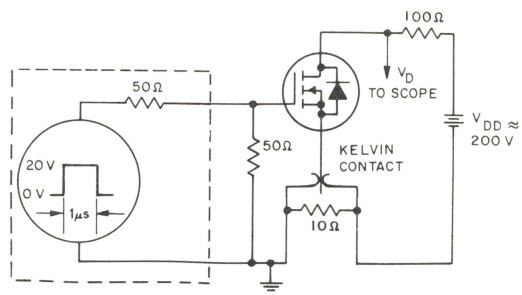


Fig. 11 — Switching Time Test Circuit

HARRIS

RFP4N100

High Voltage N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 4.3A, 1000V
- $r_{DS(on)} = 3.5\Omega$
- UIS SOA Rating Curve (Single Pulse)
- -55°C to +150°C Operating Temperature

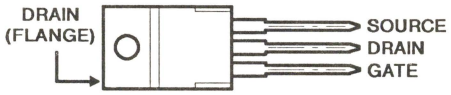
Description

The RFP4N100 is an n-channel enhancement mode silicon-gate power field effect transistor. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from an integrated circuit.

The RFP4N100 is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 1000V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR} 1000V
Gate-Source Voltage, V_{GS} ..... ±20V
Drain Current:
  RMS Continuous, I_D 4.3A
  Pulsed, I_{DM} 17A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve 490mJ
Power Dissipation, P_D:
  T_C = +25°C 150W
  Derate Above T_C = +25°C ..... 0.83W/°C
Operating and Storage Junction
Temperature Range, T_J, T_{STG} ..... -55 to +150°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.
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File Number **2457.1**

Electrical Characteristics (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	1000	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA	2.0	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V	-		µA
		V_{DS} = 1000V T_C = 25°C	-	250	µA
		V_{DS} = 800V T_C = 150°C	-	1000	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	±500	nA
On Resistance	$r_{DS(ON)}$	I_D = 2.5A, V_{GS} = 10V	-	3.5	Ω
Forward Transconductance	g_{fs}	I_D = 2.5A, V_{DS} = 100V	3.5	-	S (℧)
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 500V, I = 3.9A	-	30	ns
Rise Time	t_r	R_G = 9.1Ω	-	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$	R_D = 120Ω	-	170	ns
Fall Time	t_f	See Figure 14	-	50	ns
Total Gate Charge	Q_g	I_D = 3.9A, V_{DS} = 800V, V_{GS} = 10V	-	120	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	0.83	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 4.3A	-	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 3.9A, d_{IF}/dT = 100 A/µs	-	1000	ns

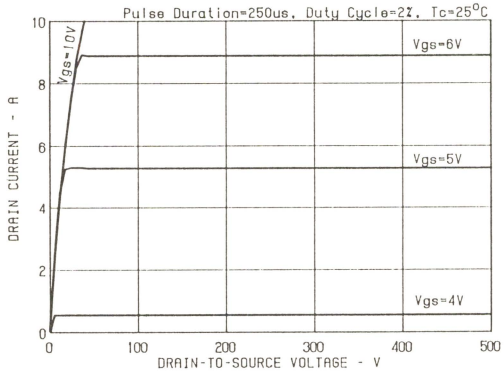


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

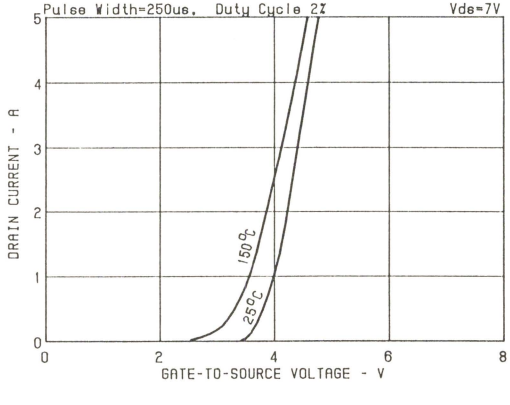


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

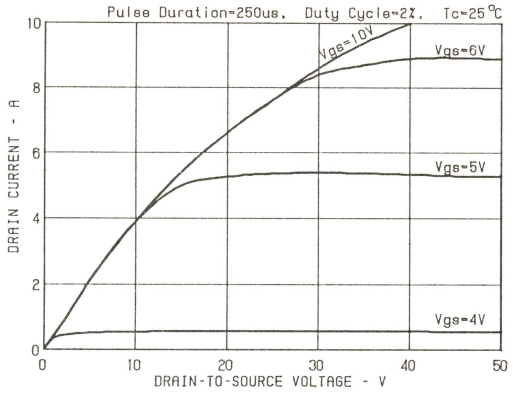


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

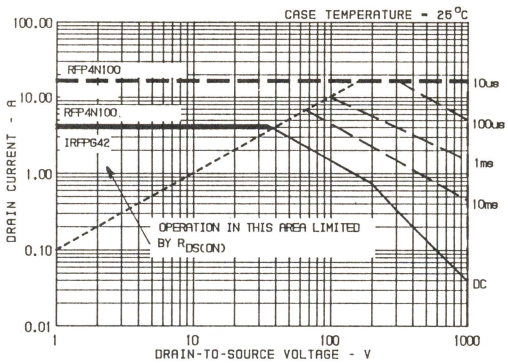


FIGURE 4. MAXIMUM SAFE OPERATING AREA

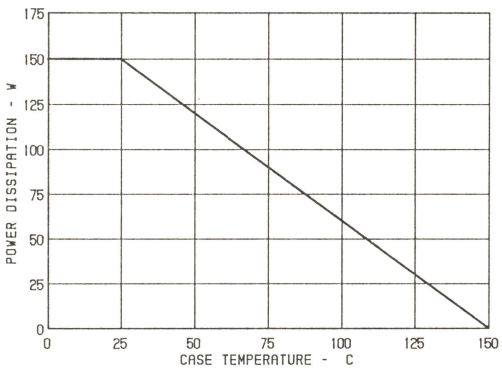


FIGURE 5. POWER vs. TEMPERATURE DERATING CURVE

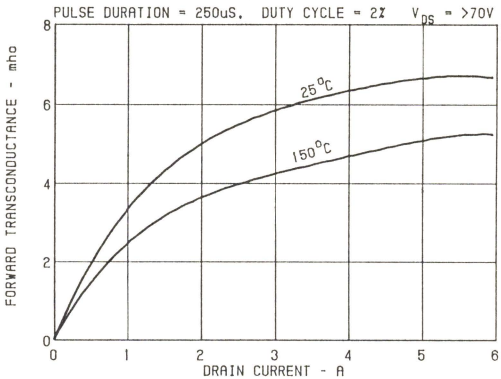


FIGURE 6. TYPICAL FORWARD TRANSCONDUCTANCE

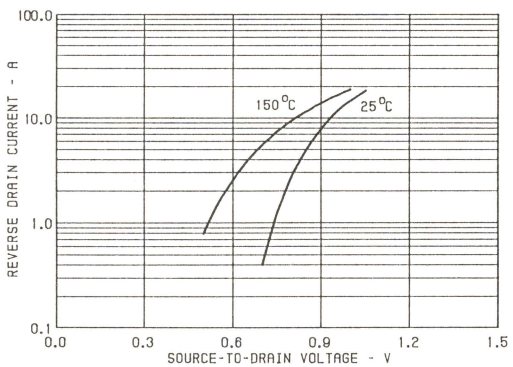


FIGURE 7. TYPICAL SOURCE-TO-DRAIN DIODE FORWARD VOLTAGE

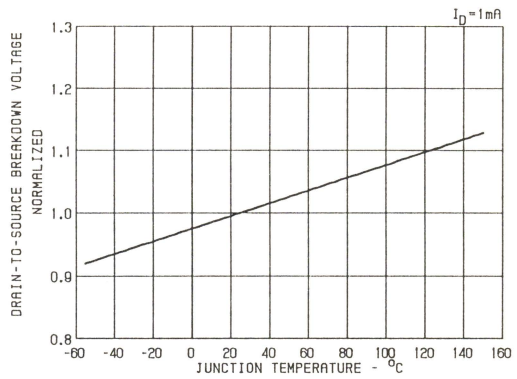


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

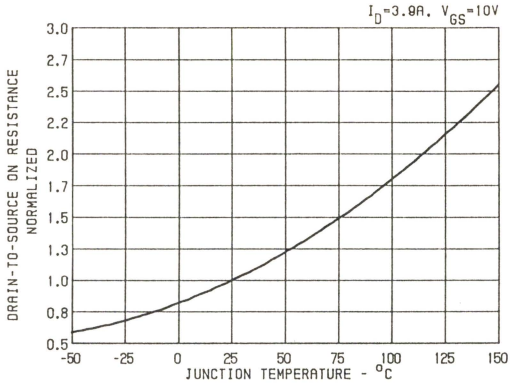


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE ON RESISTANCE

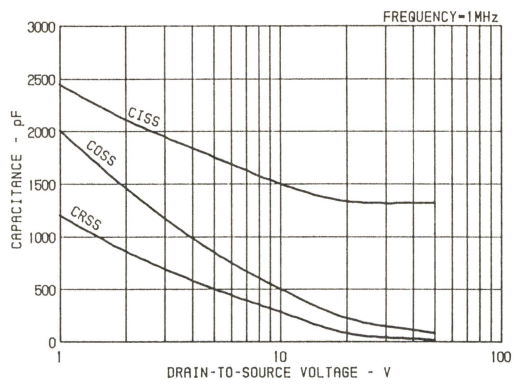


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

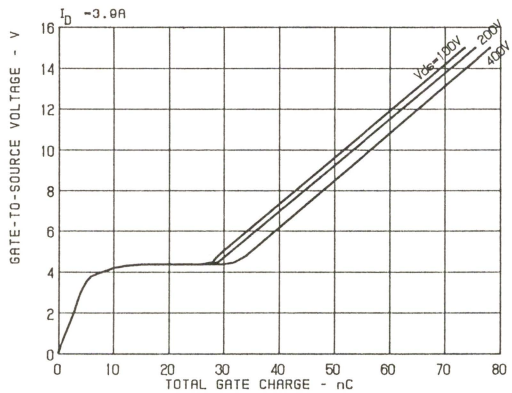


FIGURE 11. TYPICAL GATE CHARGE

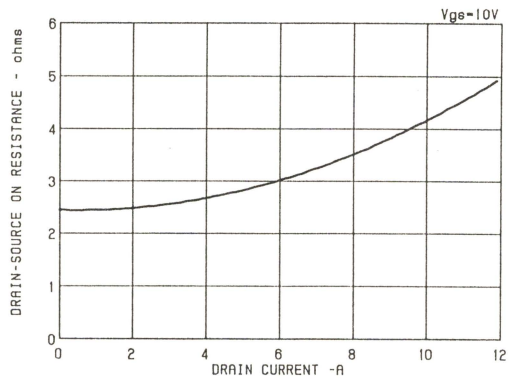


FIGURE 12. TYPICAL DRAIN-SOURCE ON RESISTANCE

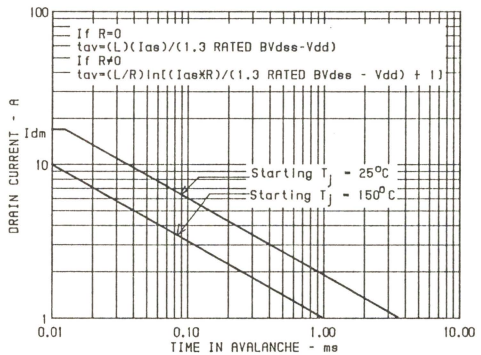


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING SOA

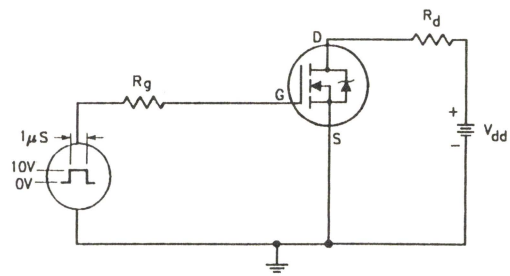


FIGURE 14. SWITCHING TIME TEST CIRCUIT

HARRIS

RFM6N45/6N50
RFP6N45/6N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 6A, 450V and 500V
- $r_{DS(on)} = 1.25\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

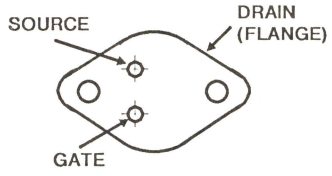
Description

The RFM6N45 and RFM6N50 and the RFP6N45 and RFP6N50 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

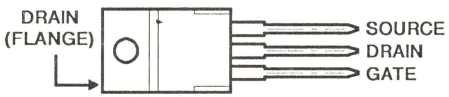
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

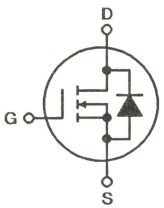


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM6N45	RFM6N50	RFP6N45	RFP6N50	UNITS
Drain-Source Voltage ..... V_{DSS}	450	500	450	500	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	450	500	450	500	V
Continuous Drain Current					
RMS Continuous ..... I_D	6	6	6	6	A
Pulsed Drain Current ..... I_{DM}	15	15	15	15	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1494.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V V_{DS}=400 V	— —	10 —	— —	— 10	μA
		T_C=125° C V_{DS}=360 V V_{DS}=400 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	3.75	—	3.75	V
		I_D=6 A V_{GS}=10 V	—	12	—	12	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	1.25	—	1.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	250	—	250	pF
Reverse Transfer Capacitance	C_{rss}	f=1 MHz	—	200	—	200	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 250 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r	I_D=3 A	40(typ)	80	40(typ)	80	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	190(typ)	300	190(typ)	300	ns
Fall Time	t_f	V_{GS}=10 V	60(typ)	100	60(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6N45, RFM6N50	—	1.25	—	1.25	°C/W
		RFP6N45, RFP6N50	—	1.67	—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} [a]	I_{SD} = 3A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	800(typ.)		800(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

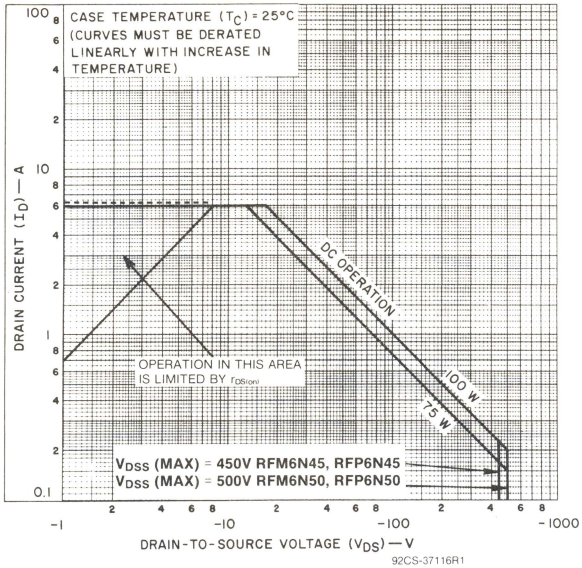


Fig. 1 — Maximum operating areas for all types.

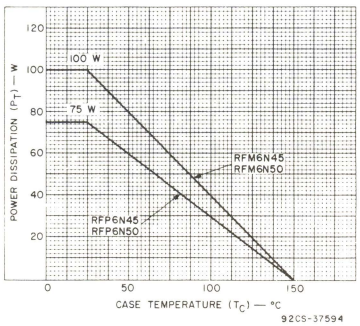


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

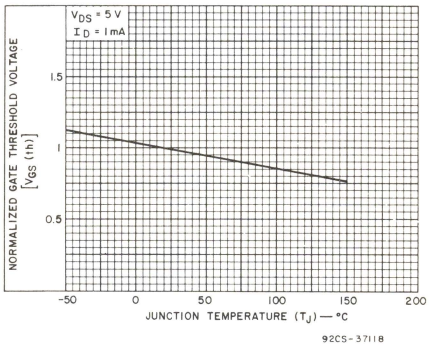


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

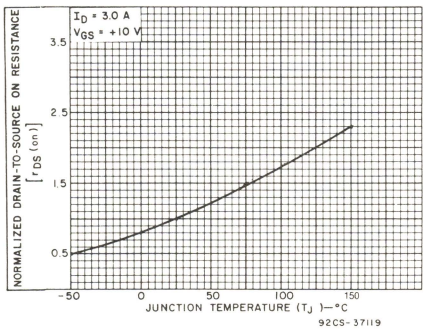


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

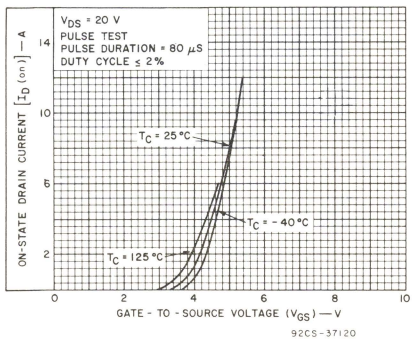


Fig. 5 — Typical transfer characteristics for all types.

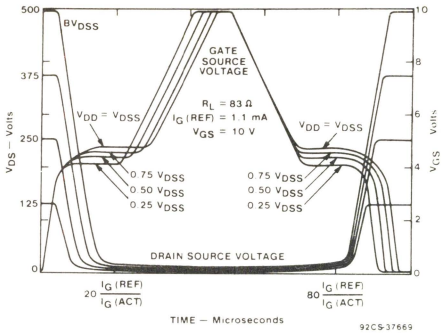


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

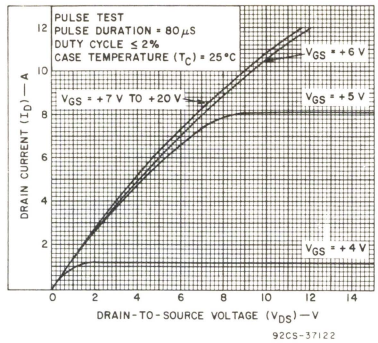


Fig. 7 — Typical saturation characteristics for all types.

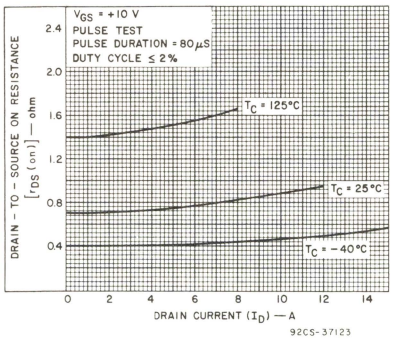


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

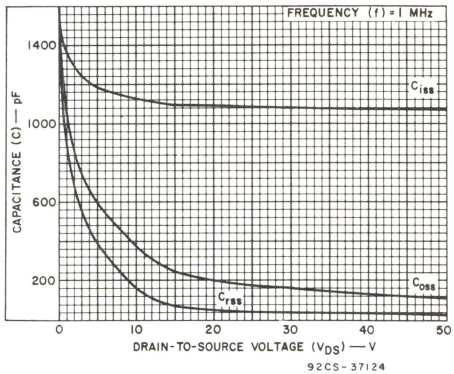


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

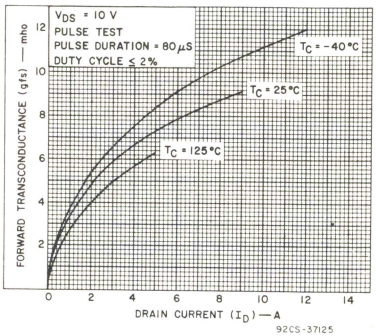


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

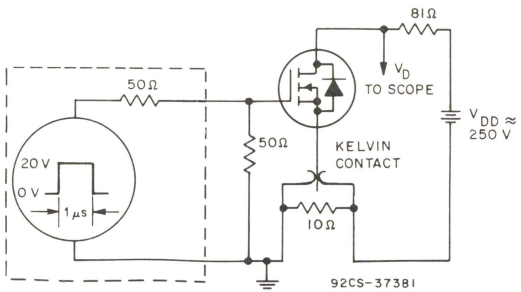


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFM7N35/7N40
RFP7N35/7N40

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 7A, 350V and 400V
- $r_{DS(on)} = 0.75\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

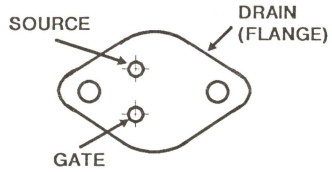
Description

The RFM7N35 and RFM7N40 and the RFP7N35 and RFP7N40 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

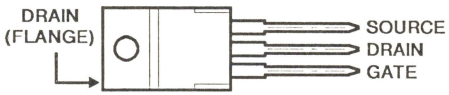
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

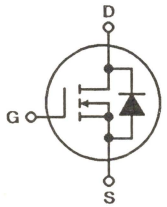


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM7N35	RFM7N40	RFP7N35	RFP7N40	UNITS
Drain-Source Voltage ..... V_{DSS}	350	400	350	400	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	350	400	350	400	V
Continuous Drain Current					
RMS Continuous ..... I_D	7	7	7	7	A
Pulsed Drain Current ..... I_{DM}	15	15	15	15	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	$W/^oC$
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1536.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V	—	1	—	—	μA
		V_{DS}=320 V	—	—	—	1	
		T_C=125° C V_{DS}=280 V	—	50	—	—	
		V_{DS}=320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D=3.5 A V_{GS}=10 V	—	2.63	—	2.63	V
		I_D=7 A V_{GS}=10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D=3.5 A V_{GS}=10 V	—	0.75	—	0.75	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1600	—	1600	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f= 1 MHz	—	200	—	200	
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=200 V	16(typ)	45	16(typ)	45	ns
Rise Time	t_r	I_D=3.5 A	54(typ)	75	54(typ)	75	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen}=R_{gs}=50 Ω	170(typ)	250	170(typ)	250	
Fall Time	t_f	V_{GS}=10 V	62(typ)	100	62(typ)	100	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM7N35, RFM7N40	—	1.25	—	1.25	°C/W
		RFP7N35, RFP7N40	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=3.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A di_F/dt=100 A/μs	870 (typ)				ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

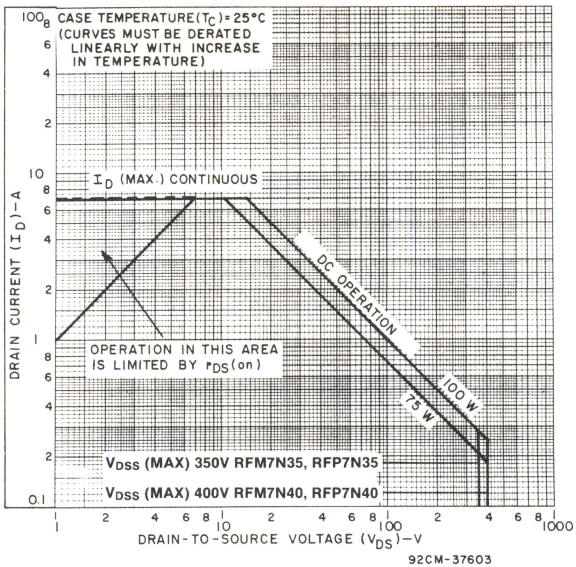


Fig. 1 - Maximum safe operating areas for all types.

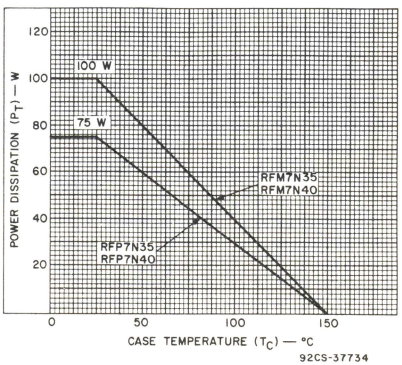


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

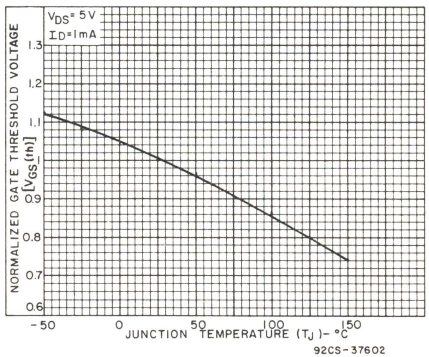


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

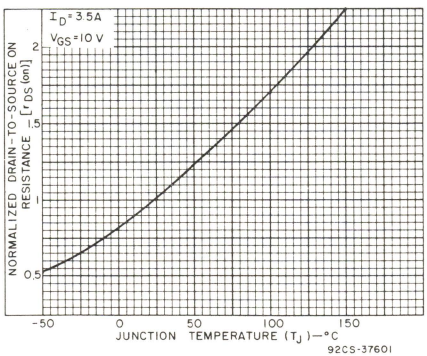


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

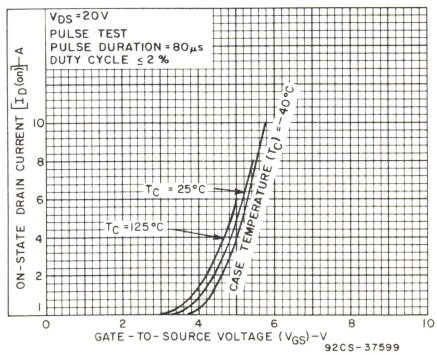


Fig. 5 - Typical transfer characteristics for all types.

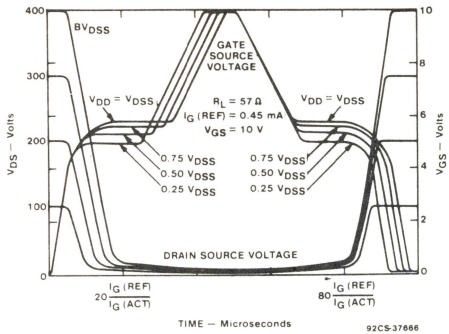


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

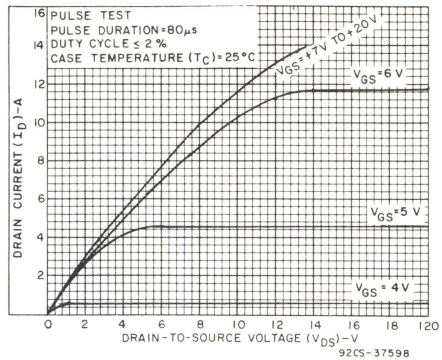


Fig. 7 - Typical saturation characteristics for all types.

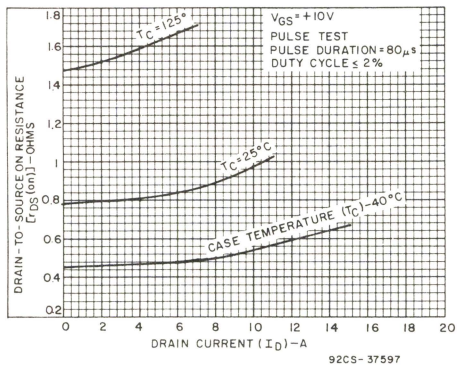


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

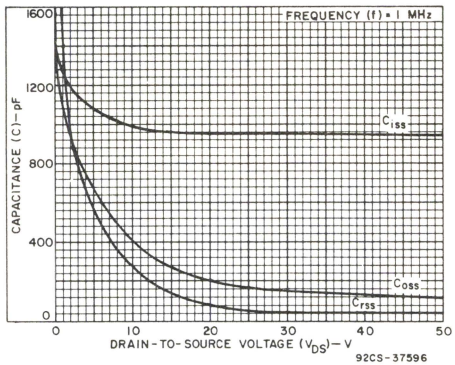


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

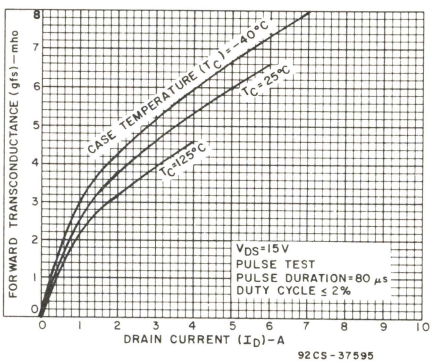


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

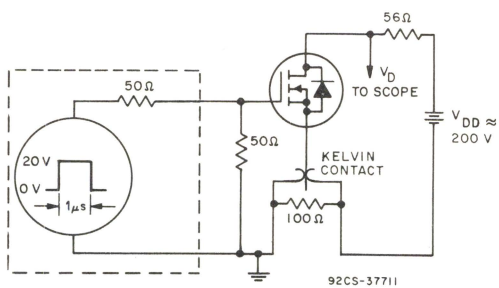


Fig. 11 - Switching time test circuit.

HARRIS

RFM10N12/10N15
RFP10N12/10N15

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 10A, 120V and 150V
- $r_{DS(on)} = 0.3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

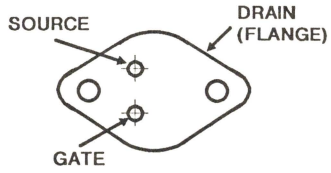
Description

The RFM10N12 and RFM10N15 and the RFP10N12 and RFP10N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

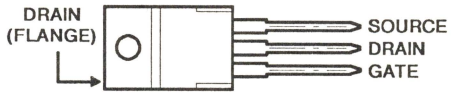
The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

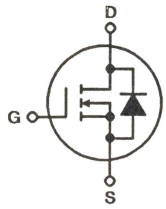


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM10N12	RFM10N15	RFP10N12	RFP10N15	UNITS
Drain-Source Voltage ..... V_{DSS}	120	150	120	150	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	120	150	120	150	V
Continuous Drain Current					
RMS Continuous ..... I_D	10	10	10	10	A
Pulsed Drain Current ..... I_{DM}	25	25	25	25	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1445.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM10N12 RFP10N12 MIN.	LIMITS RFM10N12 RFP10N12 MAX.	LIMITS RFM10N15 RFP10N15 MIN.	LIMITS RFM10N15 RFP10N15 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 100 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	1.5	—	1.5	V
		I_D = 10 A, V_{GS} = 10 V	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	230	—	230	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V	40(typ.)	60	40(typ.)	60	ns
Rise Time	t_r	I_D = 5 A	165(typ.)	250	165(typ.)	250	
Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	90(typ.)	135	90(typ.)	135	
Fall Time	t_f	V_{GS} = 10 V	90(typ.)	135	90(typ.)	135	
Thermal Resistance Junction-to-Case	RθJC	RFM10N12, RFM10N15	—	1.67	—	1.67	°C/W
		RFP10N12, RFP10N15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM10N12 RFP10N12 MIN.	LIMITS RFM10N12 RFP10N12 MAX.	LIMITS RFM10N15 RFP10N15 MIN.	LIMITS RFM10N15 RFP10N15 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

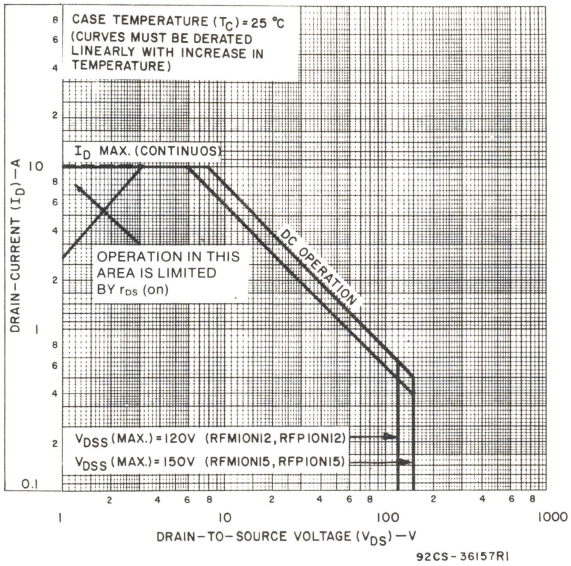


Fig. 1 — Maximum safe operating areas for all types.

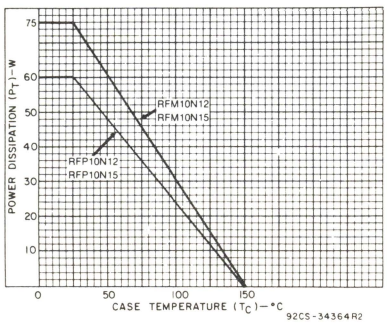


Fig. 2 — Power vs. temperature derating curve for all types.

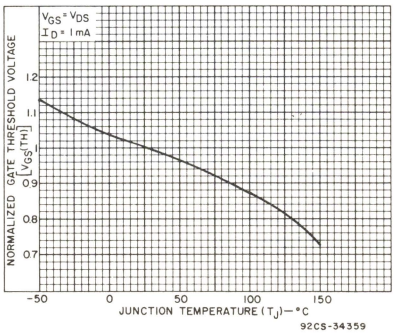


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

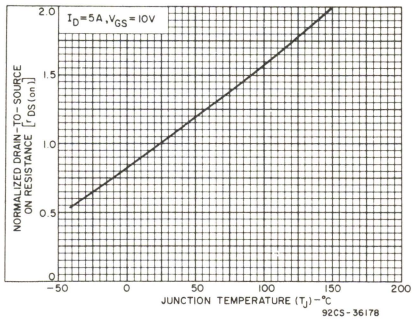


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

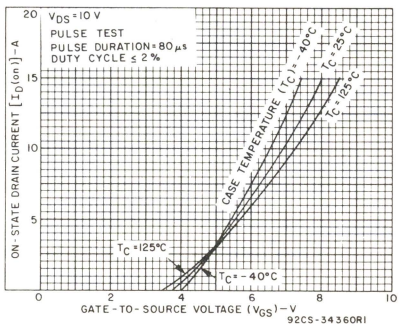


Fig. 5 — Typical transfer characteristics for all types.

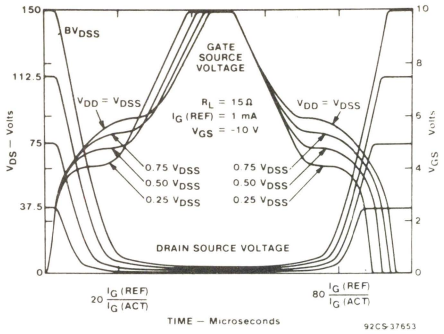


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

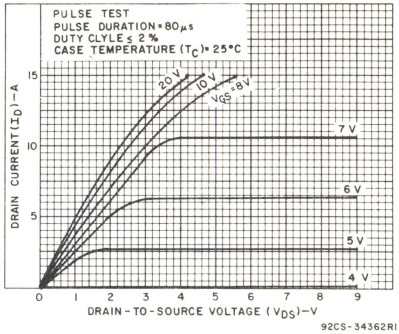


Fig. 7 — Typical saturation characteristics for all types.

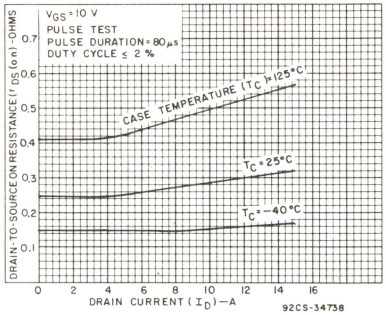


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

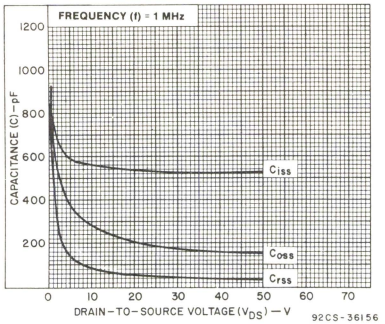


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

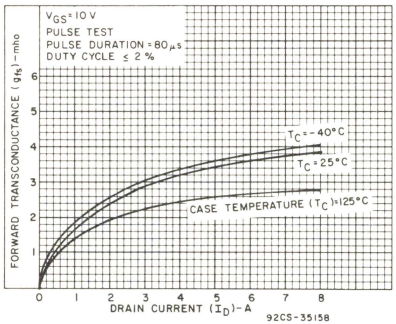


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

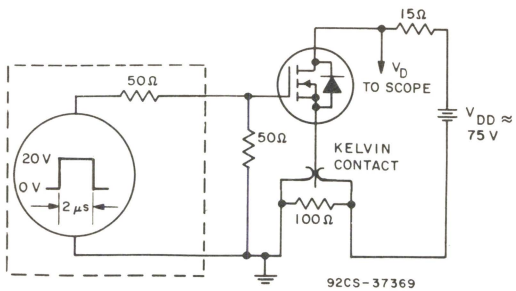


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH10N45
RFH10N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 10A, 450V and 500V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

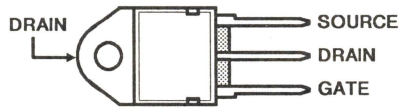
Description

The RFH10N45 and RFH10N50 n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The RFH types are supplied in the JEDEC TO-218AC plastic package.

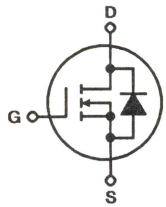
Packages

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		RFH10N45	RFH10N50	UNITS
Drain-Source Voltage	V_{DSS}	450	500	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	450	500	V
Continuous Drain Current				
RMS Continuous	I_D	10	10	A
Pulsed Drain Current	I_{DM}	20	20	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Above T_C = +25°C, Derate Linearly		1.2	1.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1629.1

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V	—	1	—	—	μA
		V_{DS} = 400 V	—	—	—	1	
		T_C = 125° C					
		V_{DS} = 360 V	—	50	—	—	
		V_{DS} = 400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 250 V	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	525(typ)	900	525(typ)	900	
Fall Time	t_f	V_{GS} = 10 V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH10N45, RFH10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

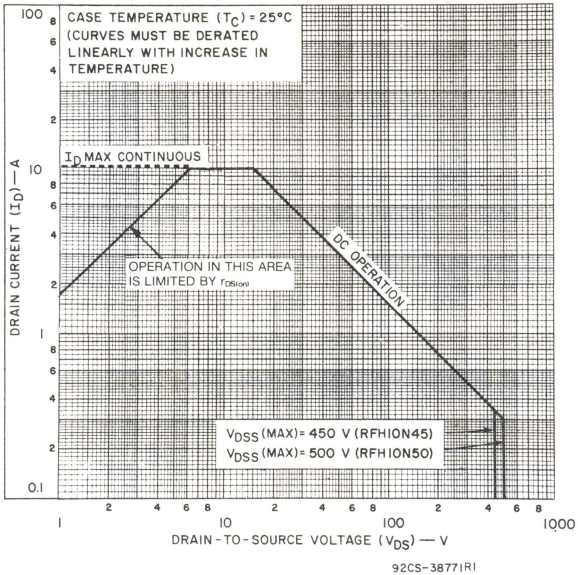


Fig. 1 - Maximum safe operating areas for all types.

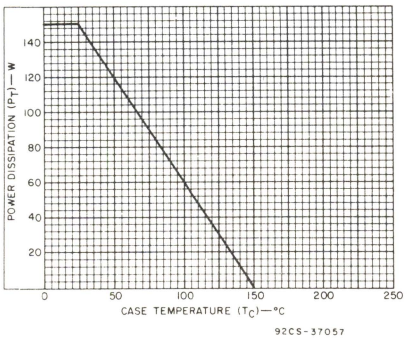


Fig. 2 - Power vs. temperature derating curve for all types.

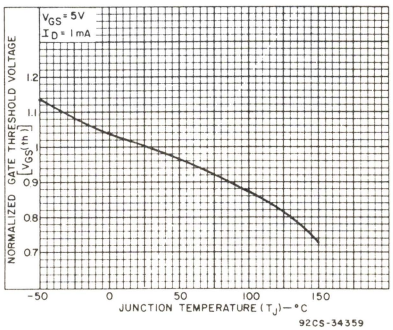


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

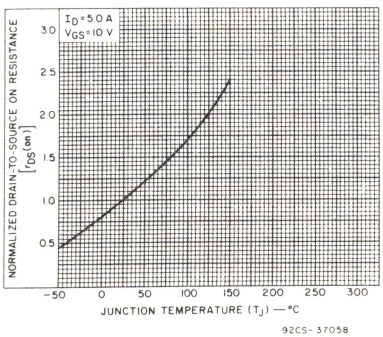


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

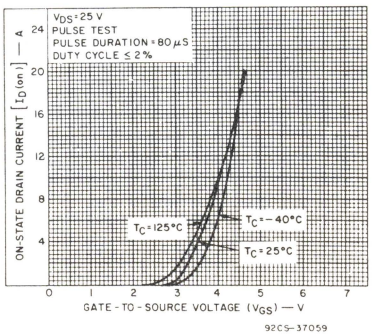


Fig. 5 - Typical transfer characteristics for all types.

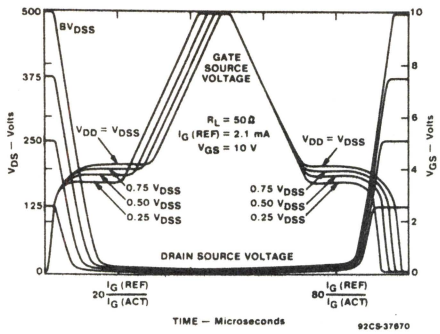


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

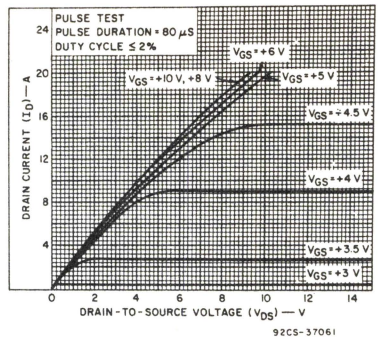


Fig. 7 - Typical saturation characteristics for all types.

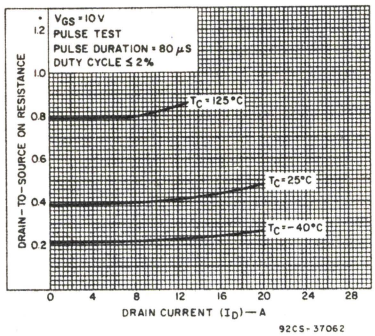


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

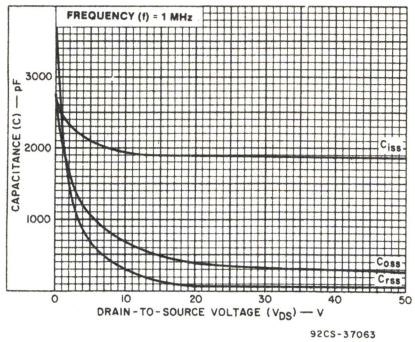


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

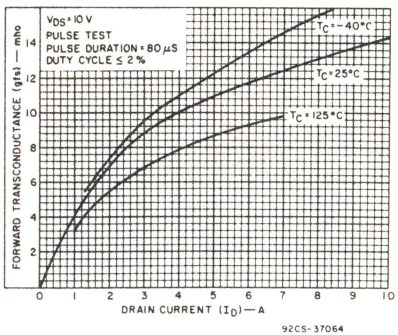


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

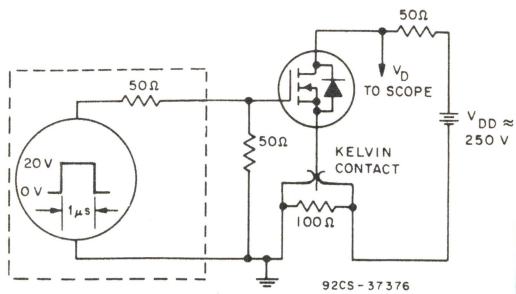


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM10N45
RFM10N50

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 10A, 450V and 500V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

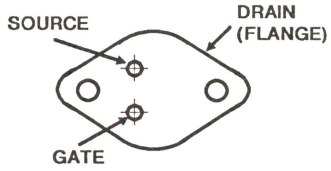
Description

The RFM10N45 and RFM10N50 n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The RFM types are supplied in the JEDEC TO-204AA steel package.

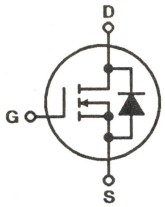
Packages

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		RFM10N45	RFM10N50	UNITS
Drain-Source Voltage	V_{DSS}	450	500	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	450	500	V
Continuous Drain Current				
RMS Continuous	I_D	10	10	A
Pulsed Drain Current	I_{DM}	20	20	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Above T_C = +25°C, Derate Linearly		1.2	1.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1788

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V	—	1	—	—	μA
		V_{DS} = 400 V	—	—	—	1	
		T_C = 125° C					
		V_{DS} = 360 V	—	50	—	—	
		V_{DS} = 400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 250	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	525(typ)	900	525(typ)	900	
Fall Time	t_f	V_{GS} = 10 V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N45, RFM10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

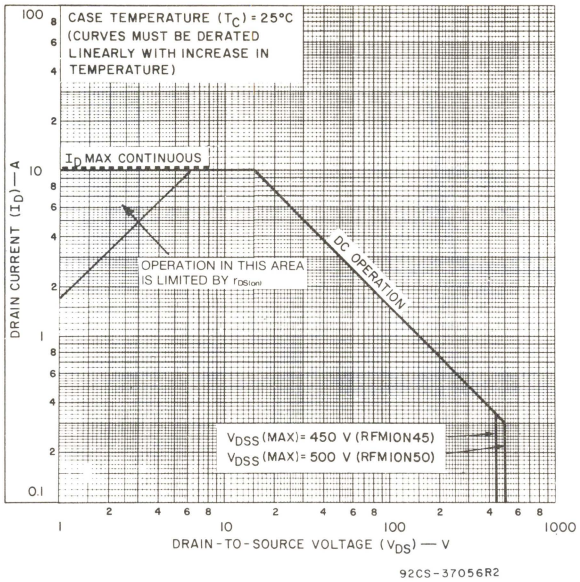


Fig. 1 - Maximum safe operating areas for all types.

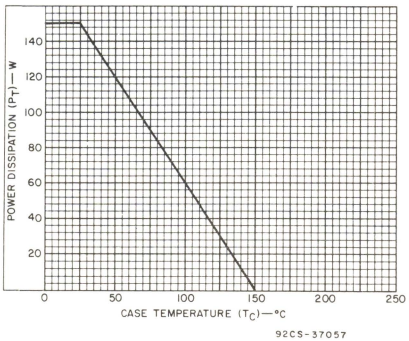


Fig. 2 - Power vs. temperature derating curve for all types.

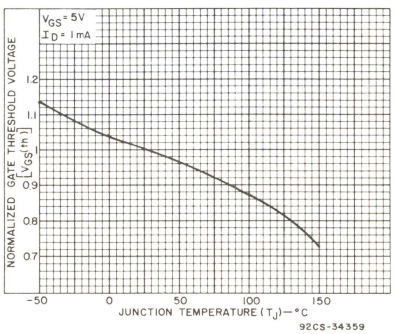


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

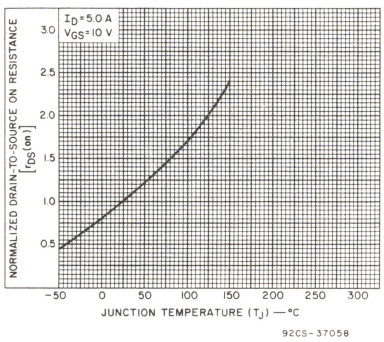


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

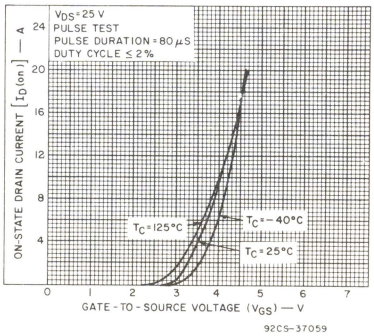


Fig. 5 - Typical transfer characteristics for all types.

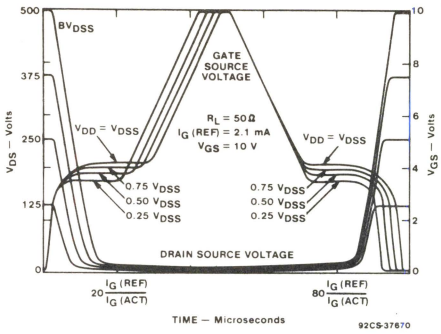


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

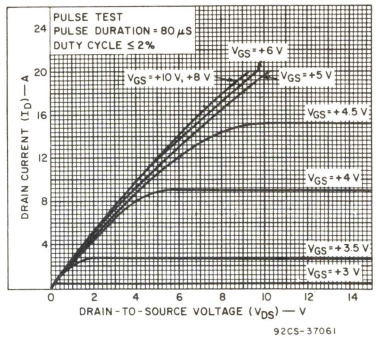


Fig. 7 - Typical saturation characteristics for all types.

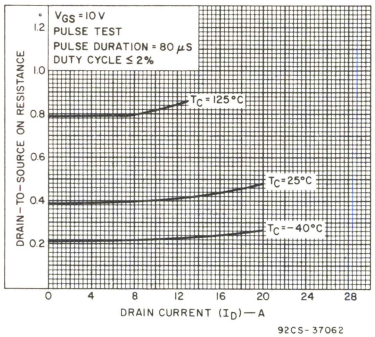


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

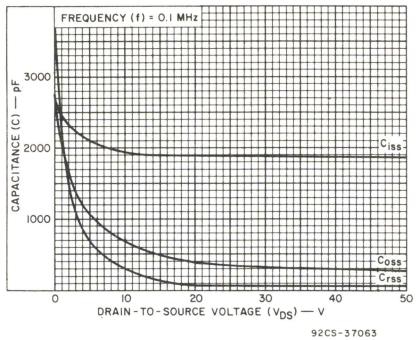


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

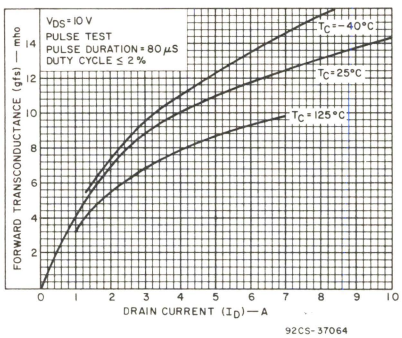


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

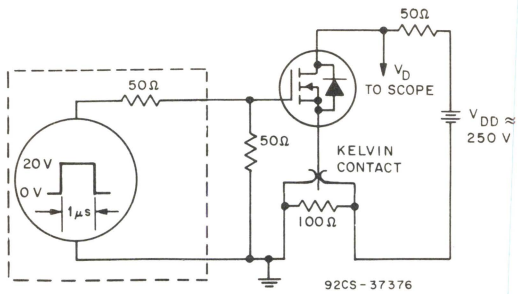


Fig. 11 - Switching Time Test Circuit.

RFD3055, RFD3055SM RFP3055

12A, 60V, Avalanche Rated, N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

February 1994

Features

- 12A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD3055, RFD3055SM and RFP3055 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

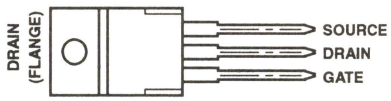
The RFD3055 is supplied in the JEDEC TO-251AA plastic package, the RFD3055SM is supplied in the JEDEC TO-252AA plastic package and the RFP3055 is supplied in the JEDEC TO-220AB plastic package. Due to space limitations the RFD3055 and RFD3055SM are branded FD3055.

When ordering use the entire part number; eg. RFD3055SM.

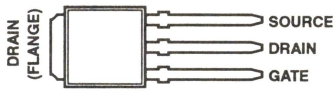
Developmental type TA49082.

Packaging

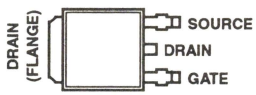
JEDEC TO-220AB
TOP VIEW



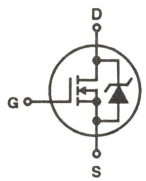
JEDEC TO-251AA
TOP VIEW



JEDEC TO-252AA
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	RFD3055, RFD3055SM, RFP3055	UNITS
Drain Source Voltage ..... V_{DSS}	60	V
Drain Gate Voltage ..... V_{DGR}	60	V
Gate Source Voltage ..... V_{GS}	±20	V
Drain Current		
RMS Continuous ..... I_D	12	A
Pulsed Drain Current ..... I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating ..... E_{AS}	Refer to UIS Curve	
Maximum Avalanche Current ..... I_{AM}	30	A
Power Dissipation		
T_C = +25°C ..... P_D	53	W
Derate above +25°C ..... P_T	0.357	W/°C
Operating and Storage Temperature ..... T_{STG}, T_J	-55 to +175	°C

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Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 12A, V_{GS} = 10V		-	-	0.150	W
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 12A, R_L = 2.5Ω, V_{GS} = +10V, R_{GS} = 10Ω		-	-	40	ns
Turn-On Delay Time	$t_{D(ON)}$			-	7	-	ns
Rise Time	t_R			-	21	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	16	-	ns
Fall Time	t_F			-	10	-	ns
Turn-Off Time	t_{OFF}			-	-	40	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 48V, I_D = 12A, R_L = 4Ω	-	19	23	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0 to 10V		-	10	12	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to 2V		-	0.6	0.8	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 12A, V_{DS} = 15V		-	-	7.5	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	300	-	pF
Output Capacitance	C_{OSS}			-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	30	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	2.8	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251 and TO-252 Package		-	-	100	°C/W
		TO-220 Package		-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 12A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 12A, dI_{SD}/dt = 100A/µs	-	-	100	ns

Typical Performance Curves

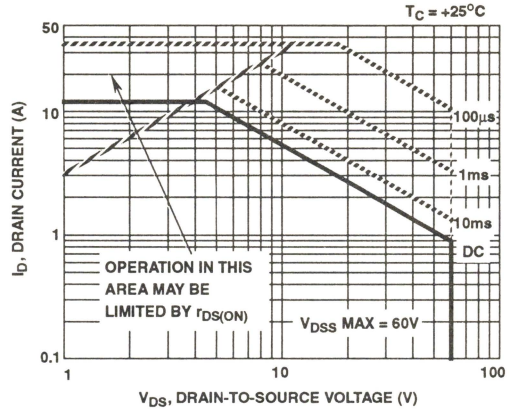


FIGURE 1. SAFE- OPERATING AREA CURVE

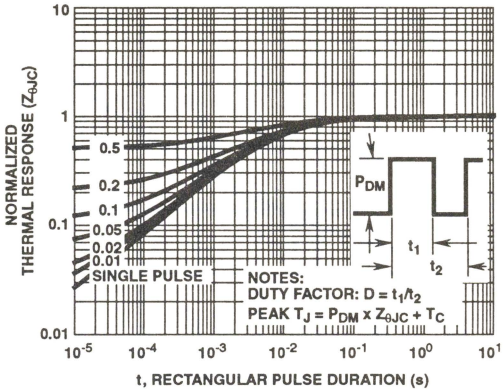


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

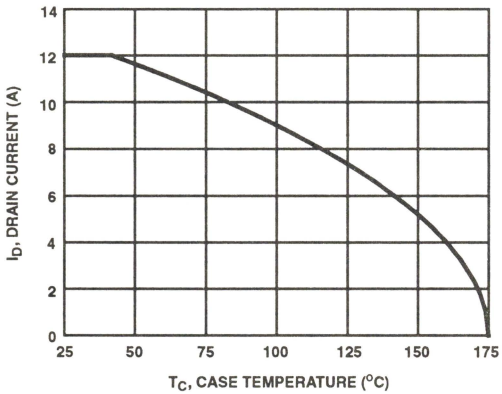


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

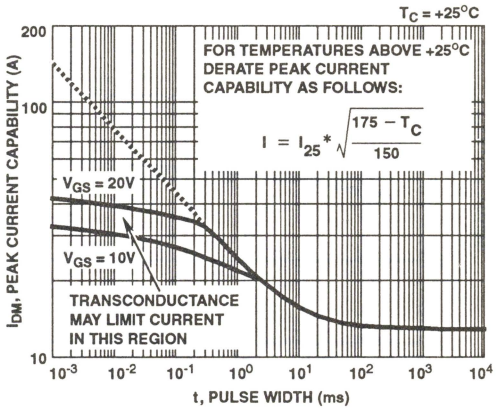


FIGURE 4. PEAK CURRENT CAPABILITY

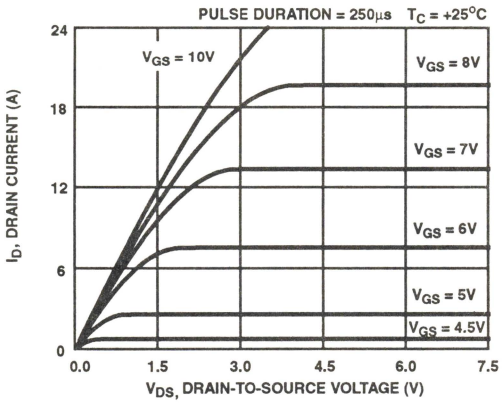


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

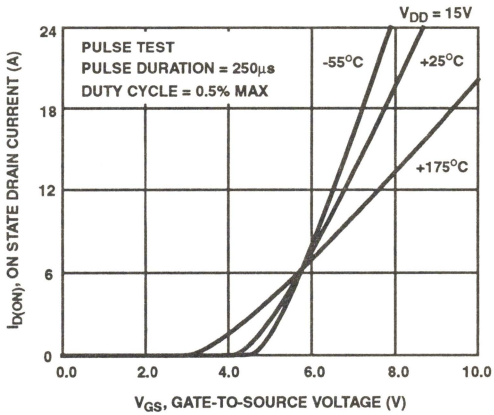


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

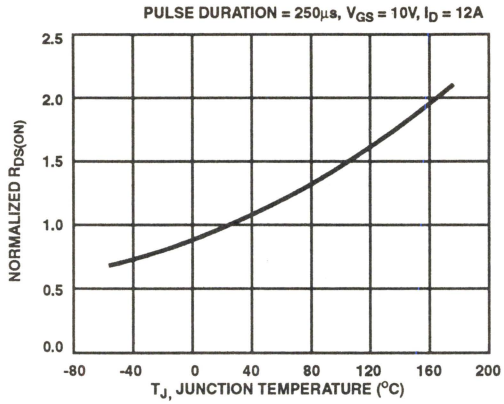


FIGURE 7. NORMALIZED $R_{DS(ON)}$ vs JUNCTION TEMPERATURE

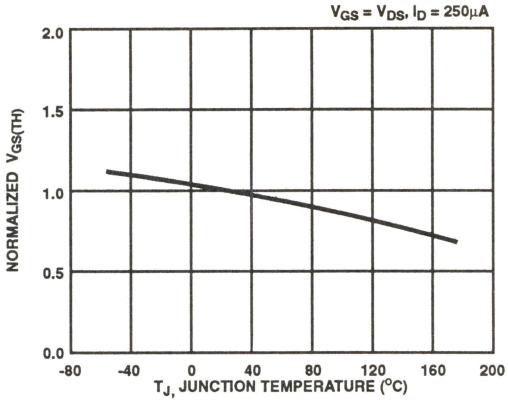


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

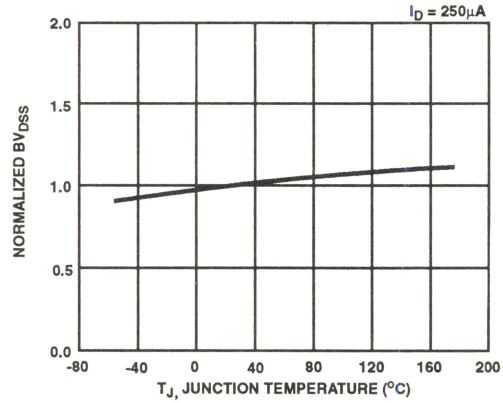


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

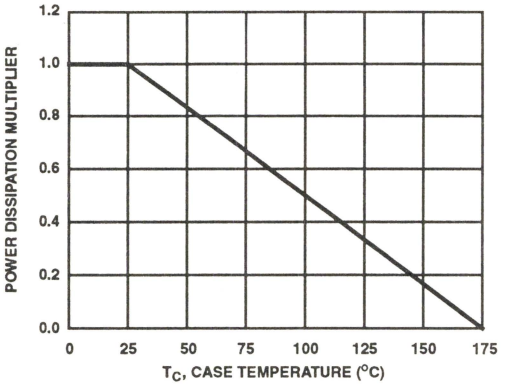


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

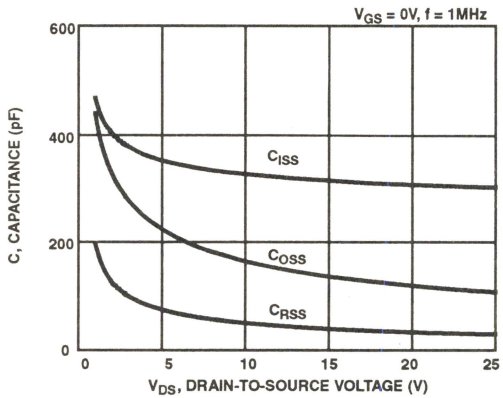


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

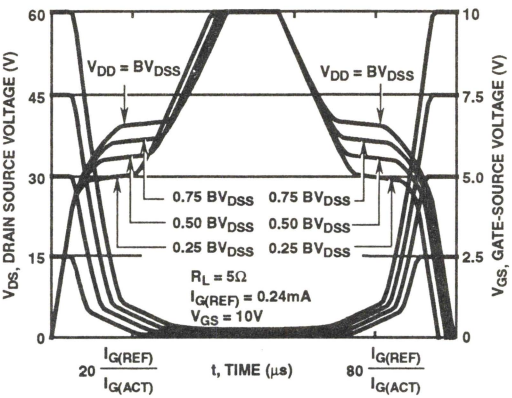


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

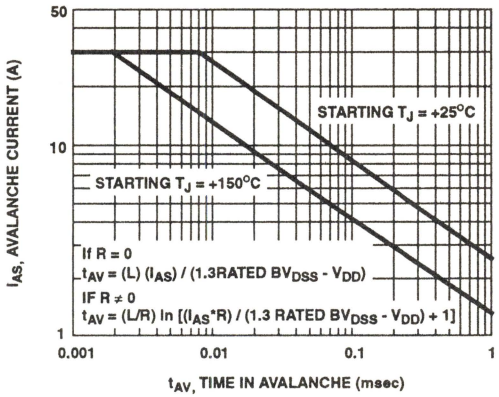


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

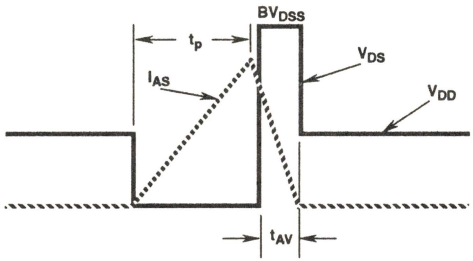


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

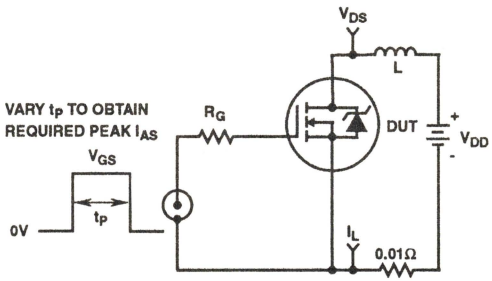


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

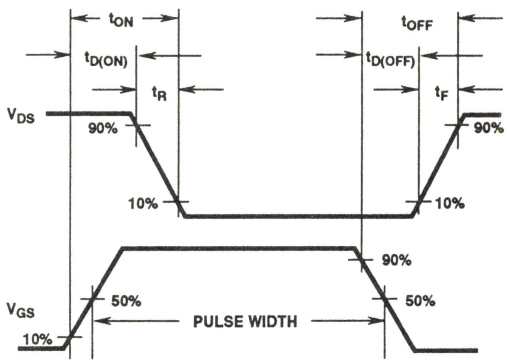


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

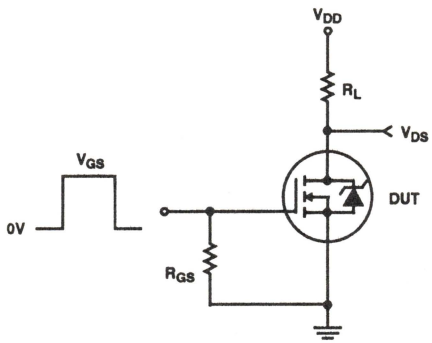


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

PSpice Model Listing

Temperature Compensated PSPICE Model for the RFD3055, RFD3055SM, RFP3055

```
.SUBCKT RFP3055  2 1 3 ;       rev 10/26/93

CA 12 8 0.540e-9
CB 15 14 0.540e-9
CIN 6 8  0.300e-9

DBODY 7  5  DBDMOD
DBREAK 5 11  DBKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK 11 7  17 18  67.9
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN  2  5  1e-9
LGATE 1  9  4.61e-9
LSOURCE 3 7  4.61e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 1e-4
RGATE 9 20 7.23
RIN 6 8 1e9
RSCL1  5  51  RSLVCMOD 1e-6
RSCL2  5  50  1e3
RSOURCE 8 7 RDSMOD 108e-3
RVTO 18 19 RVTOMOD 1

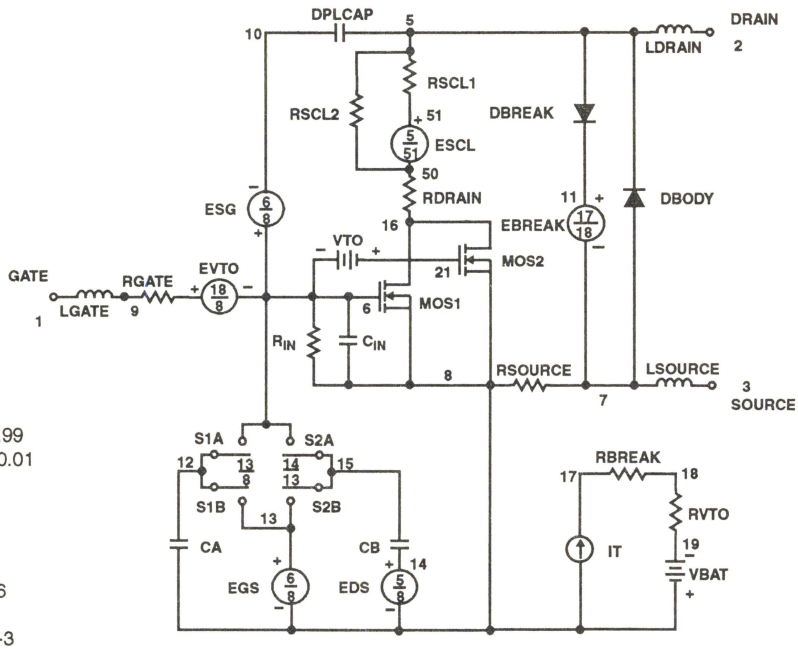
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6  0.5

ESCL  51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/30,6.5))}

.MODEL DBDMOD D (IS=4.33e-14  RS=2.78e-2  TRS1=1.10e-3  TRS2=5.19e-6  CJO=3.94e-10  TT=7.63e-8)
.MODEL DBKMOD D (RS=0.676  TRS1=1.94e-3  TRS2=-1.09e-6)
.MODEL DPLCAPMOD D (CJO=0.238e-9  IS=1e-30  N=10)
.MODEL MOSMOD NMOS (VTO=4.078  KP=12  IS=1e-30  N=10  TOX=1  L=1u  W=1u)
.MODEL RBKMOD RES (TC1=1.06e-3  TC2=-1.92e-6)
.MODEL RDSMOD RES (TC1=5.03e-3  TC2=1.53e-5)
.MODEL RSLVCMOD RES (TC1=2.2e-3  TC2=-5e-6)
.MODEL RVTOMOD RES (TC1=-5.02e-3  TC2=-9.16e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-6.5  VOFF=-3.5)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3.5  VOFF=-6.5)
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-2.50  VOFF=2.50)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=2.50  VOFF=-2.50)

.ENDS
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options;** authored by William J. Hepp and C. Frank Wheatley.

HARRIS

RFM12N08/12N10
RFP12N08/12N10

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 12A, 80V and 100V
- $r_{DS(on)} = 0.2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

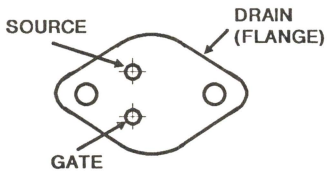
Description

The RFM12N08 and RFM12N10 and the RFP12N08 and RFP12N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

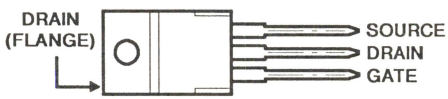
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

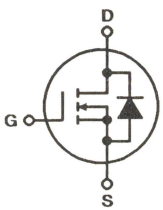


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM12N08	RFM12N10	RFP12N08	RFP12N10	UNITS
Drain-Source Voltage ..... V_{DSS}	80	100	80	100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1386.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFP12N08		RFM12N10 RFP12N10		
			Min.	Max.	Min.	Max.	
Drain Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	μA
		V_{DS}=80 V	—	—	—	1	
		T_C=125° C V_{DS}=65 V	—	50	—	—	
		V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=10 V	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	150	—	150	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	45(Typ)	70	45(Typ)	70	ns
Rise Time	t_r	I_D=6 A	250(Typ)	375	250(Typ)	375	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	85(Typ)	130	85(Typ)	130	
Fall Time	t_f	V_{GS}=10 V	100(Typ)	150	100(Typ)	150	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N08, RFM12N10	—	1.67	—	1.67	°C/W
		RFP12N08, RFP12N10	—	2.083	—	2.083	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFM12N10		RFP12N08 RFP12N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

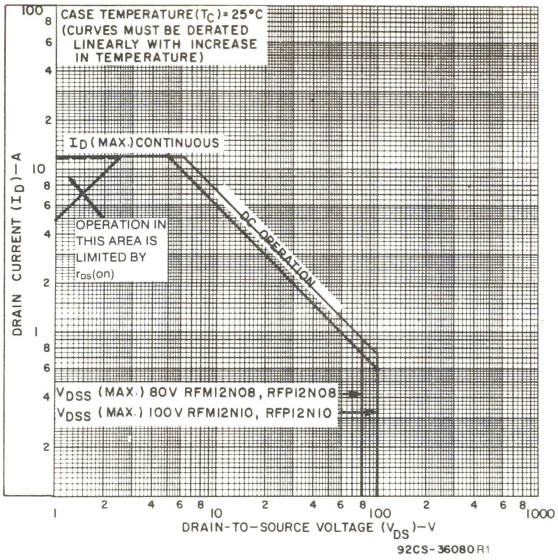


Fig. 1 - Maximum operating areas for all types.

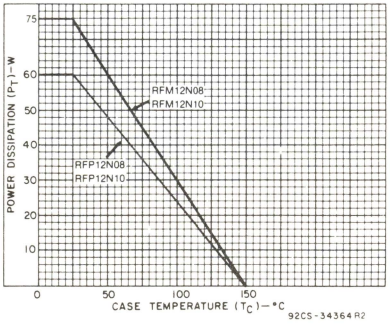


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

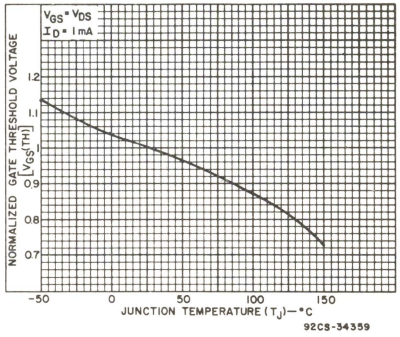


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

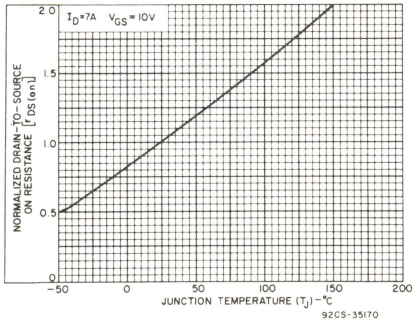


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

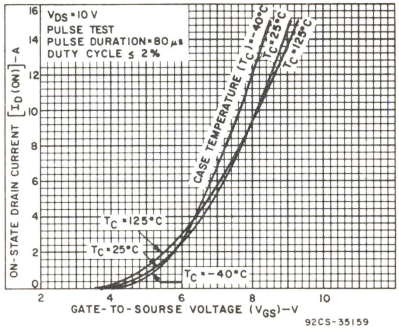


Fig. 5 - Typical transfer characteristics for all types.

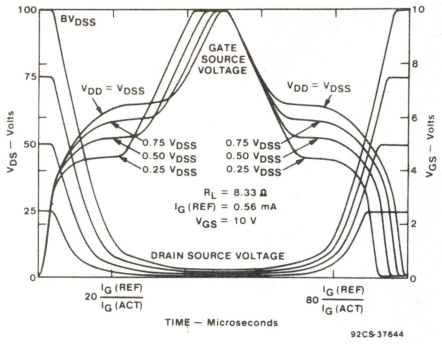


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

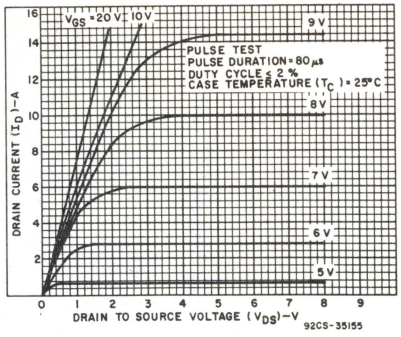


Fig. 7 - Typical saturation characteristics for all types.

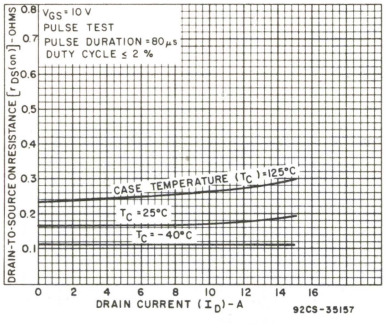


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

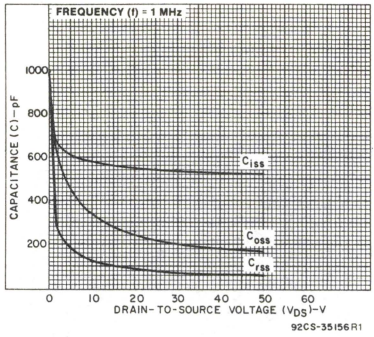


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

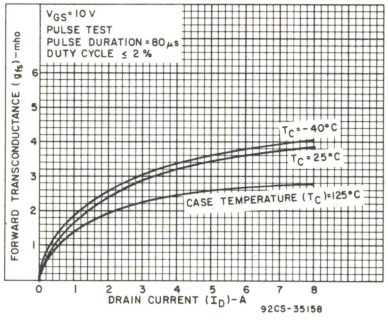


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

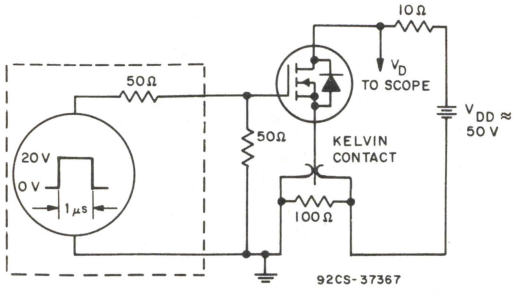


Fig. 11 — Switching Time Test Circuit

HARRIS

RFM12N18/12N20
RFP12N18/12N20

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 12A, 180V and 200V
- $r_{DS(on)} = 0.25\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

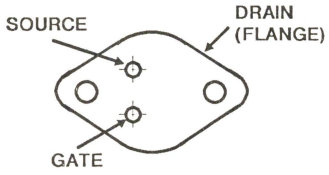
Description

The RFM12N18 and RFM12N20 and the RFP12N18 and RFP12N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

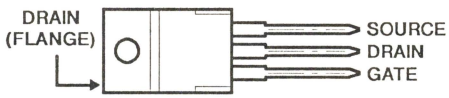
The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

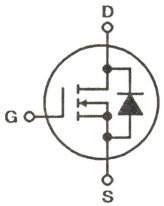


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM12N18	RFM12N20	RFP12N18	RFP12N20	UNITS
Drain-Source Voltage ..... V_{DSS}	180	200	180	200	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	180	200	180	200	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	W/^{o}C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1461.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125° C V_{DS}=145 V	—	50	—	—	
		V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.5	—	1.5	V
		I_D=12 A V_{GS}=10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.25	—	0.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	600	—	600	
Reverse-Transfer Capacitance	C_{rss}		—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V I_D=6 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r		130(typ)	200	130(typ)	200	
Turn-Off Delay Time	$t_d(off)$		120(typ)	180	120(typ)	180	
Fall Time	t_f		105(typ)	160	105(typ)	160	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N18, RFM12N20	—	1.25	—	1.25	°C/W
		RFP12N18, RFP12N20	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	325(typ)		325(typ)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

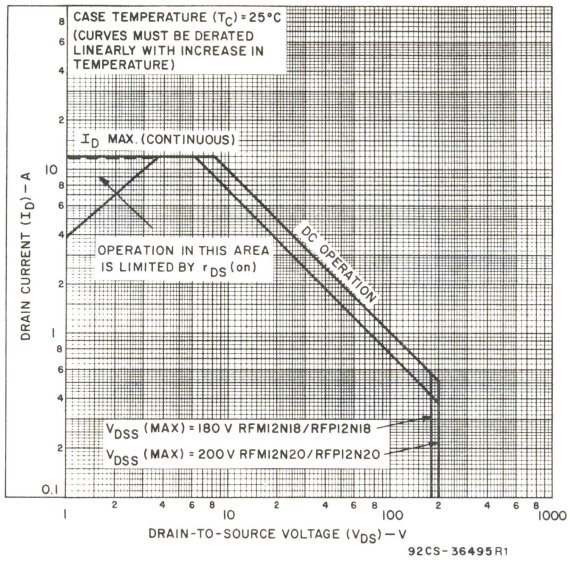


Fig. 1 - Maximum safe operating areas for all types.

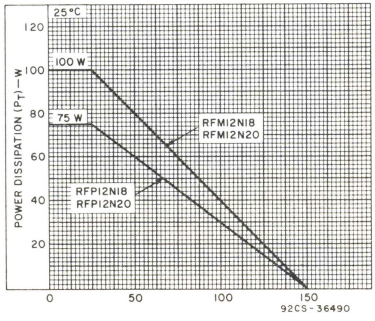


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

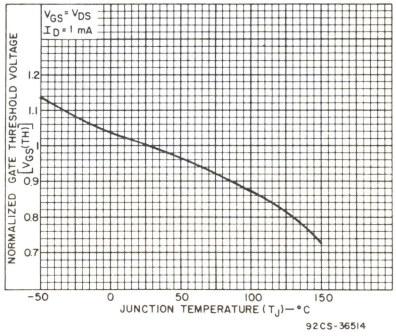


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

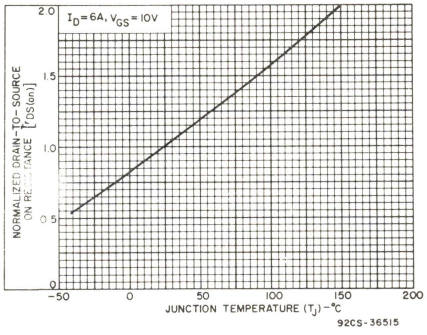


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

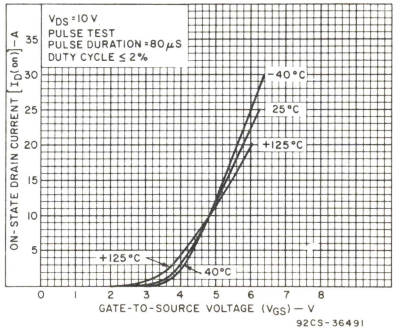


Fig. 5 - Typical transfer characteristics for all types.

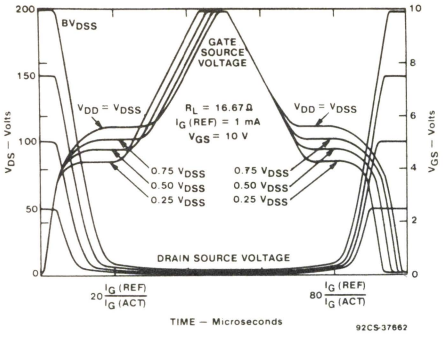


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

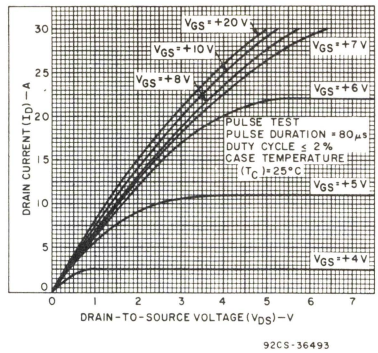


Fig. 7 - Typical saturation characteristics for all types.

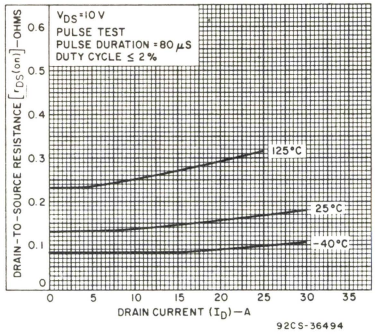


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

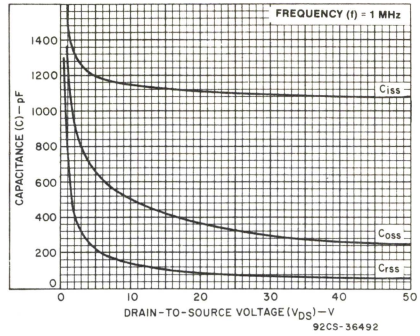


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

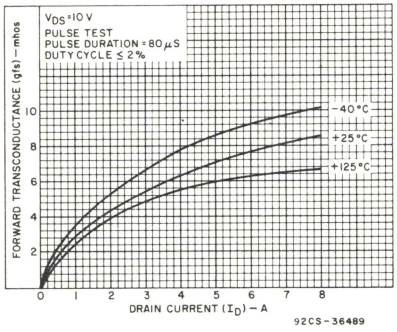


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

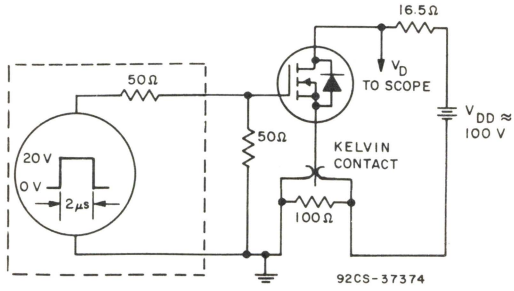


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH12N35
RFH12N40

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 12A, 350V and 400V
- $r_{DS(on)} = 0.038\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

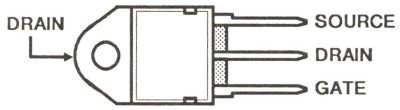
Description

The RFH12N35 and RFH12N40 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

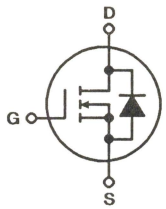
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH12N35	RFH12N40	UNITS
Drain-Source Voltage	V_{DSS}	350	400	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	350	400	V
Continuous Drain Current	I_D	12	12	A
Pulsed Drain Current	I_{DM}	24	24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1630.1**

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V	—	1	—	—	μA
		V_{DS} = 320 V	—	—	—	1	
		T_C = 125°C V_{DS} = 280 V	—	50	—	—	
		V_{DS} = 320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	2.28	—	2.28	V
		I_D = 12 A V_{GS} = 10 V	—	6.75	—	6.75	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	0.38	—	0.38	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	900	—	900	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 200 V	30(typ)	50	30(typ)	50	ns
Rise Time	t_r	I_D = 6 A	105(typ)	150	105(typ)	150	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	480(typ)	750	480(typ)	750	
Fall Time	t_f	V_{GS} = 10 V	140(typ)	200	140(typ)	200	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH12N35, RFH12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 6A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

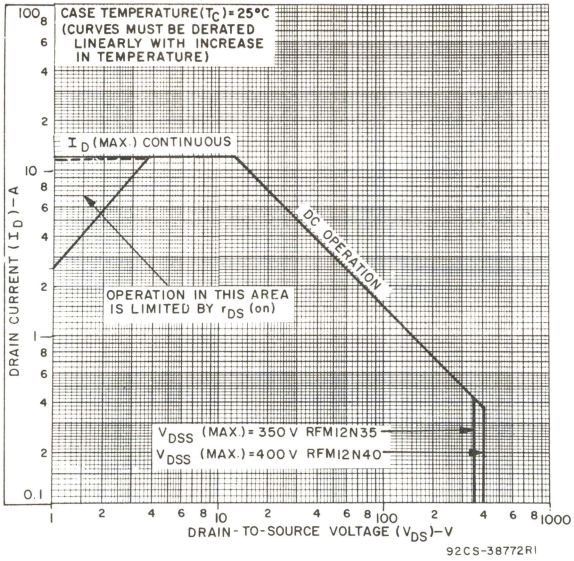


Fig. 1 - Maximum safe operating areas for all types.

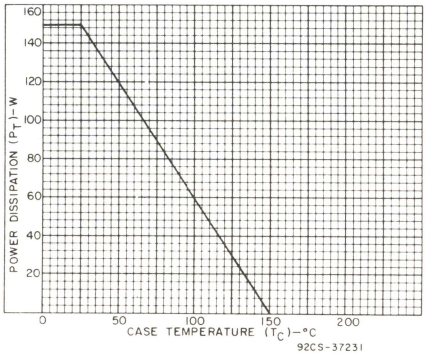


Fig. 2 - Power vs. temperature derating curve for all types.

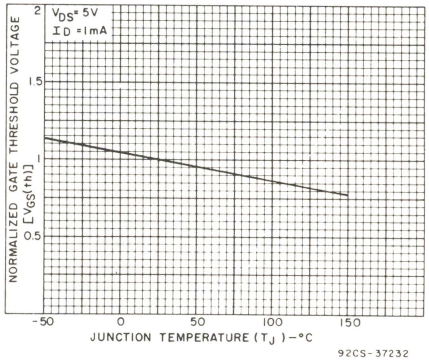


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

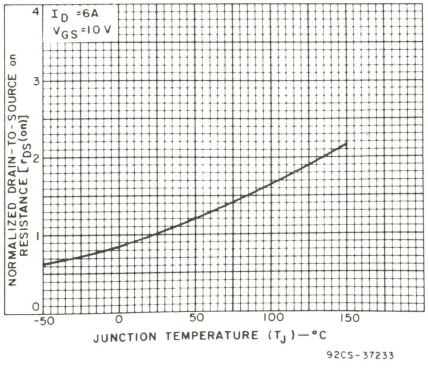


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

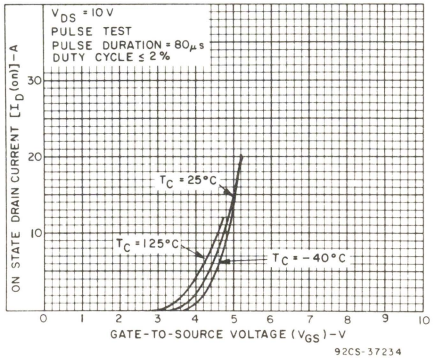


Fig. 5 - Typical transfer characteristics for all types.

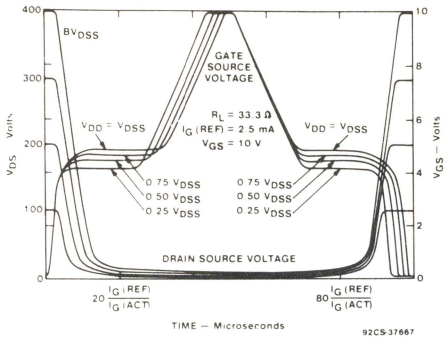


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

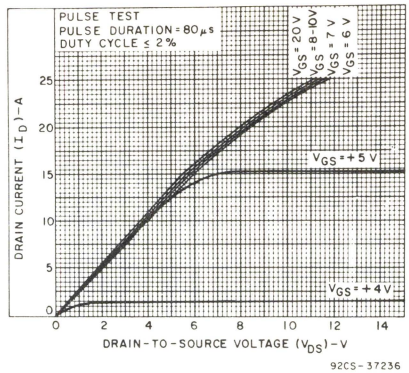


Fig. 7 - Typical saturation characteristics for all types.

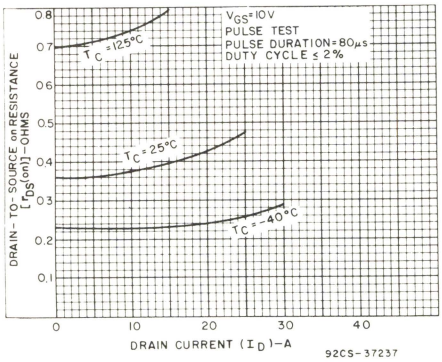


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

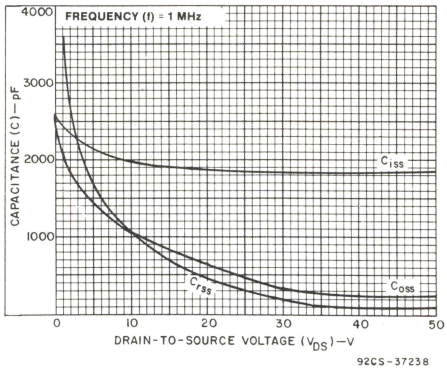


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

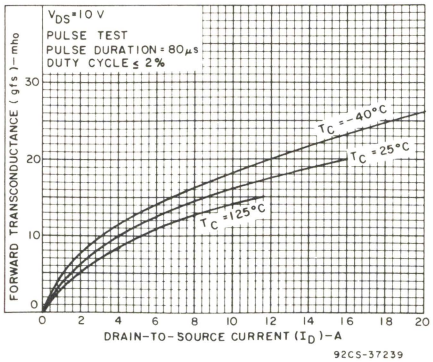


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

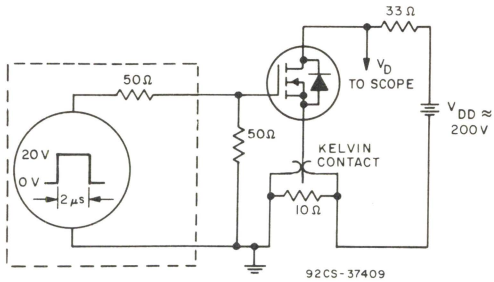


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM12N35
RFM12N40

N-Channel Enhancement Mode Power Field Effect Transistors

August 1991

Features

- 12A, 350V and 400V
- $r_{DS(on)} = 0.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

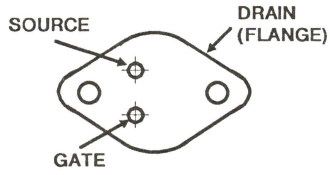
Description

The RFM12N35 and RFM12N40 n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar transistors requiring high speed and low gate-drive power. These transistors can be operated directly from integrated circuits.

The RFM types are supplied in the JEDEC TO-204AA steel package.

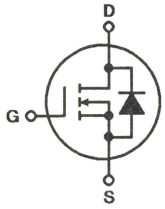
Packages

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		RFM12N35	RFM12N40	UNITS
Drain-Source Voltage	V_{DSS}	350	400	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	350	400	V
Continuous Drain Current				
RMS Continuous	I_D	12	12	A
Pulsed Drain Current	I_{DM}	24	24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Above T_C = +25°C, Derate Linearly		1.2	1.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1787

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V V_{DS} = 320 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 280 V V_{DS} = 320 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	3	—	3	V
		I_D = 12 A V_{GS} = 10 V	—	10	—	10	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 200 I_D = 6 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	30(typ)	50	30(typ)	50	ns
Rise Time	t_r		105(typ)	150	105(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		480(typ)	750	480(typ)	750	ns
Fall Time	t_f		140(typ)	200	140(typ)	200	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N35, RFM12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4 A, dI_F/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

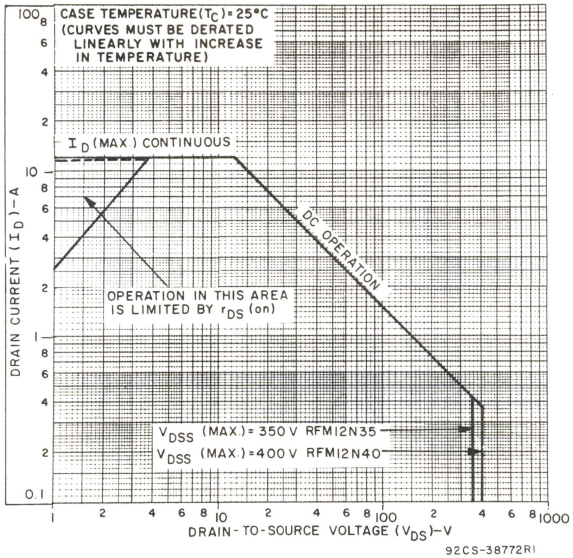


Fig. 1 - Maximum safe operating areas for all types.

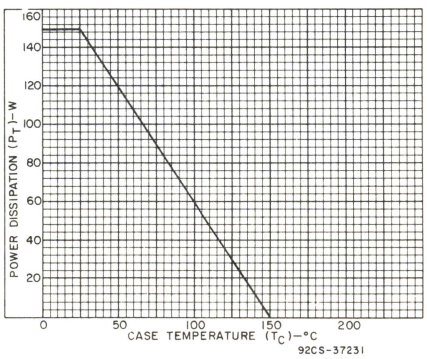


Fig. 2 - Power vs. temperature derating curve for all types.

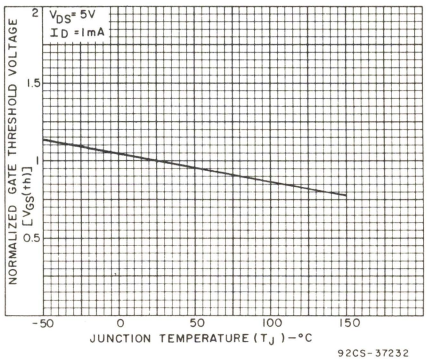


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

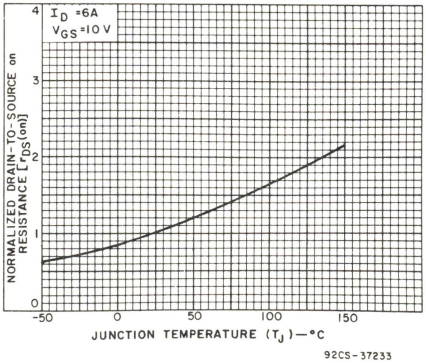


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

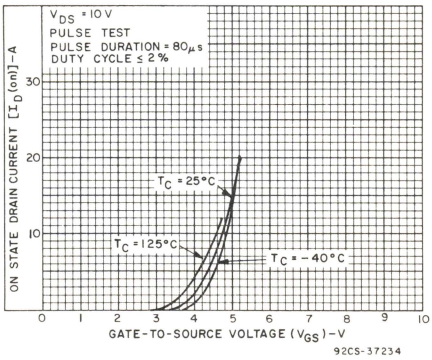


Fig. 5 - Typical transfer characteristics for all types.

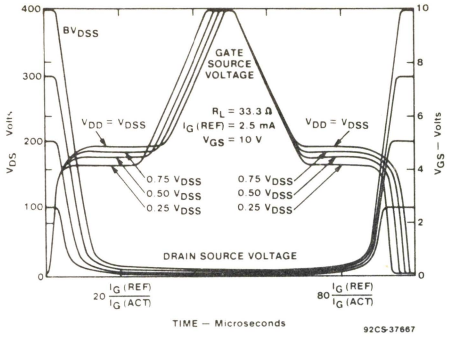


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

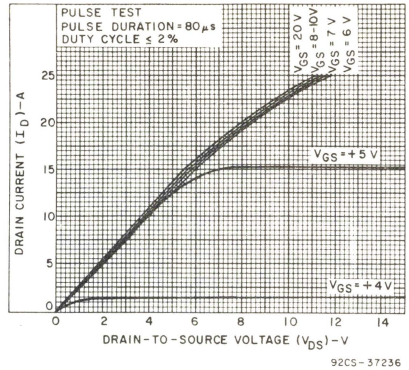


Fig. 7 - Typical saturation characteristics for all types.

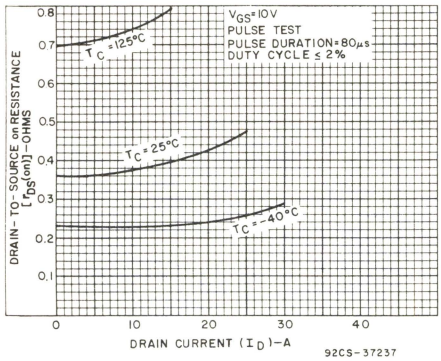


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

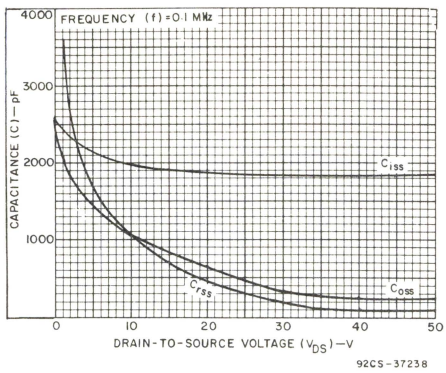


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

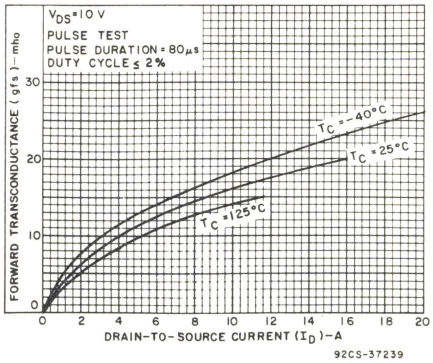


Fig. 10 - Typical forward transconductance as a function of drain for all types.

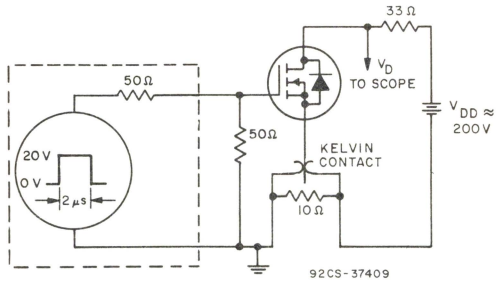


Fig. 11 - Switching Test Time Circuit.

HARRIS

RFD14N05/05SM
RFP14N05

N-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

May 1991

Features

- 14A, 50V
- $R_{DS(on)} = 0.1\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

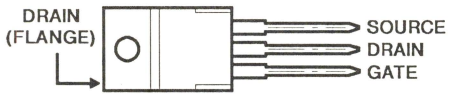
Description

The RFD14N05, RFD14N05SM, and RFP14N05 n-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

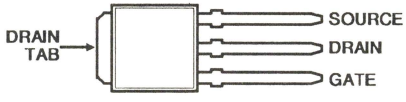
The RFD14N05 is supplied in the JEDEC TO-251 plastic package, the RFD14N05SM in the JEDEC TO-252 plastic package and the RFP14N05 in the JEDEC TO-220AB plastic package.

Packages

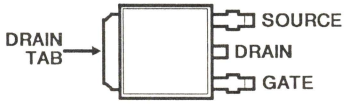
TO-220AB
TOP VIEW



TO-251AA
TOP VIEW

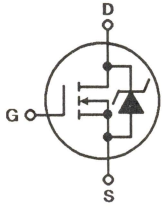


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 50V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR} 50V
Gate-Source Voltage, V_{GS} ..... ±20V
Drain Current:
  RMS Continuous, I_D 14A
  Pulsed, I_{DM} 35A
Single Pulse Avalanche Energy Rating, (Refer to UIS SOA Curve)
Power Dissipation, P_D:
  T_C = +25°C 48W
  Derate Above T_C = +25°C ..... 0.32W/°C
Operating and Storage Junction
Temperature Range, T_J, T_{STG} ..... -55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2268.1**

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150° C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 10 V		—	0.1	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A I_{g1} = I_{g2} = 0.2 A V_{GS} (clamp) + 10 V, − 0.6 V R_L = 3.57 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	14 (typ.)	
Rise Time	t_r			—	26 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	45 (typ.)	
Fall Time	t_f			—	17 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	$Q_g(total)$	V_{DD} = 40 V	V_{GS} = 0-20 V	—	40	nC
Gate Charge at 10 V	$Q_g(10)$	I_D = 14 A	V_{GS} = 0-10 V	—	25	
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-2 V	—	1.5	
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, L = 0.2μH R_L = 3.57 Ω, I_{g1} = I_{g2} = 0.2 A V_{GS} (clamp) + 10 V, −0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	
		TO-220		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/dt = 100 A/μs	—	125	ns

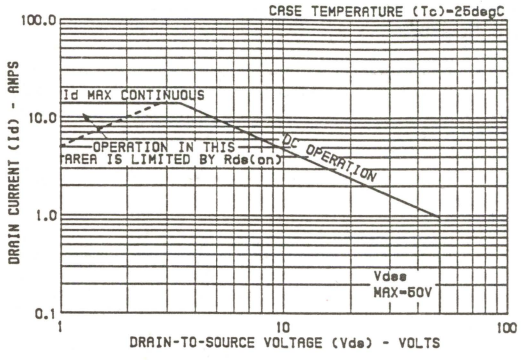


FIGURE 1. SAFE OPERATING AREA CURVE

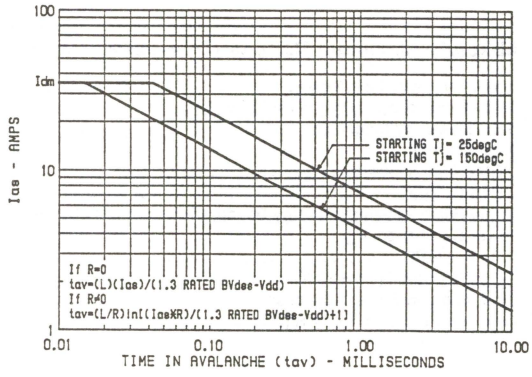


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING

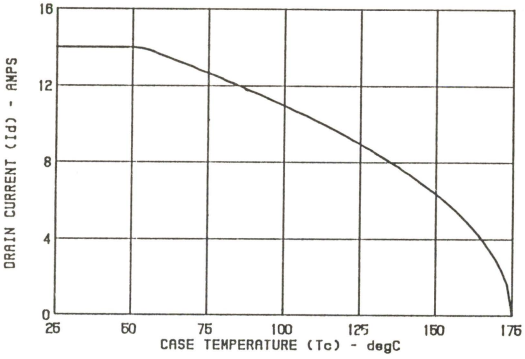


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

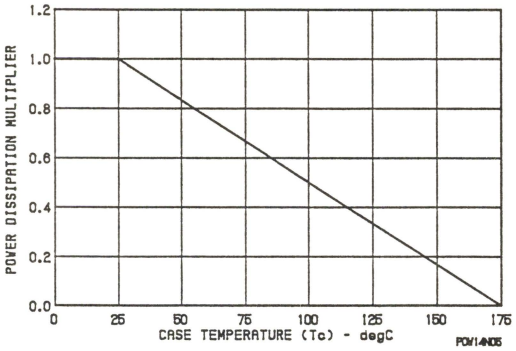


FIGURE 4. NORMALIZED POWER DISTRIBUTION vs TEMPERATURE DERATING

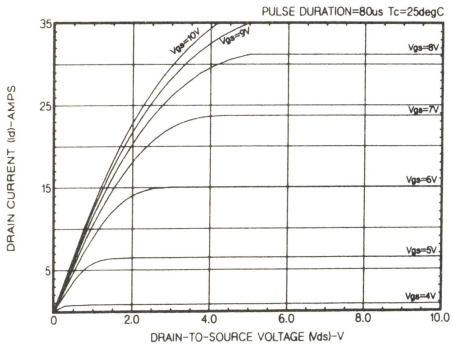


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

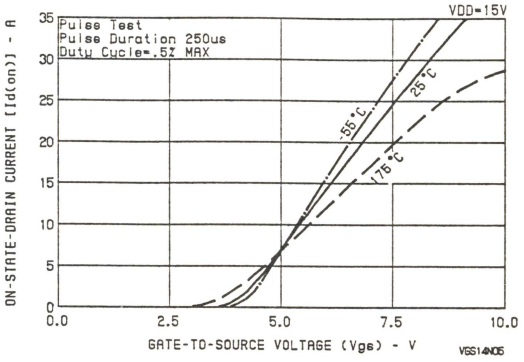


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

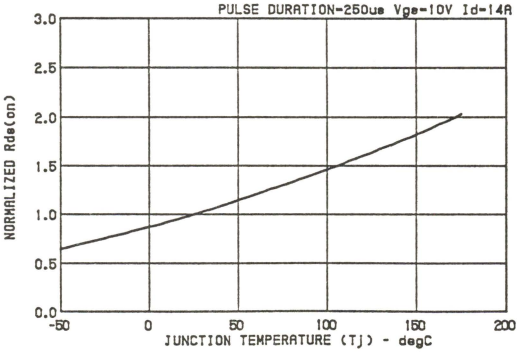


FIGURE 7. NORMALIZED RDS(on) vs JUNCTION TEMPERATURE

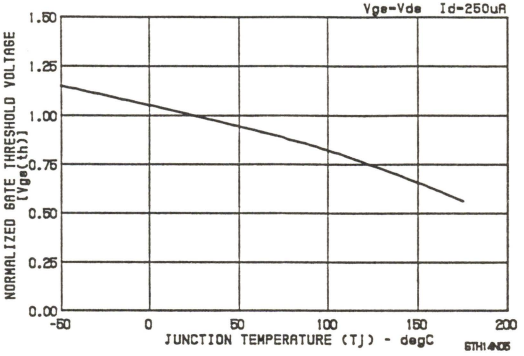


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

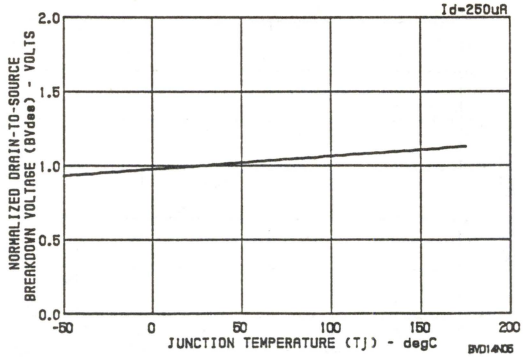


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

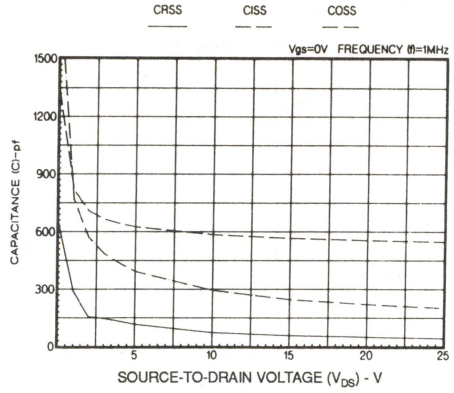


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

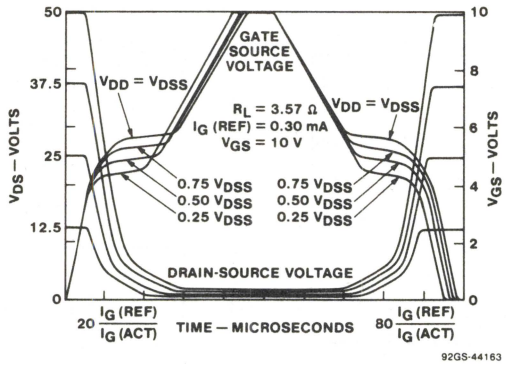


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

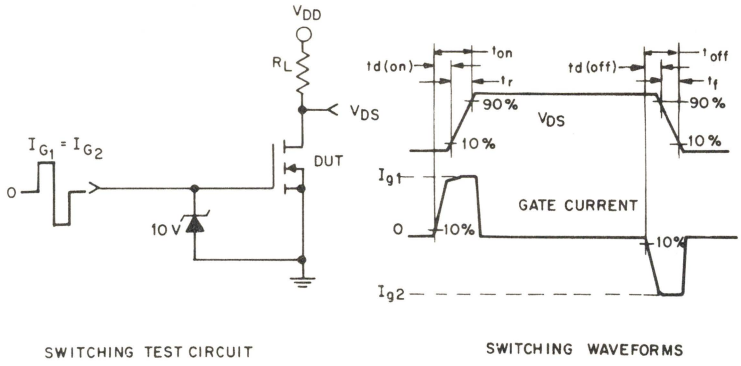


FIGURE 12. RESISTIVE SWITCHING

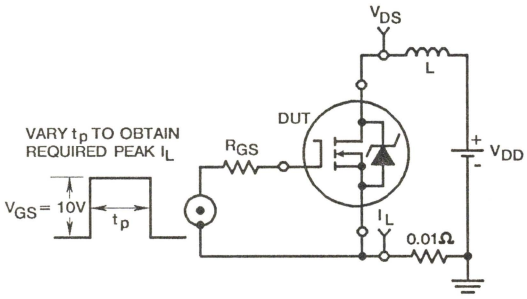


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

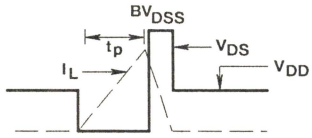


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

HARRIS

RFM15N05/15N06
RFP15N05/15N06

N-Channel Enhancement Mode Power Field Effect Transistors

May 1992

Features

- 15A, 50V and 60V
- $r_{DS(on)} = 0.14\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Temperature Compensated SPICE Model Provided

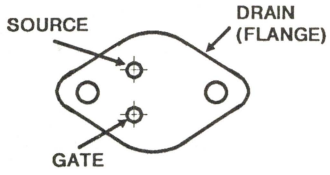
Description

The RFM15N05 and RFM15N06 and the RFP15N05 and RFP15N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

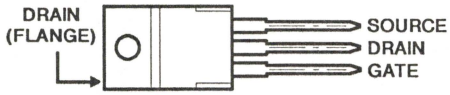
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

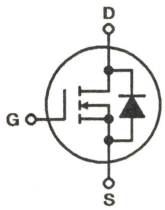


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

	RFM15N05	RFM15N06	RFP15N05	RFP15N06	UNITS
Drain-Source Voltage ..... V_{DSS}	50	60	50	60	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	50	60	50	60	V
Continuous Drain Current					
RMS Continuous ..... I_D	15	15	15	15	A
Pulsed Drain Current ..... I_{DM}	40	40	40	40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	90	90	90	90	W
Above $T_C = +25^oC$, Derate Linearly	0.48	0.48	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1478.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	μA
		V_{DS}=50 V	—	—	—	1	
		T_C=125° C V_{DS}=40 V	—	50	—	—	
		V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=7.5 A V_{GS}=10 V	—	1.05	—	1.05	V
		I_D=15 A V_{GS}=10 V	—	2.5	—	2.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=7.5 A V_{GS}=10 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=7.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	850	—	850	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	180	—	180	
Turn-On Delay Time	$t_d(on)$	V_{DD}=30 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r	I_D=7.5 A	100(typ)	175	100(typ)	175	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	72(typ)	175	72(typ)	175	
Fall Time	t_f	V_{GS}=10 V	66(typ)	140	66(typ)	140	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM15N05, RFM15N06	—	1.67	—	1.67	°C/W
		RFP15N05, RFP15N06	—	1.67	—	1.67	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD} = 15A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	100 (typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

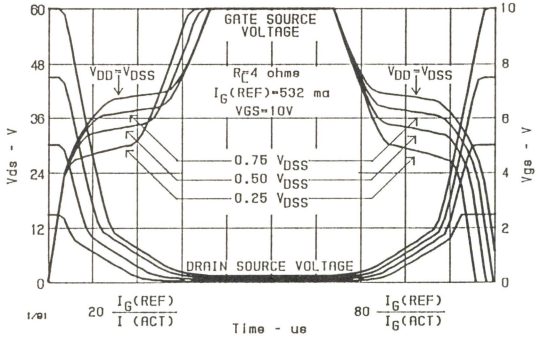


FIGURE 1. NORMALIZED SWITCHING WAVEFORMS

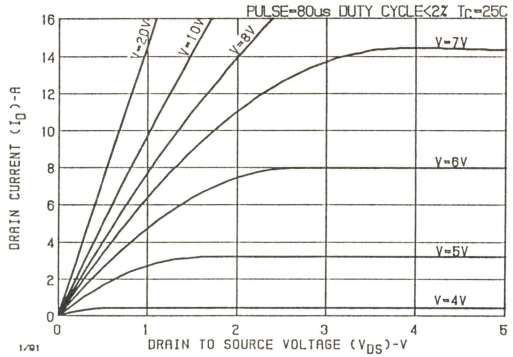


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

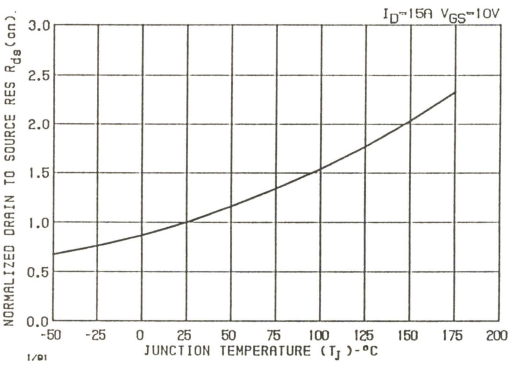


FIGURE 3. NORMALIZED $r_{DS(ON)}$ vs TEMPERATURE

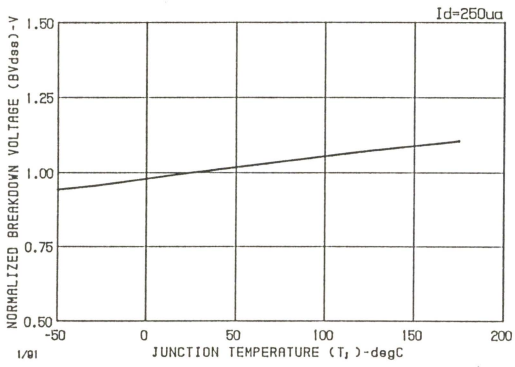


FIGURE 4. BREAKDOWN VOLTAGE vs TEMPERATURE

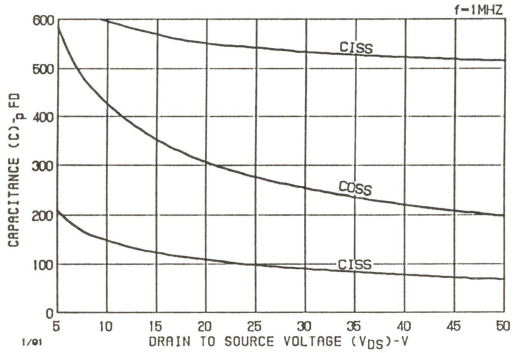


FIGURE 5. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

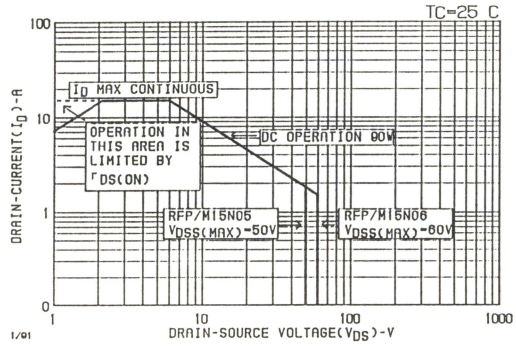


FIGURE 6. MAXIMUM SAFE OPERATING AREA

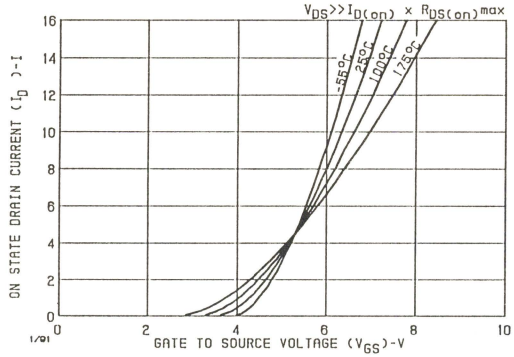


FIGURE 7. TYPICAL TRANSFER CHARACTERISTICS

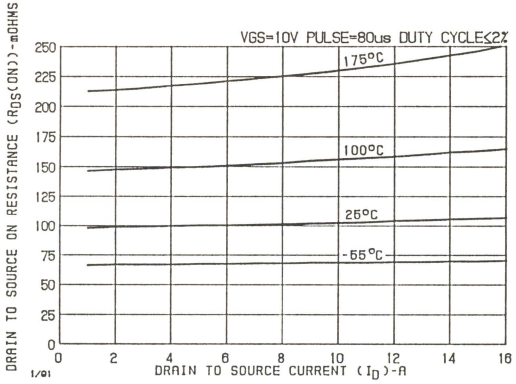


FIGURE 8. $r_{DS(ON)}$ vs DRAIN CURRENT

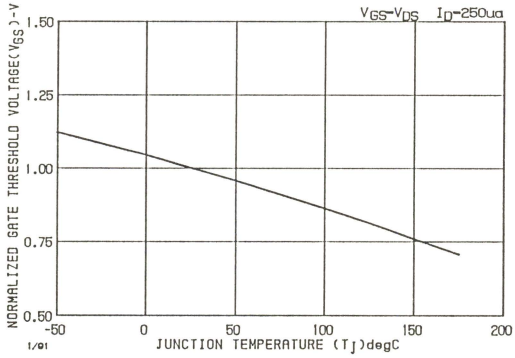


FIGURE 9. THRESHOLD VOLTAGE vs TEMPERATURE (T_J)

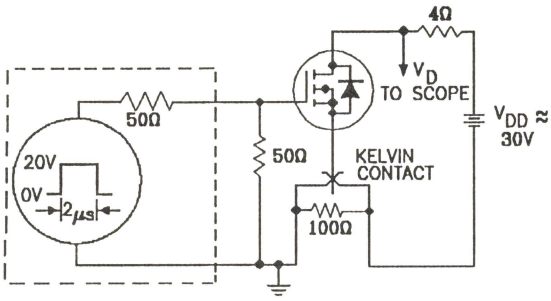
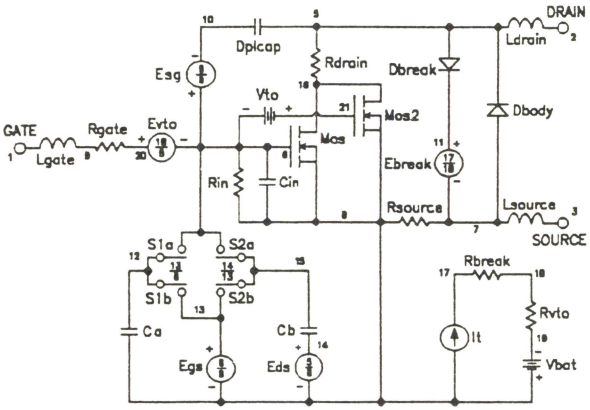


FIGURE 10. SWITCHING TIME TEST CIRCUIT

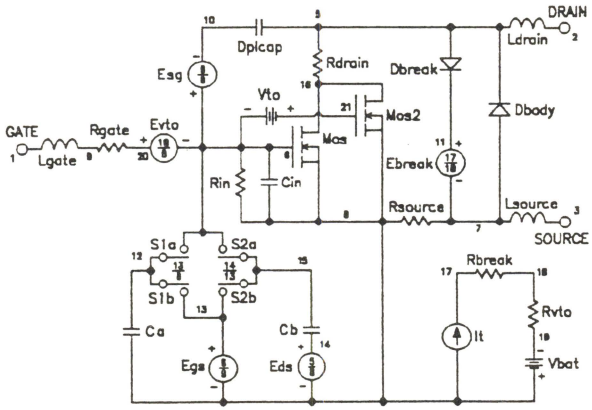
Spice Model (RFM15N06)

```
.SUBCKT RFM15N06  2  1  3;  rev 01/07/91
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=3.46  KP=3.09  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  .74
Rsource  8  7  RDSMOD  34.82e-3
Rdrain  5  16  RDSMOD  13.3e-3
.MODEL RDSMOD RES (TCI=6.5e-3  TC2=3.28e-5)
.MODEL RVTOMOD RES (TCI=-4.30e-3  TC2=-3.77e-6)
.MODEL RVTOMOD2 RES (TCI=0  TC2=0)
Ebreak  11  7  17  18  102.35
.MODEL RBKMOD RES (TCI=8.33e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBKMOD D (RS=3.83e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBDMOD D (IS=8.16e-13  RS=1.54e-2  TRS1=1.77e-3  TRS2=1.85e-5)
+CJO=9.16e-10  TT=7e-8
Cin  6  8  4.44e-10
Ca  12  8  9.14e-10
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3.66  VOFF=-1.66)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.66  VOFF=-3.66)
.MODEL DPLCAPMOD D (CJO=4.90e-10  IS=1e-30  N=10)
Cb  12  14  5.81e-10
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.07  VOFF=8.07)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON8.07  VOFF=3.07)
Rgate  9  20  20.43
Lgate  1  9  1.32e-8
Ldrain  2  5  1.0e-10
Lsource  3  7  1.68e-8
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
Mos  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
Sla  6  12  13  8  S1AMOD
Slb  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS
```



Spice Model (RFM15N06)

```
.SUBCKT RFM15N06  2  1  3;  rev 01/07/91
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=3.46  KP=3.09  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  .74
Rsource  8  7  RDSMOD  34.82e-3
Rdrain  5  16  RDSMOD  13.3e-3
.MODEL RDSMOD RES (TCl=6.5e-3  TC2=3.28e-5)
.MODEL RVTOMOD RES (TCl=-4.30e-3  TC2=-3.77e-6)
.MODEL RVTOMOD2 RES (TCl=0  TC2=0)
Ebreak  11  7  17  18  102.35
.MODEL RBKMOD RES (TCl=8.33e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBKMOD D (RS=3.83e-1  TRS1=7.81e-4  TRS2=-9.28e-6)
.MODEL DBDMOD D (IS=8.16e-13  RS=1.54e-2  TRS1=1.77e-3  TRS2=1.85e-5 +CJO=9.16e-10  TT=7e-8)
Cin  6  8  4.44e-10
Ca  12  8  9.14e-10
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3.66  VOFF=-1.66)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.66  VOFF=-3.66)
.MODEL DPLCAPMOD D (CJO=4.90e-10  IS=1e-30  N=10)
Cb  12  14  5.81e-10
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.07  VOFF=8.07)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=8.07  VOFF=3.07)
Rgate  9  20  20.43
Lgate  1  9  1.32e-8
Ldrain  2  5  1.0e-10
Lsource  3  7  1.68e-8
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
Mos  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
Sla  6  12  13  8  S1AMOD
Slb  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS
```



HARRIS

RFM15N12/15N15
RFP15N12/15N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 15A, 120V and 150V
- $r_{DS(on)} = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

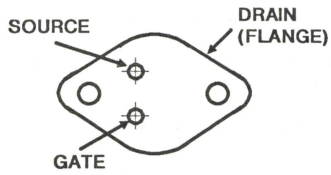
Description

The RFM15N12 and RFM15N15 and the RFP15N12 and RFP15N15 are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

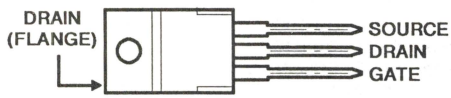
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

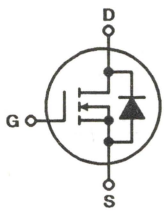


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	RFM15N12	RFM15N15	RFP15N12	RFP15N15	UNITS
Drain-Source Voltage ..... V_{DSS}	120	150	120	150	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	120	150	120	150	V
Continuous Drain Current					
RMS Continuous ..... I_D	15	15	15	15	A
Pulsed Drain Current ..... I_{DM}	40	40	40	40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	100	100	75	75	W
Above T_C = +25°C, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1443**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM15N12 RFP15N12 MIN.	LIMITS RFM15N12 RFP15N12 MAX.	LIMITS RFM15N15 RFP15N15 MIN.	LIMITS RFM15N15 RFP15N15 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V V_{DS} = 120 V T_C = 125° C V_{DS} = 100 V V_{DS} = 120 V	— — — —	1 — 50 —	— — — —	— 1 — 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.5 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 15 A V_{GS} = 10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.5 A V_{GS} = 10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 7.5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	750	—	750	
Reverse Transfer Capacitance	C_{rss}		—	350	—	350	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V I_D = 7.5 A R_{gen} = R_{gs} = 50 Ω V_{GS} = 10 V	50(typ.)	75	50(typ.)	75	ns
Rise Time	t_r		150(typ.)	225	150(typ.)	225	
Turn-Off Delay Time	$t_d(off)$		185(typ.)	280	185(typ.)	280	
Fall Time	t_f		125(typ.)	190	125(typ.)	190	
Thermal Resistance Junction-to-Case	RθJC	RFM15N12, RFM15N15	—	1.25	—	1.25	°C/W
		RFP15N12, RFP15N15	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM15N12 RFP15N12 MIN.	LIMITS RFM15N12 RFP15N12 MAX.	LIMITS RFM15N15 RFP15N15 MIN.	LIMITS RFM15N15 RFP15N15 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

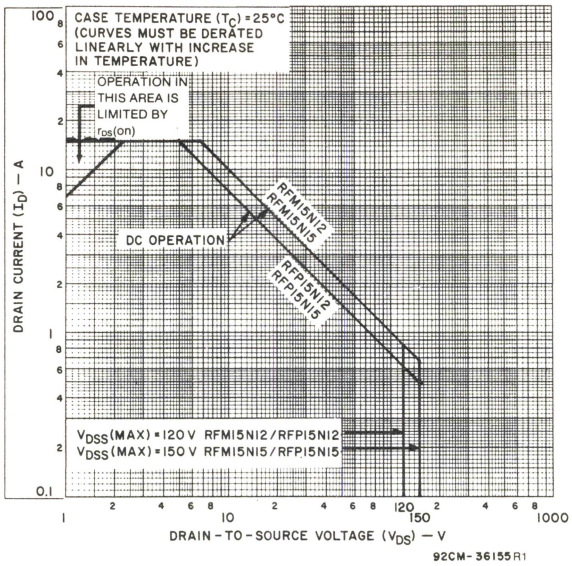


Fig. 1 — Maximum operating areas for all types.

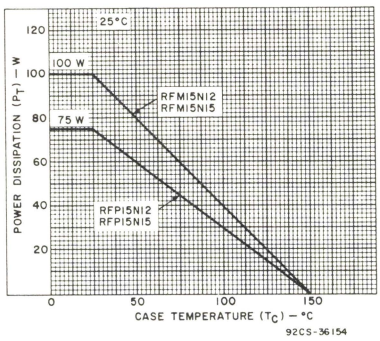


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

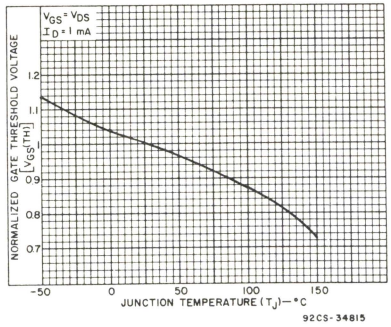


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

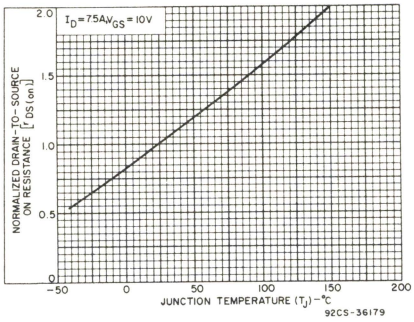


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

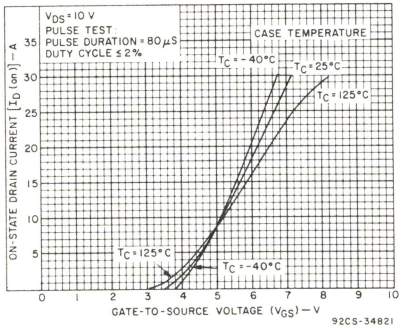


Fig. 5 — Typical transfer characteristics for all types.

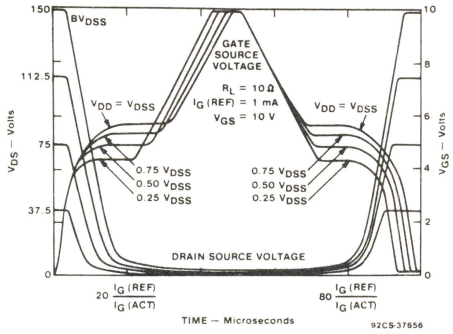


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

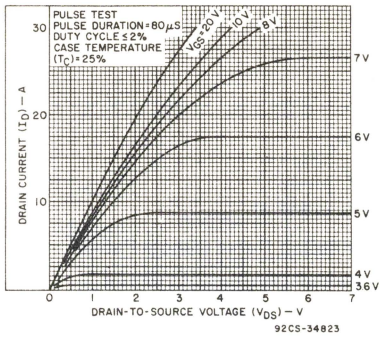


Fig. 7 — Typical saturation characteristics for all types.

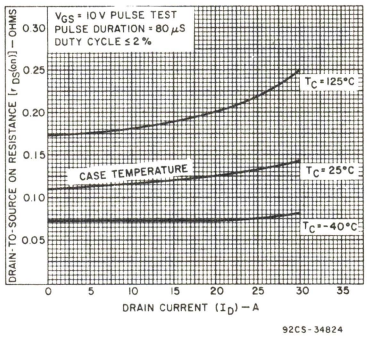


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

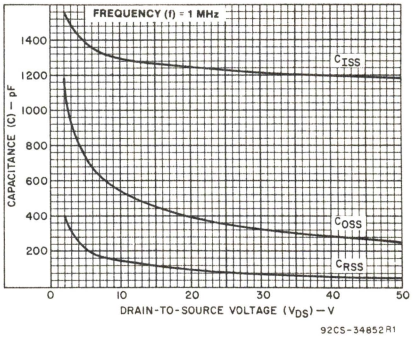


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

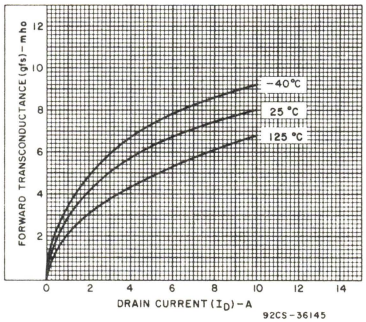


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

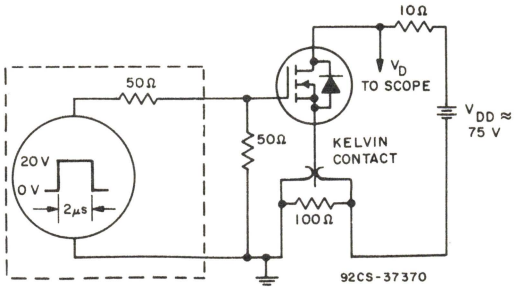


Fig. 11 — Switching Time Test Circuit

HARRIS

RFD16N05
RFD16N05SM

N-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

May 1992

Features

- 16A, 50V
- $r_{DS(on)} = 0.047\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

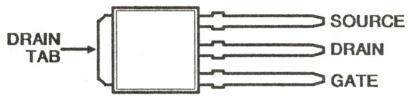
Description

The RFD16N05 and RFD16N05SM n-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

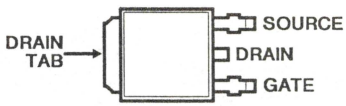
The RFD16N05 is supplied in the JEDEC TO-251AA plastic package and the RFD16N05SM in the TO-252AA plastic package.

Packages

TO-251AA
TOP VIEW

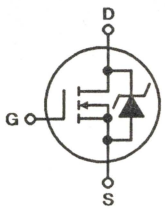


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 50V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR} 50V
Gate-Source Voltage, V_{GS} ..... ±20V
Drain Current:
  RMS Continuous, I_D 16A
  Pulsed, I_{DM} 45A
Single Pulse Avalanche Rating, Refer to UIS SOA
Power Dissipation, P_D:
  T_C = +25°C 72W
  Derate Above T_C = +25°C ..... 0.48W/°C
Operating and Storage Junction
Temperature Range, T_J, T_{STG} ..... -55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **2267.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS} = V_{DS}$, I_D = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150°C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 16 A, V_{GS} = 10 V		—	0.047	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 8 A $I_{g1} = I_{g2}$ = 0.4 A V_{GS} (clamp) + 10 V, −0.6 V R_L = 3.125 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	14 (typ.)	ns
Rise Time	t_r			—	30 (typ.)	ns
Turn-Off Delay Time	$t_d(off)$			—	52 (typ.)	ns
Fall Time	t_f			—	16 (typ.)	ns
Turn-Off Time	t(off)			—	100	ns
Total Gate Charge	Q_g(total)	V_{GS} = 0-20 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 10 V	$Q_g(10)$	V_{GS} = 0-10 V	I_D = 16 A	—	45	nC
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-2 V	R_L = 2.5 Ω	—	3	nC
Plateau Voltage	V(plateau)	I_D = 16 A, V_{DS} = 15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 8 A, R_L = 3.125 Ω L = 0.2 μH, $I_{g1} = I_{g2}$ = 0.4 A V_{GS} (clamp) + 10 V, −0.6 V		—	19	μJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			—	2.083	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			—	100	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16 A, dI_F/d_t = 100 A/μs	—	125	ns

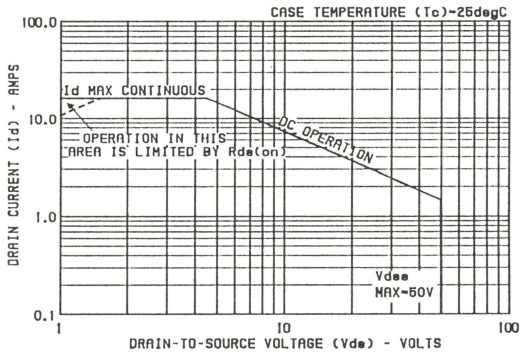


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

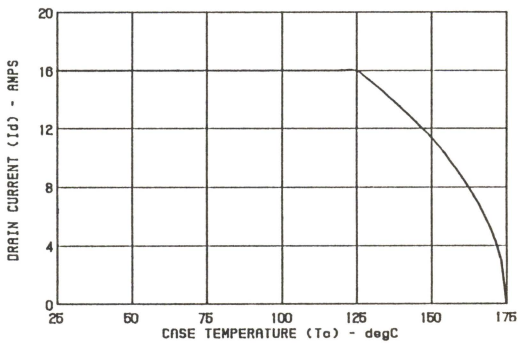


Fig. 2 - Maximum continuous drain current vs. temperature.

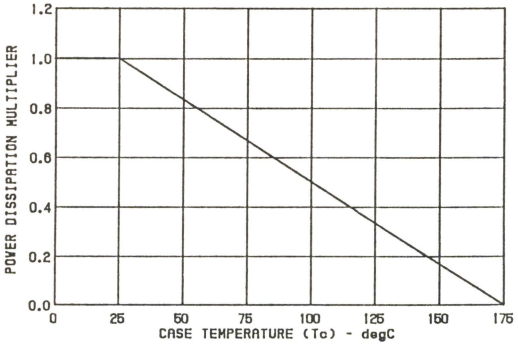


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

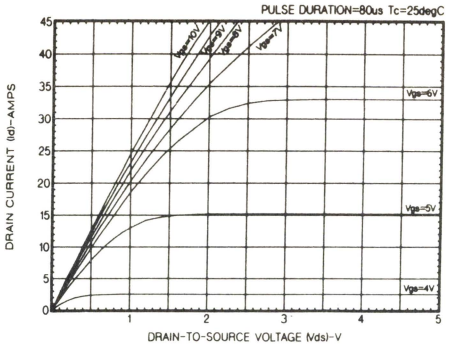


Fig. 4 - Typical saturation characteristics.

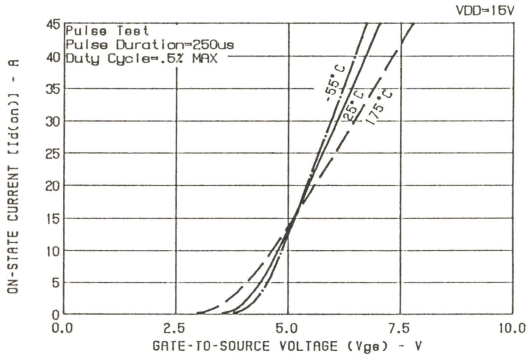


Fig 5 - Typical transfer characteristics.

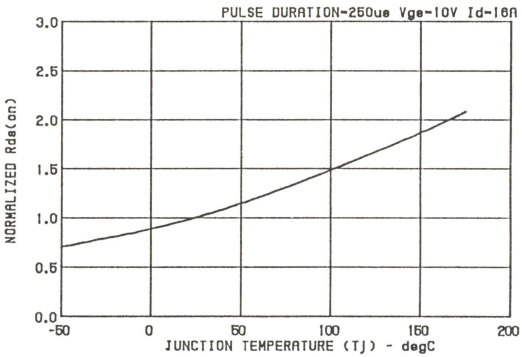


Fig 6 - Normalized $R_{ds}(on)$ vs. junction temperature.

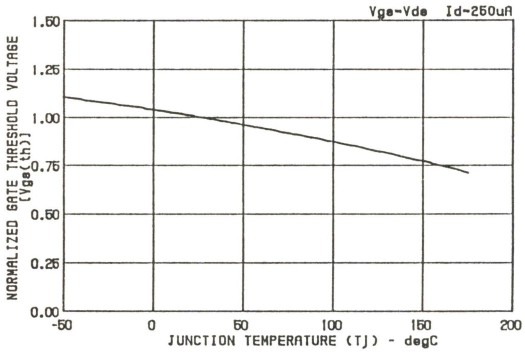


Fig. 7 - Normalized gate threshold voltage.

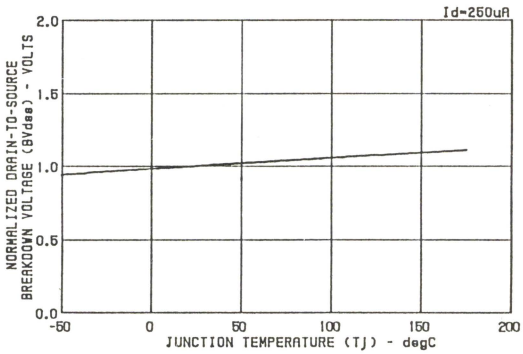


Fig. 8 - Normalized drain source breakdown voltage vs. temperature.

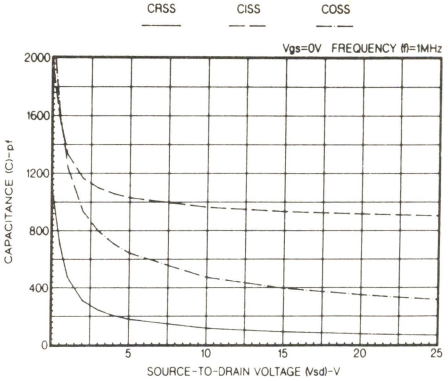


Fig. 9 - Typical capacitance vs. voltage.

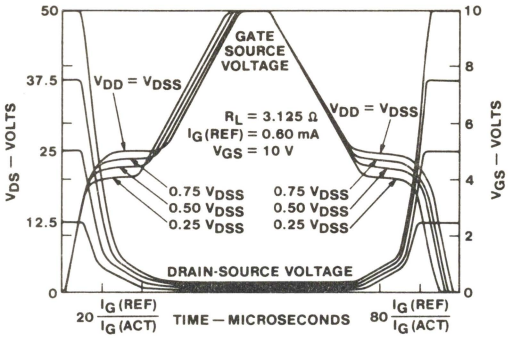
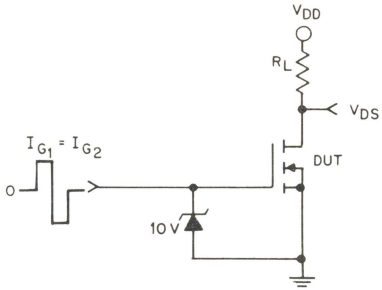
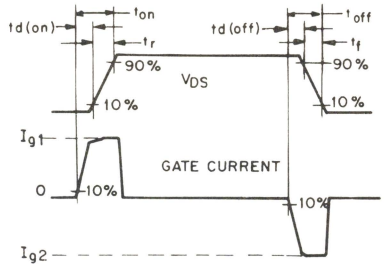


Fig. 10 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.



Switching Test Circuit



Switching Waveforms

Fig. 11 - Resistive Switching.

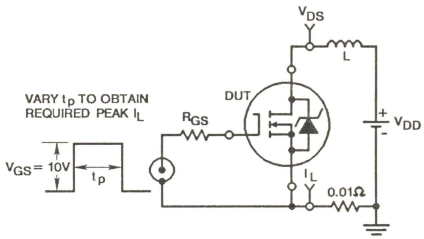


Fig. 12 - Unclamped energy test circuit.

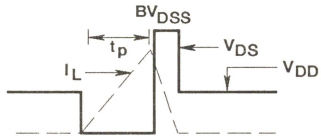


Fig. 13 - Unclamped energy waveforms.

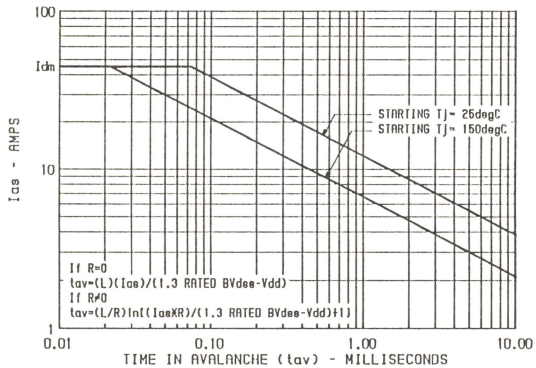


Fig. 14 - Unclamped-Inductive-Switching SOA. (Single Pulse UIS SOA)

HARRIS

RFM18N08/18N10
RFP18N08/18N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 18A, 80V and 100V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

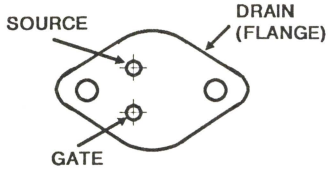
Description

The RFM18N08 and RFM18N10 and the RFP18N08 and RFP18N10 are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

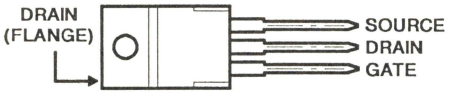
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

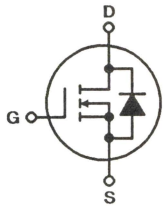


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFM18N08	RFM18N10	RFP18N08	RFP18N10	UNITS
Drain-Source Voltage ..... V_{DSS}	80	100	80	100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	18	18	18	18	A
Pulsed Drain Current ..... I_{DM}	45	45	45	45	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	100	100	75	75	W
Above $T_C = +25^oC$, Derate Linearly	0.8	0.8	0.6	0.6	$W/^oC$
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1446**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFP18N08 MIN.	MAX.	LIMITS RFM18N10 RFP18N10 MIN.	MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V	—	1	—	—	μA
		V_{DS} = 80 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 65 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 9 A, V_{GS} = 10 V	—	0.9	—	0.9	V
		I_D = 18 A, V_{GS} = 10 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 9 A, V_{GS} = 10 V	—	0.10	—	0.10	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 9 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	750	—	750	
Reverse Transfer Capacitance	C_{rss}		—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V, I_D = 9 A, R_{gen} = R_{gs} = 50 Ω, V_{GS} = 10 V	60(typ.)	90	60(typ.)	90	ns
Rise Time	t_r		300(typ.)	450	300(typ.)	450	
Turn-Off Delay Time	$t_d(off)$		150(typ.)	225	150(typ.)	225	
Fall Time	t_f		150(typ.)	225	150(typ.)	225	
Thermal Resistance Junction-to-Case	RθJC	RFM18N08, RFM18N10	—	1.25	—	1.25	°C/W
		RFP18N08, RFP18N10	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFM18N10 MIN.	MAX.	LIMITS RFP18N08 RFP18N10 MIN.	MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=9 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

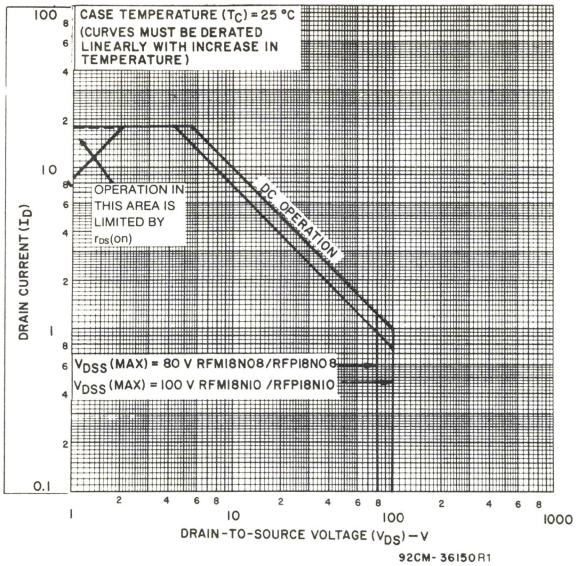


Fig. 1 — Maximum operating areas for all types.

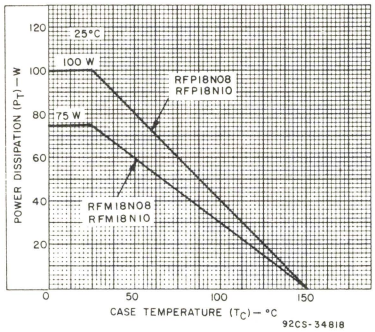


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

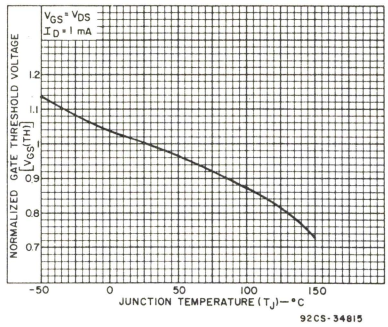


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

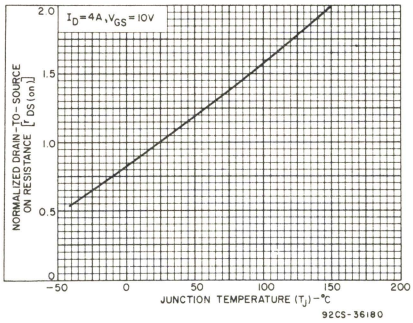


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

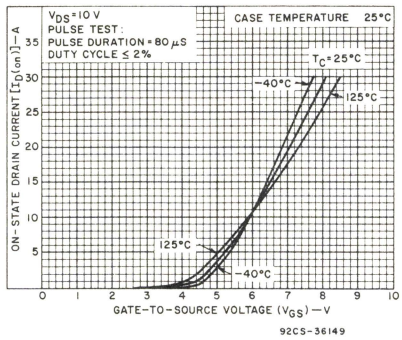


Fig. 5 — Typical transfer characteristics for all types.

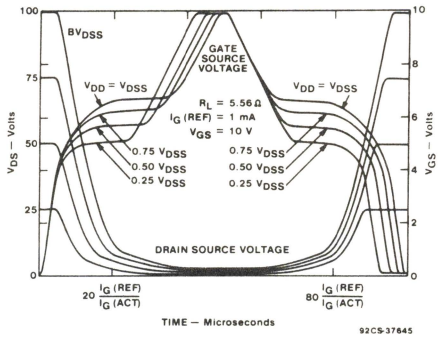


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

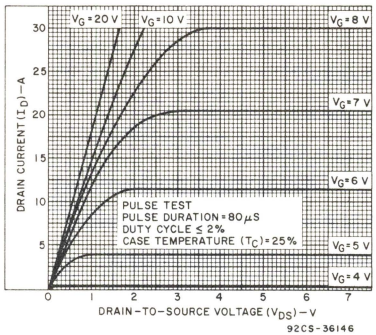


Fig. 7 — Typical saturation characteristics for all types.

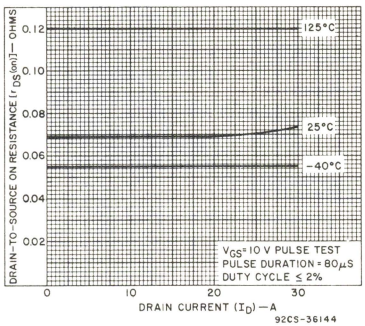


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

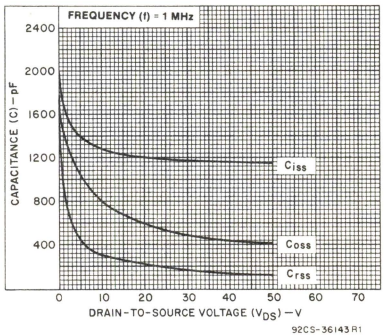


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

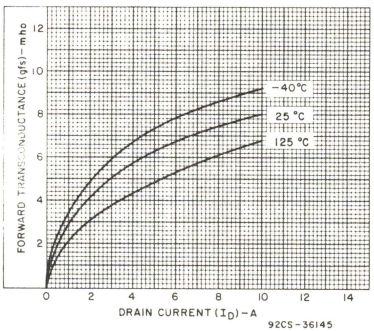


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

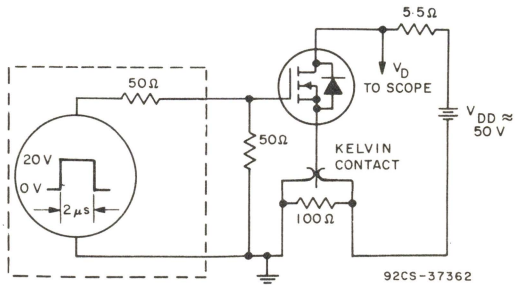


Fig. 11 — Switching Time Test Circuit

HARRIS

RFP22N10

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

August 1991

Features

- 22A, 100V
- $r_{DS(on)} = 0.080\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

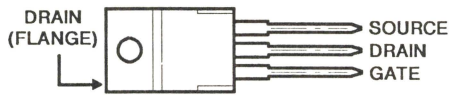
Description

The RFP22N10 n-channel power MOSFETs is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFP22N10 was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. This transistor can be operated directly from integrated circuits.

The RFP22N10 is supplied in the JEDEC TO-220AB plastic package.

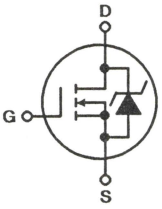
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP22N10	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	100	V
Continuous Drain Current	I_D	22	A
Pulsed Drain Current	I_{DM}	50	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	100	W
Derated Above T_C = 25°C		0.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve			

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2385.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=0.25 mA, V_{GS}=0 V		100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=0.25 mA		2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V T_C=150°C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D=22 A, V_{GS}=10 V		—	0.080	Ω
Turn-On Time	t(on)	V_{DD}=50 V, I_D=11 A I_{g1}=I_{g2}=0.6 A V_{GS} (clamp): +10 V, -0.6 V R_L=4.55 Ω (See Fig. 12)		—	60	ns
Turn-On Delay Time	$t_d(on)$			13 (typ.)	—	
Rise Time	t_r			24 (typ.)	—	
Turn-Off Delay Time	$t_d(off)$			65 (typ.)	—	
Fall Time	t_f			18 (typ.)	—	
Turn-Off Time	t(off)			—	120	
Total Gate Charge	Q_g(total)	V_{GS}=0 to 20V	V_{DD}=80 V	—	150	nC
Gate Charge at 10 V	Q_g(10)	V_{GS}=0 to 10V	I_D=22 A	—	75	
Threshold Gate Charge	Q_g(th)	V_{GS}=0 to 2V	R_L=3.64 Ω	—	3.5	
Plateau Voltage	V(plateau)	I_D=22 A, V_{DS}=15 V		—	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD}=50V, I_D=11A, R_L=4.55Ω L=0.2 μH, I_{g1}=I_{g2}=0.6 A V_{GS} (clamp): +10 V, -0.6 V		—	80	μJ
Thermal Resistance, Junction to Case	$R\theta_{JC}$			—	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$			—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=22 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F=22 A, dI_F/d_t=100 A/μs	—	200	ns

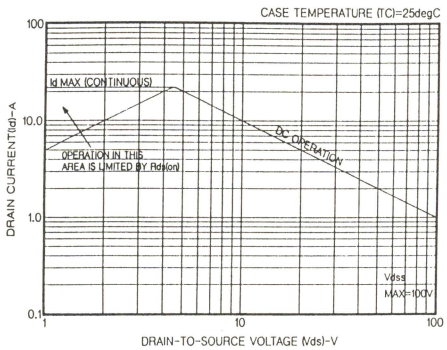


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in temperature.)

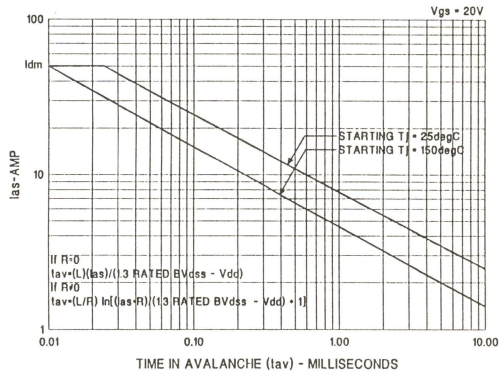


Fig. 2 - Unclamped-inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Fig. 13 for test circuit.

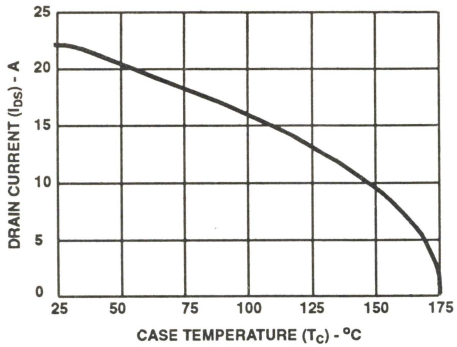


Fig. 3 - Maximum continuous drain current vs. temperature.

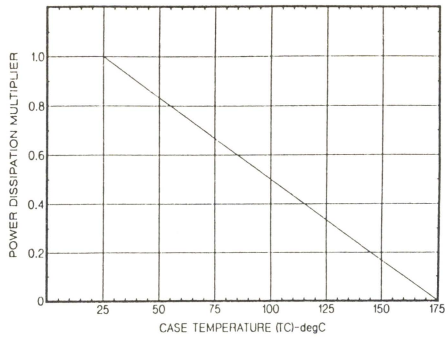


Fig. 4 - Normalized power dissipation vs. temperature derating curve.

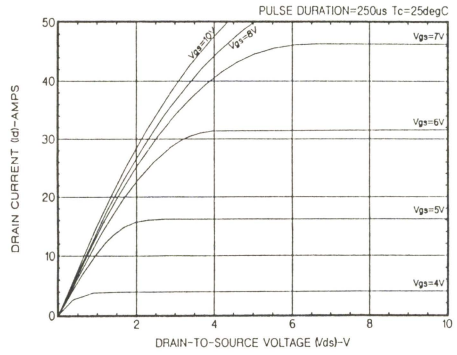


Fig. 5 - Typical saturation characteristics.

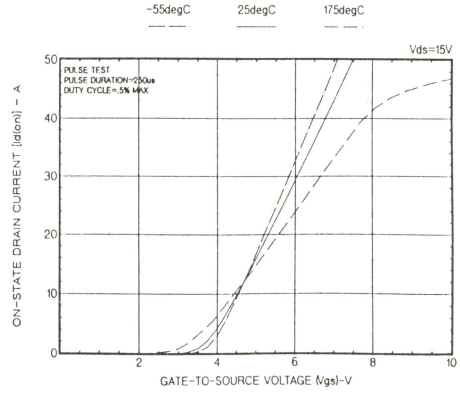


Fig. 6 - Typical transfer characteristics.

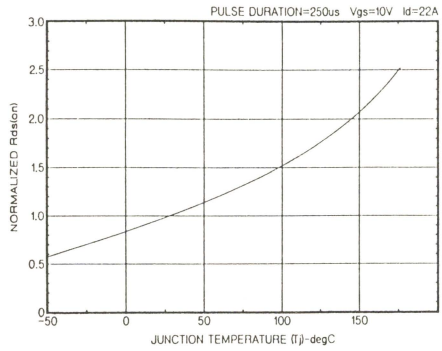


Fig. 7 - Normalized $r_{DS}(on)$ vs. junction temperature.

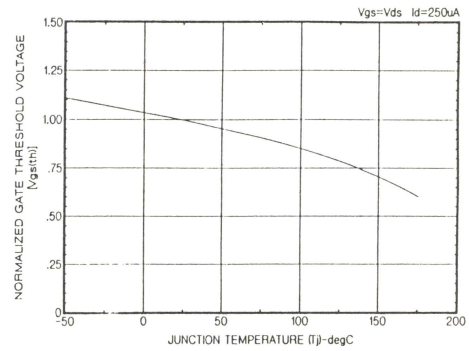


Fig. 8 - Normalized gate threshold voltage.

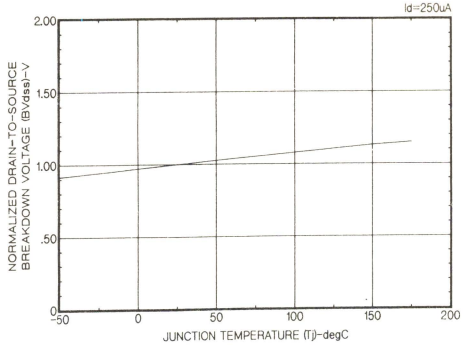


Fig. 9 - Normalized drain source breakdown voltage vs. temperature.

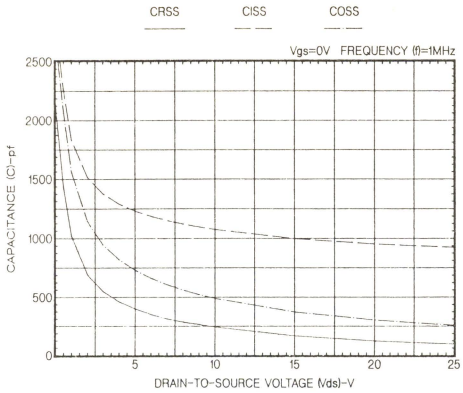


Fig. 10 - Typical capacitance vs. voltage.

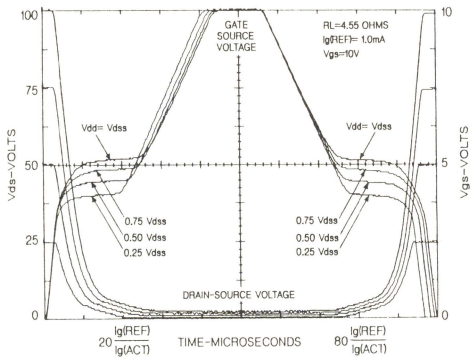


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

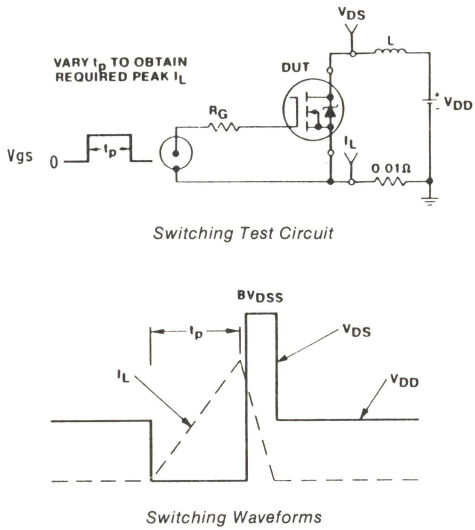


Fig. 12 - Resistive switching.

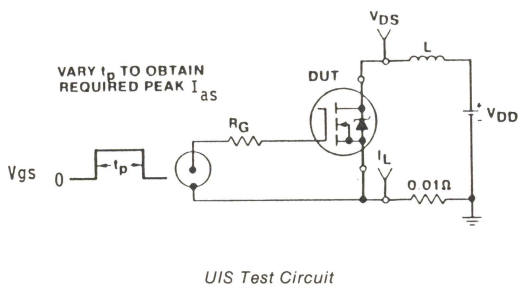


Fig. 13 - Unclamped-inductive-switching test.

HARRIS

RFP25N05

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

August 1991

Features

- 25A, 50V
- $r_{DS(on)} = 0.047\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

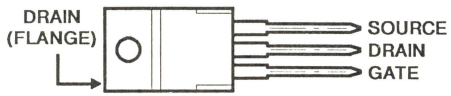
Description

The RFP25N05 n-channel power MOSFETs is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05 was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. This transistor can be operated directly from integrated circuits.

The RFP25N05 is supplied in the JEDEC TO-220AB plastic package.

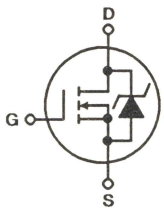
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

		RFP25N05	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	50	V
Continuous Drain Current	I_D	25	A
Pulsed Drain Current	I_{DM}	65	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
$T_C = +25^oC$	P_D	72	W
Derated Above $T_C = 25^oC$		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve			

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2112.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =80V, V_{GS} = 0V		-	-	1	µA
		T_C =+150°C		-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 25A, V_{GS} = 10V		-	-	0.047	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 12.5A		-	-	60	ns
Turn-On Delay Time	$t_{d(on)}$	R_L = 2Ω		-	14	-	ns
Rise Time	t_r	$I_{G1} = I_{G2}$ = 0.5A		-	30	-	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS(clamp)}$ = +10V, -0.6V		-	45	-	ns
Fall Time	t_f			-	14	-	ns
Turn-Off Time	$t_{(off)}$			-	-	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0 - 20V	V_{DD} = 40V	-	-	80	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0 - 10V	I_D = 25A	-	-	45	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0 - 2V	R_L = 1.6Ω	-	-	3	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 25A, V_{DS} = 15V		-	-	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 12.5A, $I_{G1} = I_{G2}$ = 0.5A $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 2Ω		-	-	30	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	2.083	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 25A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 25A, dI_f/dt = 100A/µs	-	-	125	ns

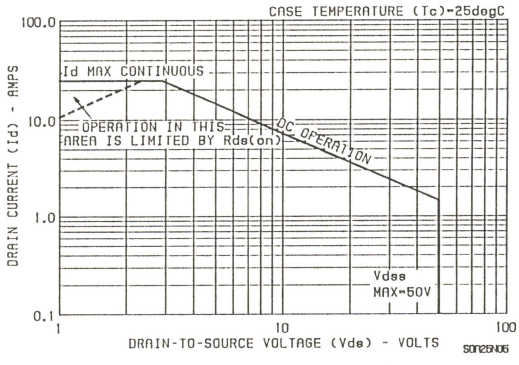


FIGURE 1. SAFE-OPERATING-AREA CURVE (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

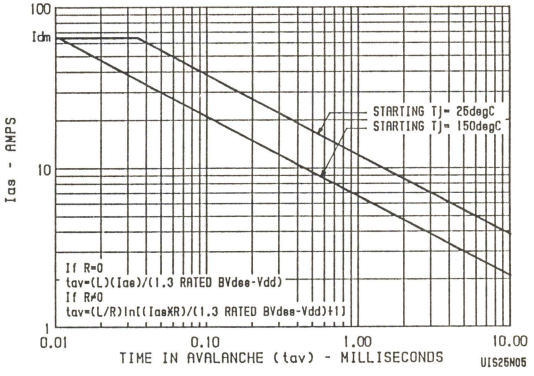


FIGURE 2. UNCLAMPED -INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

Performance Curves

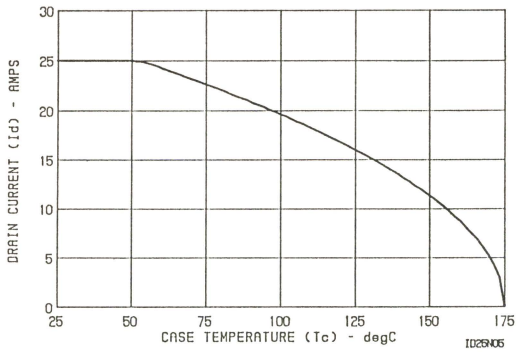


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

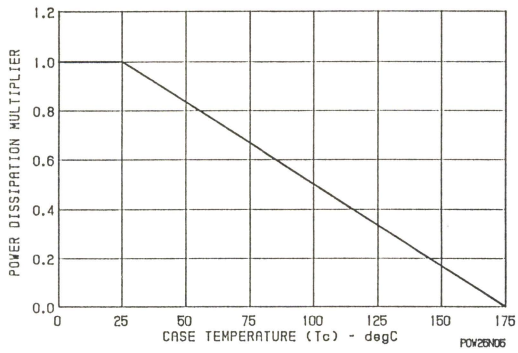


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

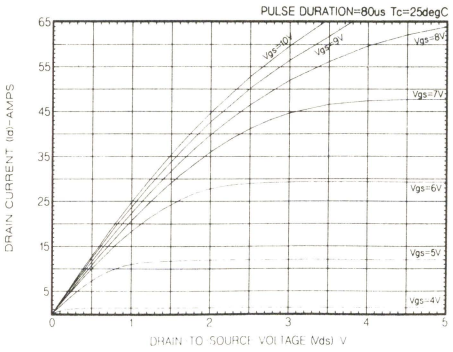


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

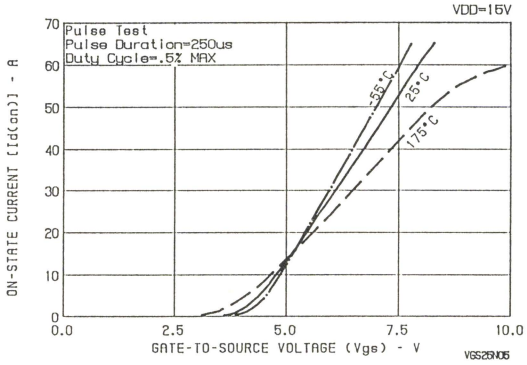


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

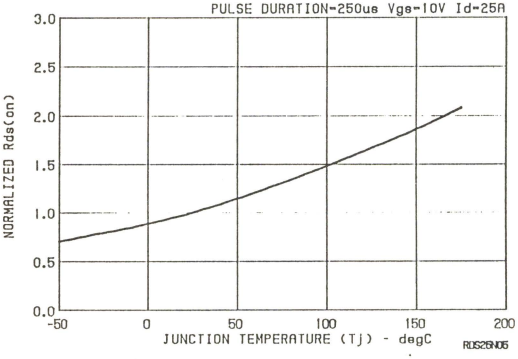


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

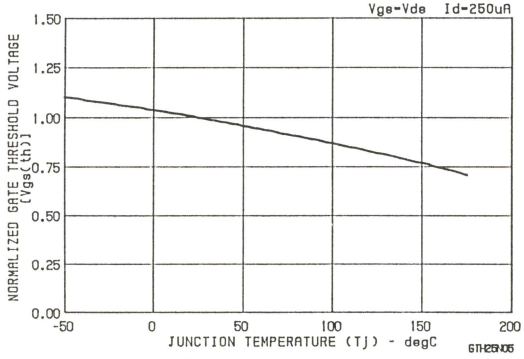


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

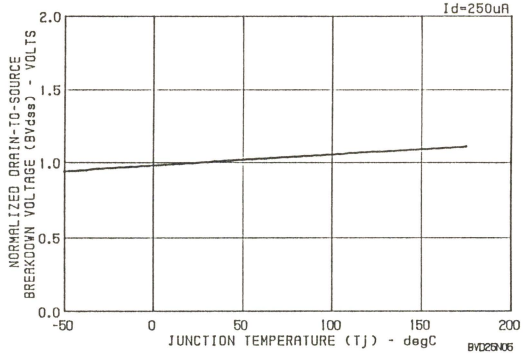


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

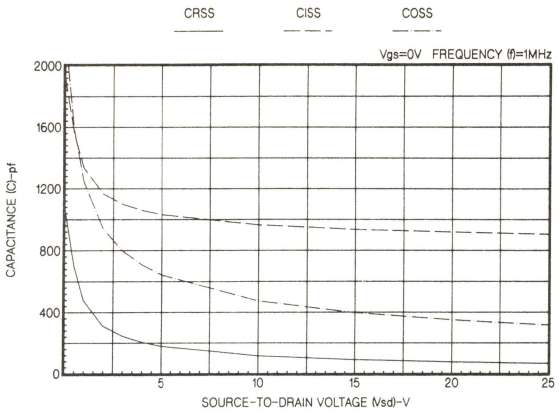


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

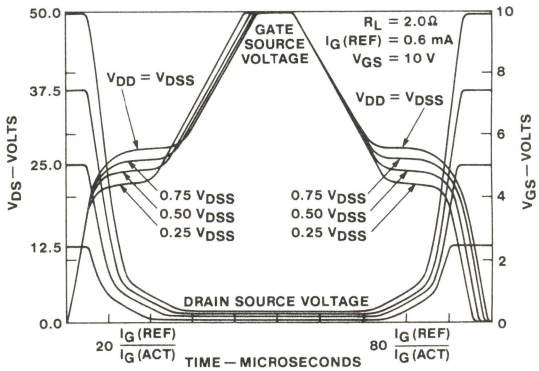


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

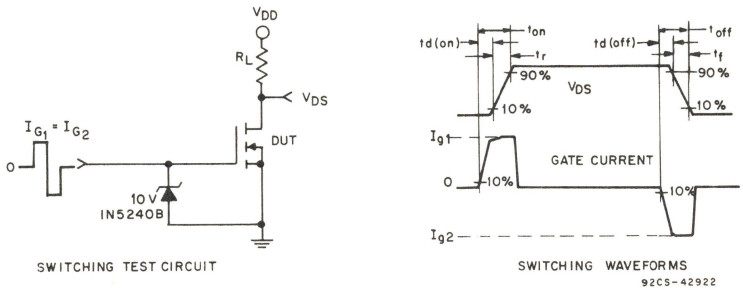


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

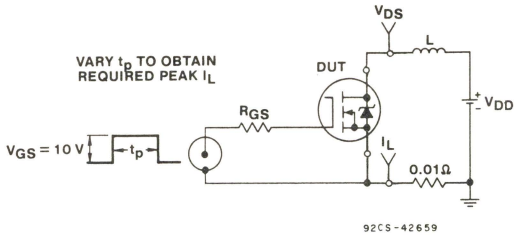


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

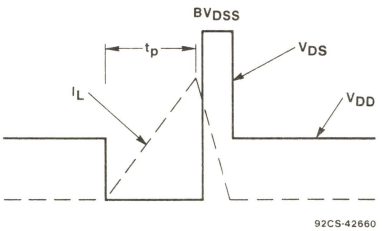


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

HARRIS

RFH25N18
RFH25N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 25A, 180V and 200V
- $r_{DS}(on) = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Carrier, Low-Inductance Package

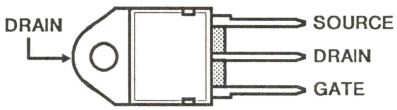
Description

The RFH25N18 and RFH25N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

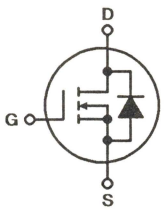
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH25N18	RFH25N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current	I_D	25	25	A
Pulsed Drain Current	I_{DM}	60	60	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1631.1

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145 V	—	1	—	—	μA
		V_{DS} = 160 V	—	—	—	1	
		T_C = 125°C V_{DS} = 145 V	—	50	—	—	
		V_{DS} = 160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	1.875	—	1.875	V
		I_D = 25 A V_{GS} = 10 V	—	5	—	5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3500	—	3500	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	900	—	900	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 100 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D = 12.5 A	150(typ)	225	150(typ)	225	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	300(typ)	400	300(typ)	400	
Fall Time	t_f	V_{GS} = 10 V	120(typ)	200	120(typ)	200	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH25N18, RFH25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 12.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	300 (typ.)		300 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

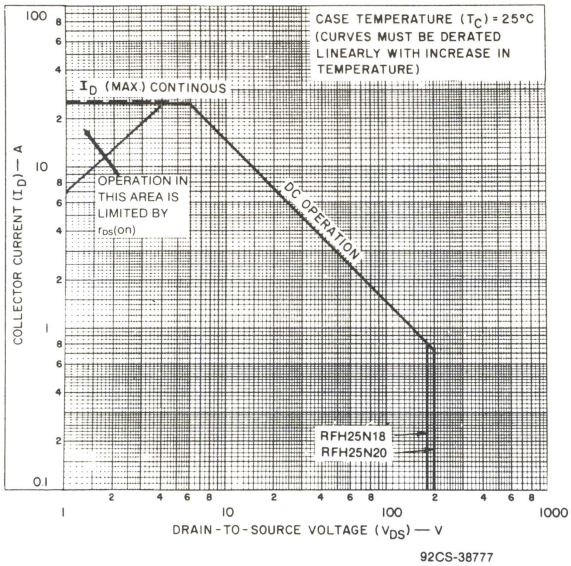


Fig. 1 - Maximum safe operating areas for all types.

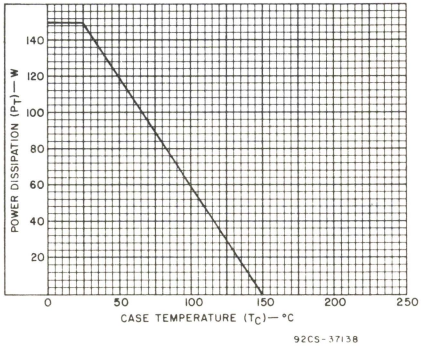


Fig. 2 - Power vs. temperature derating curve for all types.

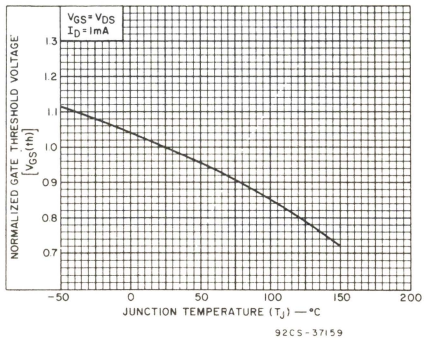


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

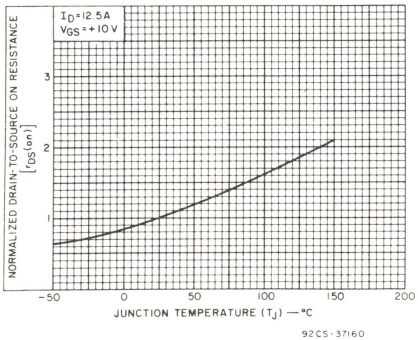


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

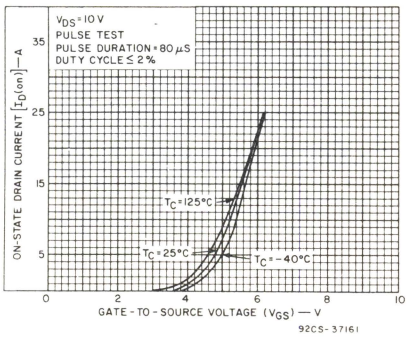


Fig. 5 - Typical transfer characteristics for all types.

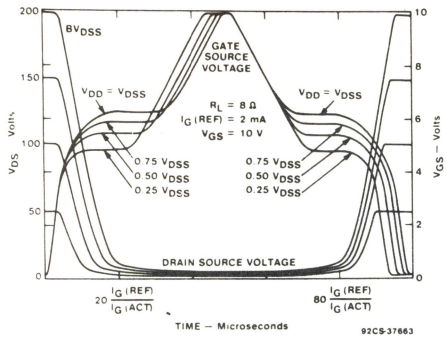


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

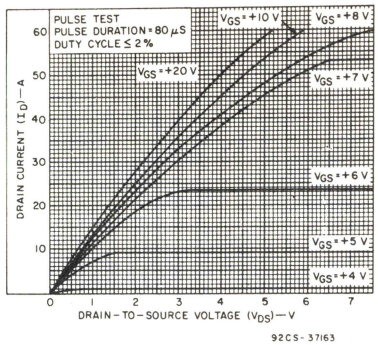


Fig. 7 - Typical saturation characteristics for all types.

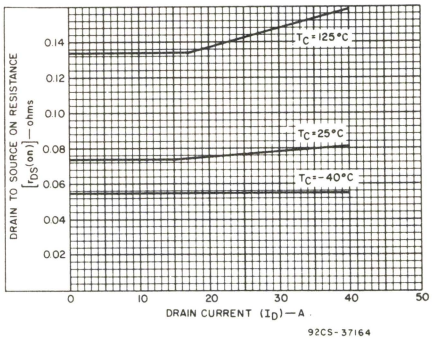


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

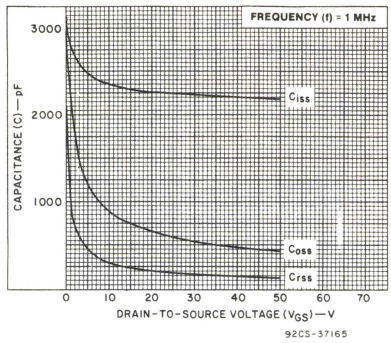


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

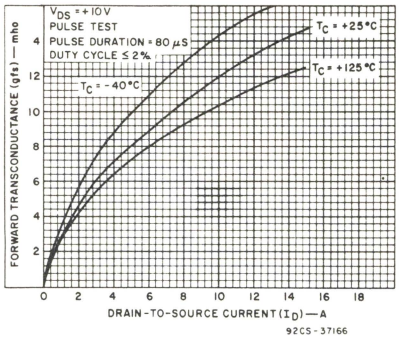


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

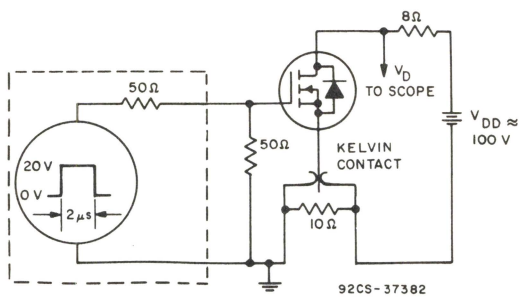


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK25N18
RFK25N20

N-Channel Enhancement-Mode Power Field-Effect Transistors

May 1992

Features

- 25A, 180V and 200V
- $r_{DS}(on) = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

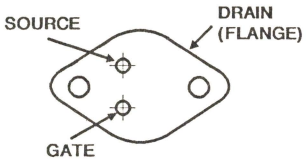
Description

The RFK25N18 and RFK25N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

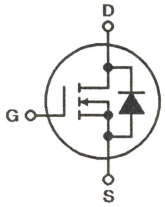
Package

TO-204AE
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK25N18	RFK25N20	UNITS
Drain-Source Voltage	V_{DSS}	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	180	200	V
Continuous Drain Current				
T_C = +25°C	I_D	25	25	A
Pulsed Drain Current	I_{DM}	60	60	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1500.2

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	1.875	—	1.875	V
		I_D=25 A V_{GS}=10 V	—	5	—	5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	3500	—	3500	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V I_D=12.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		150(typ)	225	150(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$		300(typ)	400	300(typ)	400	ns
Fall Time	t_f		120(typ)	200	120(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK25N18, RFK25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300(typ)		300(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

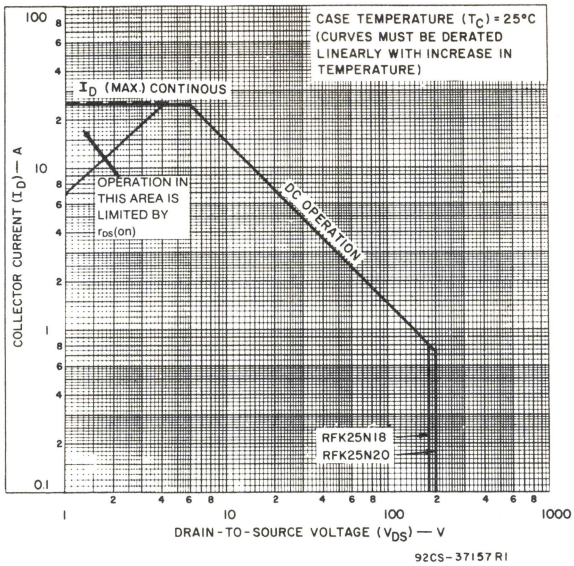


Fig. 1 — Maximum safe operating areas for all types.

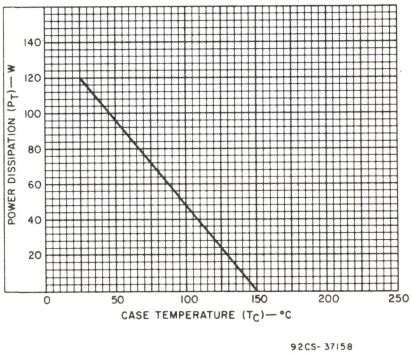


Fig. 2 — Power vs. temperature derating curve for all types.

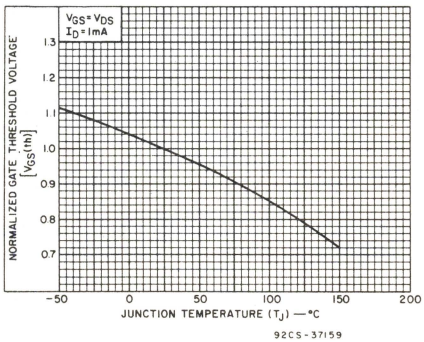


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

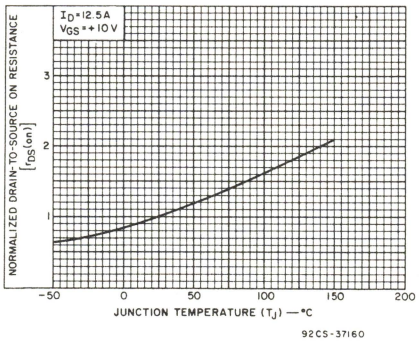


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

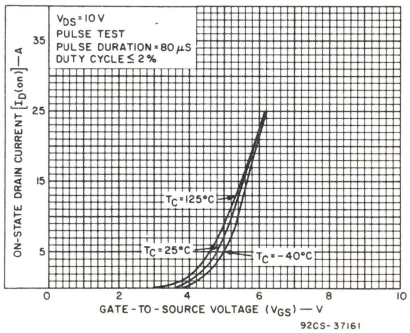


Fig. 5 — Typical transfer characteristics for all types.

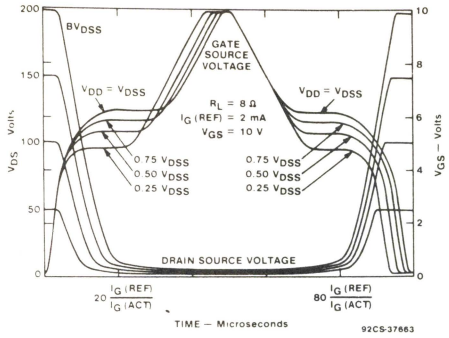


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

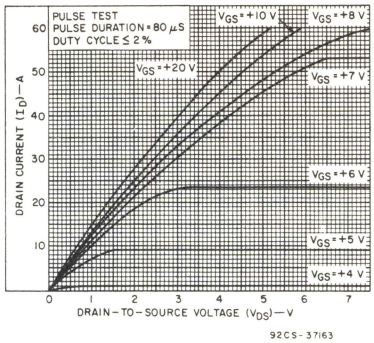


Fig. 7 — Typical saturation characteristics for all types.

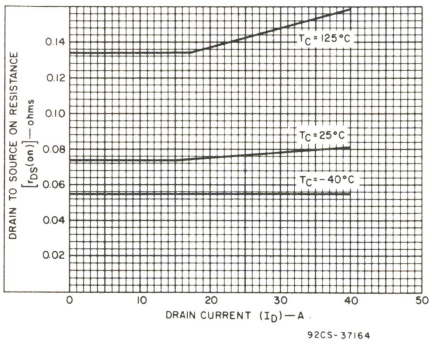


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

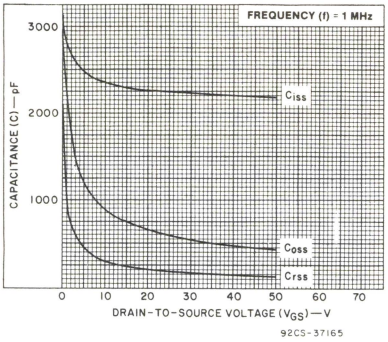


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

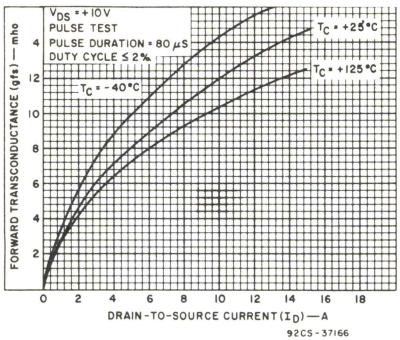


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

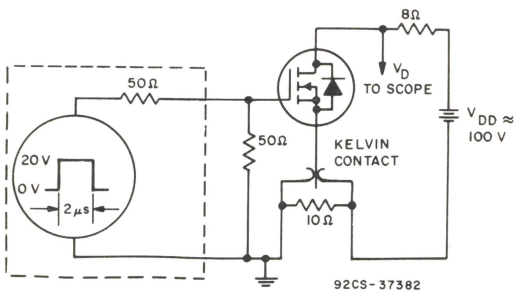


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH30N12
RFH30N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 30A, 120V and 150V
- $r_{DS}(on) = 0.075\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Carrier, Low-Inductance Package

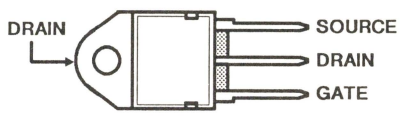
Description

The RFH30N12 and RFH30N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

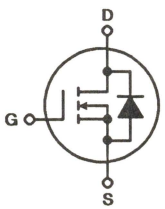
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH30N12	RFH30N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current	I_D	30	30	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

4 N-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **1633.1**

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V V_{DS} = 120 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 100 V V_{DS} = 120 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
On-State Gate Voltage	$V_{GS}(on)$[a]	V_{DS} = 5 V I_D = 15 A	—	8	—	8	V
		V_{DS} = 10 V I_D = 30 A	—	10	—	10	V
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 30 A V_{GS} = 10 V	—	2.65	—	2.65	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1200	—	1200	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	500	—	500	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 75 V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D = 15 A	420(typ)	630	420(typ)	630	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	300(typ)	450	300(typ)	450	ns
Fall Time	t_f	V_{GS} = 10 V	250(typ)	375	250(typ)	375	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH30N12, RFH30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 15A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

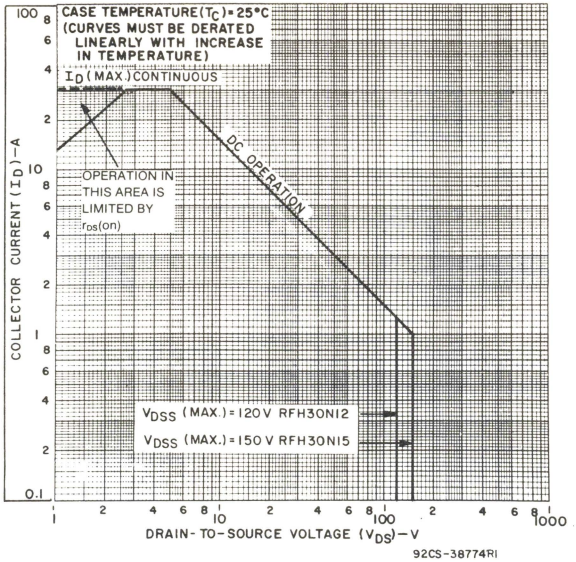


Fig. 1 - Maximum safe operating areas for all types.

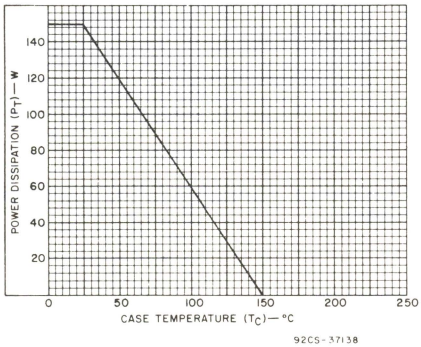


Fig. 2 - Power vs. temperature derating curve for all types.

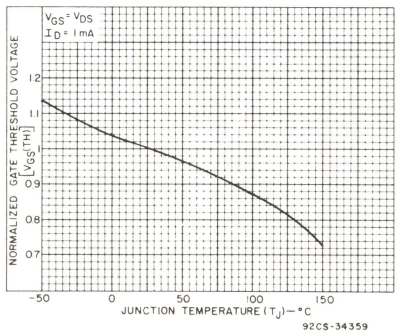


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

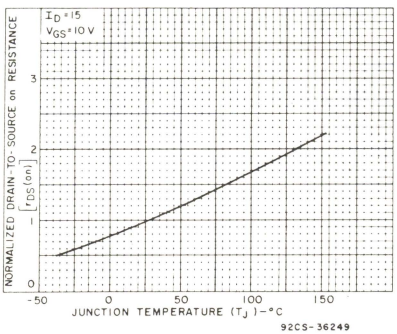


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

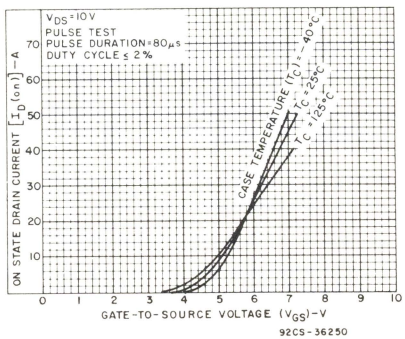


Fig. 5 - Typical transfer characteristics for all types.

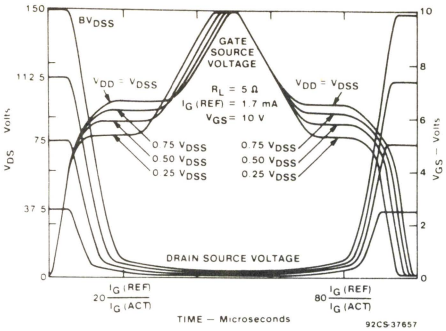


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

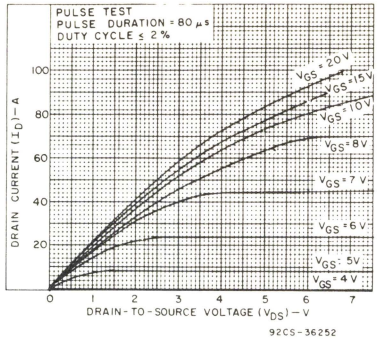


Fig. 7 - Typical saturation characteristics for all types.

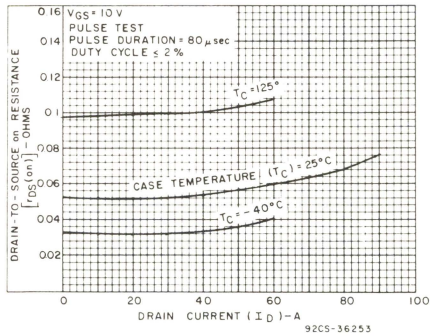


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

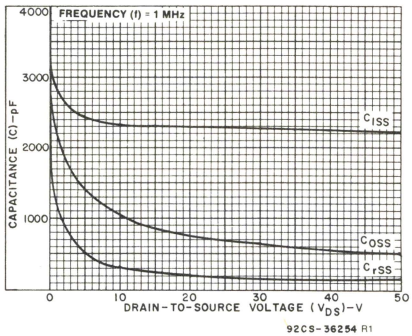


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

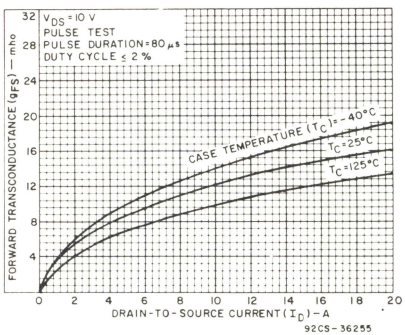


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

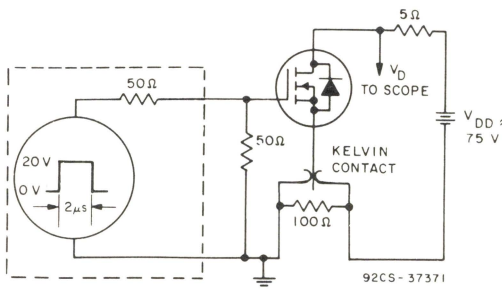


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK30N12
RFK30N15

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 30A, 120V and 150V
- $r_{DS}(on) = 0.075\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

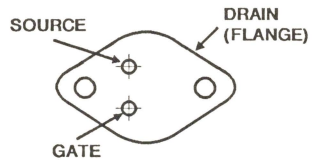
Description

The RFK30N12 and RFK30N15 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

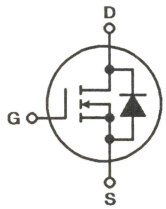
Package

TO-204AE
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK30N12	RFK30N15	UNITS
Drain-Source Voltage	V_{DSS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current				
T_C = +25°C	I_D	30	30	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	120	120	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1455.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125° C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ± 20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	1.125	—	1.125	V
		I_D=30 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D=15 A	420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	300(typ)	450	300(typ)	450	
Fall Time	t_f	V_{GS}=10 V	250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK30N12, RFK30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=15 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

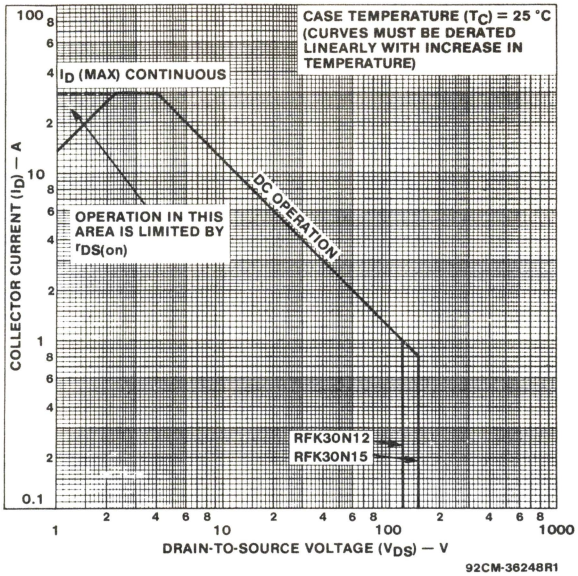


Fig. 1 - Maximum safe operating areas for all types.

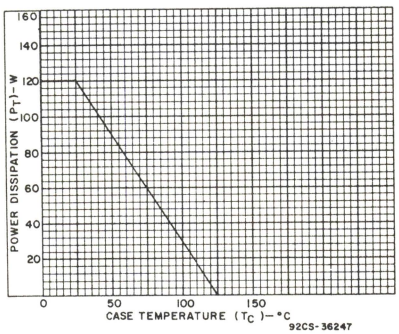


Fig. 2 - Power vs. temperature derating curve for all types.

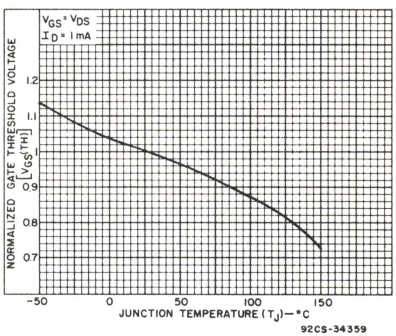


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

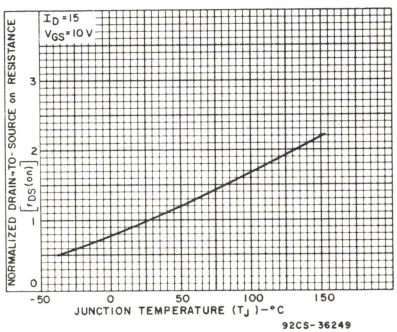


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

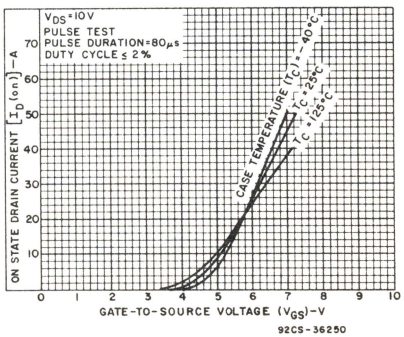


Fig. 5 - Typical transfer characteristics for all types.

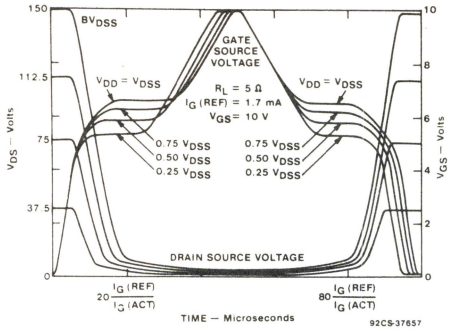


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

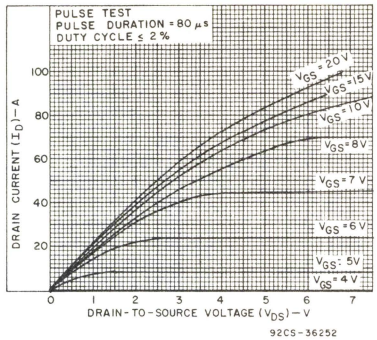


Fig. 7 - Typical saturation characteristics for all types.

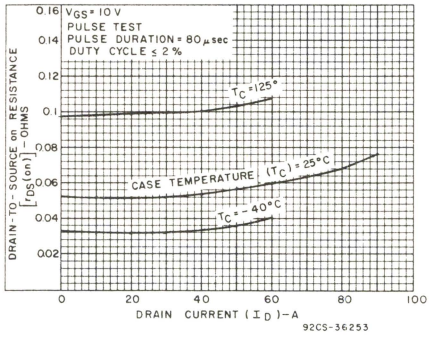


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

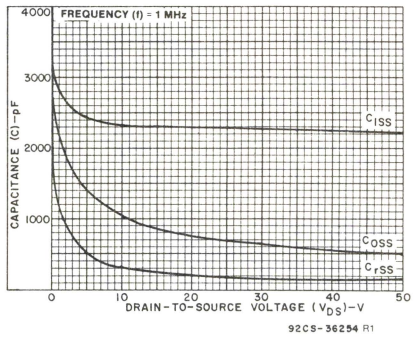


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

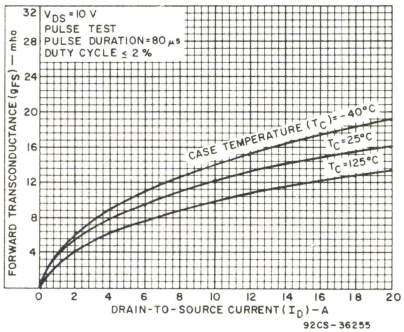


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

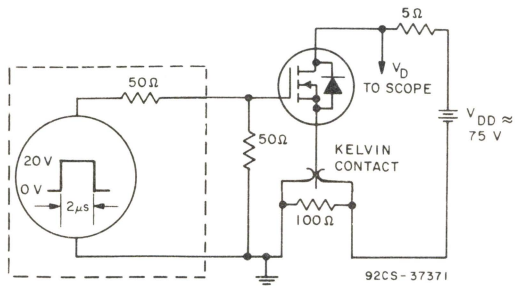


Fig. 11 — Switching Time Test Circuit

HARRIS

RFH35N08
RFH35N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 35A, 80V and 100V
- $r_{DS}(on) = 0.055\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Carrier, Low-Inductance Package

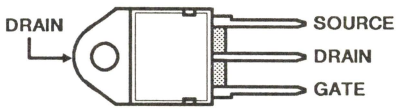
Description

The RFH35N08 and RFH35N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

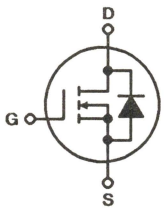
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH35N08	RFH35N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Continuous Drain Current	I_D	35	35	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1634.1

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V	—	1	—	—	μA
		V_{DS} = 80 V	—	—	—	1	
		T_C = 125°C V_{DS} = 65 V	—	50	—	—	
		V_{DS} = 80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.963	—	0.963	V
		I_D = 35 A V_{GS} = 10 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	600	—	600	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r	I_D = 17.5 A	225(typ)	450	225(typ)	450	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	240(typ)	450	240(typ)	450	
Fall Time	t_f	V_{GS} = 10 V	165(typ)	350	165(typ)	350	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH35N08, RFH35N10 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}*	I_{SD} = 17.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

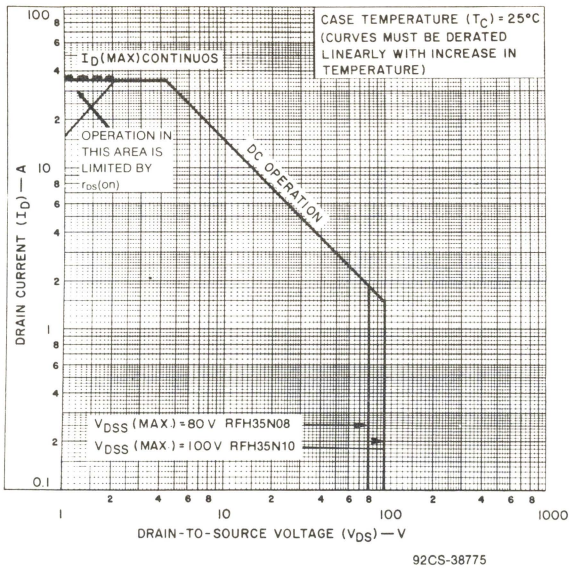


Fig. 1 - Maximum safe operating areas for all types.

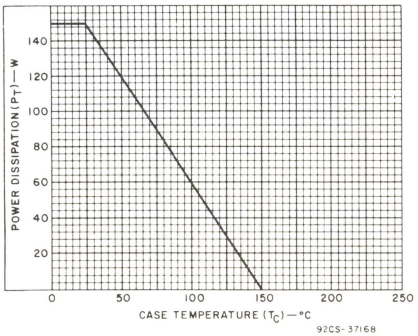


Fig. 2 - Power vs. temperature derating curve for all types.

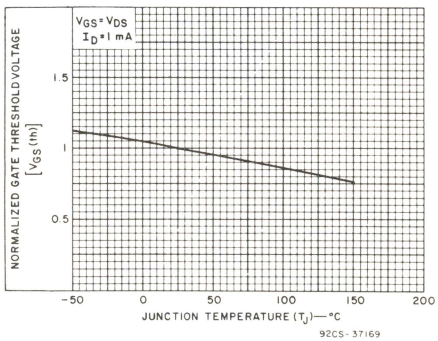


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

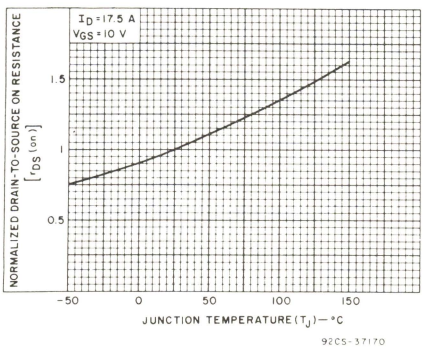
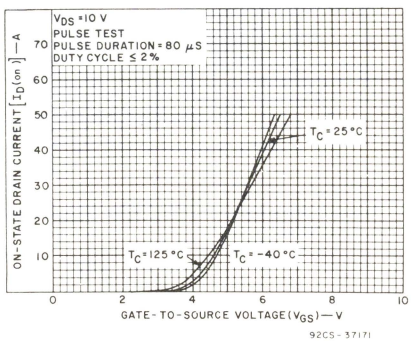


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.



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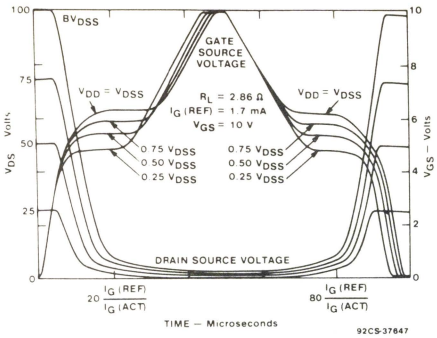

Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

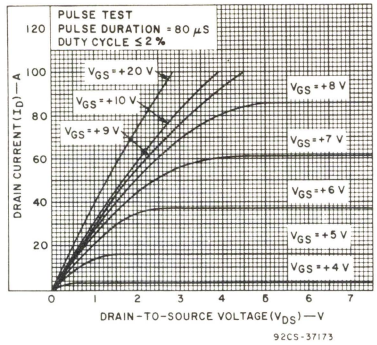

Fig. 7 - Typical saturation characteristics for all types.

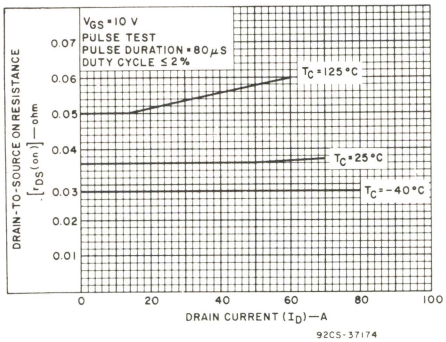

Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

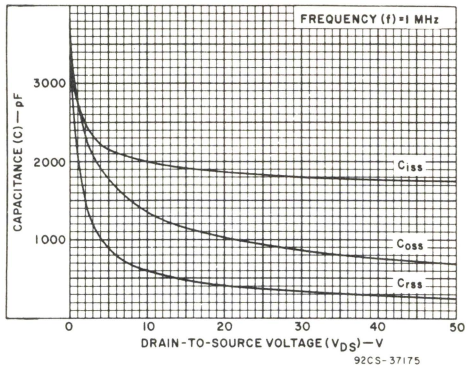

Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

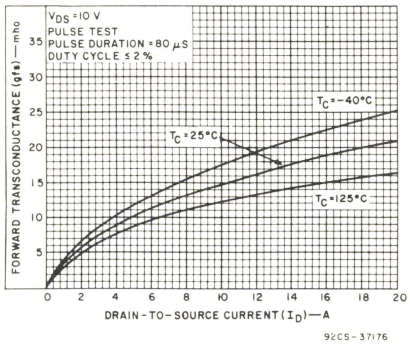

Fig. 10 - Typical forward transconductance as a function of drain current for all types.

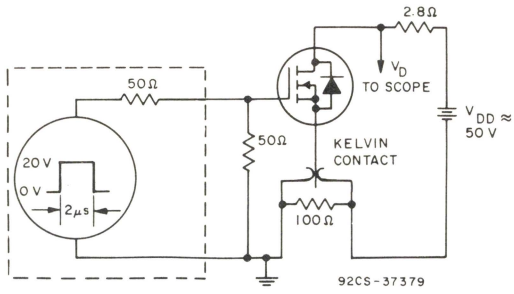

Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK35N08
RFK35N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

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- Majority Carrier Device

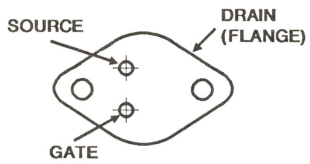
Description

The RFK35N08 and RFK35N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

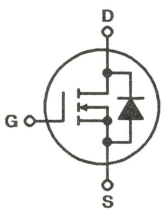
Package

TO-204AE
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK35N08	RFK35N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Continuous Drain Current				
T_C = +25°C	I_D	35	35	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1499.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.9625	—	0.9625	V
		I_D=35 A V_{GS}=10 V	—	3.5	—	3.5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1500	—	1500	pF
Reverse Transfer Capacitance	C_{rss}	f=1 MHz	—	600	—	600	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r	I_D=17.5 A	225(typ)	450	225(typ)	450	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	240(typ)	450	240(typ)	450	ns
Fall Time	t_f	V_{GS}=10 V	165(typ)	350	165(typ)	350	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK35N08, RFK35N10 Series	—	0.83	—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD} [a]	I_{SD}=17.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

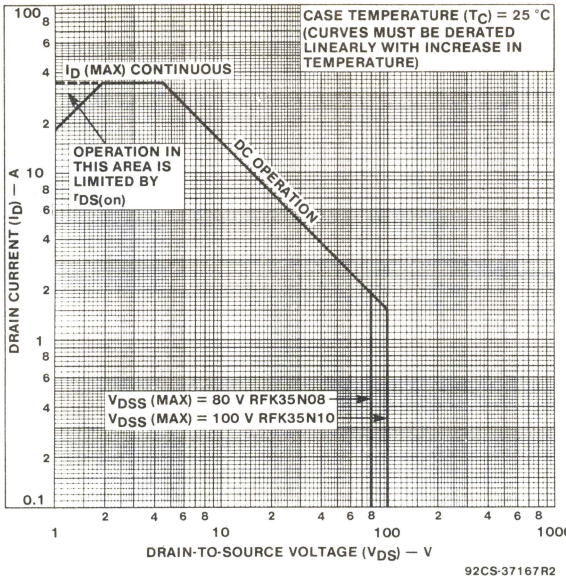


Fig. 1 — Maximum safe operating areas for all types.

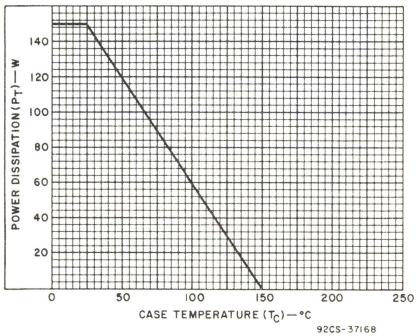


Fig. 2 — Power vs. temperature derating curve for all types.

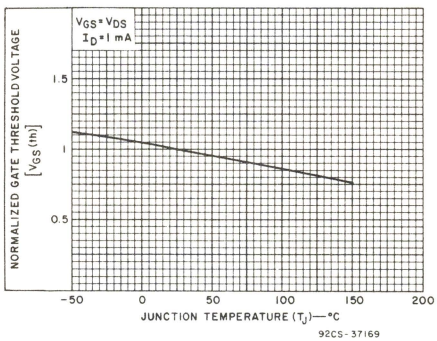


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

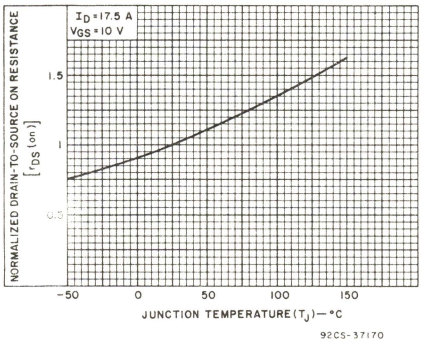


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

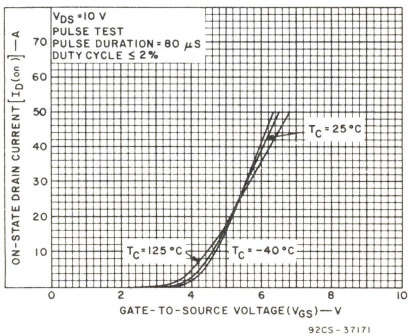


Fig. 5 — Typical transfer characteristics for all types.

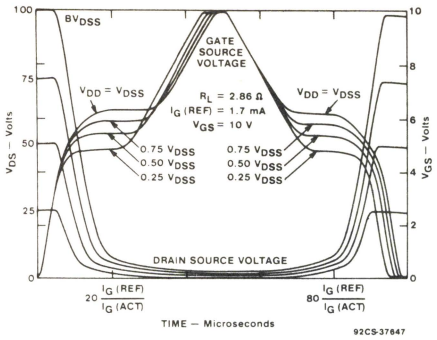


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

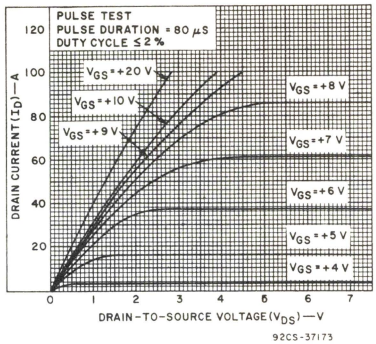


Fig. 7 — Typical saturation characteristics for all types.

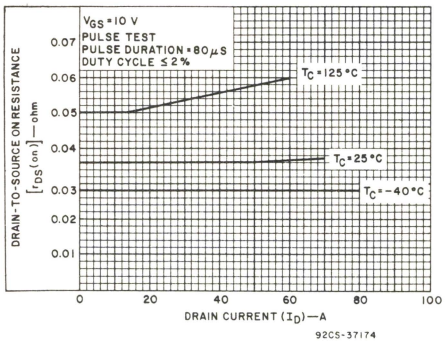


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

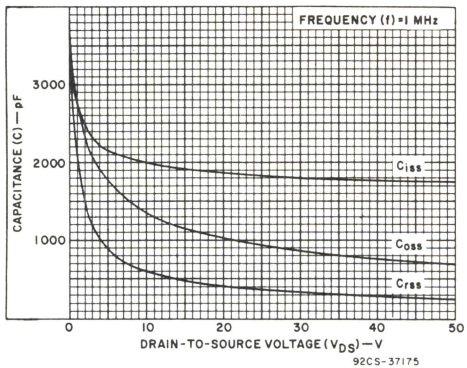


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

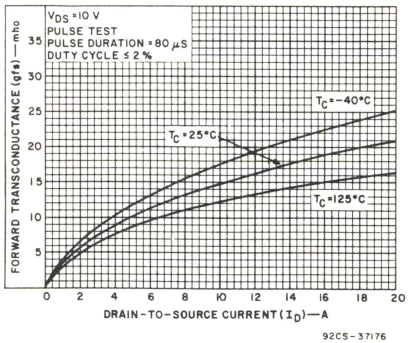


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

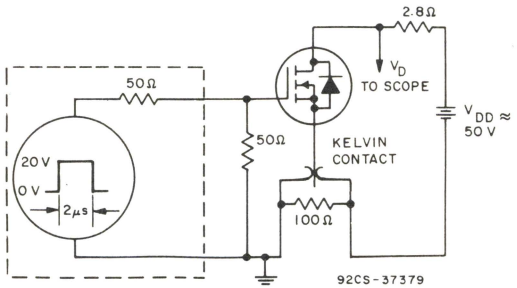


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFG40N10
RFP40N10

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

August 1991

Features

- 40A, 100V
- $r_{DS(on)} = 0.040\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

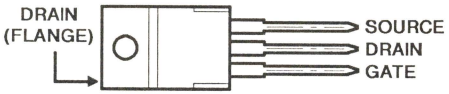
Description

The RFG40N10 and RFP40N10 n-channel ESD rated power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

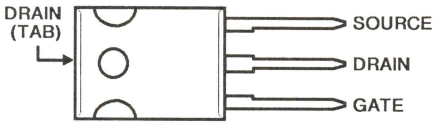
The RFP40N10 is supplied in the JEDEC TO-220AB plastic package and the RFG40N10 is supplied in the TO-247 plastic package.

Package

TO-220AB
TOP VIEW

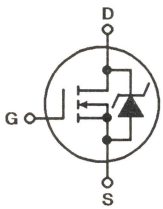


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG40N10 RFP40N10	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	V
Continuous Drain Current	I_D	40	A
Pulsed Drain Current	I_{DM}	100	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	160	W
Derated Above +25°C		1.07	W/°C
Operating and Storage Junction Temperature Range	T_{JC}, T_{STG}	-55 to +175	°C

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2431.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (Tc) = 25°C unless otherwise specified.*

CHARACTERISTICS		TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	ID = 0.25 mA, VGS = 0 V		100	–	V
Gate Threshold Voltage	VGS(th)	VGS = VDS, ID = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	IDSS	VDS = 80 V, VGS = 0 V Tc = 150°C		–	1 50	µA
Gate-Source Leakage Current	IGSS	VGS = ±20 V, VDS = 0 V		–	100	nA
Static Drain-Source on Resistance	rDS(on)	ID = 40 A, VGS = 10 V		–	0.040	Ω
Turn-On Time	t(on)	VDD = 50 V, ID = 20 A Ig1 = Ig2 = 1.2 A VGS (clamp): +10 V, -0.6 V RL = 2.5 Ω		–	80	ns
Turn-On Delay Time	td(on)			17 (typ)	–	
Rise Time	tr			30 (typ)	–	
Turn-Off Delay Time	td(off)			42 (typ)	–	
Fall Time	tr			20 (typ)	–	
Turn-Off Time	t(off)			–	100	
Total Gate Charge	Qg(total)	VGS = 0 to 20 V	VDD = 80 V	–	300	nC
Gate Charge at 10V	Qg(10)	VGS = 0 to 10 V	ID = 40 A	–	150	
Threshold Gate Charge	Qg(th)	VGS = 0 to 2 V	RL = 2 Ω	–	7.5	
Plateau Voltage	V(plateau)	ID = 40 A, VDS = 15 V		–	7.5	V
Turn-Off Energy Loss per Cycle	Eoff	VDD = 50 V, ID = 20 A, RL = 2.5 Ω L = 0.8 µH, Ig1 = Ig2 = 1.2 A VGS (clamp): +10 V, -0.6 V		–	300	µJ
Thermal Resistance, Junction to Case	RθJC			–	0.94	°C/W
Thermal Resistance, Junction to Ambient	RθJA			–	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	VSD	ISD = 40 A	–	1.5	V
Reverse Recovery Time	trr	ISD = 40 A, dISD/dt = 100 A/µs	–	200	ns

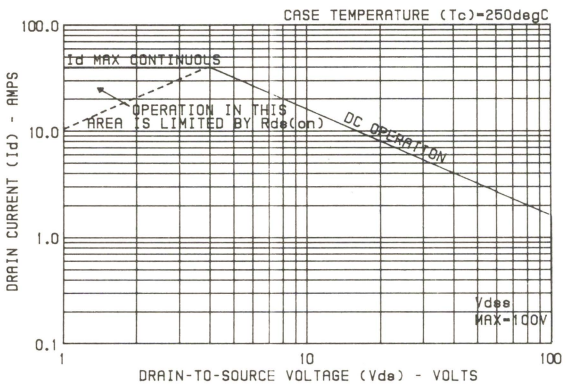


Figure 1 – Safe operating area curve.
(Curves must be derated linearly with increase in temperature.)

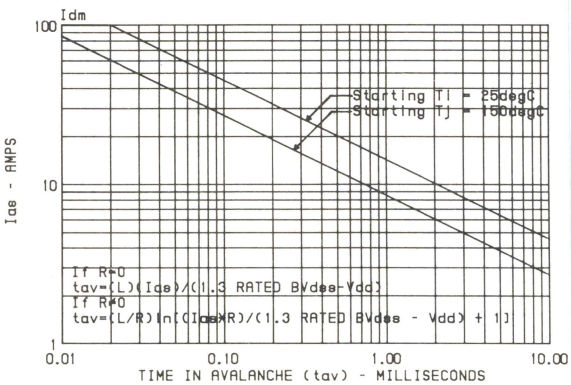


Figure 2 – Unclamped-inductive-switching safe-operating-area (single pulse UIS SOA). See Figure 13 for test circuit.

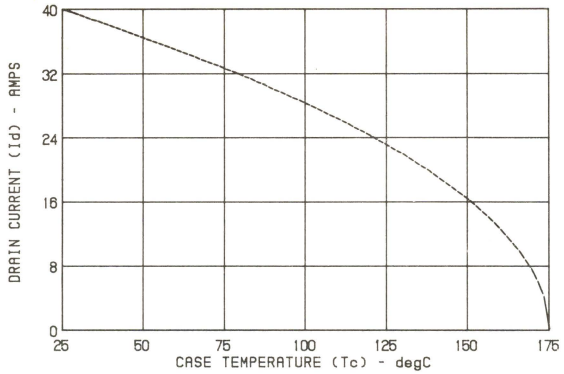


Figure 3 – Maximum continuous drain current vs. temperature.

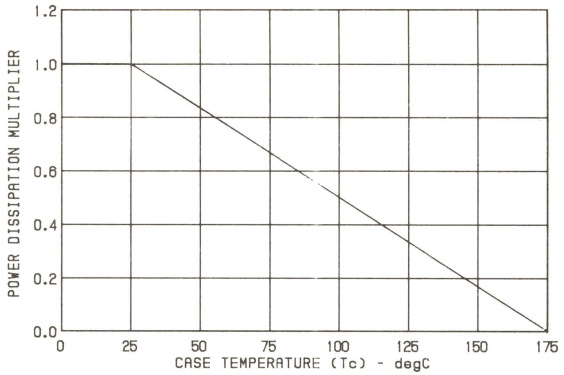


Figure 4 – Normalized power dissipation vs temperature derating curve.

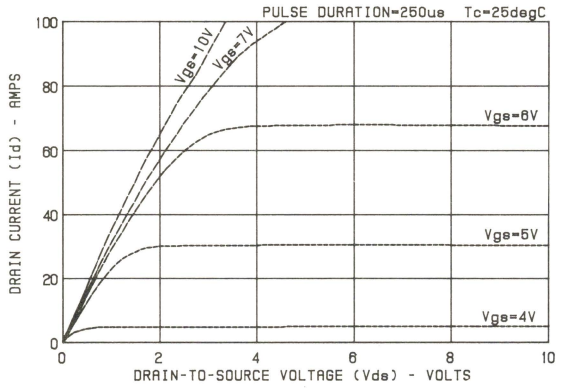


Figure 5 – Typical saturation characteristics.

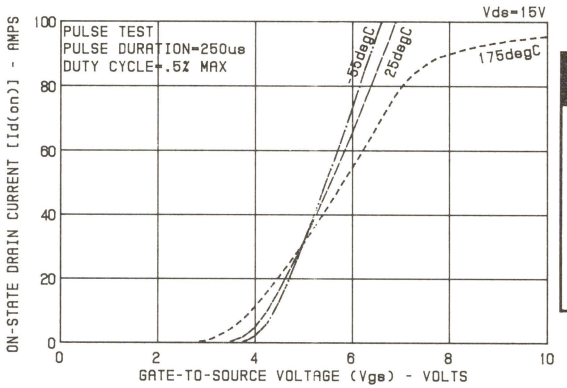


Figure 6 – Typical transfer characteristics.

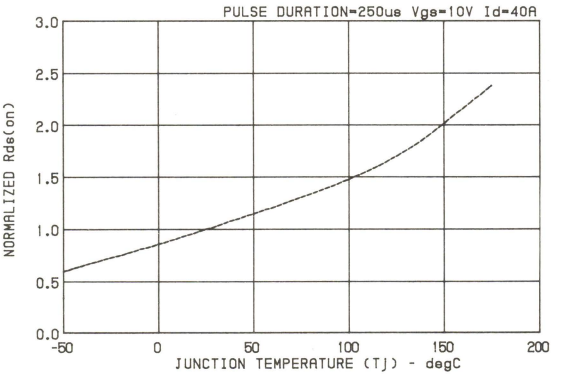


Figure 7 – Normalized Rds(on) vs junction temperature.

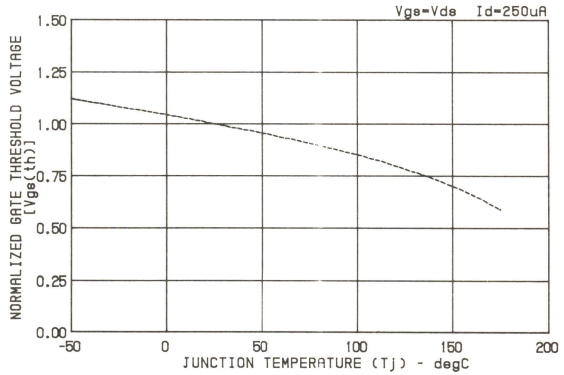


Figure 8 – Normalized gate threshold voltage.

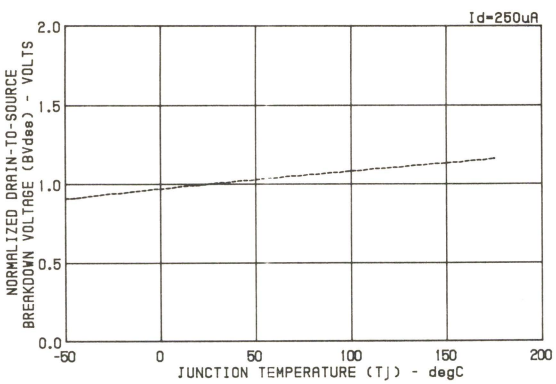


Figure 9 - Normalized drain source breakdown voltage vs temperature.

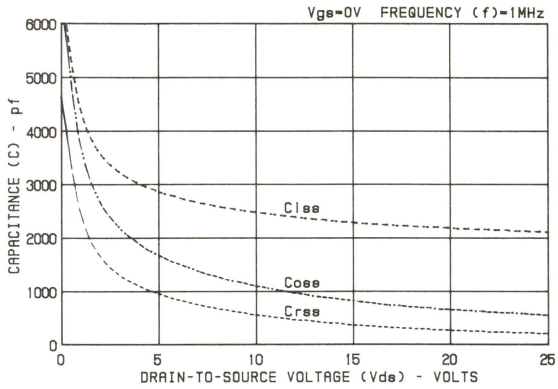


Figure 10 - Typical capacitance vs voltage.

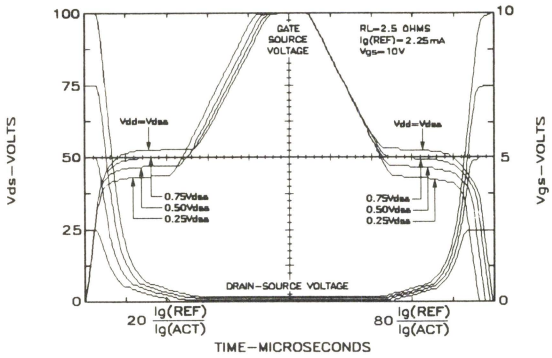


Figure 11 - Normalized switching waveforms for constant gate-current.
Refer to Harris application notes AN-7254 and AN-7260

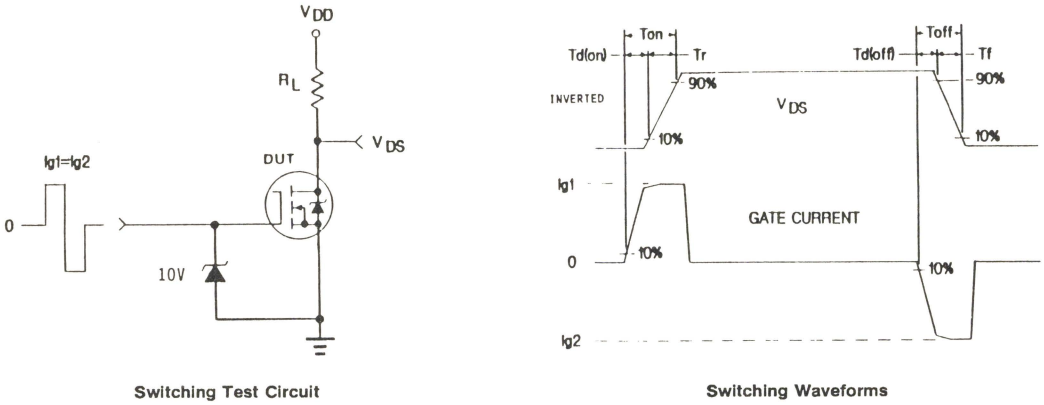
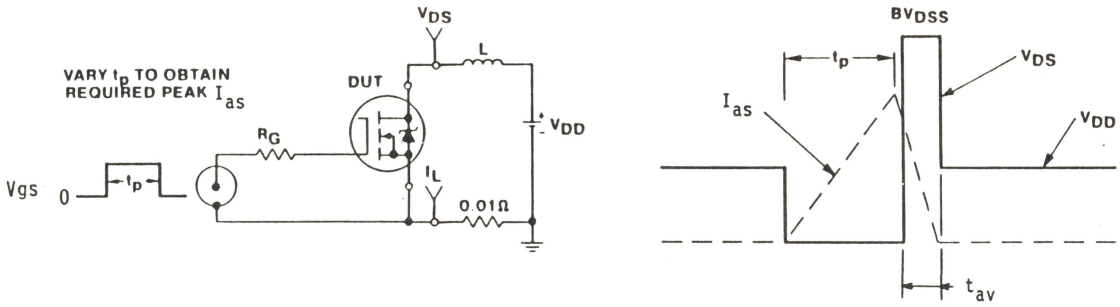


Figure 12 - Resistive switching.



UIS Test Circuit **UIS Waveforms**

Figure 13 – Unclamped-inductive-switching test.

HARRIS SEMICONDUCTOR

RFG45N06
RFP45N06

45A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

January 1994

Features

- 45A, 60V
- $r_{DS(ON)} = 0.028\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

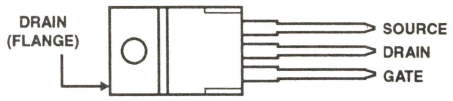
The RFG45N06, RFP45N06 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFG45N06 is supplied in a JEDEC style TO-247 plastic package and the RFP45N06 is supplied in the JEDEC TO-220AB plastic package.

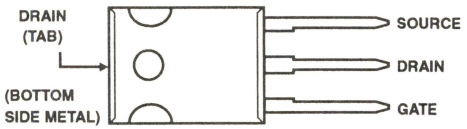
Formerly developmental type TA49028.

Packaging

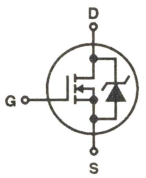
JEDEC TO-220AB
TOP VIEW



JEDEC STYLE TO-247
TOP VIEW



Symbol



Absolute Maximum Ratings ($T_C = +25°C$)

		RFG45N06, RFP45N06	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	45	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Maximum Avalanche Current	I_{AM}	125	A
Power Dissipation			
$T_C = +25°C$	P_D	131	W
Derate above +25°C	P_T	0.877	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3574**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 45A, V_{GS} = 10V		-	-	0.028	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 45A, R_L = 0.667Ω, V_{GS} = +10V, R_{GS} = 3.6Ω		-	-	120	ns
Turn-On Delay Time	$t_{D(ON)}$			-	12	-	ns
Rise Time	t_R			-	74	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	37	-	ns
Fall Time	t_F			-	16	-	ns
Turn-Off Time	t_{OFF}			-	-	80	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 48V, I_D = 45A, R_L = 1.07Ω	-	125	150	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0 to 10V		-	67	80	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to 2V		-	3.7	4.5	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 45A, V_{DS} = 15V		-	-	7.5	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	2050	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.14	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 45A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 45A, dI_{SD}/dt = 100A/µs	-	-	125	ns

Typical Performance Curves

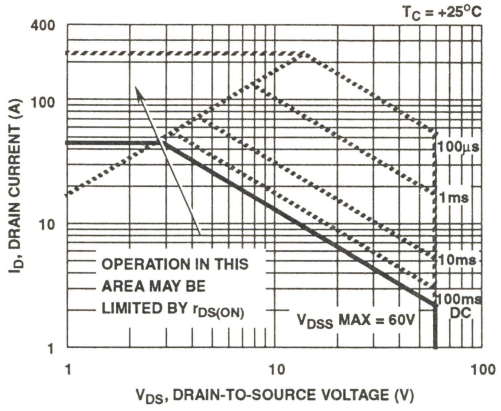

FIGURE 1. SAFE- OPERATING AREA CURVE

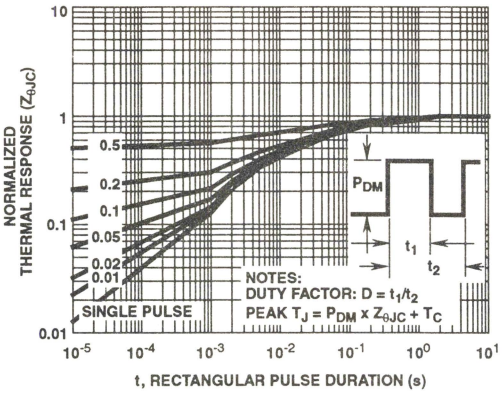

FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

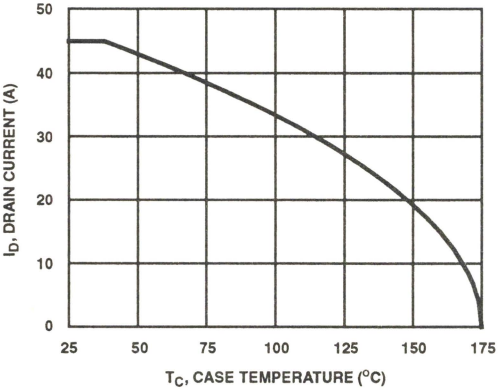

FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

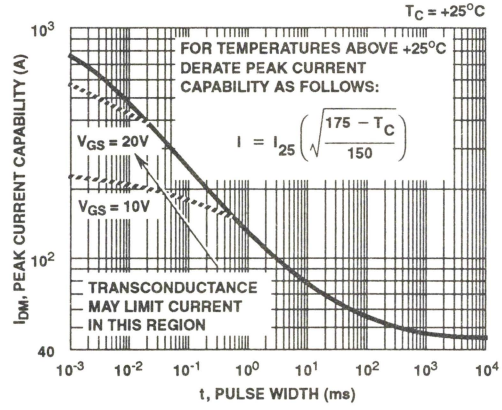

FIGURE 4. PEAK CURRENT CAPABILITY

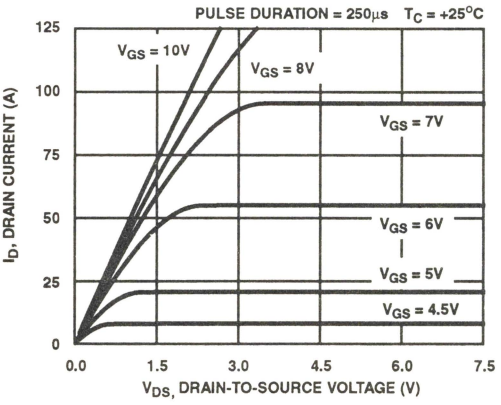

FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

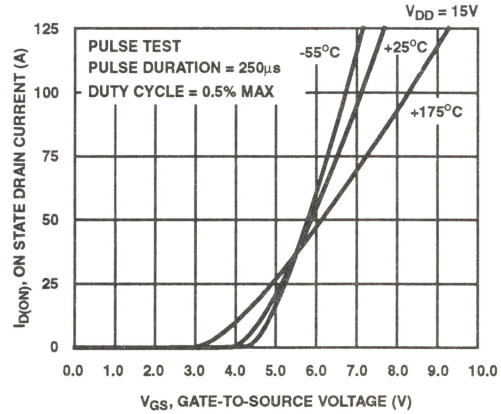

FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

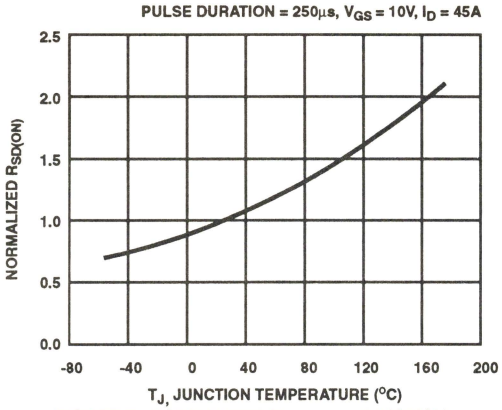

FIGURE 7. NORMALIZED $R_{DS(ON)}$ vs JUNCTION TEMPERATURE

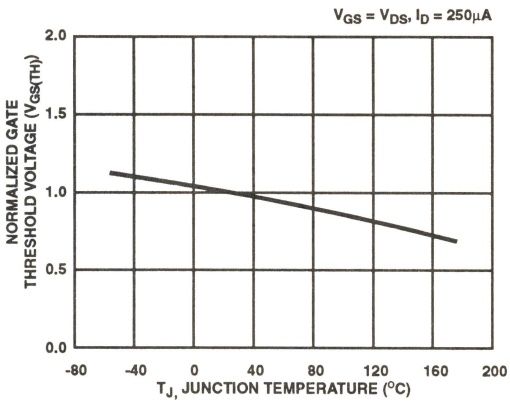

FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

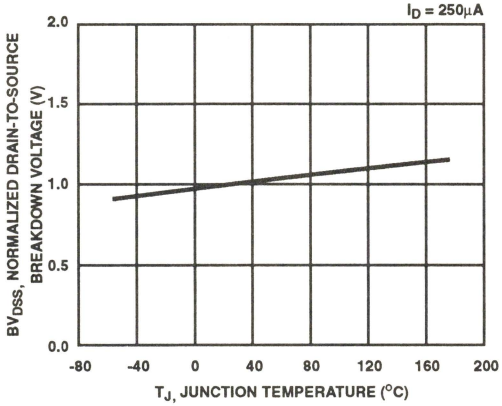

FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

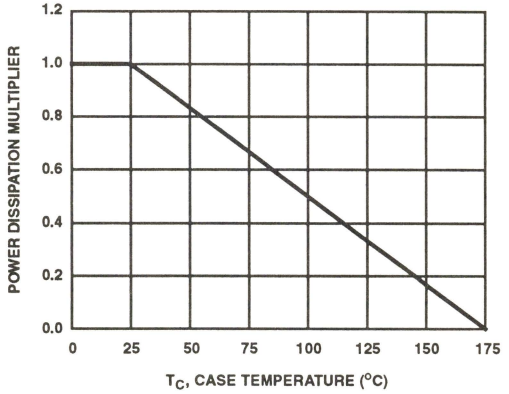

FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

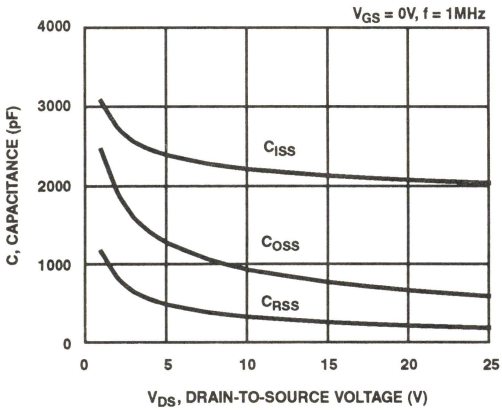

FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

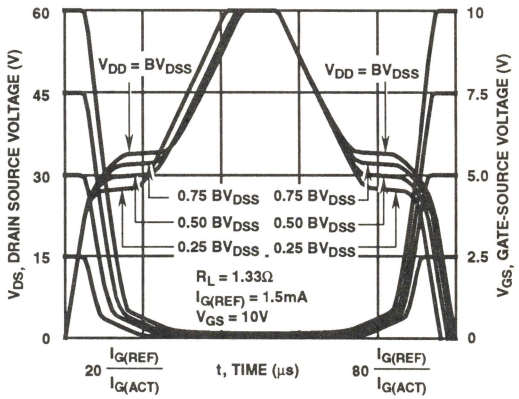

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

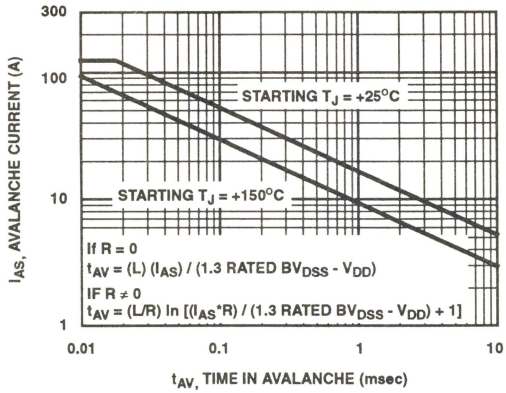

FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

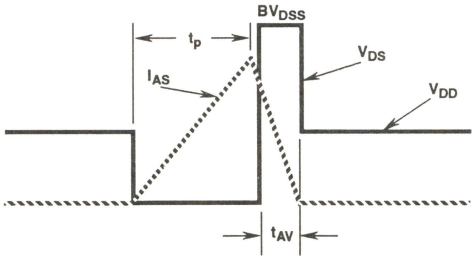

FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

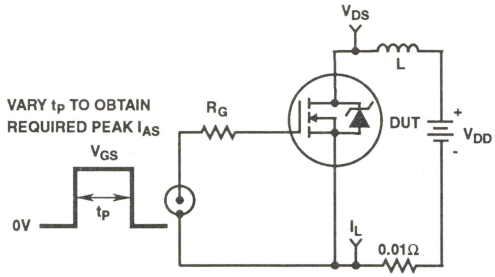

FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

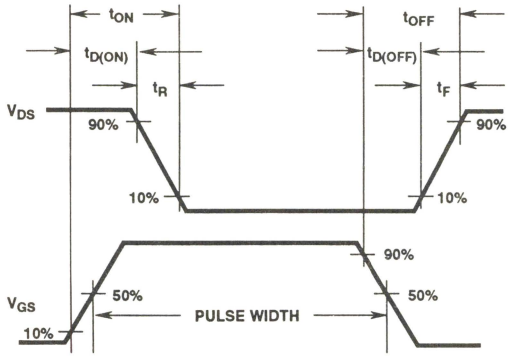

FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

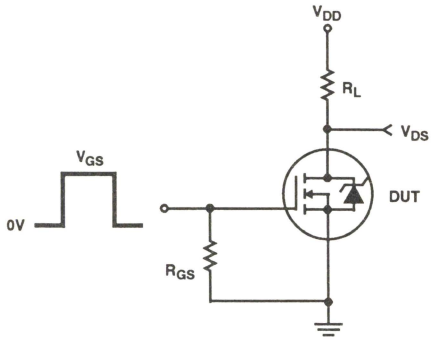

FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

PSpice Model Listing

Temperature Compensated PSPICE Model for the RFG45N06, RFP45N06

```
.SUBCKT RFP45N06 2 1 3

 REV 1/18/93

*NOM TEMP = +25°C


CA 12 8 3.49E-9
CB 15 14 3.8E-9
CIN 6 8 2E-9

DBODY 7 5 DBDMOD
DBREAK 5 11DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1E-9
LGATE 1 9 5.65E-9
LSOURCE 3 7 4.13E-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 3.58E-3
RGATE 9 20 0.681
RIN 6 8 1E9
RSOURCE 8 7 RDSMOD 13.6E-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.92

.MODEL DBDMOD D (IS=8.2E-13 RS=7.86E-3 TRS1=2.26E-3 TRS2=2.90E-6 CJO=2.07E-9 TT=5.72E-8)
.MODEL DBKMOD D (RS=1.93E-1 TRS1=5.13E-4 TRS2=-2.15E-5)
.MODEL DPLCAPMOD D (CJO=1.25E-9 IS=1E-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.862 KP=55.57 IS=1E-30 N=10 TOX=1 L=1U W=1U)
.MODEL RBKMOD RES (TC1=1.12E-3 TC2=-5.18E-7)
.MODEL RDSMOD RES (TC1=4.64E-3 TC2=1.58E-5)
.MODEL RVTOMOD RES (TC1=-4.27E-3 TC2=-6.55E-6)
.MODEL S1AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-6.5 VOFF=-1.7)
.MODEL S1BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-1.7 VOFF=-6.5)
.MODEL S2AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-3.0 VOFF=2)
.MODEL S2BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=2.0 VOFF=-3.0)

.ENDS
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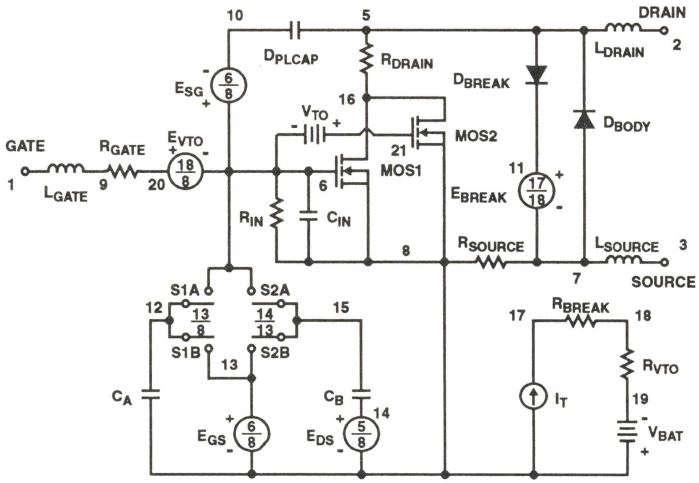


NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options;** authored by William J. Hepp and C. Frank Wheatley.

HARRIS

RFH45N05
RFH45N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 45A, 50V and 60V
- $r_{DS}(on) = 0.040\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- High-Current, Low-Inductance Package

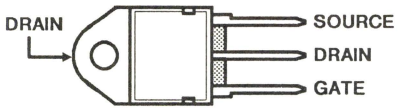
Description

The RFH45N05 and RFH45N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

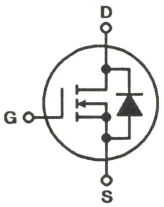
Package

TO-218AC
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFH45N05	RFH45N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Continuous Drain Current	I_D	45	45	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1635.1**

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V V_{DS} = 50 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 40 V V_{DS} = 50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	0.9	—	0.9	V
		I_D = 45 A V_{GS} = 10 V	—	3.6	—	3.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1800	—	1800	pF
Reverse Transfer Capacitance	C_{rss}		—	750	—	750	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 30 V I_D = 22.5 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		310(typ)	475	310(typ)	475	ns
Turn-Off Delay Time	$t_d(off)$		220(typ)	350	220(typ)	350	ns
Fall Time	t_f		240(typ)	375	240(typ)	375	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH45N05, RFH45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

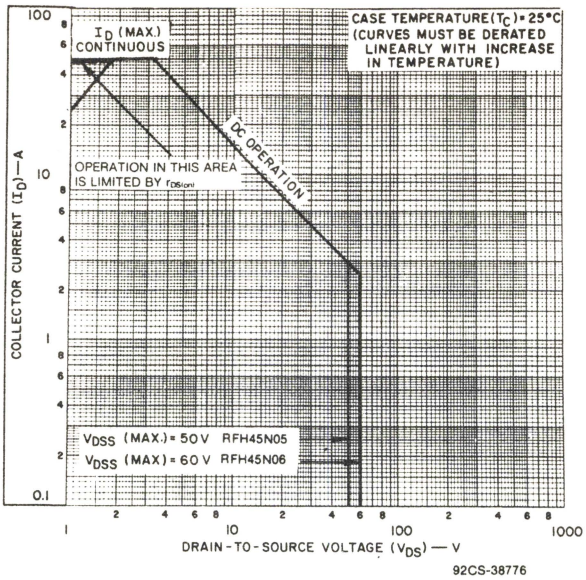


Fig. 1 - Maximum safe operating areas for all types.

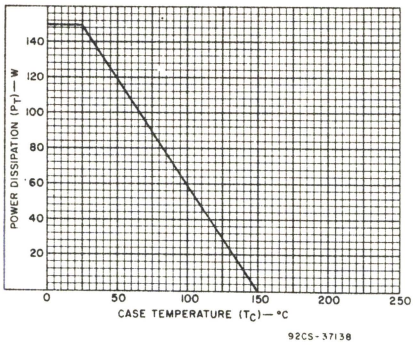


Fig. 2 - Power vs. temperature derating curve for all types.

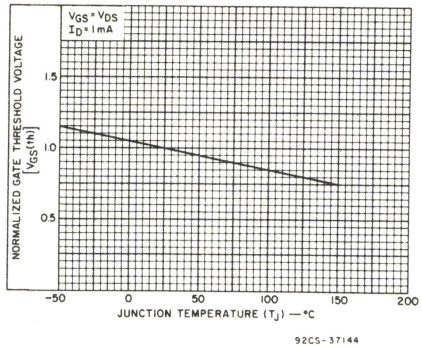


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

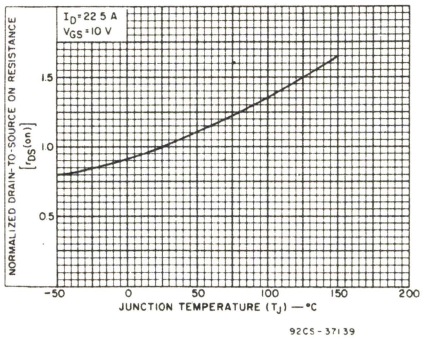


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

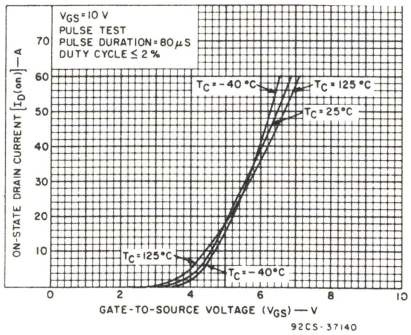


Fig. 5 - Typical transfer characteristics for all types.

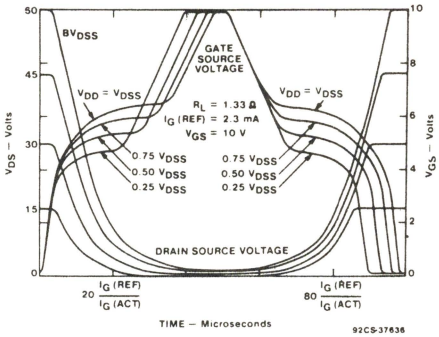


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

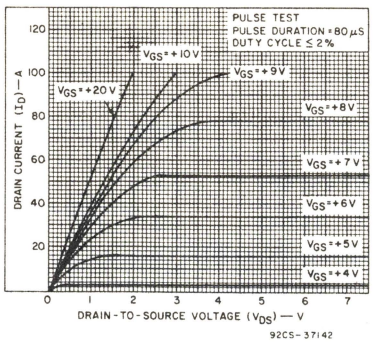


Fig. 7 - Typical saturation characteristics for all types.

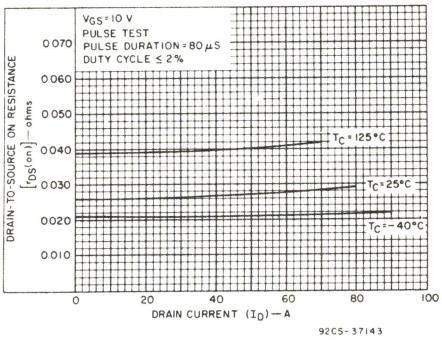


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

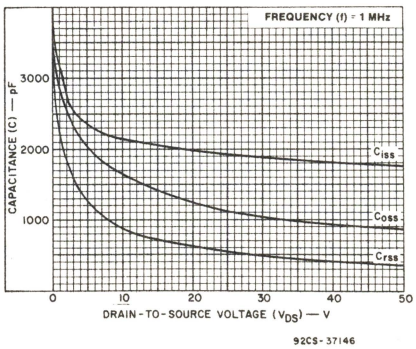


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

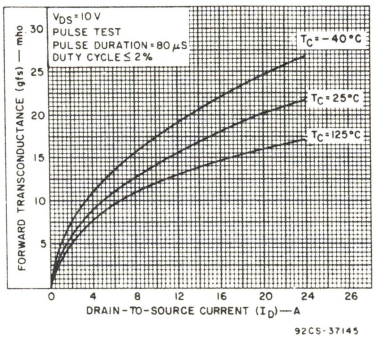


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

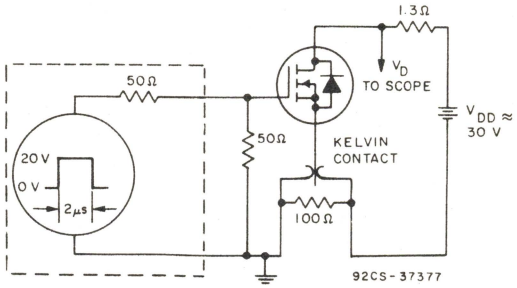


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFK45N05
RFK45N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 45A, 50V and 60V
- $r_{DS}(on) = 0.040\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

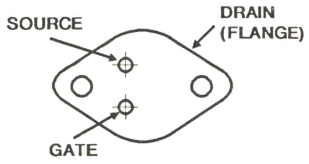
Description

The RFK45N05 and RFK45N06 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

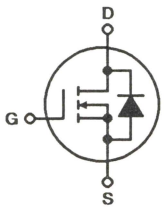
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFK45N05	RFK45N06	UNITS
Drain-Source Voltage	V_{DSS}	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	60	V
Continuous Drain Current				
T_C = +25°C	I_D	45	45	A
Pulsed Drain Current	I_{DM}	100	100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1498.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V V_{DS}=50 V	— —	1 —	— —	— 1	μA
		T_C=125° c V_{DS}=40 V V_{DS}=50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	0.9	—	0.9	V
		I_D=45 A V_{GS}=10 V	—	3.6	—	3.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1800	—	1800	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	750	—	750	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=22.5 A	310(typ)	475	310(typ)	475	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	220(typ)	350	220(typ)	350	ns
Fall Time	t_f	V_{GS}=10 V	240(typ)	375	240(typ)	375	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK45N05, RFK45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	150(typ.)		150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

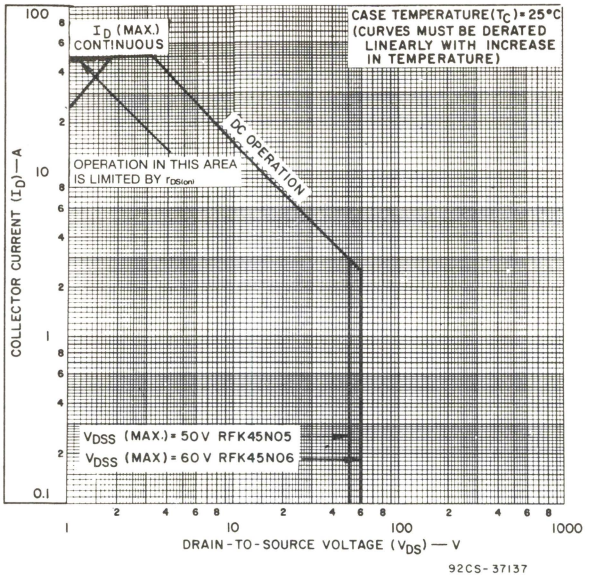


Fig. 1 — Maximum safe operating areas for all types.

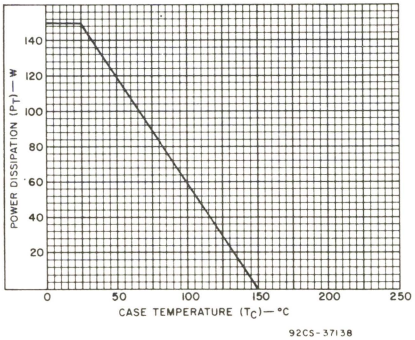


Fig. 2 — Power vs. temperature derating curve for all types.

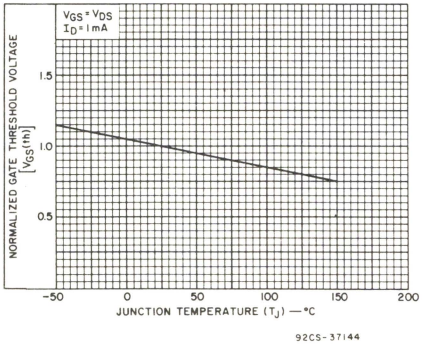


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

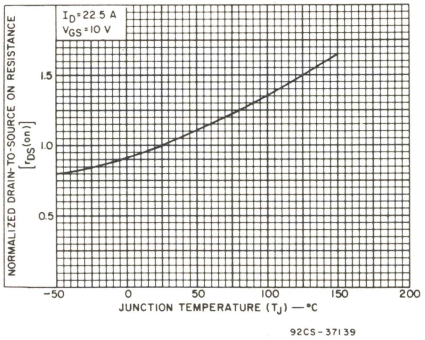


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

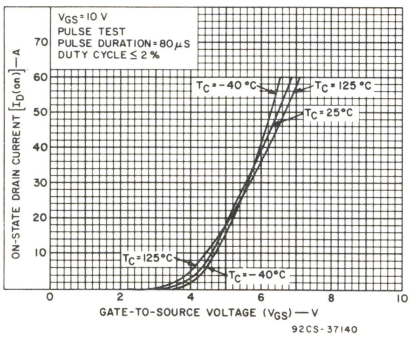


Fig. 5 — Typical transfer characteristics for all types.

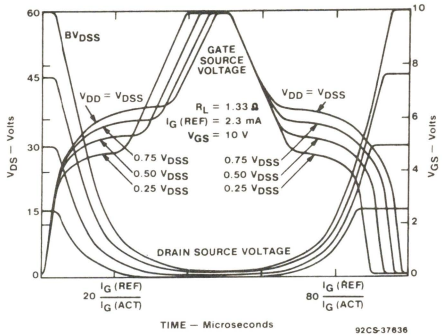


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260

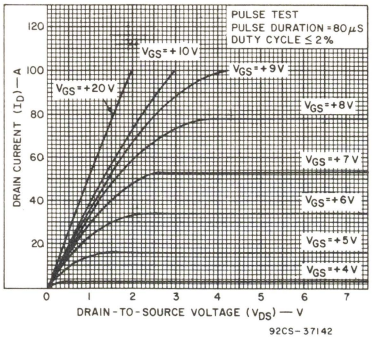


Fig. 7 — Typical saturation characteristics for all types.

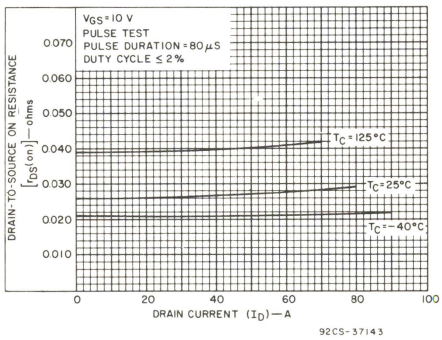


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

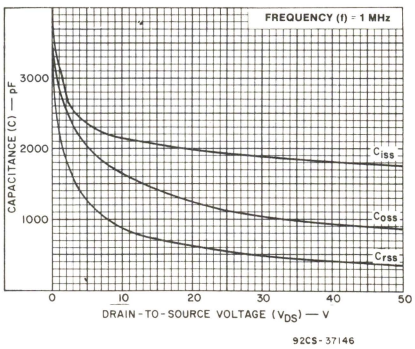


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

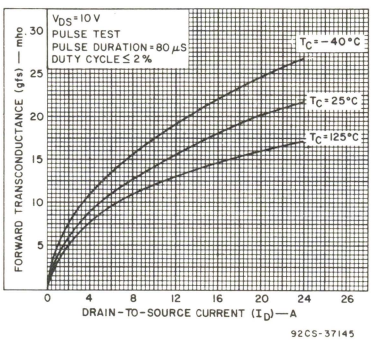


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

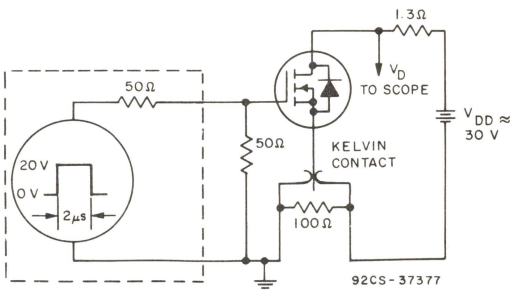


Fig. 11 - Switching Time Test Circuit.

4 N-CHANNEL POWER MOSFETs

HARRIS

RFP50N05
RFG50N05

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

May 1992

Features

- 50A, 50V
- $r_{DS(on)} = 0.022\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

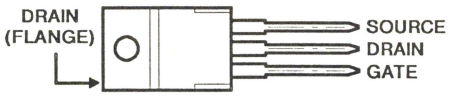
Description

The RFP50N05 and RFG50N05 n-channel power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors.

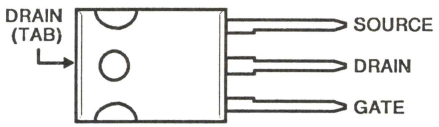
The RFP50N05 is supplied in the JEDEC TO-220AB plastic package and the RFG50N05 is supplied in the TO-247 plastic package.

Package

TO-220AB
TOP VIEW

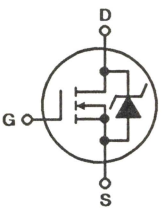


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	RFP50N05 RFG50N05	UNITS
Drain-Source Voltage ..... V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ) ..... V_{DGR}	50	V
Continuous Drain Current ..... I_D	50	A
Pulsed Drain Current ..... I_{DM}	120	A
Gate-Source Voltage ..... V_{GS}	±20	V
Maximum Power Dissipation		
T_C = +25°C ..... P_D	132	W
Derated Above +25°C	0.88	W/°C
Operating and Storage Junction Temperature Range ..... T_{JC}, T_{STG}	-55 to +175	°C
Single-Pulse Avalanche Ratings	Refer to UIS SOA Curve	

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2873.1**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	–	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		–	–	1	µA
		T_C =+150°C		–	–	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		–	–	100	nA
On Resistance	$r_{DS(on)}$	I_D = 50A, V_{GS} = 10V		–	–	0.022	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 25A, R_L = 1.0Ω, $I_{G}1 = I_{G}2$ = 1.5A, $V_{GS(clamp)}$ = +10V, -0.6V		–	–	100	ns
Turn-On Delay Time	$t_{d(on)}$			–	15	–	ns
Rise Time	t_r			–	55	–	ns
Turn-Off Delay Time	$t_{d(off)}$			–	60	–	ns
Fall Time	t_f			–	15	–	ns
Turn-Off Time	$t_{(off)}$			–	–	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-20V	V_{DD} = 40V	–	–	160	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0-10V	I_D = 50A	–	–	80	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0-2V	R_L = 0.8Ω	–	–	6	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 50A, V_{DS} = 15V		–	–	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 25A, $I_{G}1 = I_{G}2$ = 1.5A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 1.0Ω		–	–	150	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			–	–	1.14	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			–	–	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 50A	–	–	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 50A, dI_f/dt = 100A/µs	–	–	125	ns

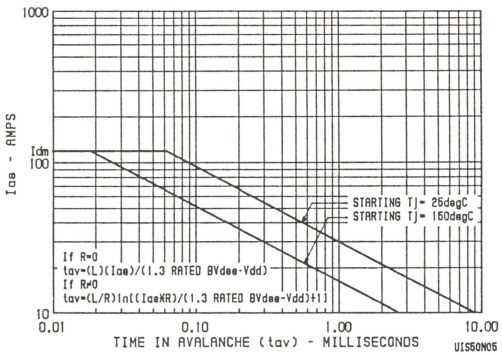


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

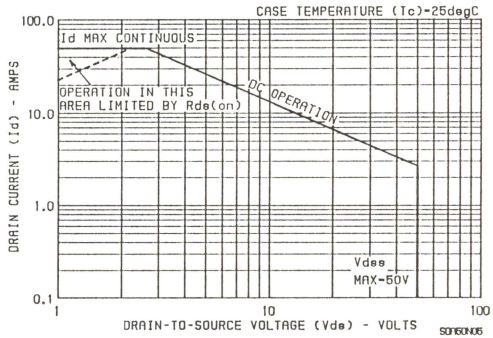


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

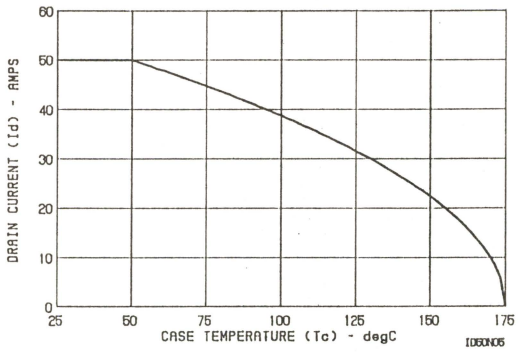


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

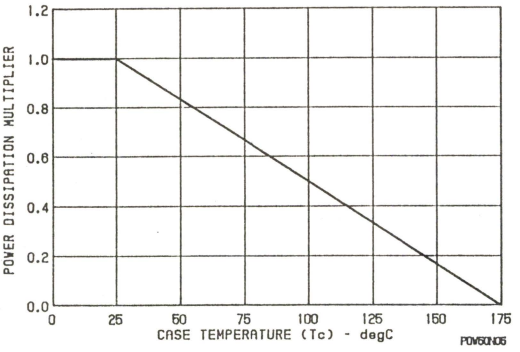


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

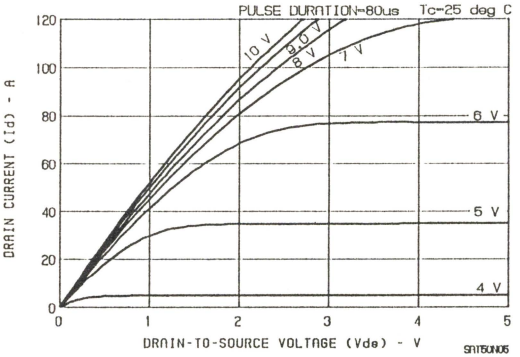


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

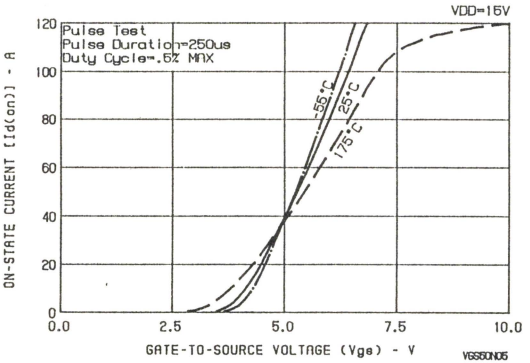


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

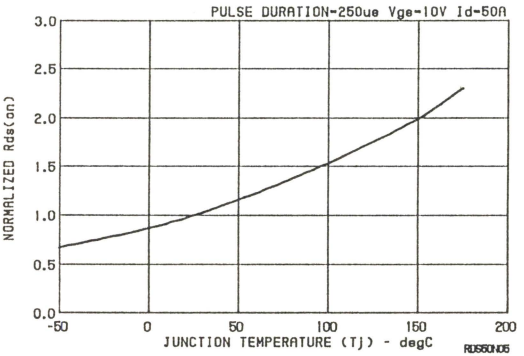


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

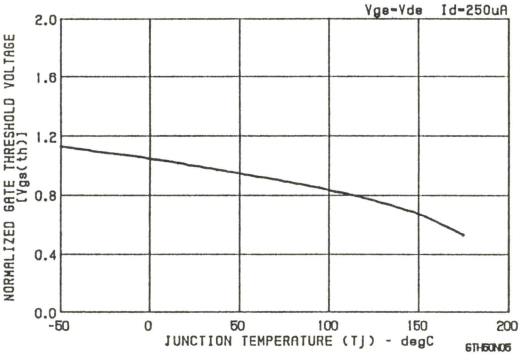


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

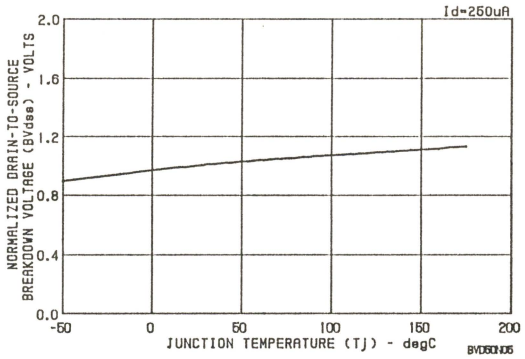


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

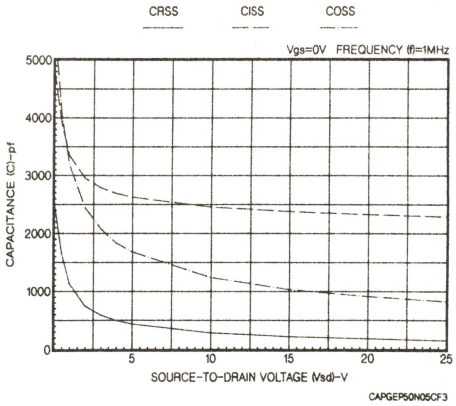


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

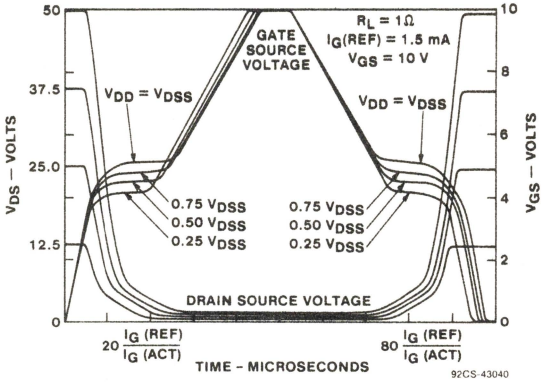


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

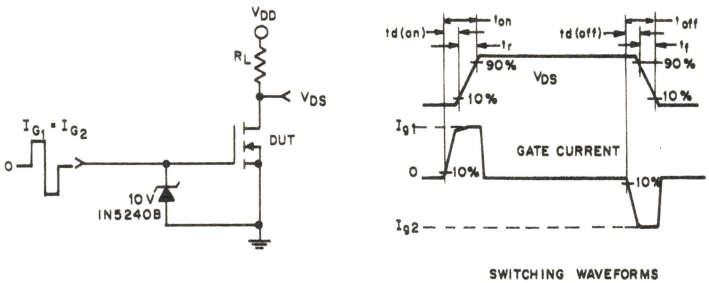


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

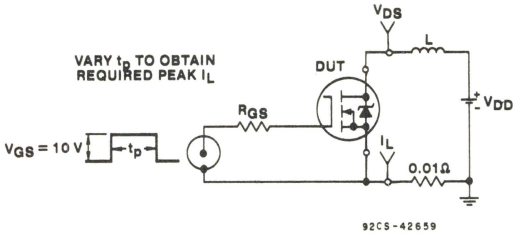


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

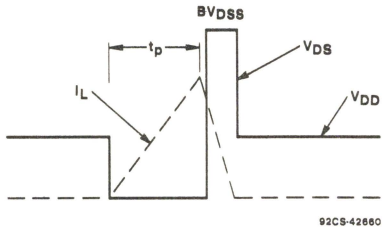


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

HARRIS SEMICONDUCTOR

RFG50N06
RFP50N06

50A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

February 1994

Features

- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG50N06 and RFP50N06 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

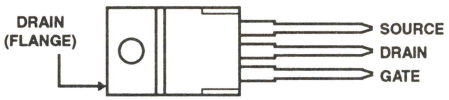
The RFG50N06 is supplied in the JEDEC TO-247 plastic package; the RFP50N06 is supplied in the JEDEC TO-220AB plastic package.

When ordering use the entire part number; eg. RFG50N06

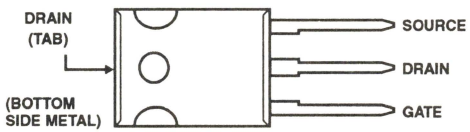
Formerly developmental type TA49018.

Package

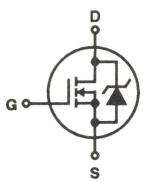
JEDEC TO-220AB
TOP VIEW



JEDEC STYLE TO-247
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RFG50N06, RFP50N06	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	50	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Maximum Avalanche Current	I_{AM}	125	A
Power Dissipation			
T_C = +25°C	P_D	131	W
Derate above +25°C	P_T	0.877	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3575

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 50A, V_{GS} = 10V		-	-	0.022	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 50A, R_L = 0.6Ω, V_{GS} = +10V, R_{GS} = 3.6Ω		-	-	95	ns
Turn-On Delay Time	$t_{D(ON)}$			-	12	-	ns
Rise Time	t_R			-	55	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	37	-	ns
Fall Time	t_F			-	13	-	ns
Turn-Off Time	t_{OFF}			-	-	75	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 48V, I_D = 50A, R_L = 0.96Ω	-	125	150	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0 to 10V		-	67	80	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to 2V		-	3.7	4.5	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 50A, V_{DS} = 15V		-	-	7.5	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	2020	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.14	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 50A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 50A, dI_{SD}/dt = 100A/µs	-	-	125	ns

Typical Performance Curves

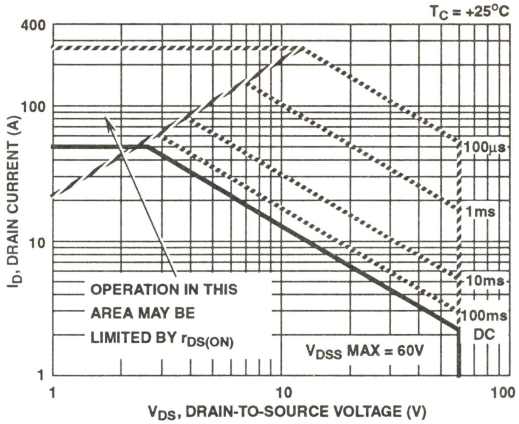

FIGURE 1. SAFE OPERATING AREA CURVE

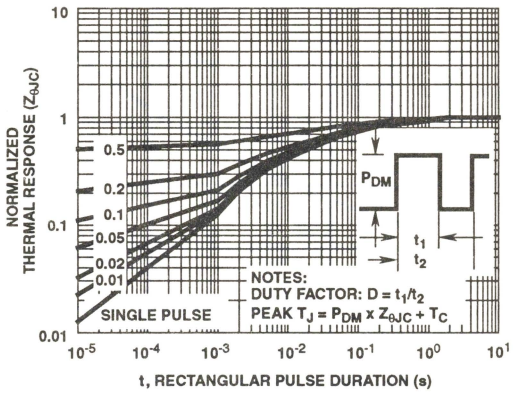

FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

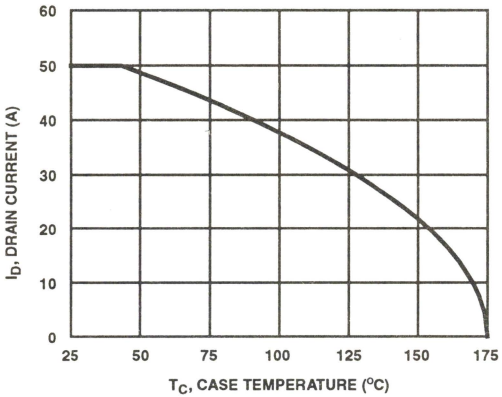

FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

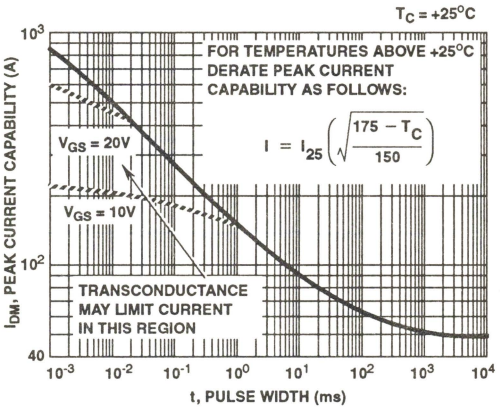

FIGURE 4. PEAK CURRENT CAPABILITY

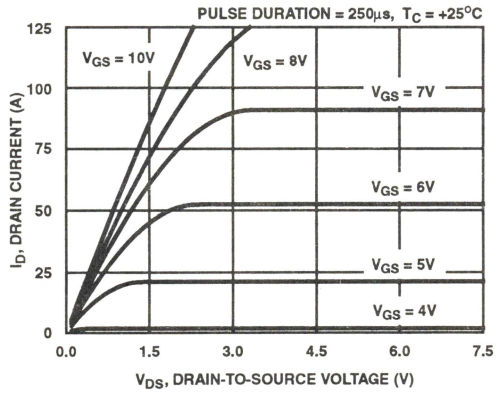

FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

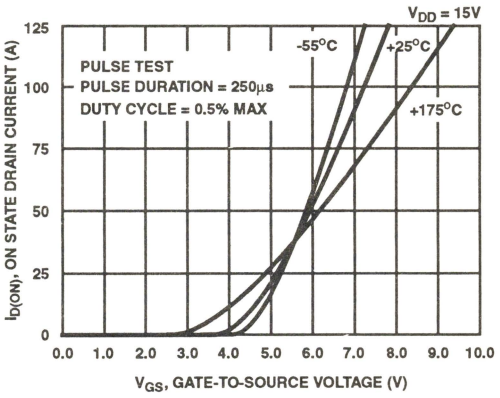

FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

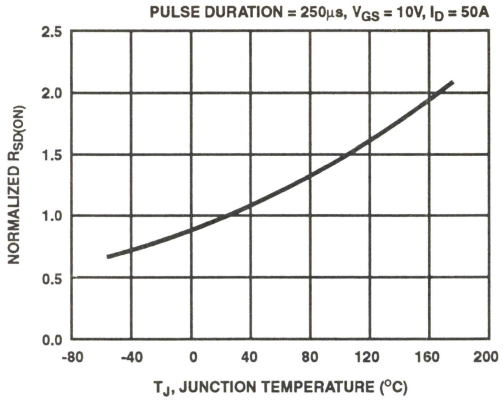

FIGURE 7. NORMALIZED $R_{DS(ON)}$ vs JUNCTION TEMPERATURE

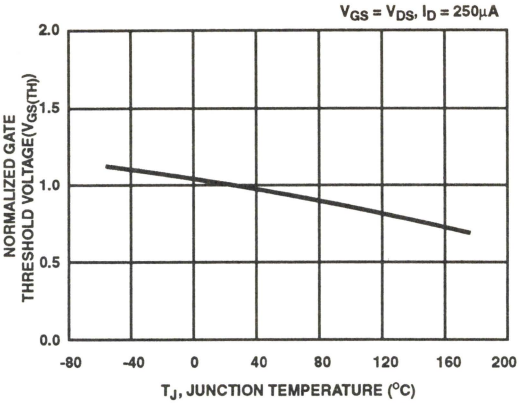

FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

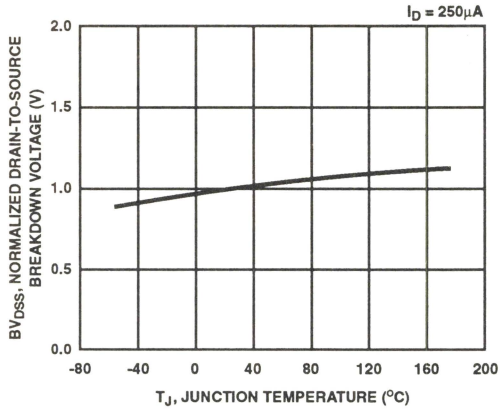

FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

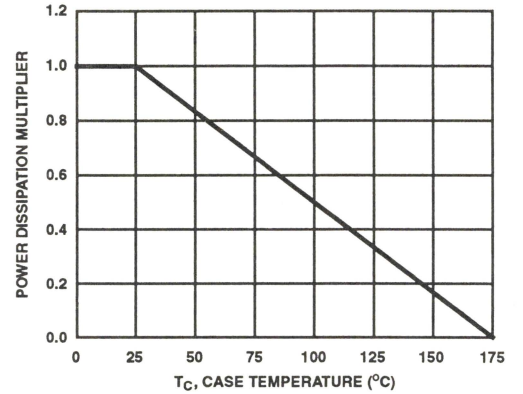

FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

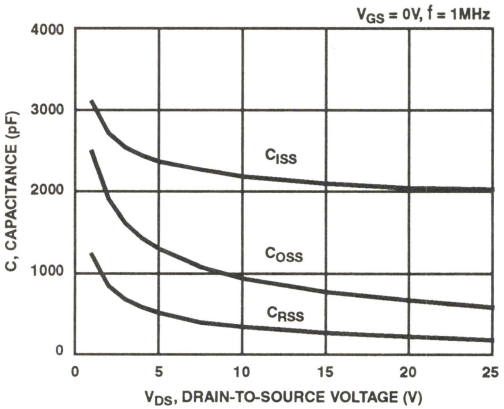

FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

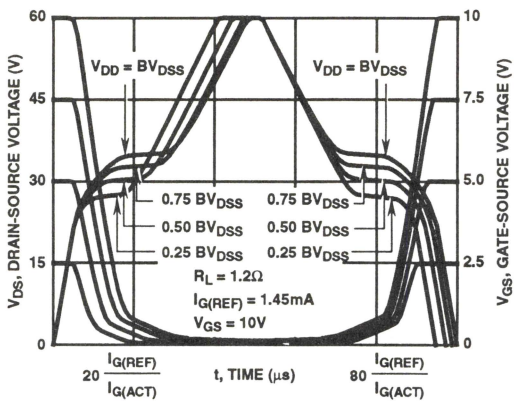

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

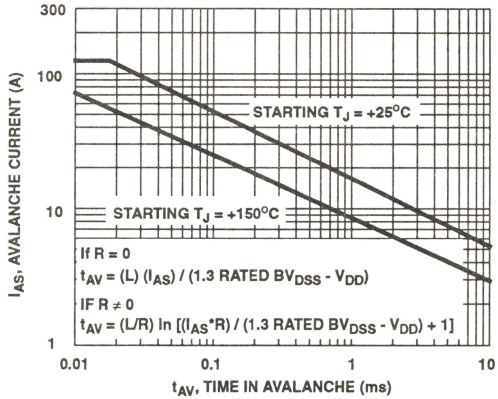

FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

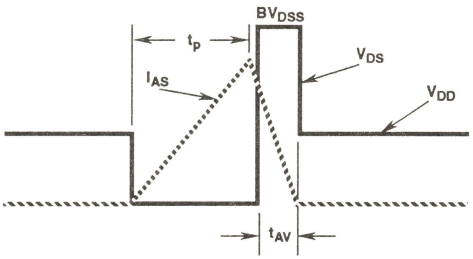

FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

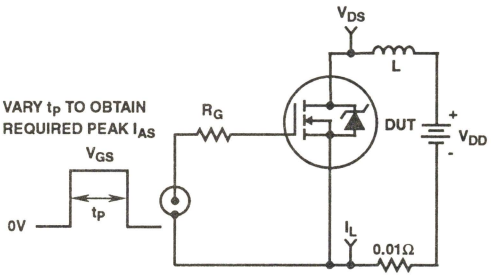

FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

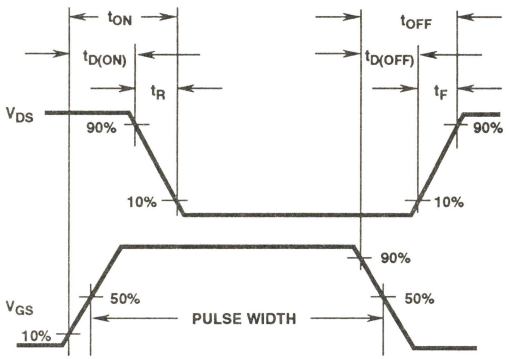

FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

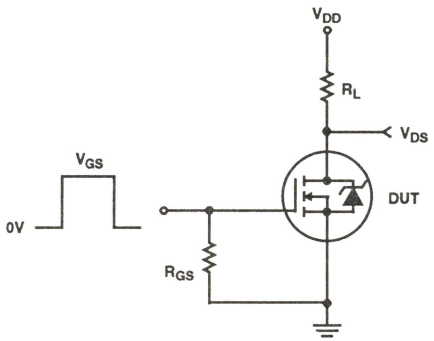

FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

PSpice Model Listing

Temperature Compensated PSpice Model for the RFG50N06, RFP50N06

```
.SUBCKT RFP50N06 2 1 3
 REV 2/22/93
*NOM TEMP = +25°C
CA 12 8 3.68e-9
CB 15 14 3.625e-9
CIN 6 8 1.98e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.59
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 5.65e-9
LSOURCE 3 7 4.13e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1e-4
RGATE 9 20 0.690
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 12e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.678

.MODEL DBDMOD D (IS=9.851e-13 RS=4.91e-3 TRS1=2.07e-3 TRS2=2.51e-7 CJO=2.05e-9 TT=4.33e-8)
.MODEL DBKMOD D (RS=1.98e-1 TRS1=-2.35e-3 TRS2=-3.83e-6)
.MODEL DPLCAPMOD D (CJO=1.42e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.65 KP=35 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.23e-3 TC2=-2.34e-6)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.49e-5)
.MODEL RVTOMOD RES (TC1=-5.03e-3 TC2=-5.16e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.75 VOFF=-2.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.5 VOFF=-6.75)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.7 VOFF=2.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.3 VOFF=-2.7)

.ENDS
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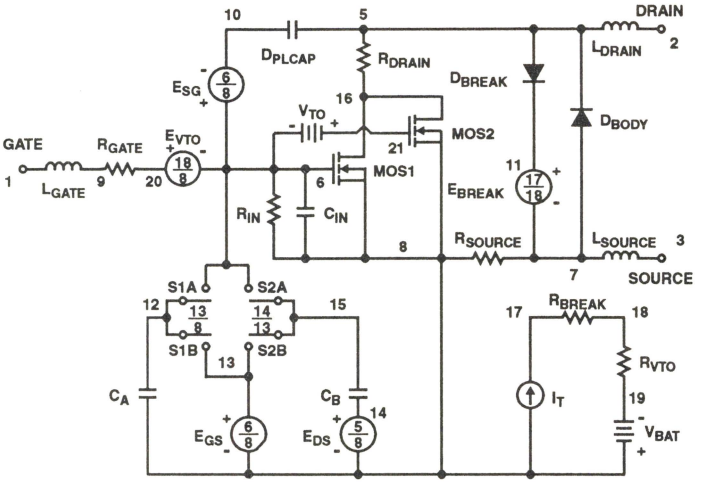


NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options; authored by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFP70N03

70A, 30V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFET (MegaFET)

March 1994

Features

- 70A, 30V
- $r_{DS(ON)} = 0.010\Omega$
- UIS Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- PSPICE Model

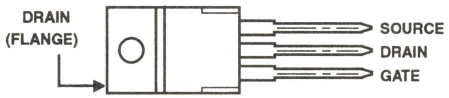
Description

The RFP70N03 (TA49025) N-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

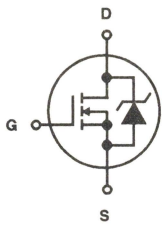
The RFP70N03 is supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Symbol



4 N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP70N03	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	200	A
Single Pulse Avalanche Rating	E_{AS}	(Refer to UIS Curve)	
Power Dissipation			
T_C = +25°C	P_D	150	W
Above T_C = +25°C, Derate Linearly	P_T	1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3404**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V	T_C = 25°C	-	-	1	µA
		V_{GS} = 0V	T_C = 150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 70A, V_{GS} = 10V		-	-	10	mΩ
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 70A		-	-	80	ns
Turn-On Delay Time	$t_{D(ON)}$	R_L = 0.214Ω, V_{GS} = +10V		-	20	-	ns
Rise Time	t_R	R_{GS} = 2.5Ω		-	20	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 24V, I_D = 70A, R_L = 0.343Ω	-	215	260	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0 to 10V		-	120	145	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to 2V		-	6.5	8.0	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 70A, V_{DS} = 15V		-	-	7.5	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V		-	3300	-	pF
Output Capacitance	C_{OSS}	f = 1MHz		-	1750	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	750	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 70A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 70A, dI_{SD}/dt = 100A/µs	-	-	125	ns

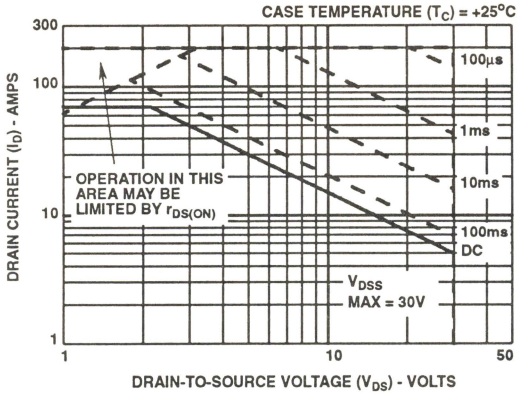


FIGURE 1. SAFE-OPERATING AREA CURVE

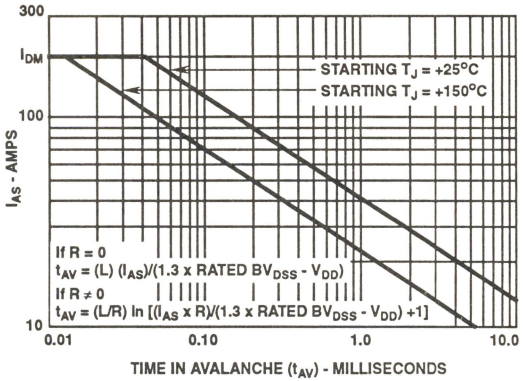


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

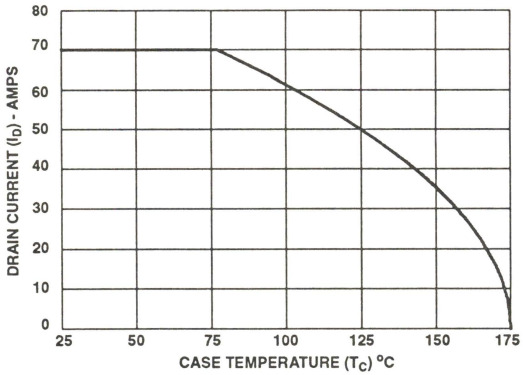


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

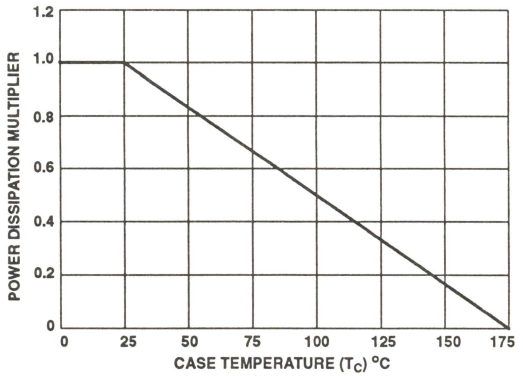


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

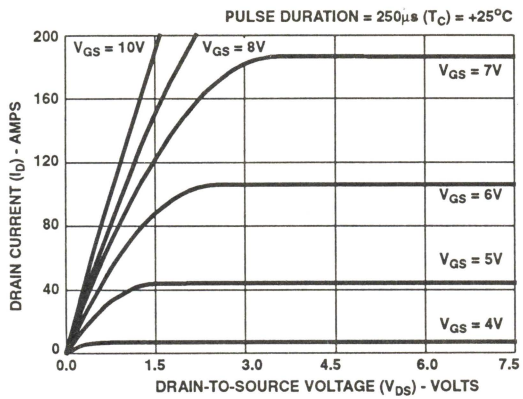


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

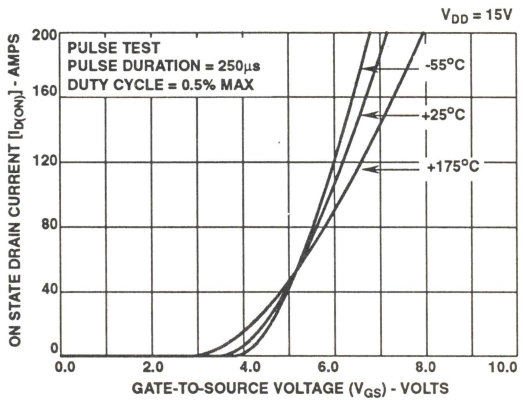


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

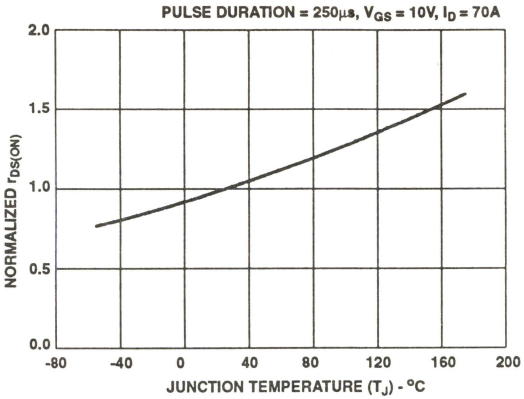


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

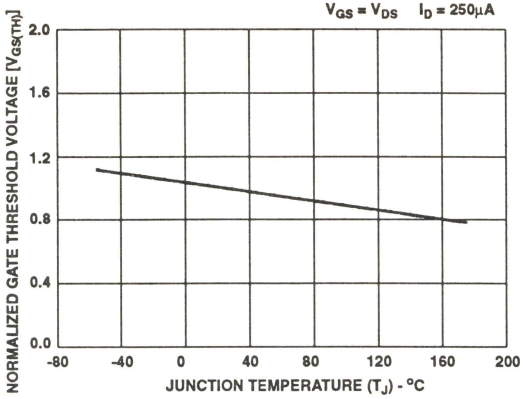


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

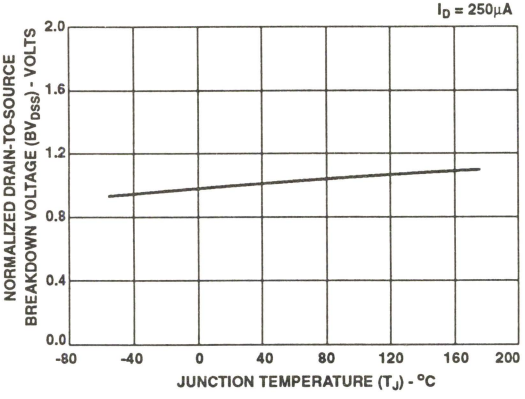


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

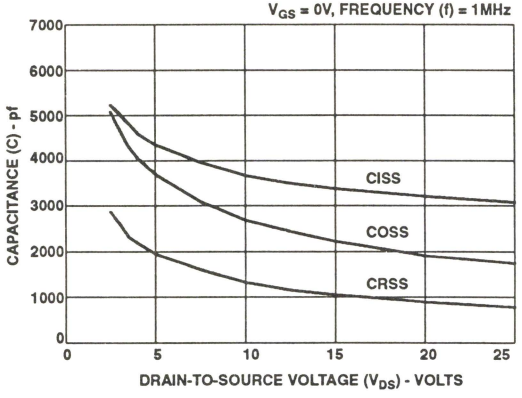


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

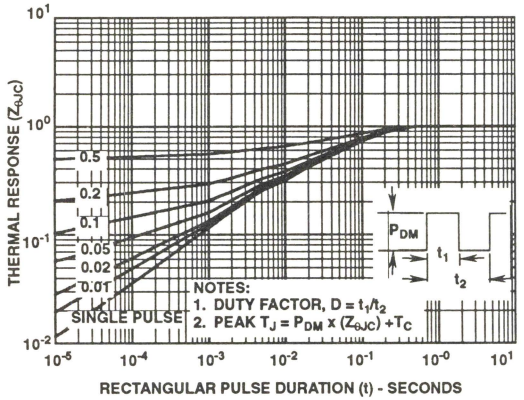


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

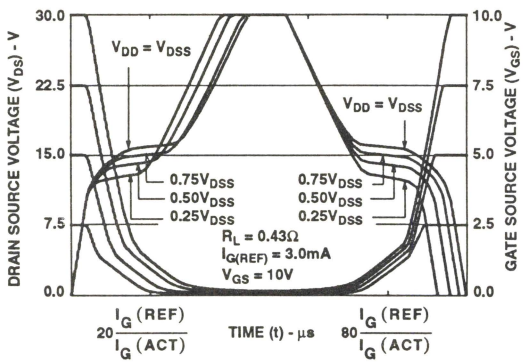


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260.

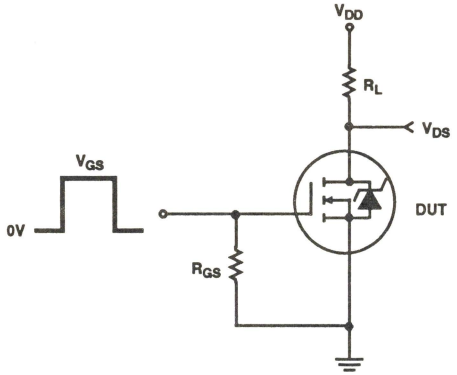


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT.

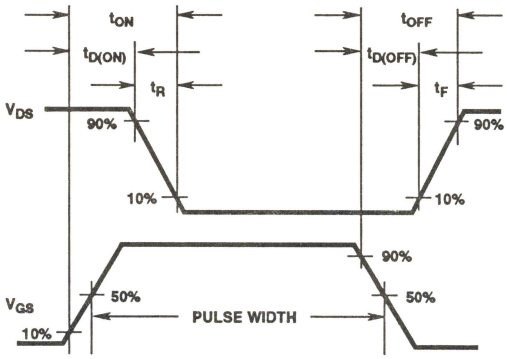


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

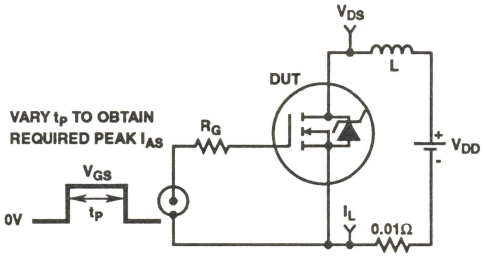


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

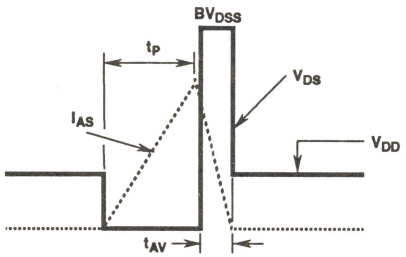


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

PSPICE Model for the RFP70N03

```
.SUBCKT RFP70N03 2 1 3 ;          rev 9/16/92
*Nom Temp=25 deg C

CA 12 8 6.09e-9
CB 15 14 6.05e-9
CIN 6 8 3.40e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

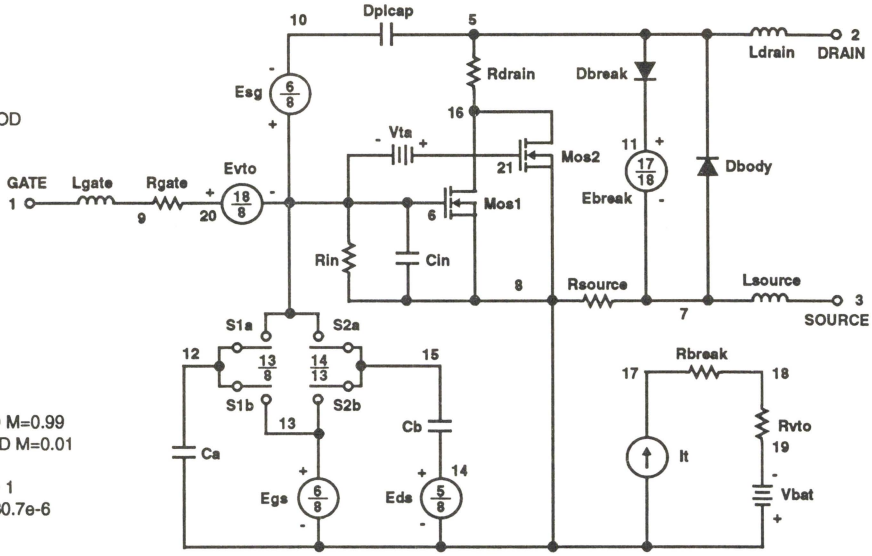
RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 30.7e-6
RGATE 9 20 0.890
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.605

.MODEL DBDMOD D (IS=7.91e-12 RS=3.87e-3 TRS1=2.71e-3 TRS2=2.50e-7 CJO=4.84e-9 TT=4.51e-8)
.MODEL DBKMOD D (RS=3.9e-2 TRS1=1.05e-4 TRS2=3.11e-5)
.MODEL DPLCAPMOD D (CJO=4.8e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.46 KP=47 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=8.46e-4 TC2=-8.48e-7)
.MODEL RDSMOD RES (TC1=2.23e-3 TC2=6.56e-6)
.MODEL RVTOMOD RES (TC1=-3.29e-3 TC2=3.49e-7)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8.35 VOFF=-6.35)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.35 VOFF=-8.35)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=3.0)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.0 VOFF=-2.0)


.ENDS
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFG70N06
RFP70N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1992

Features

- 70A, 60V
- $r_{DS(on)} = 0.014\Omega$
- UIS Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

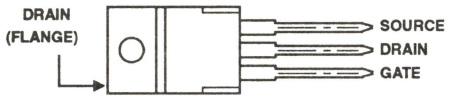
Description

The RFG70N06 and RFP70N06 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

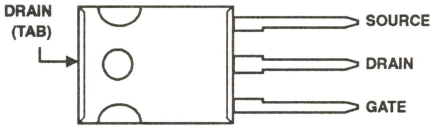
The RFG70N06 is supplied in the JEDEC TO-247 style plastic package and the RFP70N06 is supplied in the JEDEC TO-220AB plastic package.

Packages

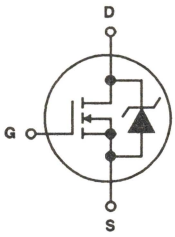
TO-220AB
TOP VIEW



TO-247
TOP VIEW



Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG70N06, RFP70N06	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	180	A
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
T_C = +25°C	P_D	150	W
Derate above +25°C		1.0	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3206

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V,	T_C = +25°C	-	-	1	µA
		V_{GS} = 0V	T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 70A, V_{GS} = 10V		-	-	14	mΩ
Turn-On Time	$t_{(on)}$	V_{DD} = 30V, I_D = 70A R_L = 0.43Ω, V_{GS} = +10V R_{GS} = 2.5Ω		-	-	125	ns
Turn-On Delay Time	$t_{d(on)}$			-	12	-	ns
Rise Time	t_r			-	50	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	40	-	ns
Fall Time	t_f			-	15	-	ns
Turn-Off Time	$t_{(off)}$			-	-	125	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0V to 20V	V_{DD} = 48V, I_D = 70A, R_L = 0.68Ω	-	185	215	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	100	115	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0V to 2V		-	5.5	6.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 70A, V_{DS} = 15V		-	-	7.5	V
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V f = 1MHz		-	3000	-	pF
Output Capacitance	C_{oss}			-	900	-	pF
Reverse Transfer Capacitance	C_{rss}			-	300	-	pF
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30V, I_D = 70A, L = 0.21µH, R_L = 0.43Ω V_{GS} = 10V, R_{GS} = 2.5Ω		-	-	1.0	mJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 70A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 70A, dI_{SD}/dt = 100A/µs	-	-	125	ns

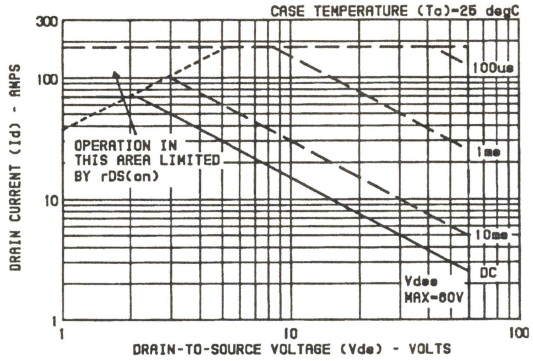


FIGURE 1. SAFE OPERATING AREA CURVE

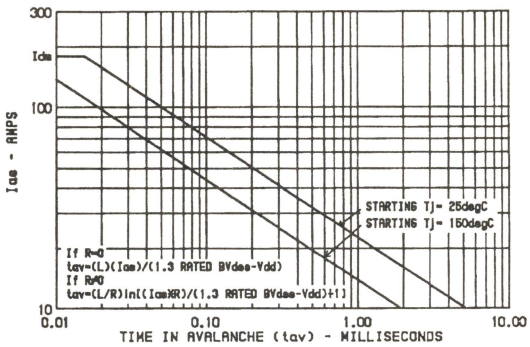


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING

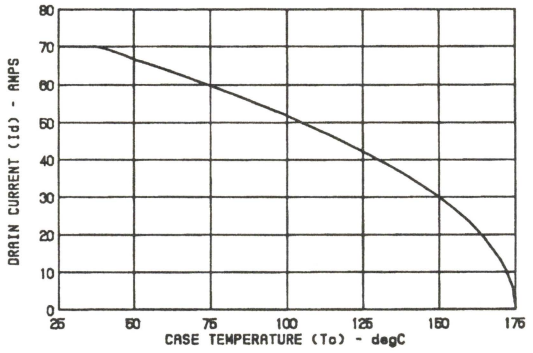


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs. TEMPERATURE

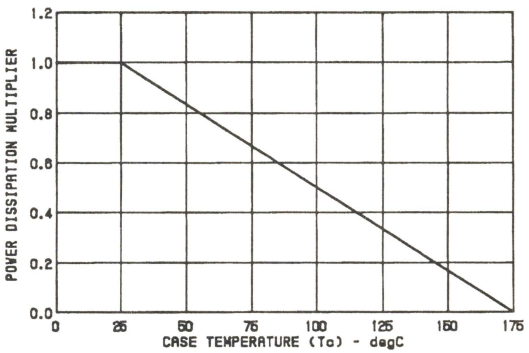


FIGURE 4. NORMALIZED POWER DISSIPATION vs. TEMPERATURE DERATING CURVE

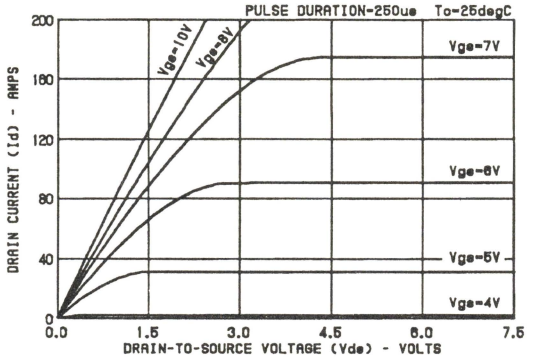


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

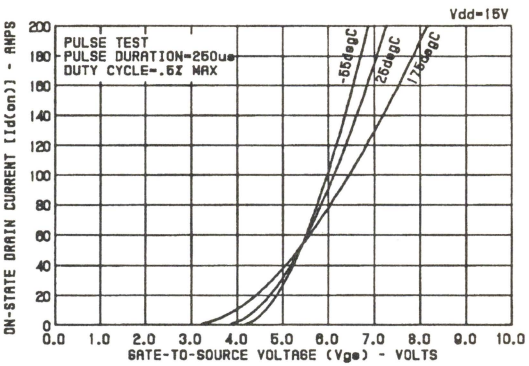


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

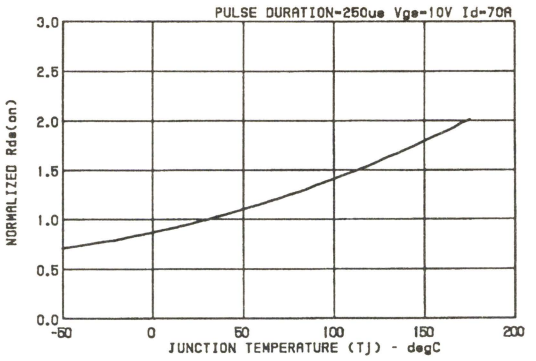


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs. JUNCTION TEMPERATURE

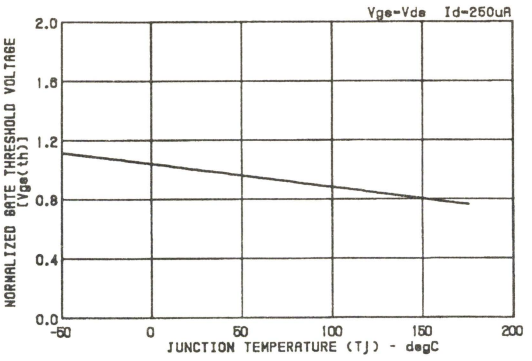


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs. TEMPERATURE

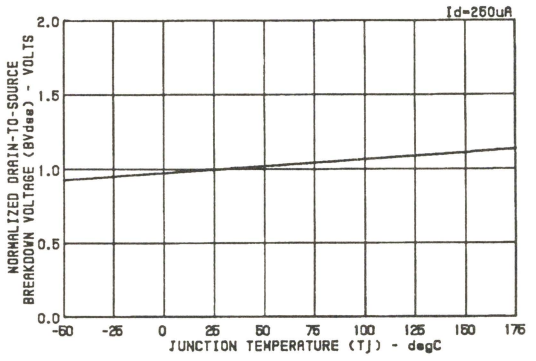


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs. TEMPERATURE

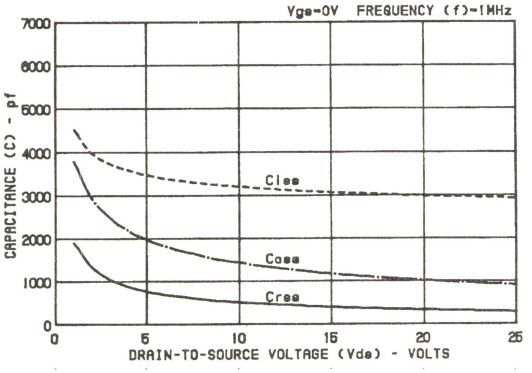


FIGURE 10. TYPICAL CAPACITANCE vs. VOLTAGE

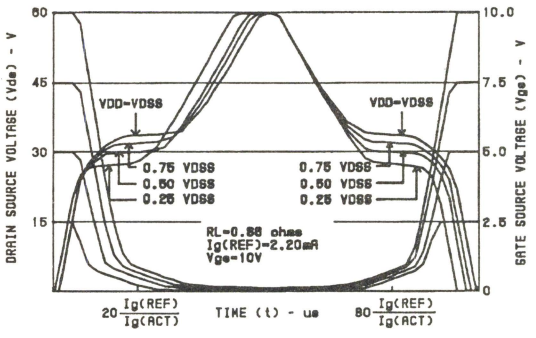


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

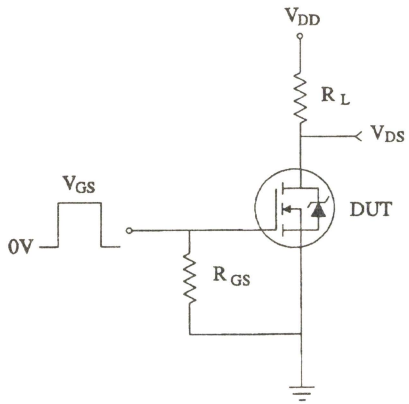


FIGURE 12. RESISTIVE SWITCHING TEST CIRCUIT

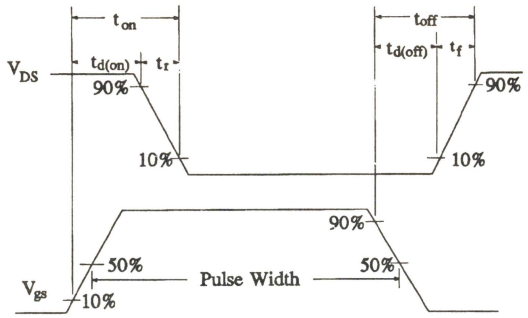


FIGURE 13. RESISTIVE SWITCHING WAVEFORMS

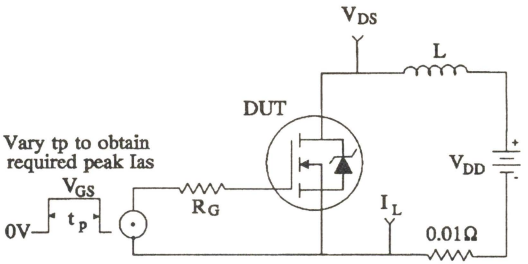


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

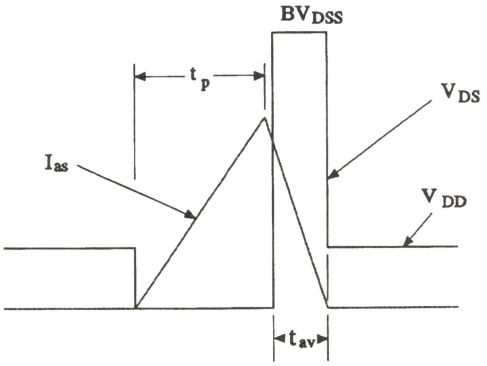


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

PSPICE Model For the RFG70N06, RFP70N06

```
SUBCKT TA49007 2 1 3 ;        rev 3/20/92
*Nom Temp=25 deg C

Ca 12 8 5.56e-9
Cb 15 14 5.303e-9
Cin 6 8 2.63e-9

Dbody 7 5 DBDMOD
Dplcap 10 5 DPLCAPMOD
Dbreak 5 11 DBKMOD

Ebreak 11 7 17 18 65.1
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evto 20 6 18 8 1

It 8 17 1

Lgate 1 9 3.10e-9
Ldrain 2 5 1e-9
Lsource 3 7 1.82e-9

Mos1 16 6 8 8 MOSMOD M=0.99
Mos2 16 21 8 8 MOSMOD M=0.01

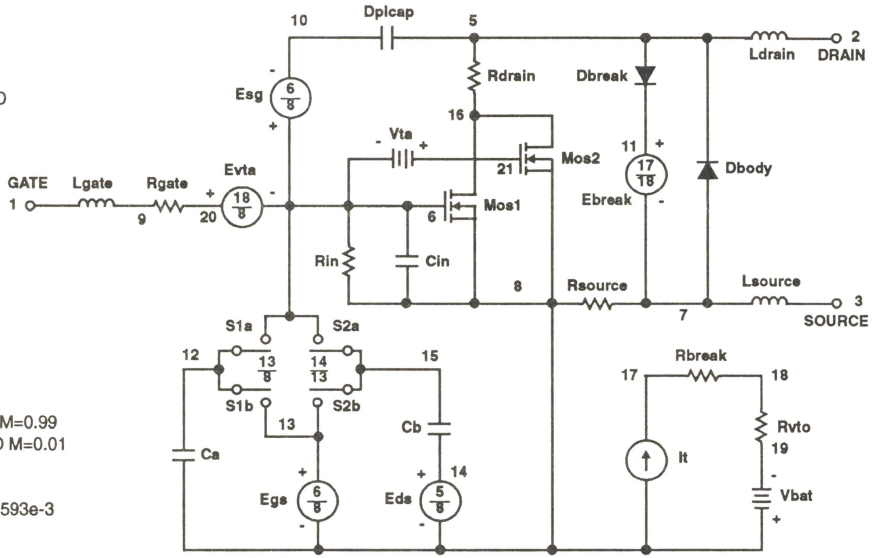
Rbreak 17 18 RBKMOD 1
Rdrain 5 16 RDSMOD 4.6593e-3
Rgate 9 20 1.21
Rin 6 8 1e9
Rsource 8 7 RDSMOD 1.822e-3
Rvto 18 19 RVTOMOD 1

S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 8 19 DC 1
Vto 21 6 0.6977

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.90 VOFF=-2.90)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.90 VOFF=-4.90)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.20 VOFF=4.80)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.80 VOFF=-3.20)
.MODEL DBDMOD D (IS=1.11e-12 RS=2.91e-3 TRS1=3.26e-3 TRS2=-5.07e-6 CJO=3.12e-9 TT=6.18e-8)
.MODEL DBKMOD D (RS=9.46e-2 TRS1=8.47e-4 TRS2=-1.31e-6)
.MODEL DPLCAPMOD D (CJO=1.92e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.674 KP=38.507 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.55e-4 TC2=5.99e-8)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=2.37e-5)
.MODEL RVTOMOD RES (TC1=-3.71e-3 TC2=-6.01e-7)

.ENDS
```



Note: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

HARRIS

RFG75N05E
RFH75N05E

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

January 1993

Features

- 75A, 50V
- $r_{DS(on)} = 0.008\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

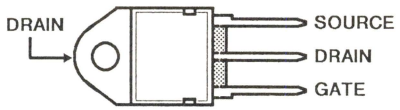
Description

The RFG75N05E and RFH75N05E n-channel ESD rated power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

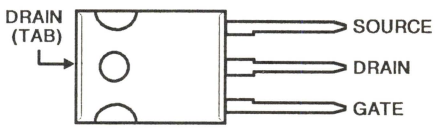
The RFG75N05E is supplied in the TO-247 style (3 lead) plastic package and the RFH75N05E is supplied in the TO-218 (3 lead) plastic package.

Package

TO-218
TOP VIEW

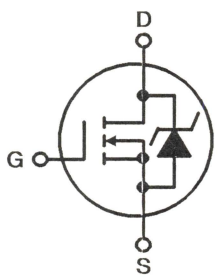


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG75N05E RFH75N05E	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	V
Continuous Drain Current	I_D	75*	A
Pulsed Drain Current	I_{DM}	200	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	240	W
Derated Above +25°C		1.6	W/°C
Operating and Storage Junction Temperature Range	T_{JC}, T_{STG}	-55 to +175	°C
Electrostatic Discharge Rating			
MIL-STD-883, Category B(2)	E_{SD}	2	kV
Single-Pulse Avalanche Rating		Refer to UIS SOA Curves	

*I_D Current Limited by Package

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2275.3

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		-	-	1	µA
		T_C =+150°C		-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 75A, V_{GS} = 10V		-	-	0.008	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 37.5A		-	-	125	ns
Turn-On Delay Time	$t_{d(on)}$	R_L = 0.67Ω		-	17	-	ns
Rise Time	t_r	$I_{G1} = I_{G2}$ = 3A		-	75	-	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS(clamp)}$ = +10V, -0.6V		-	70	-	ns
Fall Time	t_f			-	17	-	ns
Turn-Off Time	$t_{(off)}$			-	-	125	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0, 20V	V_{DD} = 40V	-	-	400	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0, 10V	I_D = 75A	-	-	220	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0, 2V	R_L = 0.53Ω	-	-	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 75A, V_{DS} = 15V		-	-	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 37.5A, $I_{G1} = I_{G2}$ = 3A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 0.67Ω		-	-	300	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.625	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 75A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 75A, dI_f/dt = 100A/µs	-	-	125	ns

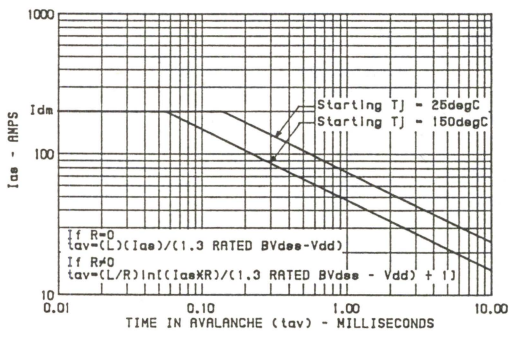


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

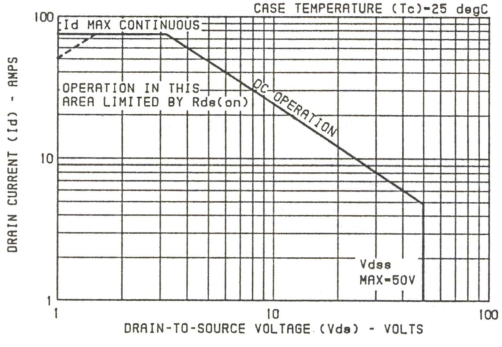


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

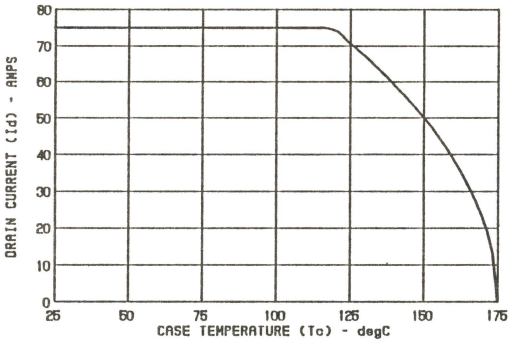


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

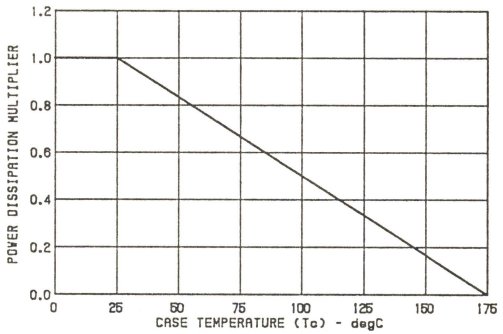


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

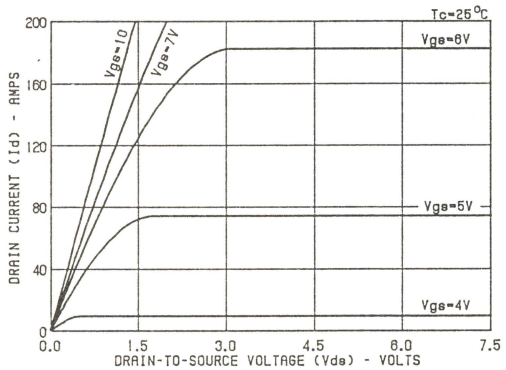


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

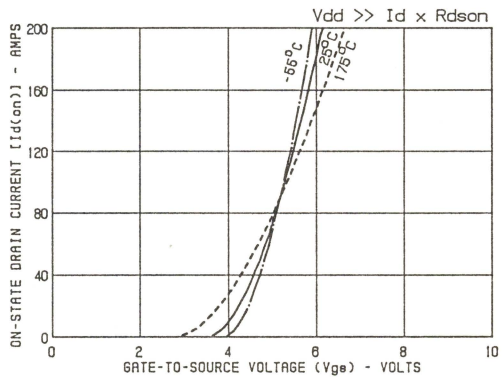


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

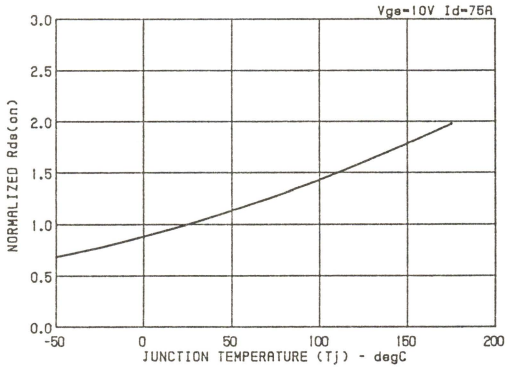


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

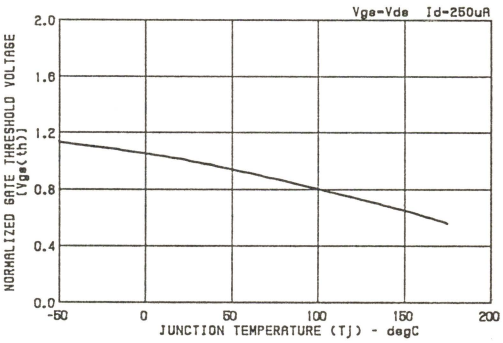


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

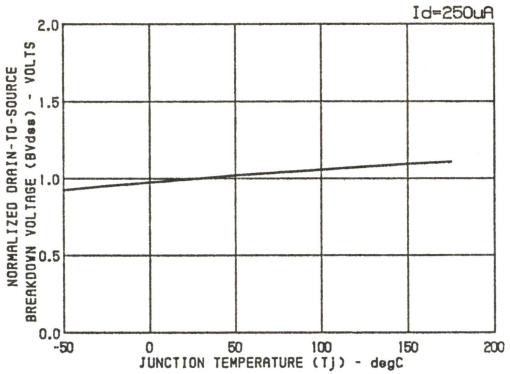


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

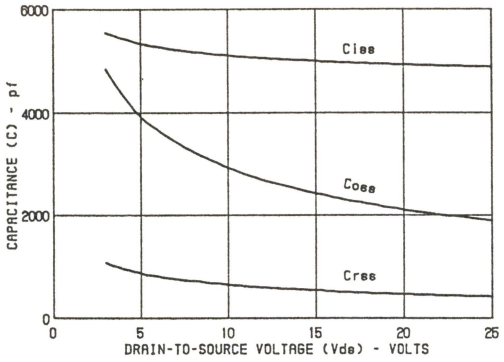


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

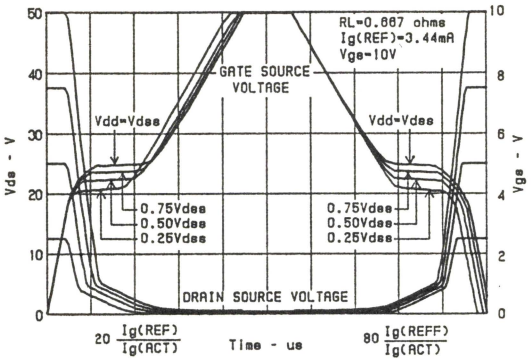


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

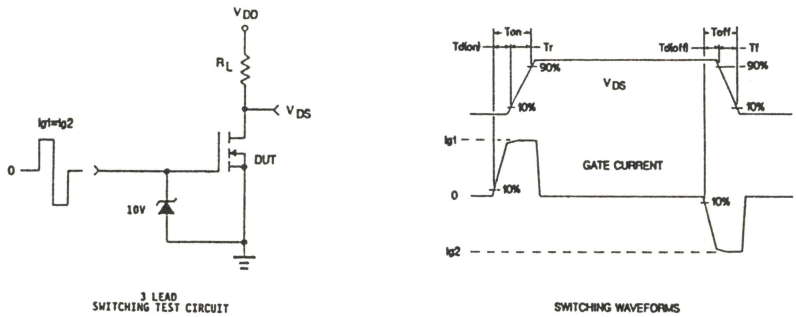


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

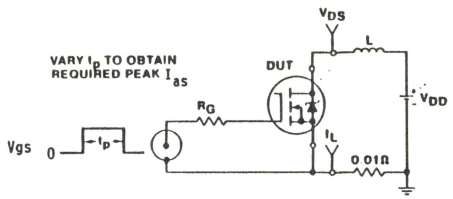


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

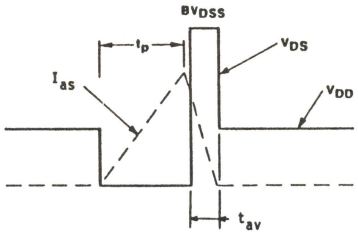
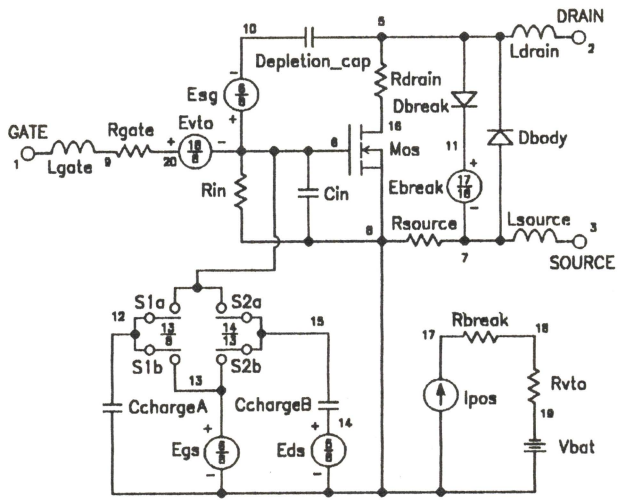


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Spice Model

```
.SUBCKT RFH75N05  2  1  3  ;  rev 10/30/90
*Nominal Temperature = 25°C
CchargeA  12  8  8.98e-9
CchargeB  15  14  8.81e-9
Cin  6  8  4.48e-9
Depletion_cap  10  5  DPLCAPMOD
Dbody  7  5  DBODYMOD
Dbreak  5  11  DBREAKMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Ebreak  11  7  17  18  58.4
Evto  20  6  18  8  1
Ipos  8  17  1
Ldrain  2  5  e-10
Lgate  1  9  5e-9
Lsource  3  7  3e-9
Mos  16  6  8  8  MOSMOD
Rbreak  17  18  RBREAKMOD  1
Rdrain  5  16  RSOURCEMOD  3.07e-3
Rgate  9  20  1.2
Rin  6  8  1e9
Rsource  8  7  RSOURCEMOD  2.e-3
Rvto  18  19  RVTONEGMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.MODEL  S1AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.48  VOFF=-0.48)
.MODEL  S1BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-0.48  VOFF=-2.48)
.MODEL  S2AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=2.75)
.MODEL  S2BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=2.75  VOFF=-2.25)
.MODEL  DBODYMOD  D  (IS=2.23e-12  RS=249e-3  TRS1=2.5e-3  CJO=7.55e-9  TT=4e-8)
.MODEL  DBREAKMOD  D  (RS=8e-2  TRS1=2.5e-3)
.MODEL  DPLCAPMOD  D  (IS=1e-30  N=10  CJO=2.14e-9)
.MODEL  RBREAKMOD  RES  (TC1=9.5e-4  TC2=-1.17e-6)
.MODEL  RSOURCEMOD  RES  (TC1=5.2e-3  TC2-1.37e-5)
.MODEL  RVTONEGMOD  RES  (TC1=-3.78e-3  TC2=-7.51e-7)
.MODEL  MOSMOD  NMOS  (VTO=3.48  N=10  IS=1e-30  KP=78.5  TOX=1  L=1u  W1u)
.ENDS
```



HARRIS

RFA100N05E

N-Channel Enhancement-Mode Power Field-Effect Transistor (MegaFET)

January 1993

Features

- 100A, 50V
- $r_{DS(on)} = 0.008\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

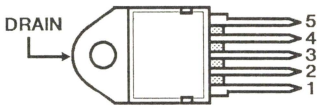
Description

The RFA100N05E n-channel ESD rated power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFA100N05E is supplied in the MO-093 plastic package.

Package

MO-093
TOP VIEW

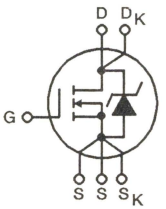


TERMINAL CONNECTIONS

1 - Gate
2 - Source Kelvin
3 - Drain Kelvin
4 - Source Current
5 - Source Current

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFA100N05E	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	V
Continuous Drain Current	I_D	100	A
Pulsed Drain Current	I_{DM}	300	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation			
T_C = +25°C	P_D	240	W
Derated Above 25°C		1.6	W/°C
Operating and Storage Junction Temperature Range	T_{JC}, T_{STG}	-55 to +175	°C
Electrostatic Discharge Rating			
MIL-STD-883, Category B(2)	E_{SD}	2	kV
Single-Pulse Avalanche Rating		Refer to UIS SOA Curves	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2869.2

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		-	-	1	µA
		T_C =+150°C		-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 100A, V_{GS} = 10V		-	-	0.008	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 50A		-	-	60	ns
Turn-On Delay Time	$t_{d(on)}$	R_L = 0.50Ω		-	17	-	ns
Rise Time	t_r	$I_{G1} = I_{G2}$ = 3A		-	8	-	ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS(clamp)}$ = +10V, -0.6V		-	50	-	ns
Fall Time	t_f			-	10	-	ns
Turn-Off Time	$t_{(off)}$			-	-	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0, 20V	V_{DD} = 40V	-	-	430	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0, 10V	I_D = 100A	-	-	230	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0, 2V	R_L = 0.40Ω	-	-	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 100A, V_{DS} = 15V		-	-	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 50A, $I_{G1} = I_{G2}$ = 3A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 0.50Ω		-	-	500	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.625	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 100A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 100A, dI_f/dt = 100A/µs	-	-	125	ns

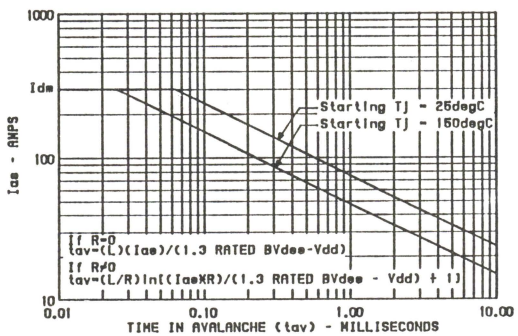


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

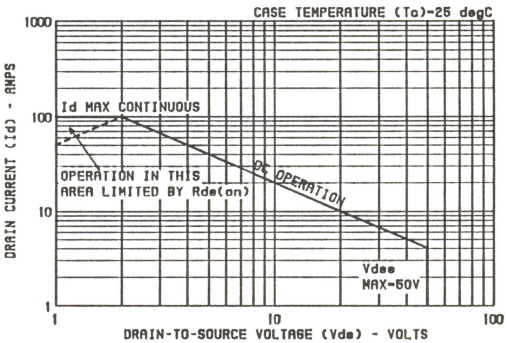


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

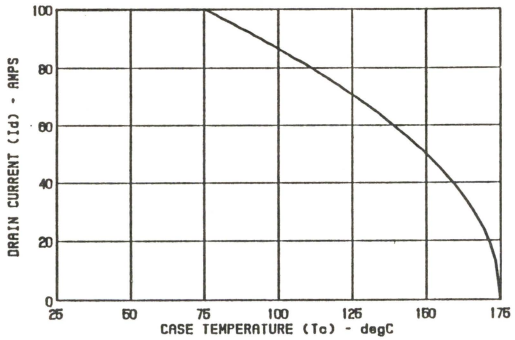


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

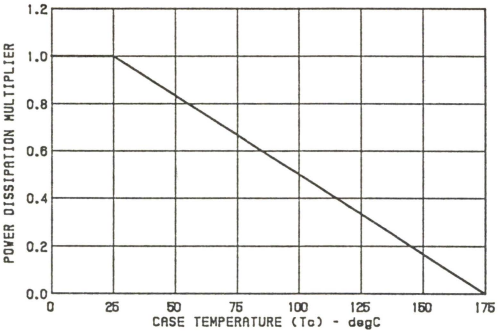


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

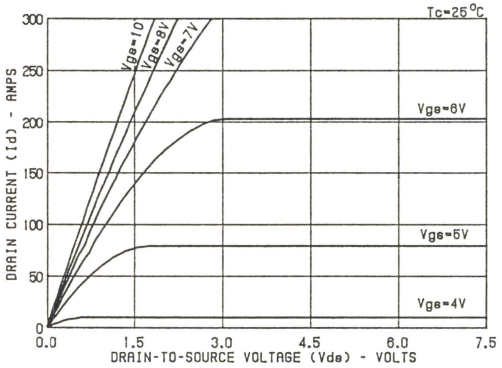


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

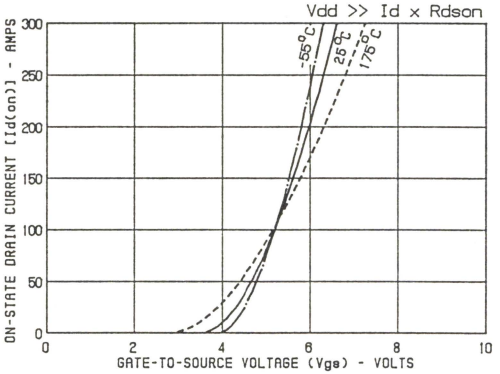


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

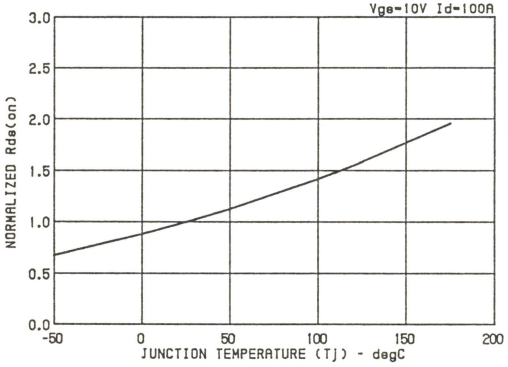


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

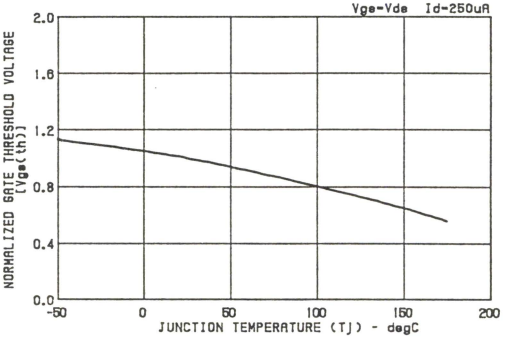


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

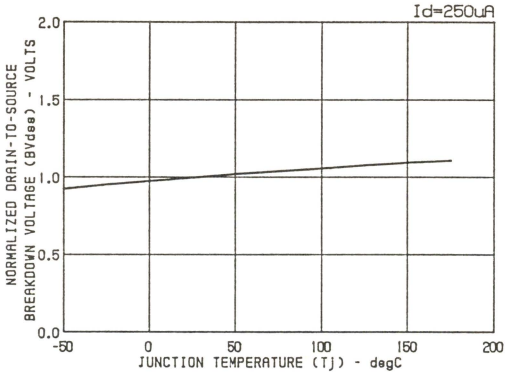


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

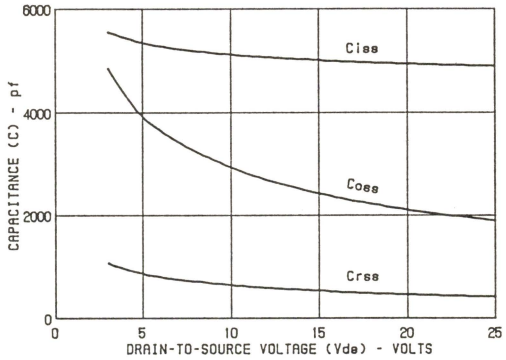


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

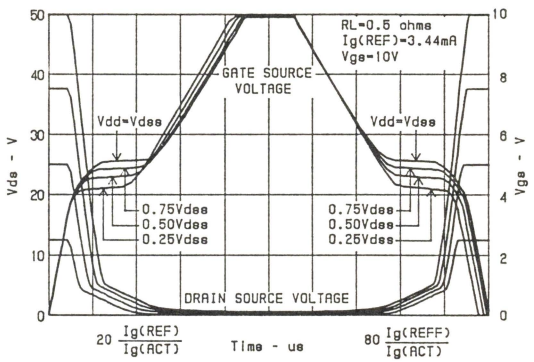


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

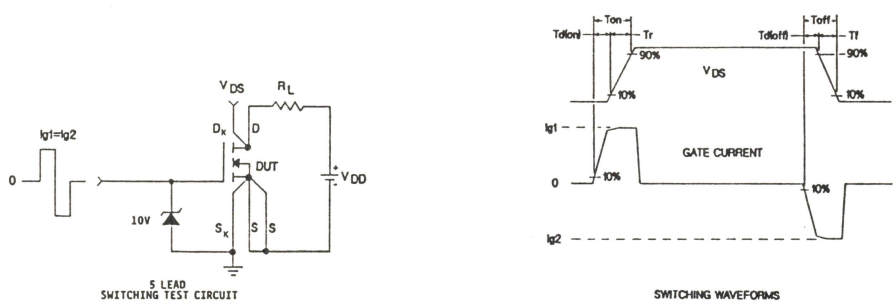
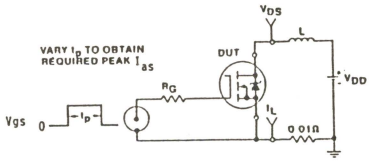


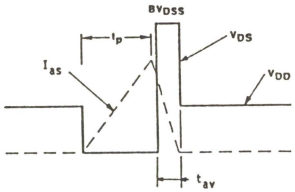
FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)



UIS TEST CIRCUIT.

FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

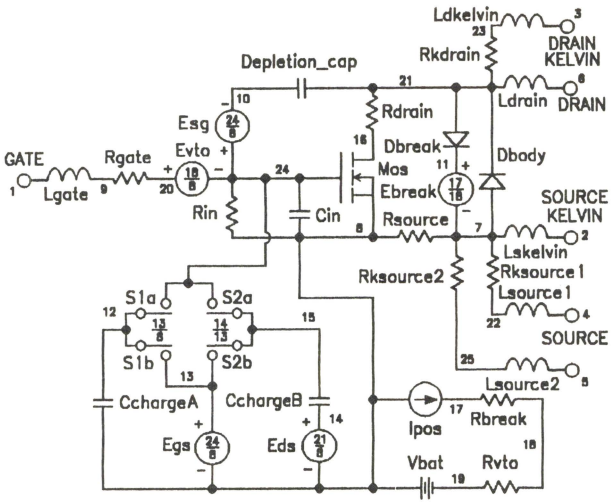


UIS WAVEFORMS.

FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Spice Model

```
.SUBCKT RFA100N05  6  1  4  5  3  2  ;  rev 10/30/90
*Nominal Temperature = 25°C
CchargeA  12  8  8.98e-9
CchargeB  15  14  8.8e-9
Cin  24  8  4.48e-009
Depletion_cap  10  21  DPLCAPMOD
Dbody  7  21  DBODYMOD
Dbreak  21  11  DBREAKMOD
Eds  14  8  21  8  1
Egs  13  8  24  8  1
Esg  24  10  24  8  1
Ebreak  11  7  17  18  58.4
Evto  20  24  18  8  1
Ipos  8  17  1
Ldkelvin  3  23  1e-9
Ldrain  6  21  2e-10
Lgate  1  9  5e-9
Lskelvin  2  7  5e-9
Lsource1  4  22  6e-9
Lsource2  5  25  6e-9
Mos  16  24  8  8  MOSMOD
Rbreak  17  18  RBREAKMOD  1
Rdrain  21  16  RSOURCEMOD  2.74e-3
Rgate  9  20  1.2
Rkdrain  23  21  0.33e-3
Rksource1  7  22  1.6e-3
Rksource2  7  25  1.6e-3
Rin  24  8  1e+9
Rsource  8  7  RSOURCEMOD  1.2e-3
Rvto  18  19  RVTONEGMOD  1
S1a  24  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  24  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.MODEL  S1AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.48  VOFF=-0.48)
.MODEL  S1BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-0.48  VOFF=-2.48)
.MODEL  S2AMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=2.75)
.MODEL  S2BMOD  VSWITCH  (RON=1e-5  ROFF=0.1  VON=2.75  VOFF=-2.25)
.MODEL  DBODYMOD  D  (IS=2.23e-12  RS=2.5e-3  TRS1=2.5e-3  CJO=7.55e-9  TT=4e-8)
.MODEL  DBREAKMOD  D  (RS=8e-2  TRS1=2.5e-3)
.MODEL  DPLCAPMOD  D  (IS=1e-030  N=10  CJO=2.14e-9)
.MODEL  RBREAKMOD  RES  (TC1=9.5e-4  TC2=-1.17e-6)
.MODEL  RSOURCEMOD  RES  (TC1=5.2e-3  TC2=1.37e-5)
.MODEL  RVTONEGMOD  RES  (TC1=-3.78e-3  TC2=-7.5e-7)
.MODEL  MOSMOD  NMOS  (VTO=3.48  N=10  IS=1e-030  KP=78.5  TOX=1  L=1u  W1u)
.ENDS
```



POWER MOSFETs 5

P-CHANNEL POWER MOSFETs

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HARRIS

2N6804

Avalanche-Energy-Rated P-Channel Power MOSFETs

August 1991

Features

- -11A, -100V
- $r_{DS(on)} = 0.30\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

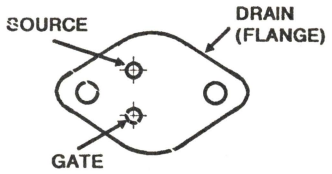
Description

The 2N6804 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6804 is supplied in the JEDEC TO-204AA steel package.

Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6804	UNITS
Drain-Source Voltage	V_{DS}	-100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
T_C = +25°C	I_D	-11*	A
T_C = +100°C	I_D	-7.0*	A
Pulsed Drain Current (Note 2)	I_{DM}	-50*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	75*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.6*	W/°C
Single Pulse Avalanche Energy (Note 3)	E_{AS}	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

*JEDEC registered values

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
2. Repetitive Rating: Pulse width limited by maximum junction temperature, See Transient Thermal Impedance Curve (Figure 5).
3. V_{DD} = 25V, Starting T_J = 25°C, L = 6.2mH, R_G = 25Ω, Peak I_L = 11A, (See Figure 15 and 16).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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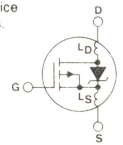
File Number 2217

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Current ①	−11*	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = −10V
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30	Ω	V_{GS} = −10V, I_D = −6.5A
g_{fs}	Forward Transconductance ①	2.0	3.7	—	S(℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = −6.5A
C_{iss}	Input Capacitance	400	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} ≃ −35V, I_D = −7.0A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

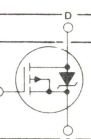


Thermal Resistance

$R_{\theta JC}$	Junction-to-Case	—	—	1.67*	°C/W	
$R_{\theta CS}$	Case-to-Sink	—	0.1	—	°C/W	Mounting surface flat, smooth, and greased.
$R_{\theta JA}$	Junction-to-Ambient	—	—	30	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−50	A	
V_{SD}	Diode Forward Voltage ①	—	—	−1.5	V	T_C = 25°C, I_S = −11A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −11A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, Starting T_J = 25°C, L = 6.2 mH, R_G = 25Ω, Peak I_L = 11 A. (See Fig. 15 and 16).

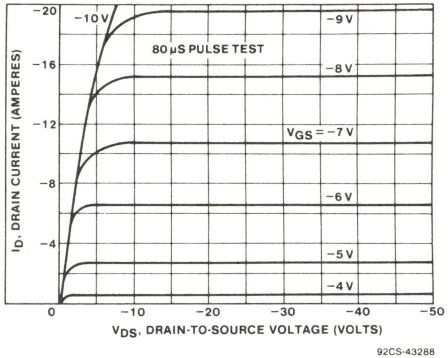


Fig. 1 - Typical Output Characteristics

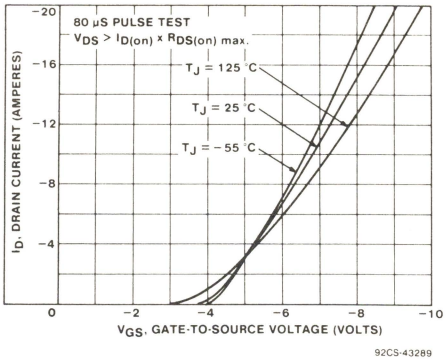


Fig. 2 - Typical Transfer Characteristics

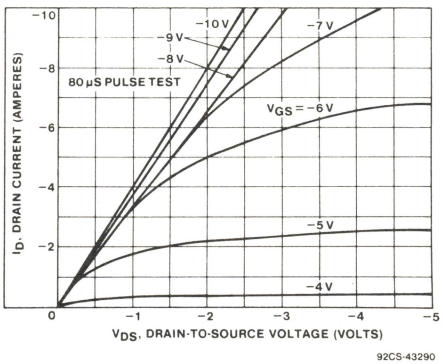


Fig. 3 - Typical saturation characteristic.

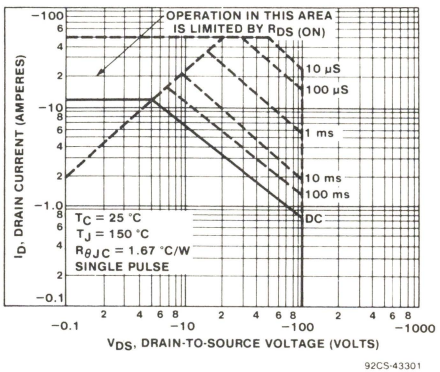


Fig. 4 - Maximum safe operating area.

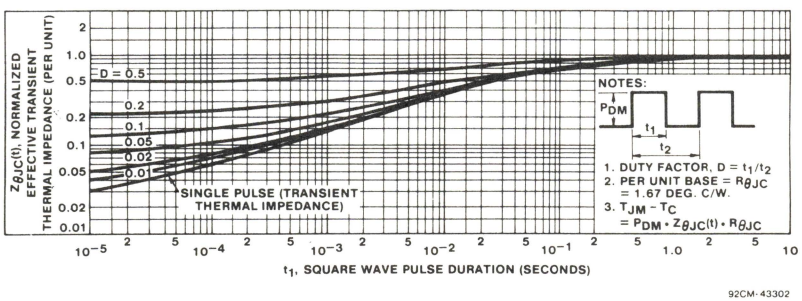


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

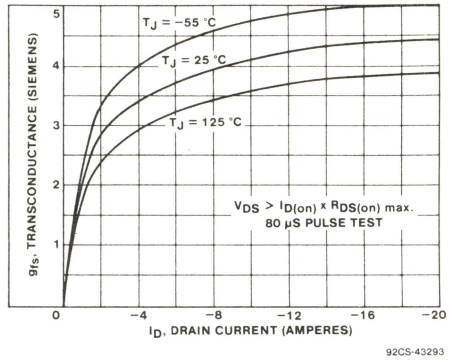


Fig. 6 - Typical transconductance vs. drain current.

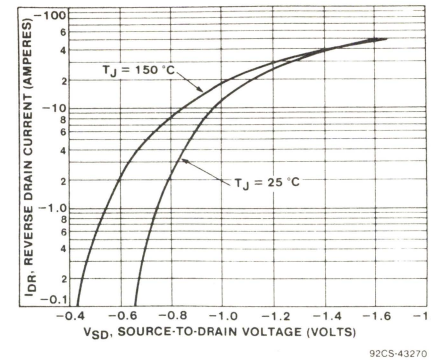


Fig. 7 - Typical source-drain diode forward voltage.

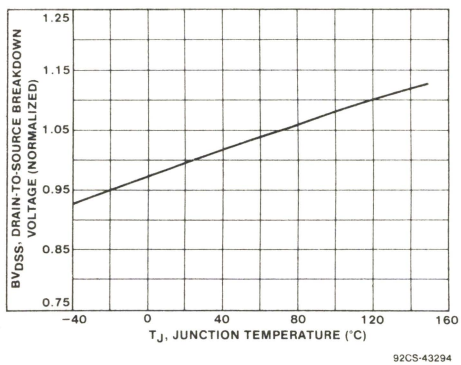


Fig. 8 - Breakdown voltage vs. temperature.

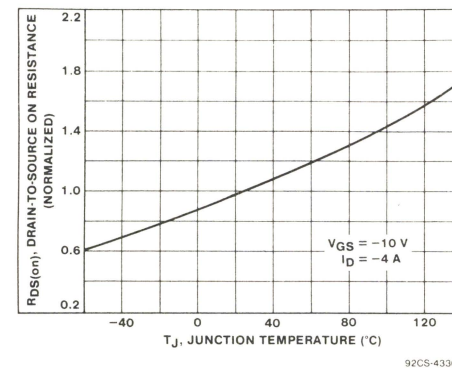


Fig. 9 - Normalized on-resistance vs. temperature.

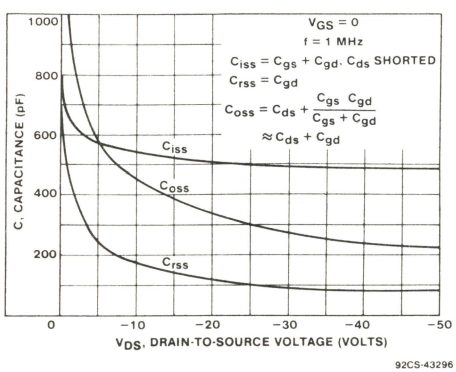


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

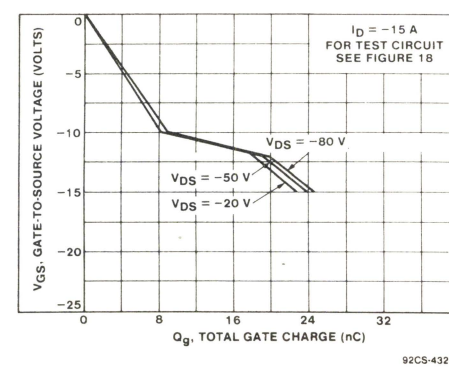


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

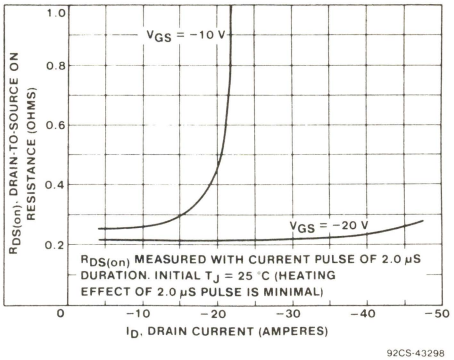


Fig. 12 - Typical on-resistance vs. drain current.

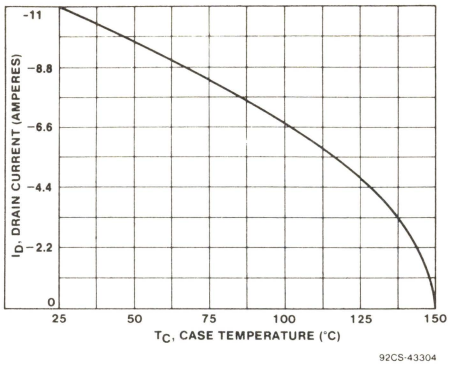


Fig. 13 - Maximum drain current vs. case temperature.

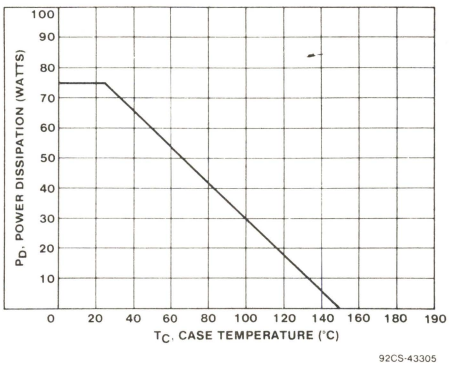


Fig. 14 - Power vs. temperature derating curve.

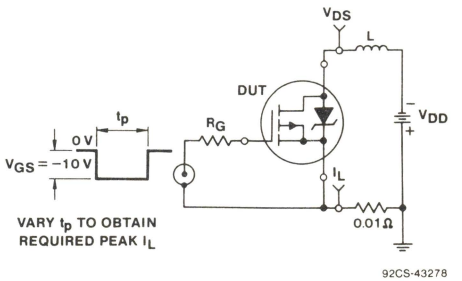


Fig. 15 - Unclamped inductive test circuit.

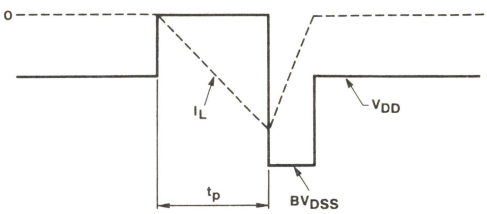


Fig. 16 - Unclamped inductive waveforms.

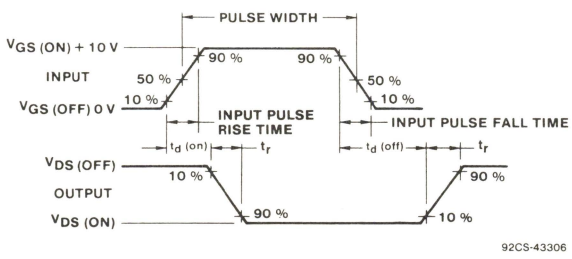


Fig. 17 - Switching time test circuit.

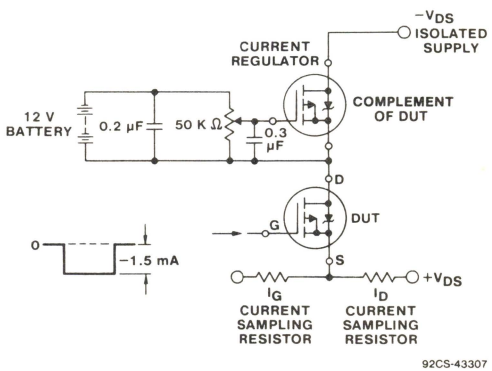


Fig. 18 - Gate charge test circuit.

HARRIS

2N6849

Avalanche-Energy-Rated P-Channel Power MOSFETs

August 1991

Features

- -6.5A, -100V
- $r_{DS(on)} = 0.30\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

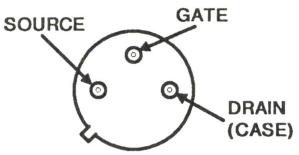
Description

The 2N6849 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6849 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

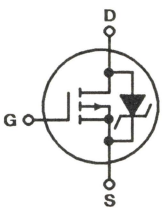
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		2N6849	UNITS
Drain-Source Voltage	V_{DS}	-100*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	V_{DGR}	-100*	V
Continuous Drain Current			
$T_C = +25^oC$	I_D	-6.5*	A
$T_C = +100^oC$	I_D	-4.1*	A
Pulsed Drain Current (Note 2)	I_{DM}	-25*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
$T_C = +25^oC$ (See Figure 14)	P_D	25*	W
Above $T_C = +25^oC$, Derate Linearly (See Figure 14)		0.2*	W/^oC
Single Pulse Avalanche Energy (Note 3)	E_{AS}	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	^oC
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	^oC

NOTES:

*JEDEC registered values

1. Pulse Test: Pulse width $\leq$ 300μs, Duty Cycle $\leq$ 2%
2. Repetitive Rating: Pulse width limited by maximum junction temperature, See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Starting T_J = 25°C, L = 17.25mH, R_G = 25Ω, Peak I_L = 6.5A, (See Figure 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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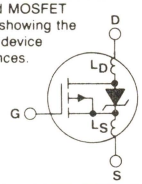
File Number 2219

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−100*	—	—	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−2.1	V	V_{DS} > $I_{D(on)}R_{DS(on)}$max., V_{GS} = −10V, I_D = 6.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.30*	Ω	V_{GS} = −10V, I_D = −4.1A
g_{fs}	Forward Transconductance ①	2.5	3.5	7.5	S(℧)	V_{DS} = −5V, $I_{D(on)}$ × $R_{DS(on)}$ max., I_D = −4.1A
C_{iss}	Input Capacitance	—	500	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}	Output Capacitance	—	300	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	—	100	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	60	ns	V_{DD} ≅ −42V, I_D = −4.1A, Z_o = 50Ω
t_r	Rise Time	—	70	140	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	70	140	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	25	45	nC	V_{GS} = −15V, I_D = −15A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	13	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	12	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

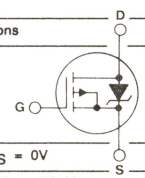


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−6.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−25	A	
V_{SD}	Diode Forward Voltage ①	—	—	−1.5	V	T_C = 25°C, I_S = −6.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	—	1.8	—	μC	T_J = 25°C, I_F = −6.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 25V, starting T_J = 25°C, L = 17.25 mH, R_G = 25Ω, Peak I_L = 6.5A. (See Fig. 15 and 16)

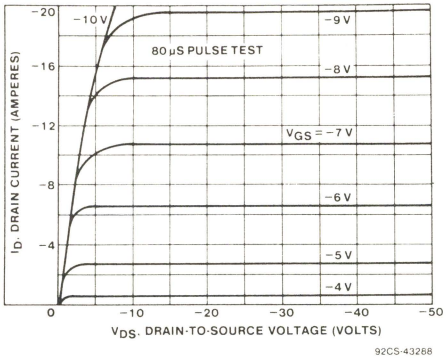


Fig. 1 - Typical Output Characteristics

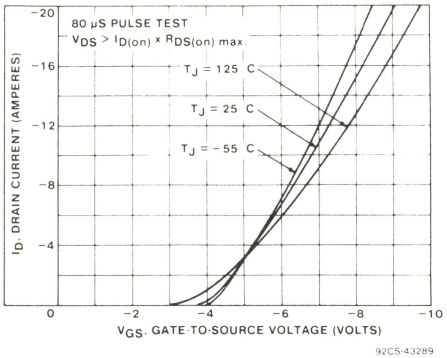


Fig. 2 - Typical Transfer Characteristics

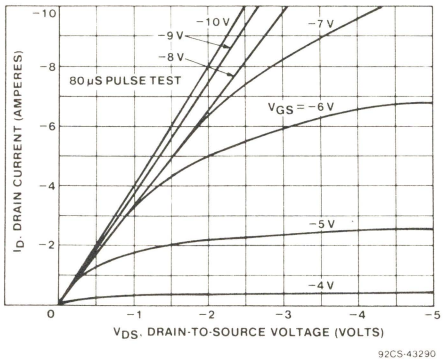


Fig. 3 - Typical Saturation Characteristics

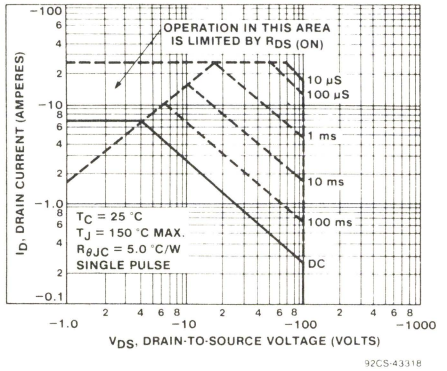


Fig. 4 - Maximum Safe Operating Area

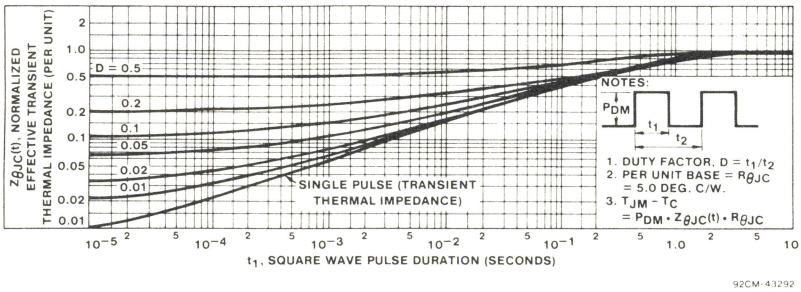


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

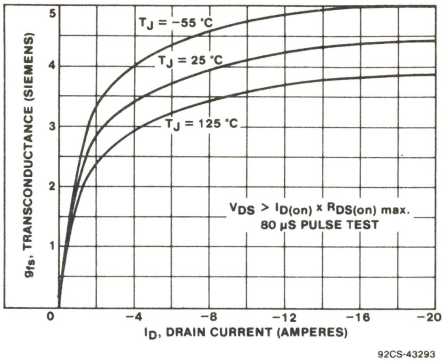


Fig. 6 - Typical Transconductance Vs. Drain Current

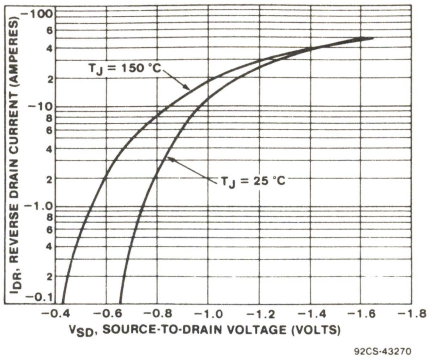


Fig. 7 - Typical Source-Drain Diode Forward Voltage

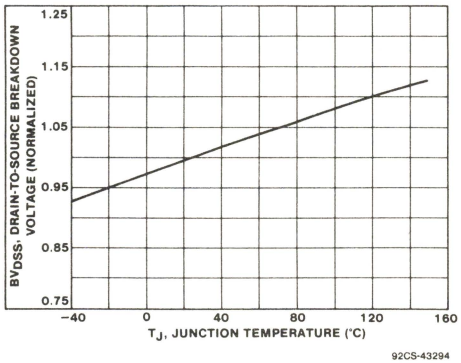


Fig. 8 - Breakdown Voltage Vs. Temperature

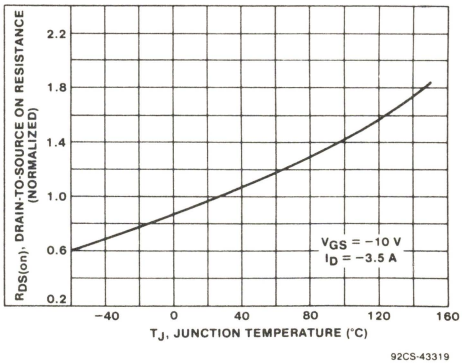


Fig. 9 - Normalized On-Resistance Vs. Temperature

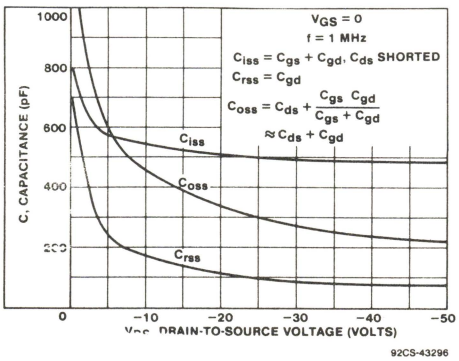


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

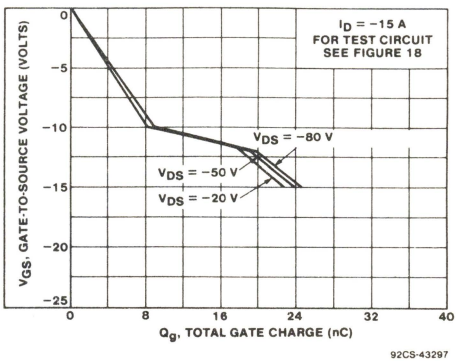


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

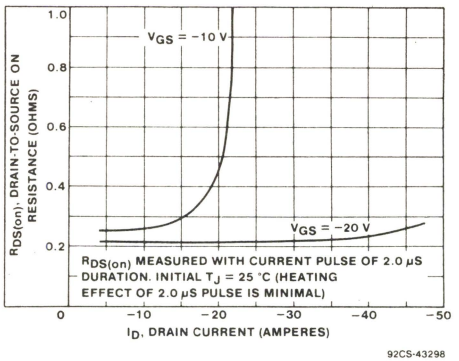


Fig. 12 - Typical On-Resistance Vs. Drain Current

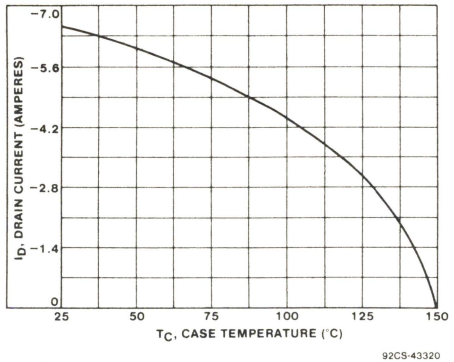


Fig. 13 - Maximum Drain Current Vs. Case Temperature

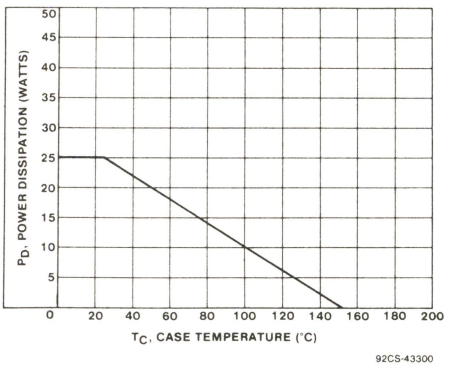


Fig. 14 - Power Vs. Temperature Derating Curve

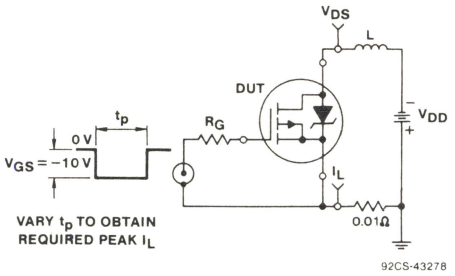


Fig. 15 - Unclamped Inductive Test Circuit

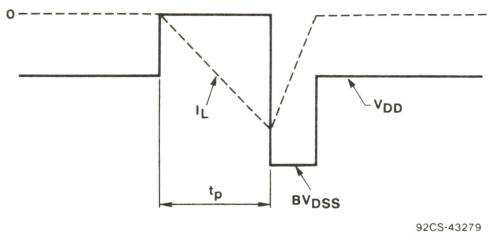


Fig. 16 - Unclamped Inductive Waveforms

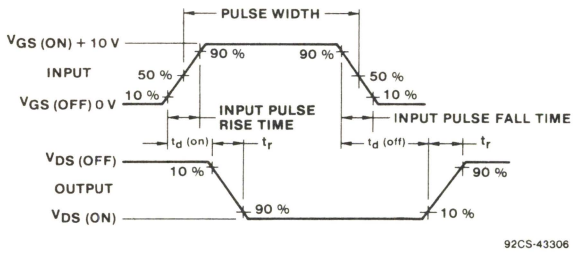


Fig. 17 - Switching Time Test Circuit

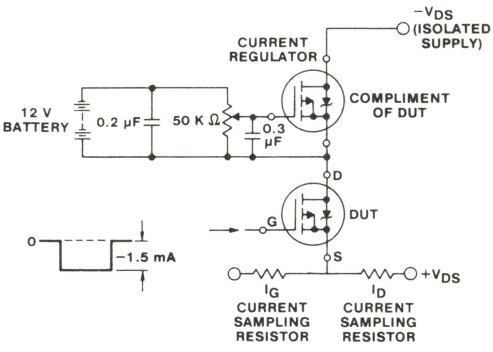


Fig. 18 - Gate Charge Test Circuit

HARRIS

2N6851

Avalanche-Energy-Rated P-Channel Power MOSFETs

August 1991

Features

- -4.0A, -200V
- $r_{DS(on)} = 0.80\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

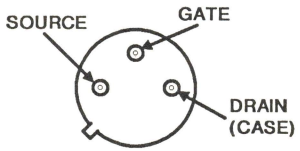
Description

The 2N6851 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6851 is supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6851	UNITS
Drain-Source Voltage	V_{DS}	-200*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	-200*	V
Continuous Drain Current			
T_C = +25°C	I_D	-4.0*	A
T_C = +100°C	I_D	-2.4*	A
Pulsed Drain Current (Note 2)	I_{DM}	-20*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C (See Figure 14)	P_D	25*	W
Above T_C = +25°C, Derate Linearly (See Figure 14)		0.2*	W/°C
Single Pulse Avalanche Energy (Note 3)	E_{AS}	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	°C

NOTES:

*JEDEC registered values

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
2. Repetitive Rating: Pulse width limited by maximum junction temperature, See Transient Thermal Impedance Curve (Figure 5).
3. V_{DD} = 50V, Starting T_J = 25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A, (See Figure 15 and 16).

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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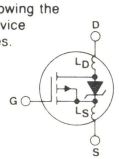
File Number 2218

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−200*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−3.3	V	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ max., V_{GS} = −10V, I_D = −4.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.80*	Ω	V_{GS} = −10V, I_D = −2.4A
g_{fs}	Forward Transconductance ①	2.2	3.5	6.6	S(℧)	V_{DS} = −5V × $R_{DS(on)max.}$, I_D = −2.4A
C_{iss}	Input Capacitance	400	550	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}*	Output Capacitance	50	170	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	40	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	50	ns	V_{DD} ≅ −95V, I_D = −2.4A, Z_o = 50Ω
t_r	Rise Time	—	50	100	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	50	80	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	40	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	31	45	nC	V_{GS} = −15V, I_D = −8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	18	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	13	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

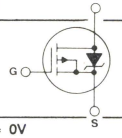


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−20	A	
V_{SD}	Diode Forward Voltage ①	—	—	−1.5	V	T_C = 25°C, I_S = −4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	400	ns	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	2.6	—	μC	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 50V, starting T_J = 25°C, L = 46.9 mH, R_G = 25Ω, Peak I_L = 4.0A. (See Fig. 15 and 16)

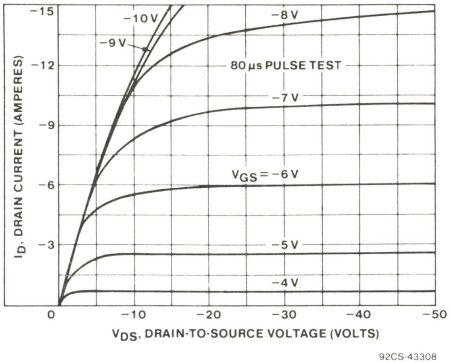


Fig. 1 - Typical Output Characteristics

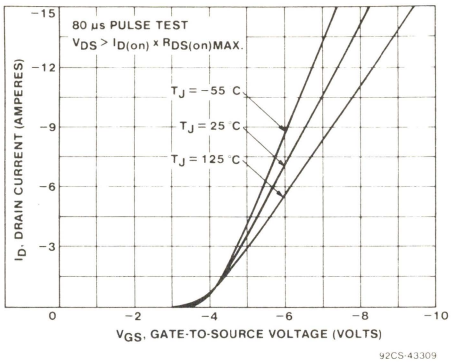


Fig. 2 - Typical Transfer Characteristics

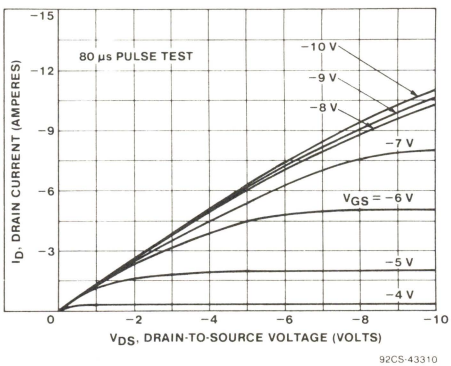


Fig. 3 - Typical Saturation Characteristics

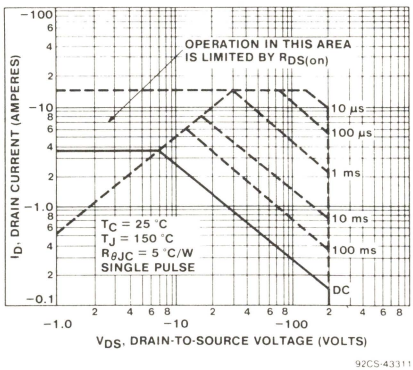


Fig. 4 - Maximum Safe Operating Area

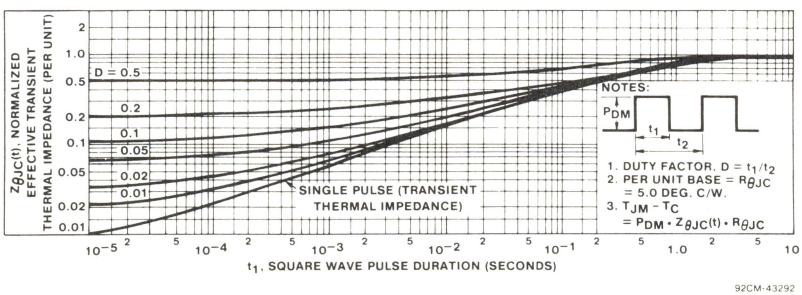


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

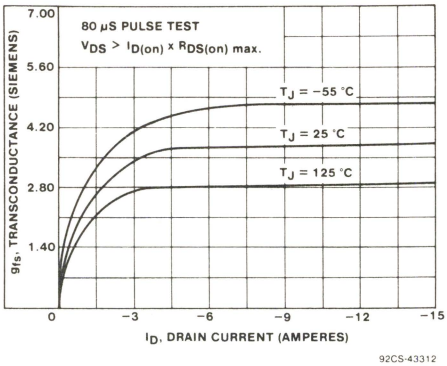


Fig. 6 - Typical Transconductance Vs. Drain Current

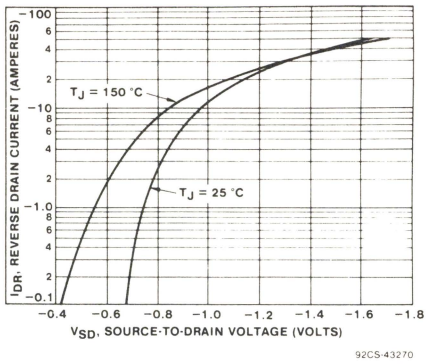


Fig. 7 - Typical Source-Drain Diode Forward Voltage

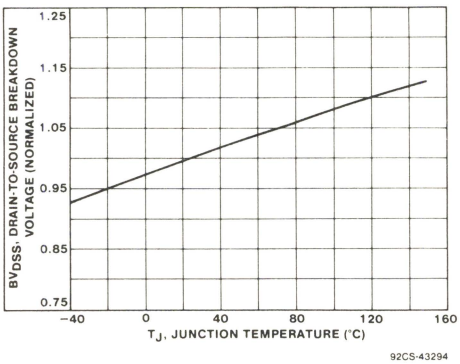


Fig. 8 - Breakdown Voltage Vs. Temperature

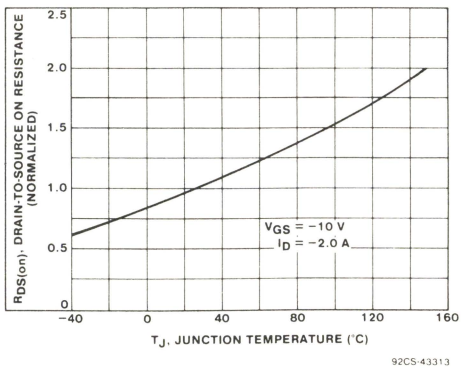


Fig. 9 - Normalized On-Resistance Vs. Temperature

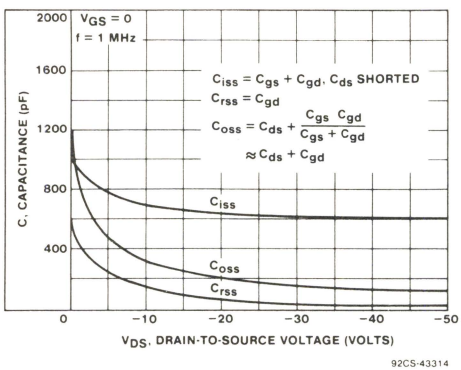


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

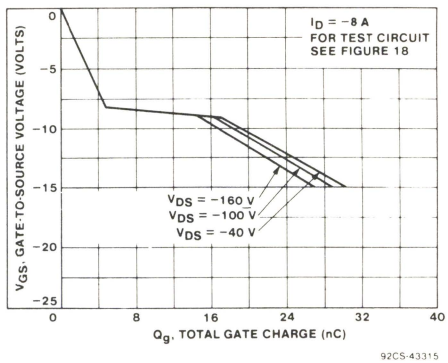


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

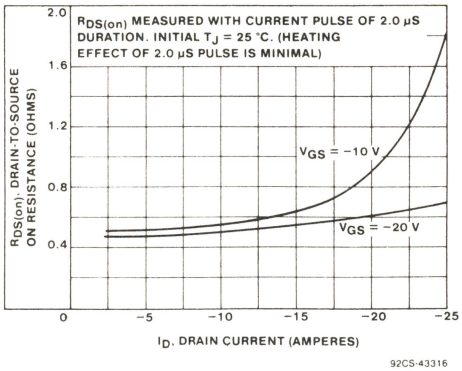


Fig. 12 - Typical On-Resistance Vs. Drain Current

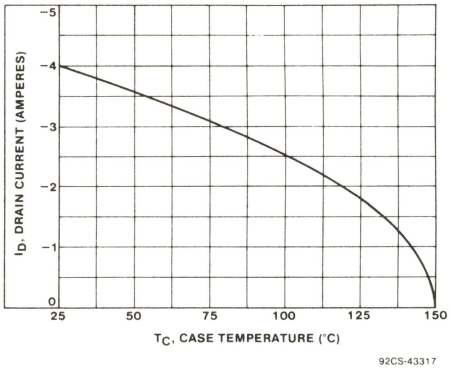


Fig. 13 - Maximum Drain Current Vs. Case Temperature

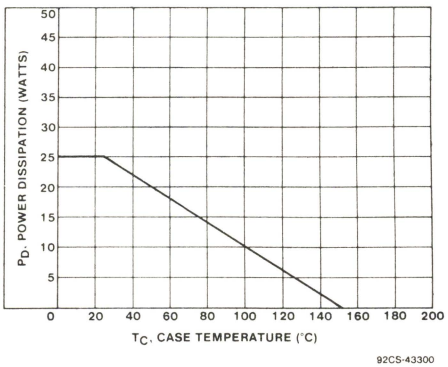


Fig. 14 - Power Vs. Temperature Derating Curve

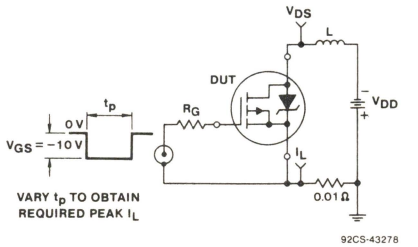


Fig. 15 - Unclamped Inductive Test Circuit

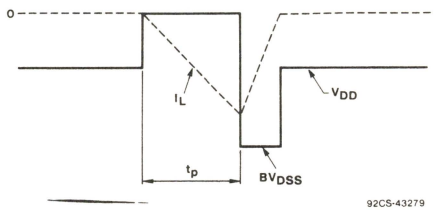


Fig. 16 - Unclamped Inductive Waveforms

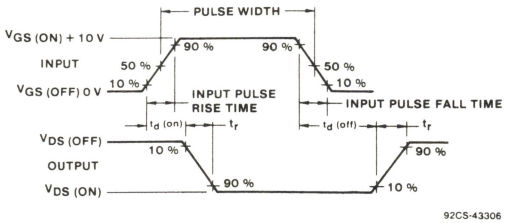


Fig. 17 - Switching Time Test Circuit

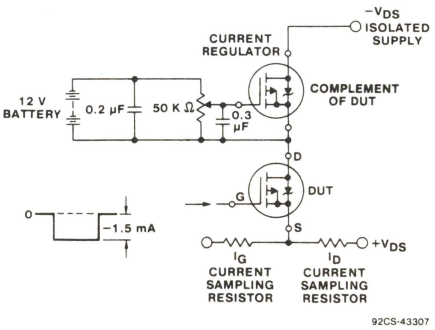


Fig. 18 - Gate Charge Test Circuit

HARRIS

2N6895

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- -1.16A, -100V
- $r_{DS(on)} = 3.65\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

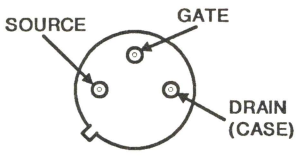
Description

The 2N6895 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6895 is supplied in the JEDEC TO-205AF metal package.

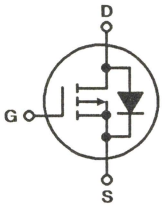
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6895	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-1.16*	A
Pulsed Drain Current	I_{DM}	-5*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	8.33*	W
Above T_C = +25°C, Derate Linearly		0.0667*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
(At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1873

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 0.74 A, V_{GS} = -10 V	—	2.7	V
			I_D = 1.16 A, V_{GS} = -10 V	—	6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 0.74 A, V_{GS} = -10 V	—	3.65	Ω
			T_C = 125°C, I_D = 0.74 A, V_{GS} = 10 V	—	5.66	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 0.74 A	200	800	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	40	150	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	20	80	
*	Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	7.5	30	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	25	ns
*	Rise Time	t_r	I_D = 0.74 A	—	45	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	45	
*	Fall Time	t_f	V_{GS} = -10 V	—	50	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1.16 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 50 A/μs	—	340	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

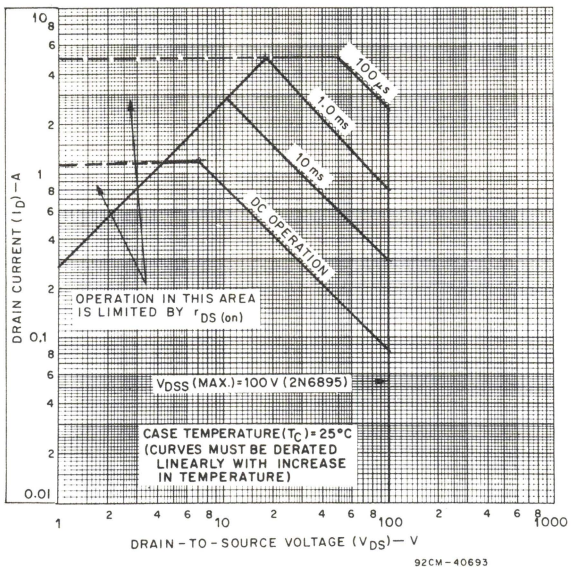


Fig. 1 - Maximum operating areas.

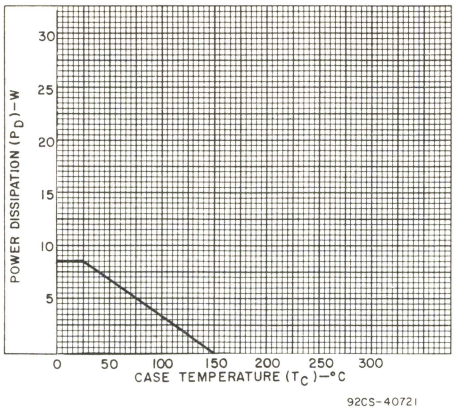


Fig. 2 - Power dissipation vs. temperature derating curve.

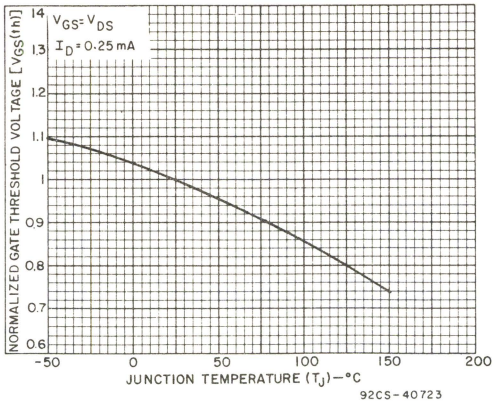


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

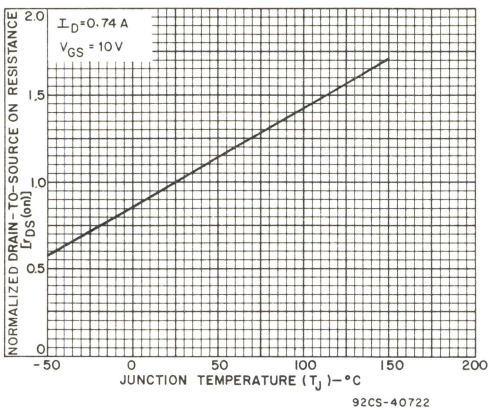


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

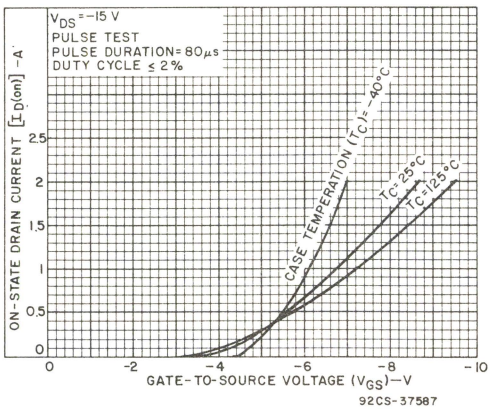


Fig. 5 - Typical transfer characteristics.

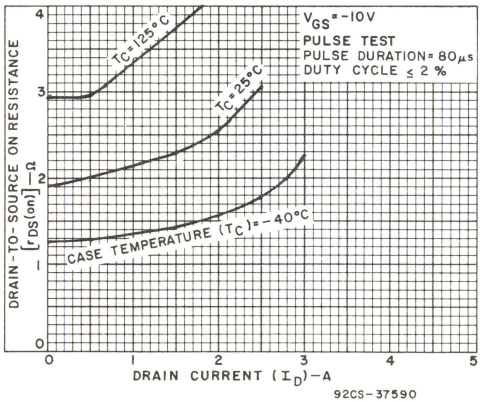


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

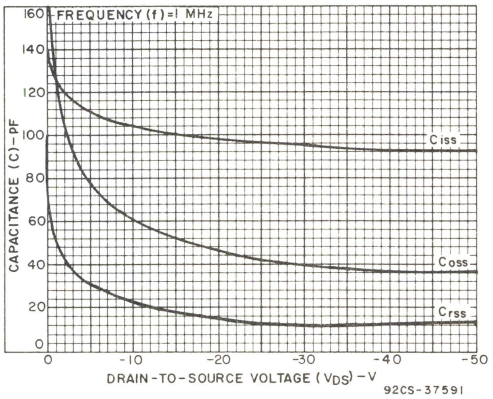


Fig. 7 - Capacitance as a function of drain-to-source voltage.

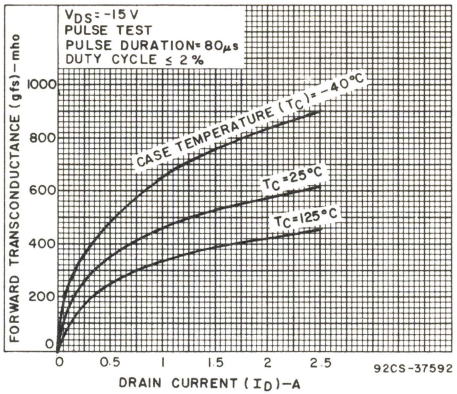


Fig. 8 - Typical forward transconductance as a function of drain current.

HARRIS

2N6896

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- -6A, -100V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

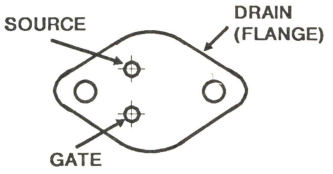
Description

The 2N6896 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The 2N6896 is supplied in the JEDEC TO-204AA metal package.

Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6896	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-6*	A
Pulsed Drain Current	I_{DM}	-20*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60*	W
Above T_C = +25°C, Derate Linearly		0.48*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)	T_L	260	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1874

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25° C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125° C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	2.28	V
			I_D = 6 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 3.8 A, V_{GS} = -10 V	—	0.6	Ω
			T_C = 125° C, I_D = 3.8 A, V_{GS} = 10 V	—	0.96	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 3.8 A	1	4	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	200	800	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	100	350	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	40	150	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	60	ns
*	Rise Time	t_r	I_D = 3.8 A	—	100	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	150	
*	Fall Time	t_f	V_{GS} = -10 V	—	100	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 50 A/μs	—	375	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

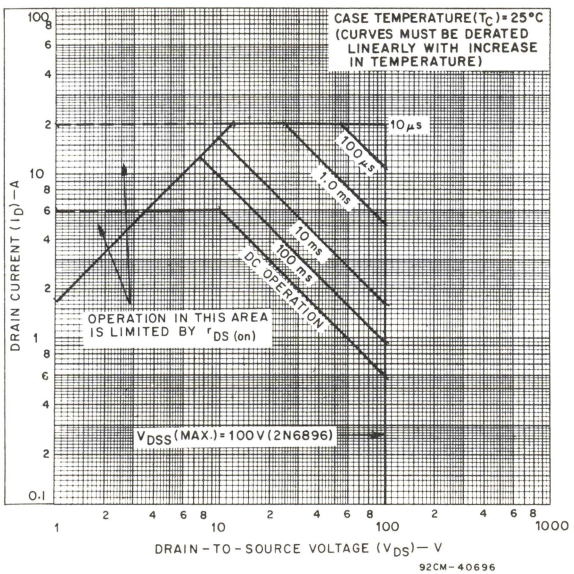


Fig. 1 - Maximum safe operating areas.

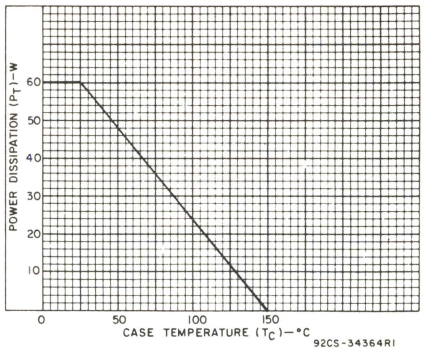


Fig. 2 - Power dissipation vs. temperature derating curve.

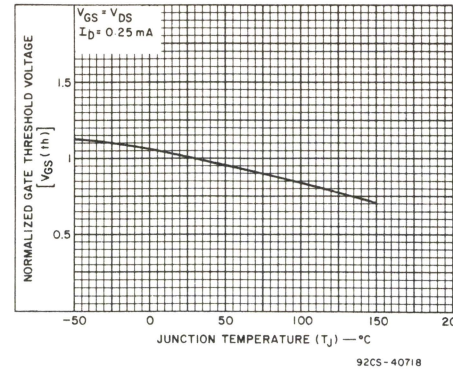


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

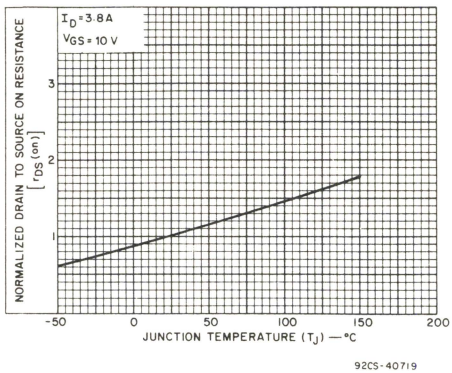


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

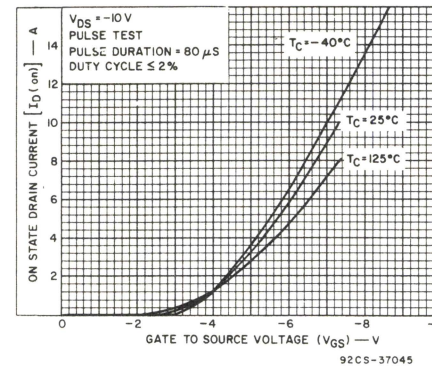


Fig. 5 - Typical transfer characteristics.

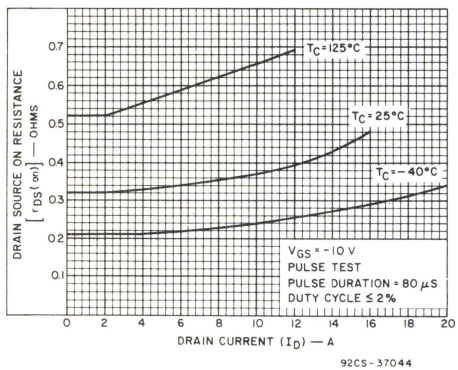


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

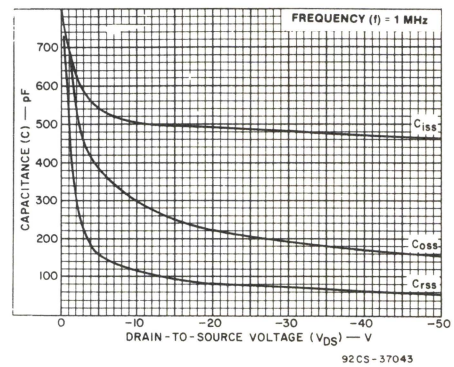


Fig. 7 - Capacitance as a function of drain-to-source voltage.

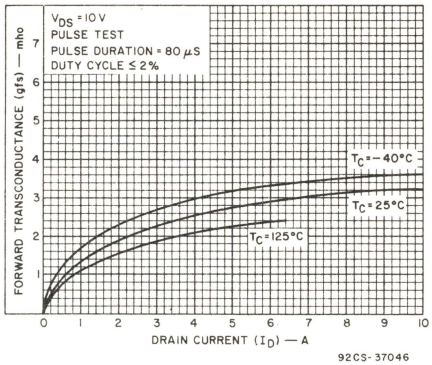


Fig. 8 - Typical forward transconductance as a function of drain current.

HARRIS

2N6897

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- -12A, -100V
- $r_{DS(on)} = 0.3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

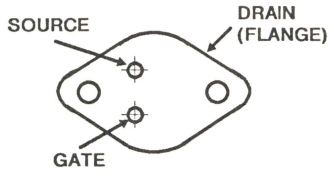
Description

The 2N6897 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6897 is supplied in the JEDEC TO-204AA metal package.

Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6897	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-12*	A
Pulsed Drain Current	I_{DM}	-30*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	100*	W
Above T_C = +25°C, Derate Linearly		0.8*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)	T_L	260*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1875

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = -10 V	—	2.28	V
			I_D = 12 A, V_{GS} = -10 V	—	-4.8	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = -10 V	—	0.3	Ω
			T_C = 125°C, I_D = 7.6 A, V_{GS} = 10 V	—	0.465	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 7.6 A	2	8	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	400	1500	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	200	700	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	60	240	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	60	ns
*	Rise Time	t_r	I_D = 7.6 A	—	175	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	275	
*	Fall Time	t_f	V_{GS} = -10 V	—	175	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	1.25	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 100 A/μs	—	500	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

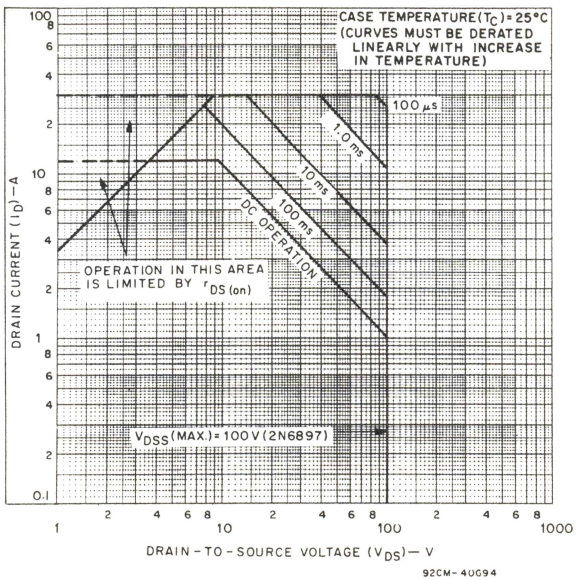


Fig. 1 - Maximum safe operating areas.

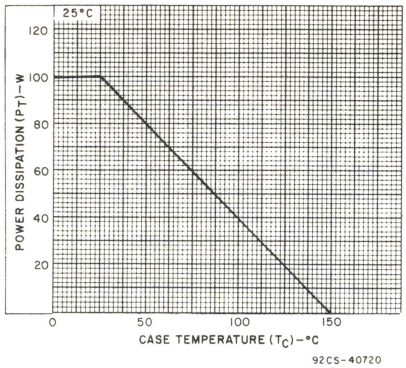


Fig. 2 - Power dissipation vs. temperature derating curve.

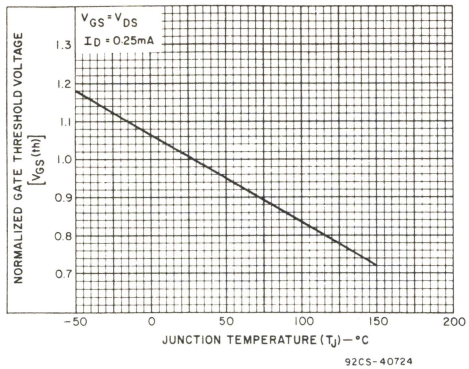


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

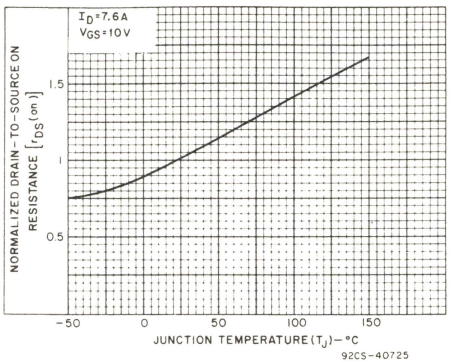


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

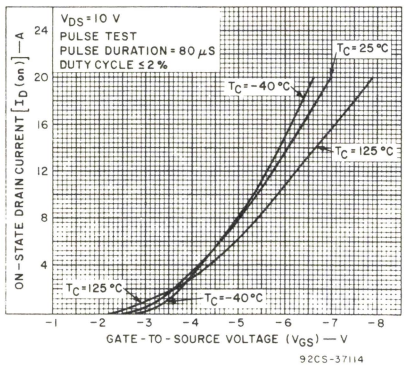


Fig. 5 - Typical transfer characteristics.

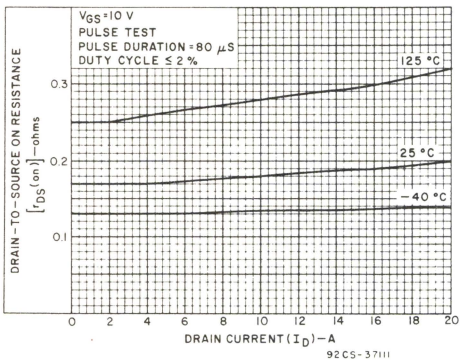


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

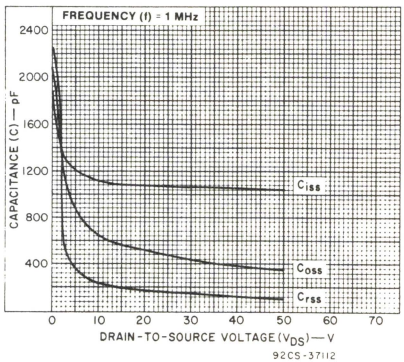


Fig. 7 - Capacitance as a function of drain-to-source voltage.

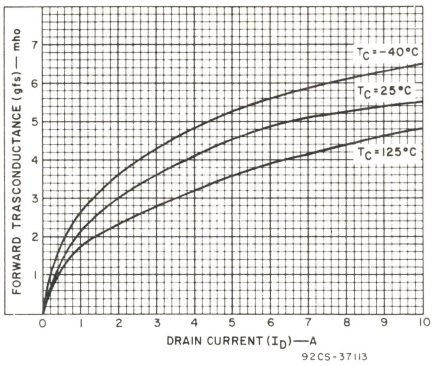


Fig. 8 - Typical forward transconductance as a function of drain current.

HARRIS

2N6898

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

August 1991

Features

- -25A, -100V
- $r_{DS(on)} = 0.20\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

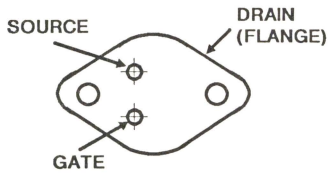
Description

The 2N6898 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6898 is supplied in the JEDEC TO-204AE steel package.

Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6898	UNITS
Drain-Source Voltage	V_{DSS}	-100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	-100*	V
Continuous Drain Current			
RMS Continuous	I_D	-25*	A
Pulsed Drain Current	I_{DM}	-60*	A
Gate-Source Voltage	V_{GS}	±20*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	150*	W
Above T_C = +25°C, Derate Linearly		1.2*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering (At distances ≥ ⅛" (3.17mm) from seating plane for 10s max)	T_L	260*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1876

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	3.16	V
			I_D = 25 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	0.2	Ω
			T_C = 125°C, I_D = 15.8 A, V_{GS} = 10 V	—	0.24	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 15.8 A	4	16	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	—	3000	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	500	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	50	ns
*	Rise Time	t_r	I_D = 12.5 A	—	250	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	—	400	
*	Fall Time	t_f	V_{GS} = -10 V	—	250	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 25 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 100 A/μs	—	750	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

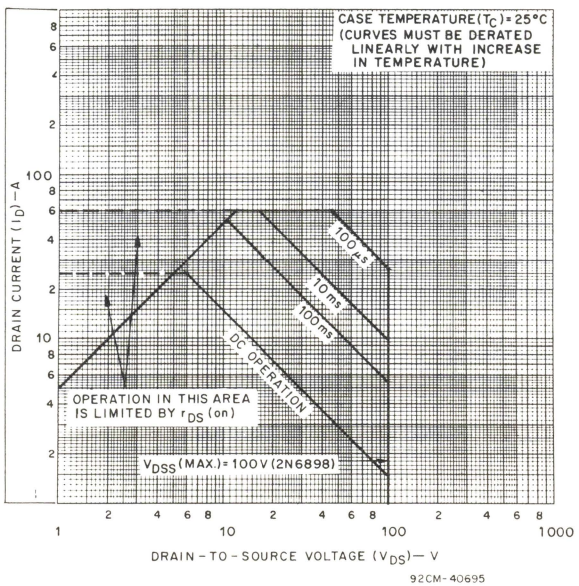


Fig. 1 - Maximum safe operating areas.

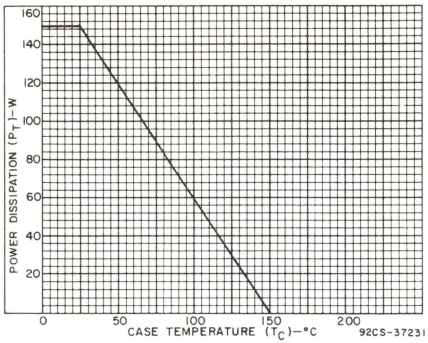


Fig. 2 - Power dissipation vs. temperature derating curve.

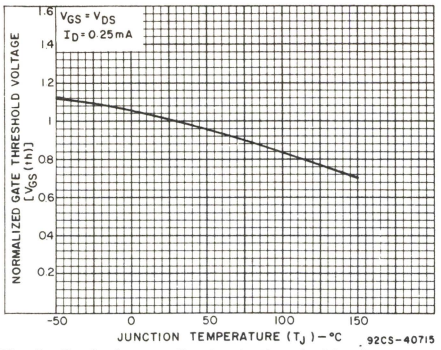


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

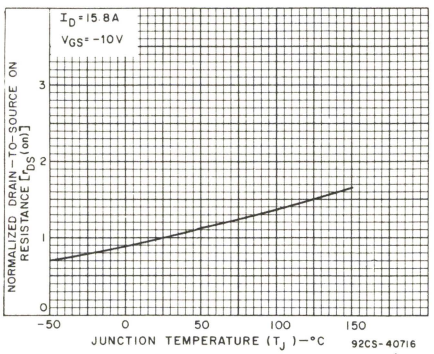


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

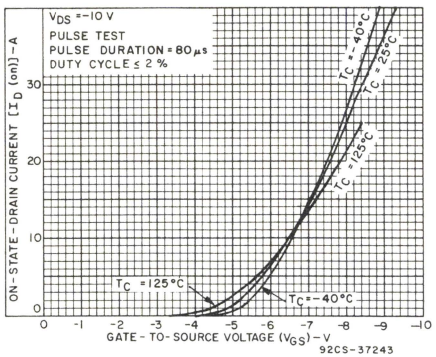


Fig. 5 - Typical transfer characteristics.

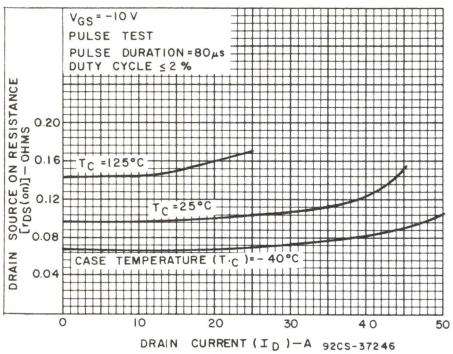


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

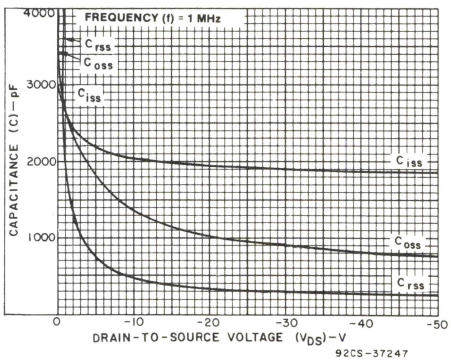


Fig. 7 - Capacitance as a function of drain-to-source voltage.

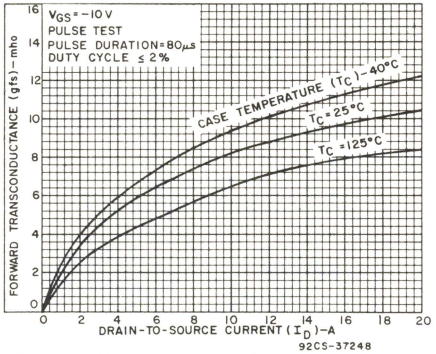


Fig. 8 - Typical forward transconductance as a function of drain current.

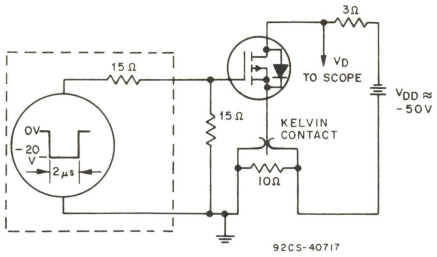


Fig. 9 - Switching time test circuit.

HARRIS

IRF9130, IRF9131 IRF9132, IRF9133

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -10A and -12A, -80V and -100V
- $r_{DS(ON)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

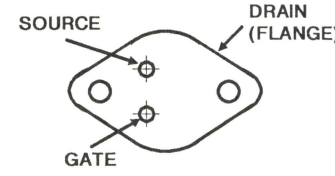
Description

The IRF9130, IRF9131, IRF9132 and IRF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

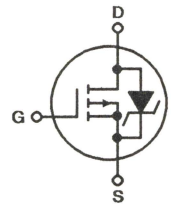
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9130	IRF9131	IRF9132	IRF9133	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-12	-12	-10	-10	A
T_C = 100°C ..... I_D	-7.5	-7.5	-6.5	-6.5	A
Pulsed Drain Current (3) ..... I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	75	75	75	75	W
Linear Derating Factor ..... (See Figure 14)	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mH, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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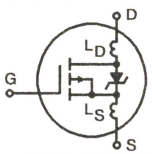
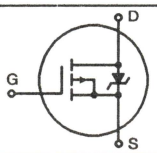
File Number **2220.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9130, IRF9132	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9131, IRF9133			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9130, IRF9131	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-12	-	-	A
IRF9132, IRF9133			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9130, IRF9131	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6.5A	-	0.25	0.30	Ω
IRF9132, IRF9133			-	0.30	0.40	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -6.5A	2	3.7	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, Z_O = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -15A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -12A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 12A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -12A, dI_F/dt = 100A/μs	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mH, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

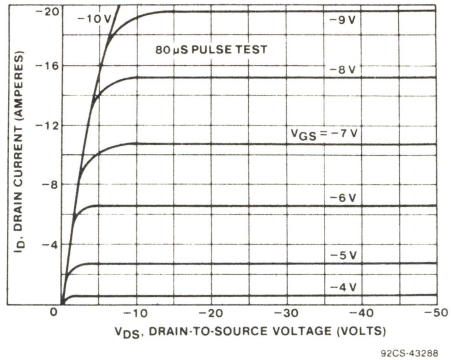


Fig. 1 - Typical Output Characteristics

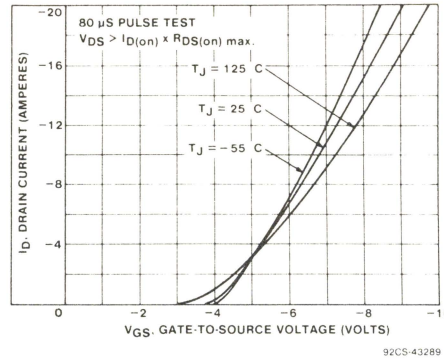


Fig. 2 - Typical Transfer Characteristics

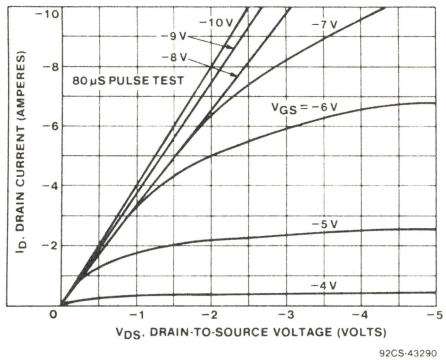


Fig. 3 - Typical Saturation Characteristics

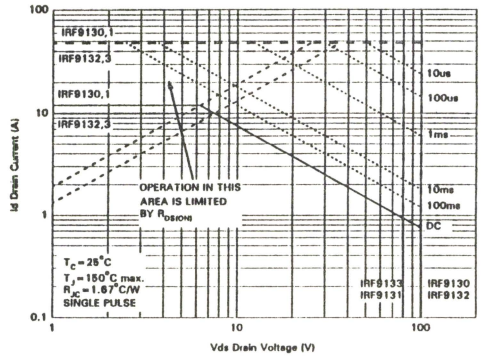


Fig. 4 - Maximum Safe Operating Area

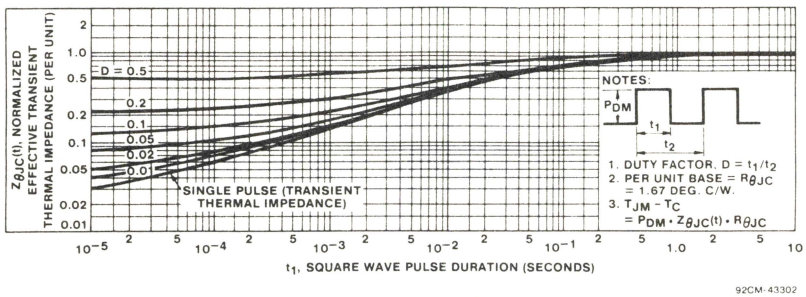


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

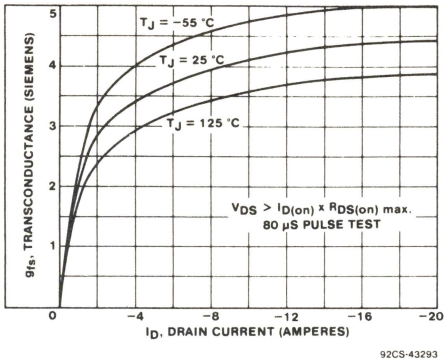


Fig. 6 - Typical Transconductance Vs. Drain Current

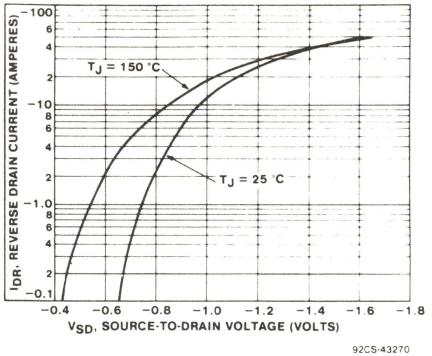


Fig. 7 - Typical Source-Drain Diode Forward Voltage

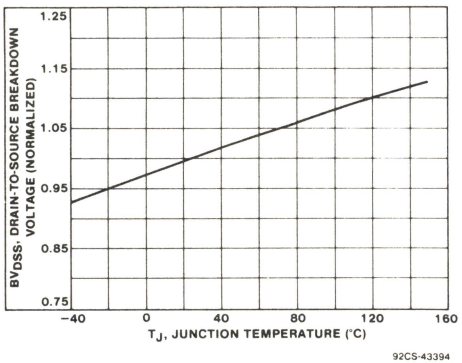


Fig. 8 - Breakdown Voltage Vs. Temperature

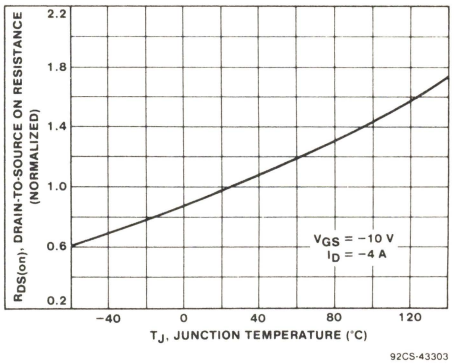


Fig. 9 - Normalized On-Resistance Vs. Temperature

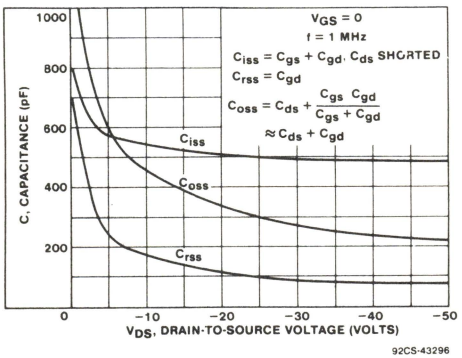


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

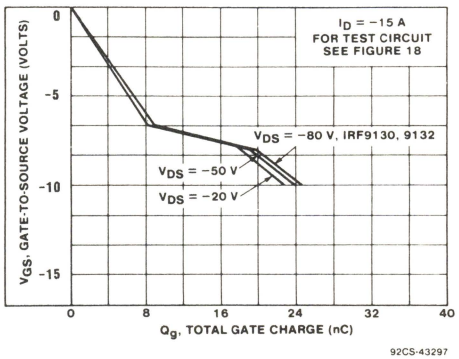


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

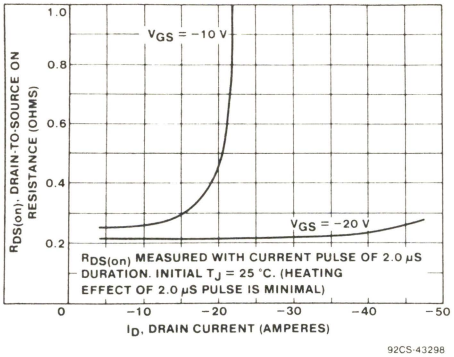


Fig. 12 - Typical On-Resistance Vs. Drain Current

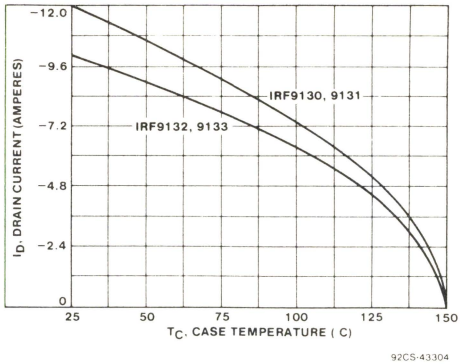


Fig. 13 - Maximum Drain Current Vs. Case Temperature

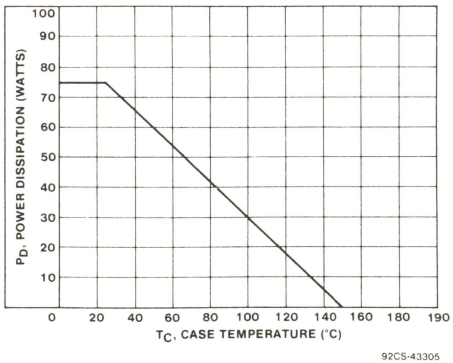


Fig. 14 - Power Vs. Temperature Derating Curve

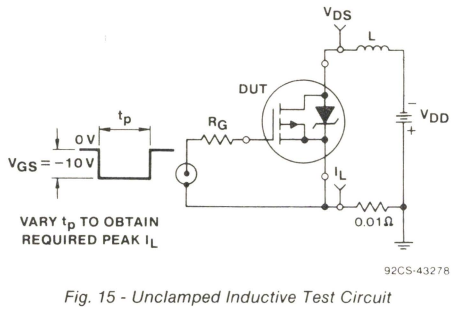


Fig. 15 - Unclamped Inductive Test Circuit

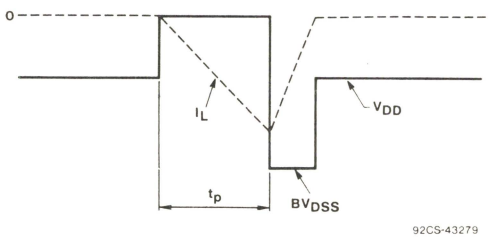


Fig. 16 - Unclamped Inductive Waveforms

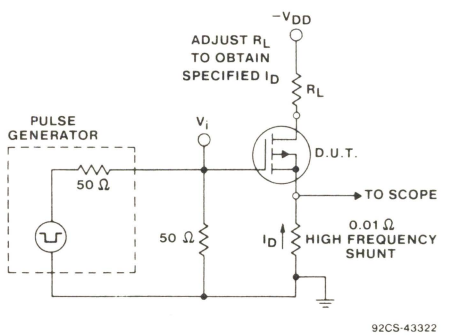


Fig. 17 - Switching Time Test Circuit

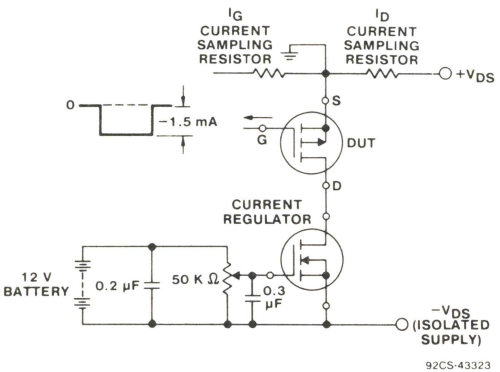


Fig. 18 - Gate Charge Test Circuit

HARRIS

IRF9140, IRF9141 IRF9142, IRF9143

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -19A and -15A, -80V and -100V
- $r_{DS(ON)}$ = 0.20Ω and 0.30Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

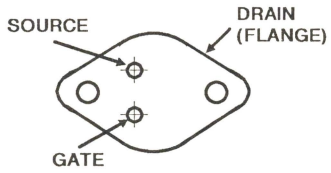
Description

The IRF9140, IRF9141, IRF9142 and IRF9143 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

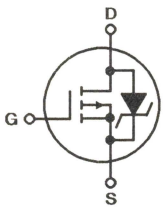
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9140	IRF9141	IRF9142	IRF9143	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-19	-19	-15	-15	A
T_C = 100°C ..... I_D	-12	-12	-10	-10	A
Pulsed Drain Current (3) ..... I_{DM}	-76	-76	-60	-60	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	125	125	125	125	W
Linear Derating Factor ..... (See Figure 14)	1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	960	960	960	960	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2278.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9140, IRF9142	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9141, IRF9143			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9140, IRF9141	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-19	-	-	A
IRF9142, IRF9143			-15	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9140, IRF9141	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.15	0.20	Ω
IRF9142, IRF9143			-	0.22	0.30	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -10A	5	7	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1100	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	250	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -19A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	20	ns
Rise Time	t_r		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	t_f		-	28	90	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -19A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	90	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	56	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-19	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-76	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -19A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 19A, dI_F/dt = 100A/μs	-	170	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -19A, dI_F/dt = 100A/μs	-	0.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

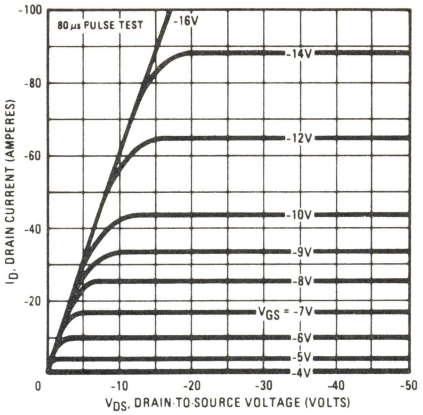


Fig. 1 - Typical output characteristics.

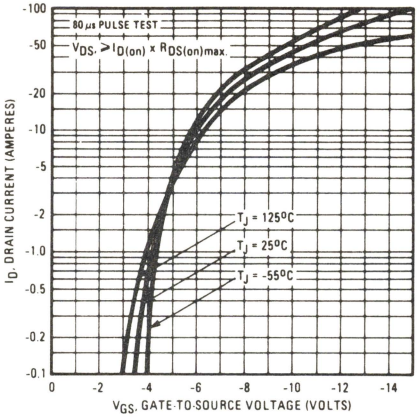


Fig. 2 - Typical transfer characteristics.

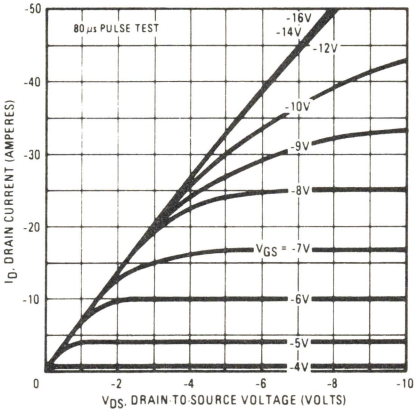


Fig. 3 - Typical saturation characteristics.

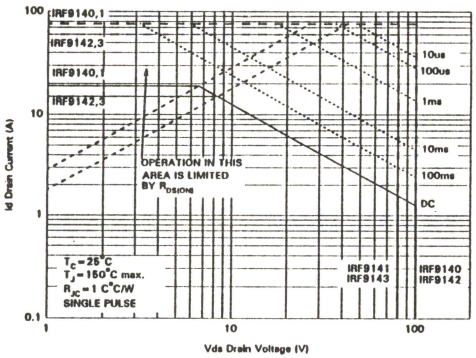


Fig. 4 - Maximum safe operating area.

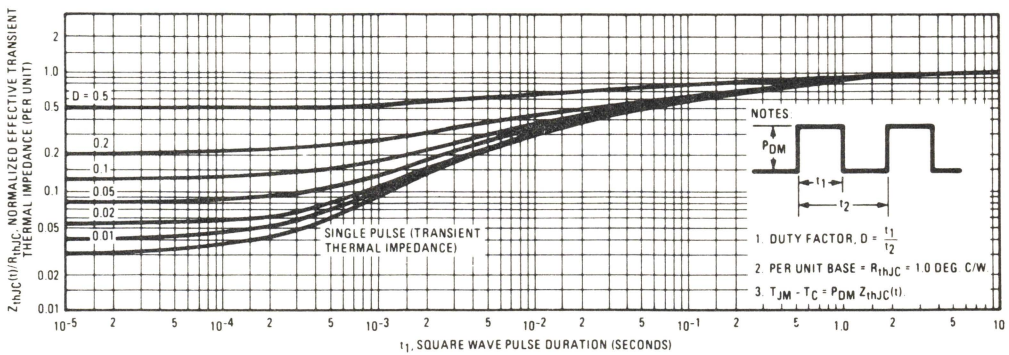


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

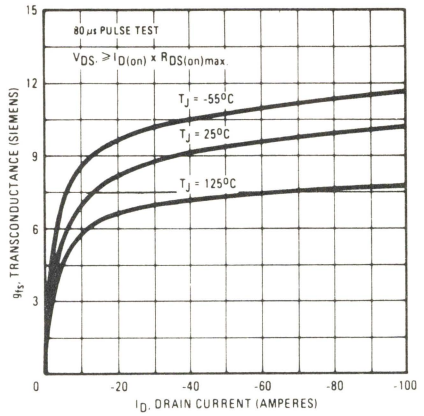


Fig. 6 - Typical transconductance vs. drain current.

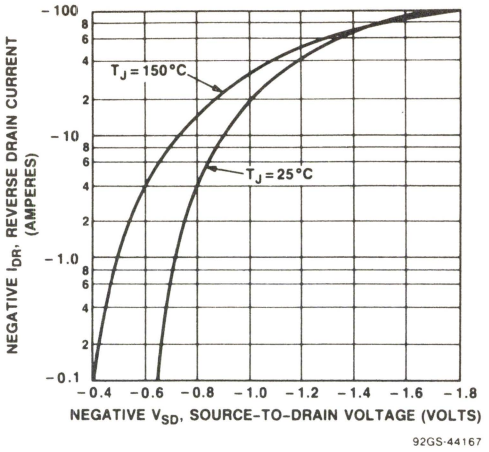


Fig. 7 - Typical source-drain diode forward voltage.

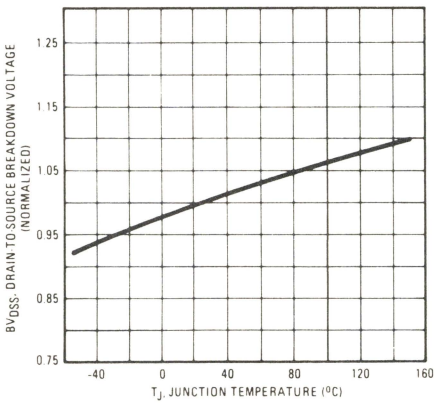


Fig. 8 - Breakdown voltage vs. temperature.

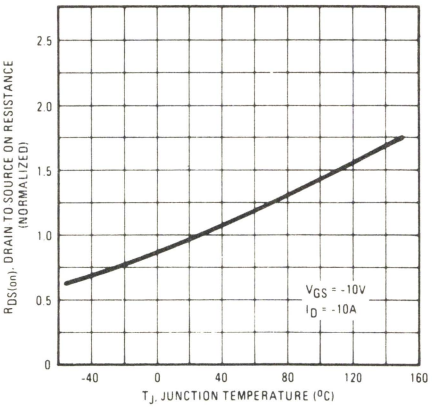


Fig. 9 - Normalized on-resistance vs. temperature.

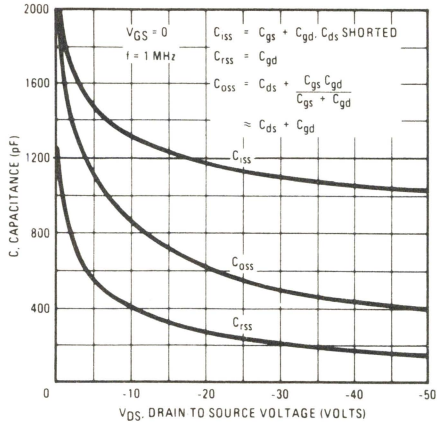


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

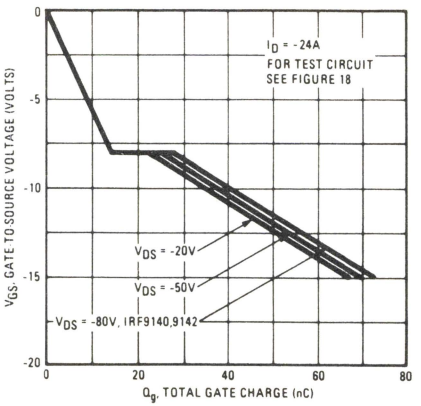


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

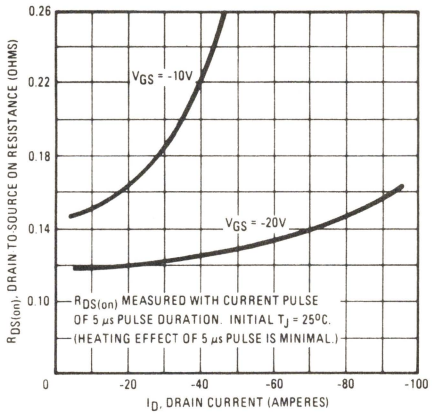


Fig. 12 - Typical on-resistance vs. drain current.

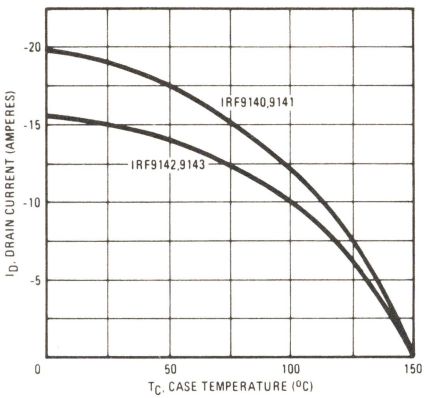


Fig. 13 - Maximum drain current vs. case temperature.

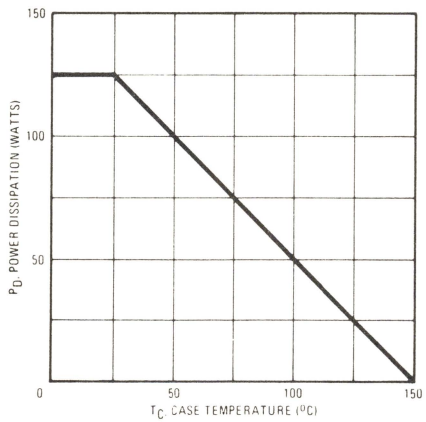


Fig. 14 - Power vs. temperature derating curve.

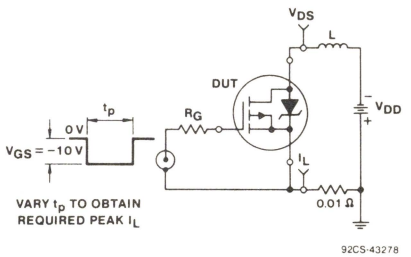


Fig. 15 - Unclamped inductive test circuit.

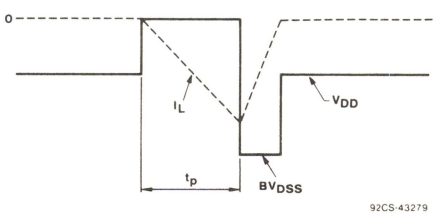


Fig. 16 - Unclamped inductive waveforms.

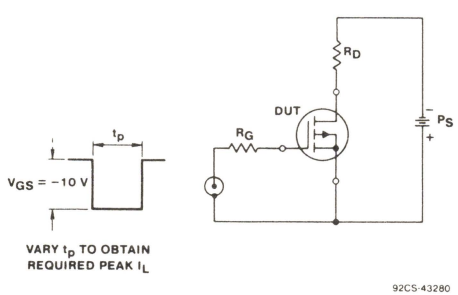


Fig. 17 - Switching time test circuit.

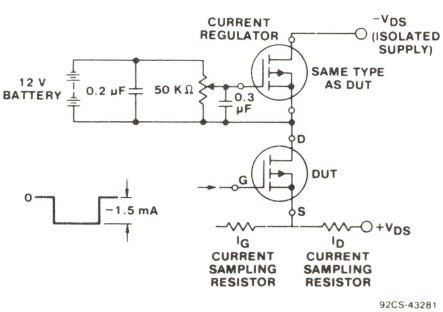


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9150
IRF9151

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -25A, -80V and -100V
- $r_{DS(ON)}$ = 0.150Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

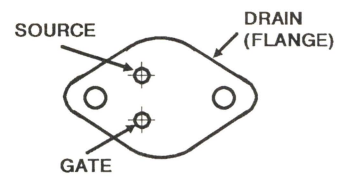
The IRF9150 and IRF9151 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRF9150 is an approximate electrical complement to the N-channel IRF150.

The IRF types are supplied in the JEDEC TO-204AE metal package.

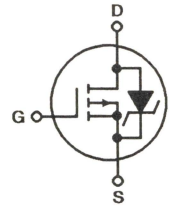
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRF9150	IRF9151	UNITS
Drain-Source Voltage	V_{DS}	-100	-80	V
Continuous Drain Current				
T_C = 25°C	I_D	-25	-25	A
T_C = 100°C	I_D	-18	-18	A
Pulsed Drain Current	I_{DM}	-100	-100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 18)	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	1300	1300	mJ
Avalanche Current (Repetitive or Nonrepetitive)	I_{AR}	-25	-25	A
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 19A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2280.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9150	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9151			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	-25	-	-	A
Static Drain-Source On-State Resistance (Note 1)	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.09	0.15	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = -10V, I_D = -12.5A	4	10	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	2400	-	pF
Output Capacitance	C_{OSS}		-	850	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	400	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -50V, I_D = -25A, R_G = 6.8Ω, R_D = 2Ω. See Figures 16 and 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	24	ns
Rise Time	t_r		-	110	160	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	65	100	ns
Fall Time	t_f		-	46	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -25A, V_{DS} = 0.8 Max Rating. See Figures 11 & 19 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	82	120	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	42	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-100	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = 25A, V_{GS} = 0V	-	0.9	1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	-	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	0.3	0.7	1.5	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 25A (See Figures 14 and 15)

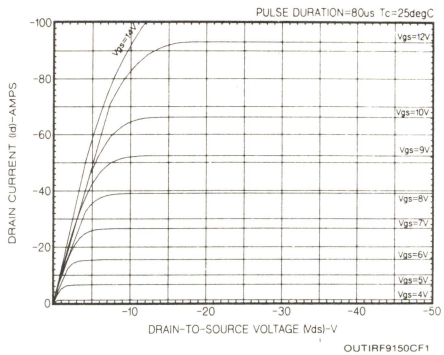


Fig. 1 - Typical output characteristics.

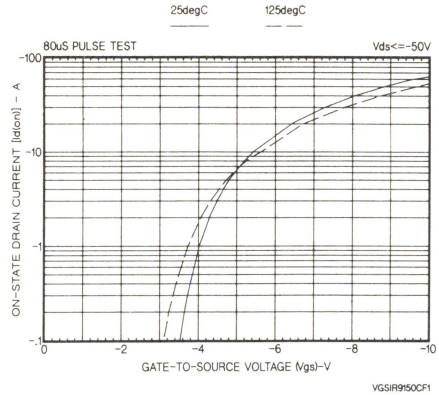


Fig. 2 - Typical transfer characteristics.

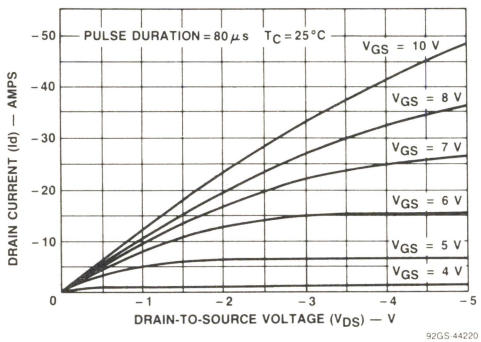


Fig. 3- Typical saturation characteristics.

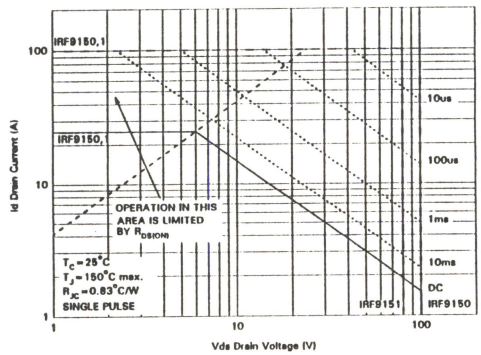


Fig. 4 - Maximum safe operating area.

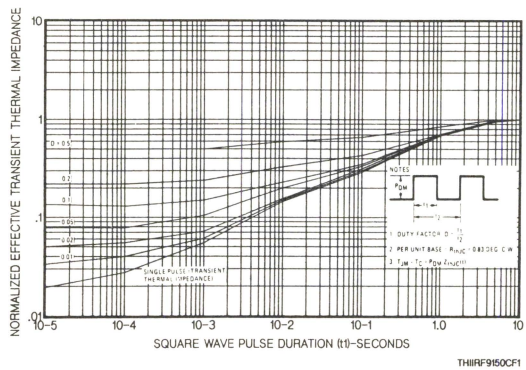


Fig. 5 - Maximum effective transient thermal impedance.

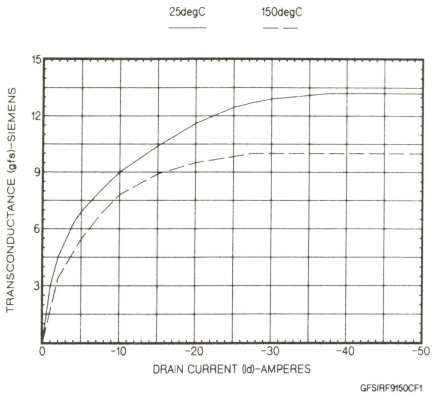


Fig. 6 - Typical transconductance vs. drain current.

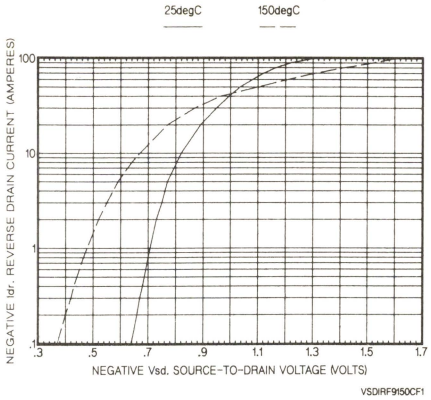


Fig. 7 - Typical source-drain diode forward voltage.

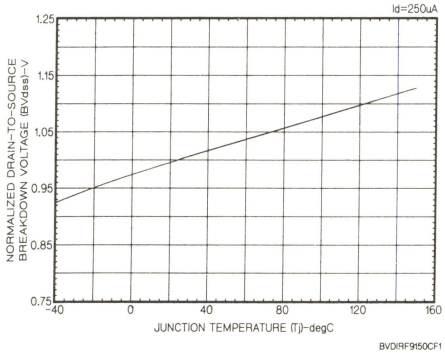


Fig. 8 - Normalized breakdown voltage vs. temperature.

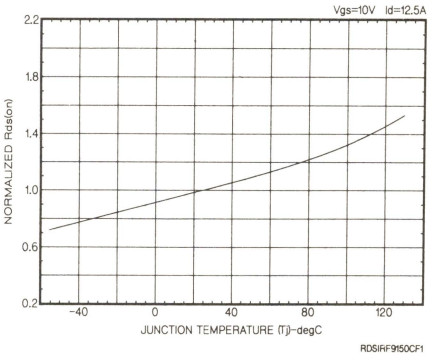


Fig. 9 - Normalized on-resistance vs. temperature.

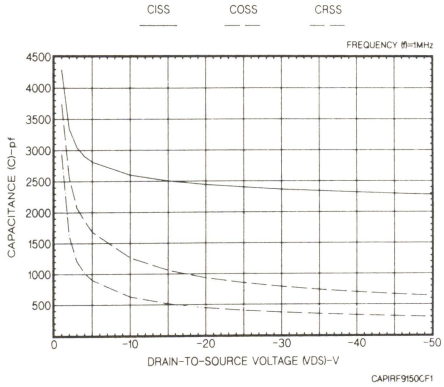


Fig. 10 - Typical capacitance vs. drain-to source voltage.

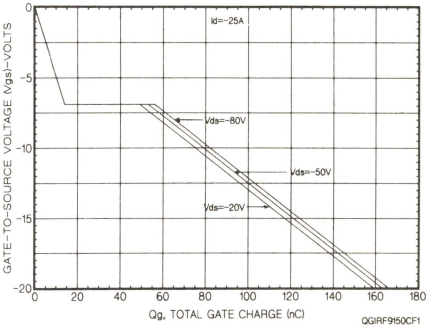


Fig. 11 - Typical gate charge vs. gate-to source voltage.

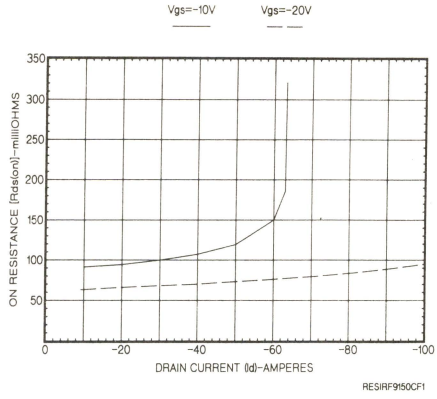


Fig. 12 - Typical on-resistance vs. drain current.

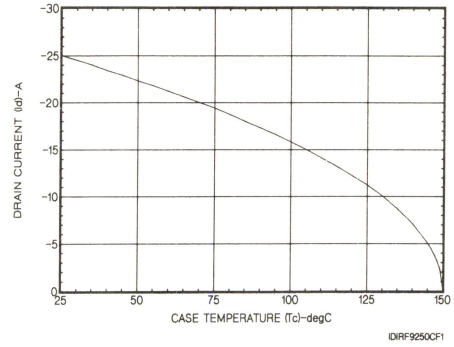


Fig. 13 - Maximum drain current vs. case temperature.

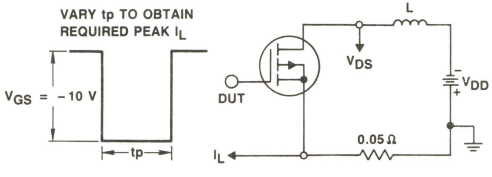


Fig. 14 - Unclamped inductive test circuit.

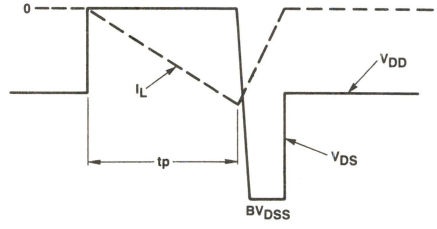


Fig. 15 - Unclamped inductive waveforms.

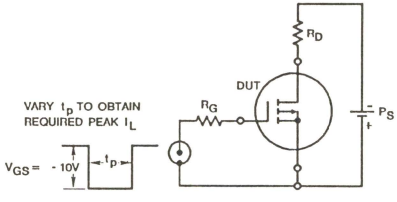


Fig. 16 - Switching time test circuit.

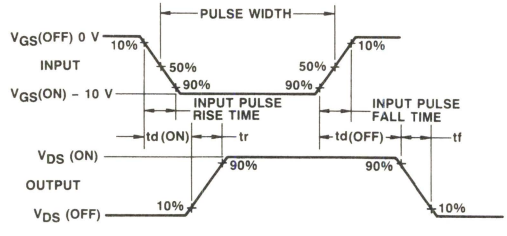


Fig. 17 - Switching time waveforms.

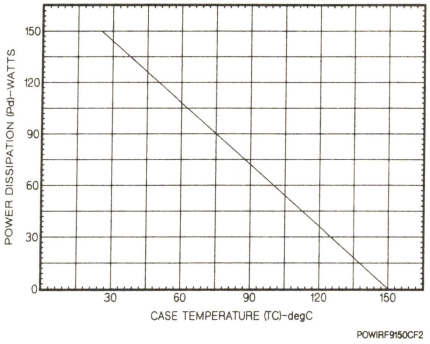


Fig. 18 - Power vs. temperature derating curve.

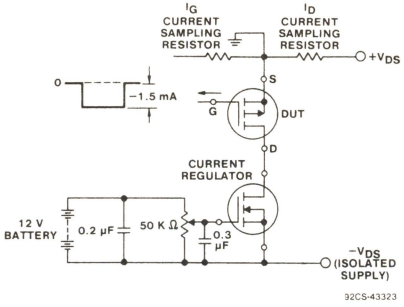


Fig. 19 - Gate charge test circuit.

HARRIS

IRF9230, IRF9231 IRF9232, IRF9233

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -5.5A and -6.5A, -150V and -200V
- $r_{DS(ON)}$ = 0.80Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

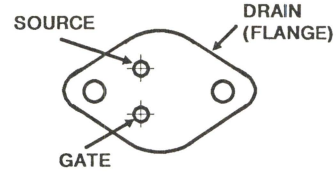
Description

The IRF9230, IRF9231, IRF9232 and IRF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

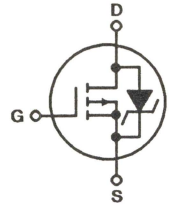
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRF9230	IRF9231	IRF9232	IRF9233	UNITS
Drain-Source Voltage (1)	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current						
T_C = 25°C	I_D	-6.5	-6.5	-5.5	-5.5	A
T_C = 100°C	I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3)	I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	75	75	75	75	W
Linear Derating Factor (See Figure 14)		0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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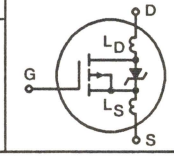
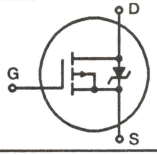
File Number **2226**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9230, IRF9232	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9231, IRF9233			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9230, IRF9231	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6.5	-	-	A
IRF9232, IRF9233			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9230, IRF9231	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3.5A	-	0.5	0.8	Ω
IRF9232, IRF9233			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -3.5A	2.2	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	550	-	pF
Output Capacitance	C_{OSS}		-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	13	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	400	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	2.6	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

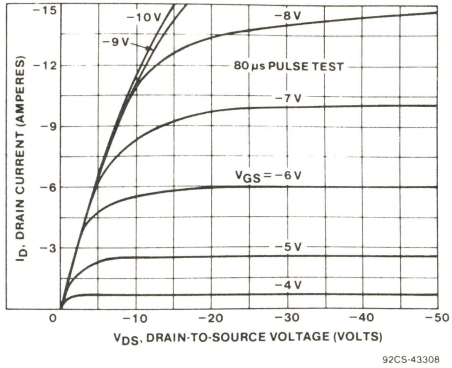


Fig. 1 - Typical output characteristics.

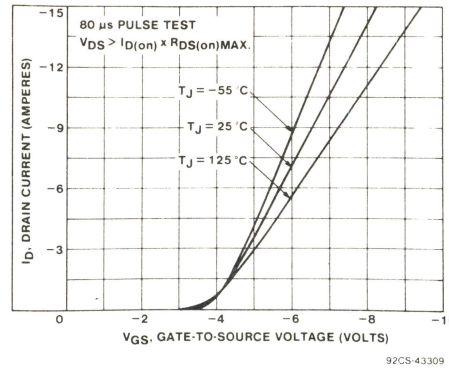


Fig. 2 - Typical transfer characteristics.

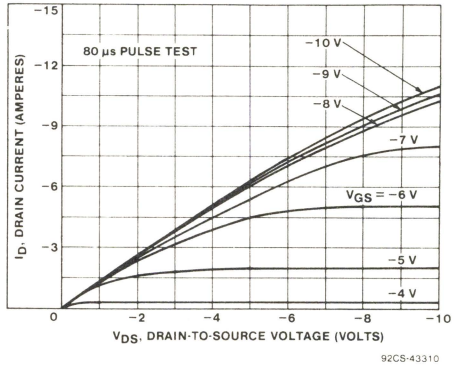


Fig. 3 - Typical saturation characteristics.

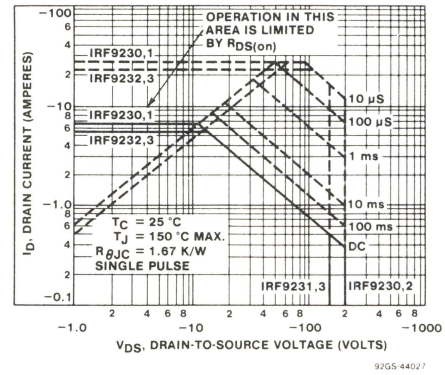


Fig. 4 - Maximum safe operating area.

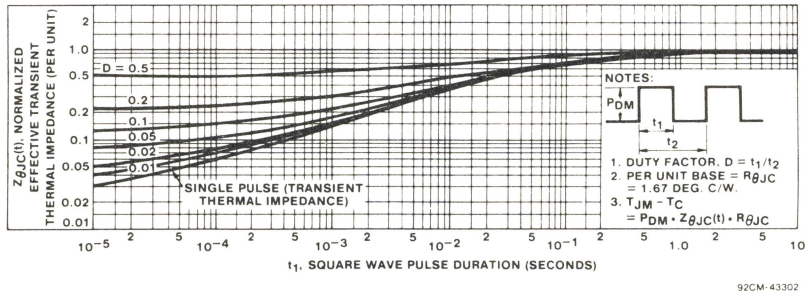


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

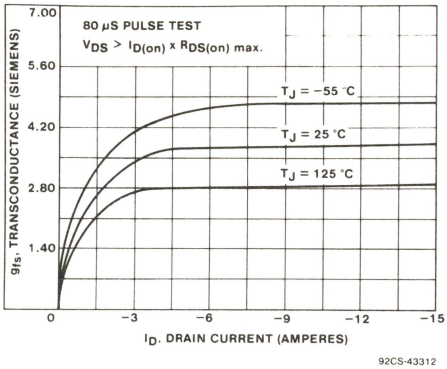


Fig. 6 - Typical transconductance vs. drain current.

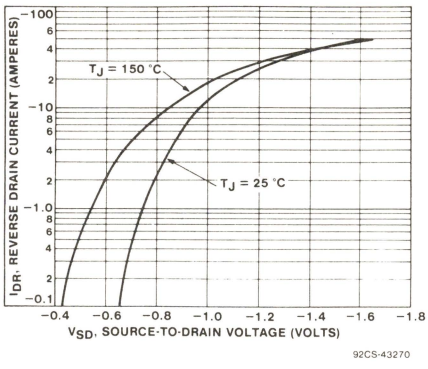


Fig. 7 - Typical source-drain diode forward voltage.

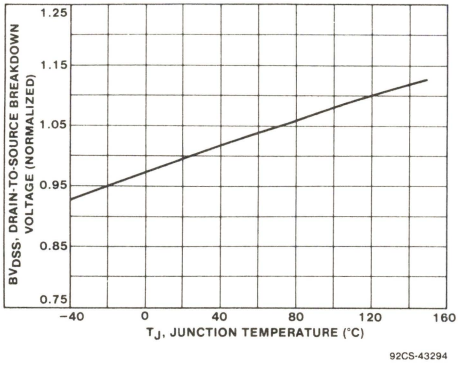


Fig. 8 - Breakdown voltage vs. temperature.

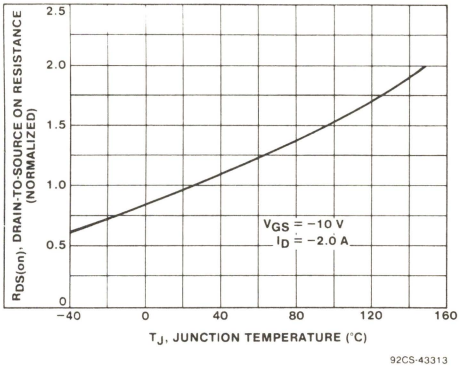


Fig. 9 - Normalized on-resistance vs. temperature.

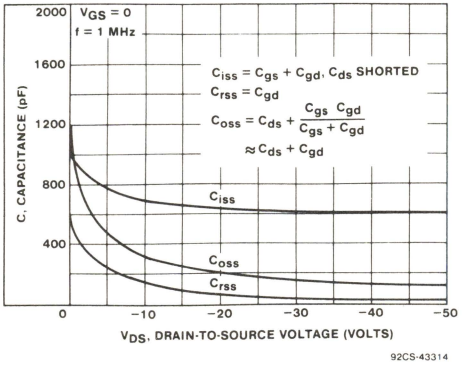


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

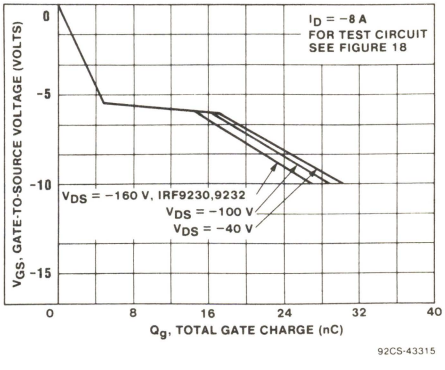


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

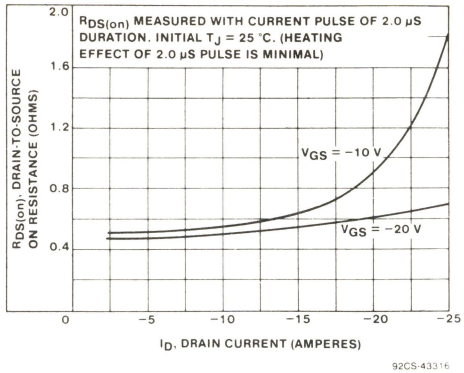


Fig. 12 - Typical on-resistance vs. drain current.

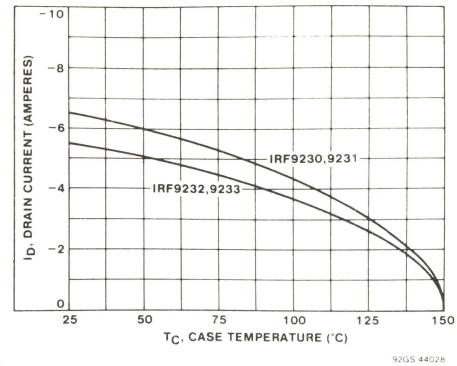


Fig. 13 - Maximum drain current vs. case temperature.

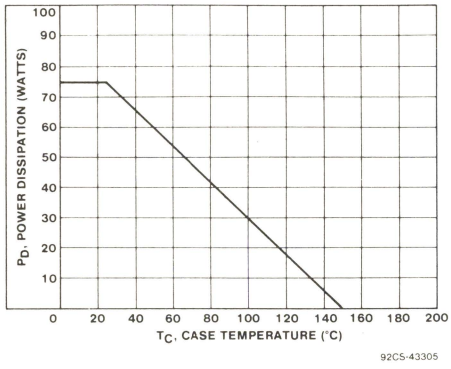


Fig. 14 - Power vs. temperature derating curve.

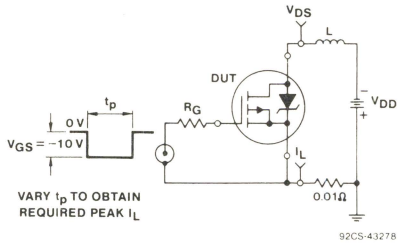


Fig. 15 - Unclamped inductive test circuit.

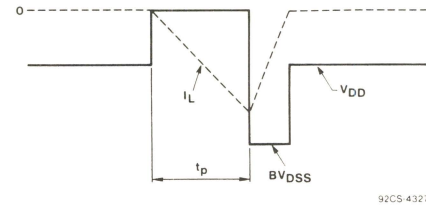


Fig. 16 - Unclamped inductive waveforms.

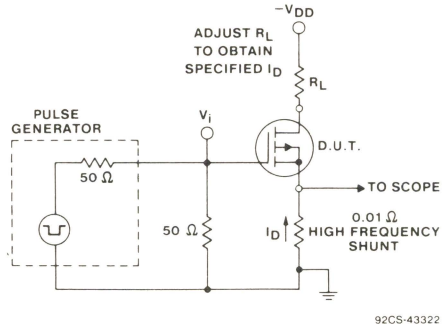


Fig. 17 - Switching time test circuit.

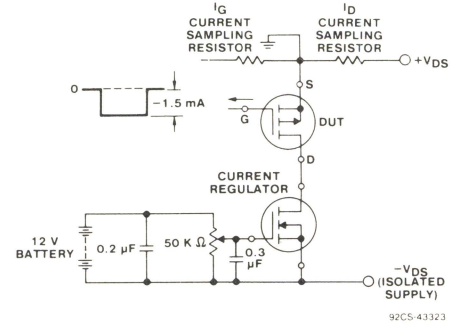


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9240, IRF9241 IRF9242, IRF9243

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -9A and -11A, -150V and -200V
- $r_{DS(ON)}$ = 0.50Ω and 0.7Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

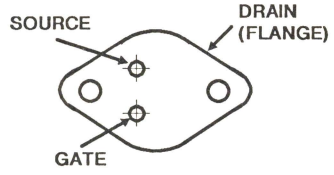
Description

The IRF9240, IRF9241, IRF9242 and IRF9243 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-204AA steel package.

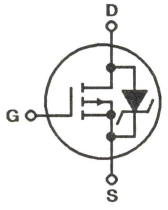
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRF9240	IRF9241	IRF9242	IRF9243	UNITS
Drain-Source Voltage (1)	V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current						
T_C = 25°C	I_D	-11	-11	-9	-9	A
T_C = 100°C	I_D	-7	-7	-6	-6	A
Pulsed Drain Current (3)	I_{DM}	-44	-44	-36	-36	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	125	125	125	125	W
Linear Derating Factor (See Figure 14)		1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	790	790	790	790	mJ
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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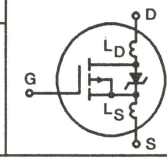
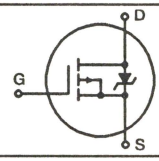
File Number 2279

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9240, IRF9242	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9241, IRF9243			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9240, IRF9241	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = -10V	-11	-	-	A
IRF9242, IRF9243			-9	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9240, IRF9241	$r_{DS(ON)}$	V_{GS} = 10V, I_D = -6A	-	0.35	0.5	Ω
IRF9242, IRF9243			-	0.55	0.7	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, I_D = -6A	4	6	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1100	-	pF
Output Capacitance	C_{OSS}		-	375	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	150	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =100 BV_{DSS}, I_D = -11A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	18	22	ns
Rise Time	t_r		-	45	68	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	90	ns
Fall Time	t_f		-	29	44	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -11A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	90	nC
Gate-Source Charge	Q_{gs}		-	55	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	15	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-11	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-44	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -11A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	270	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	2	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

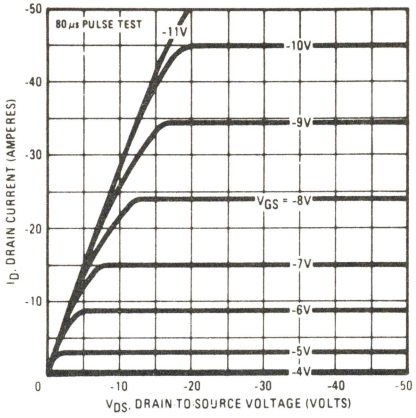


Fig. 1 - Typical output characteristics.

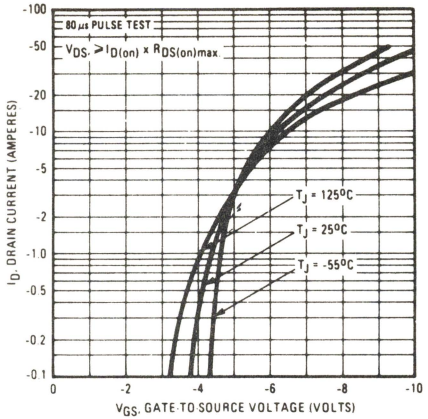


Fig. 2 - Typical transfer characteristics.

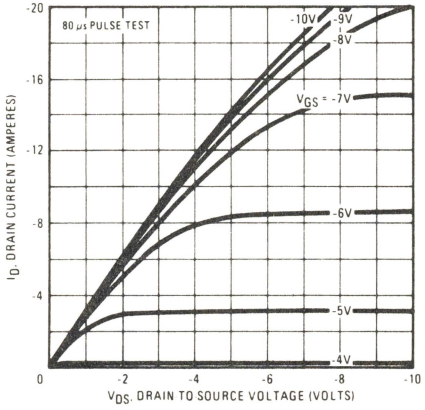


Fig. 3 - Typical saturation characteristics.

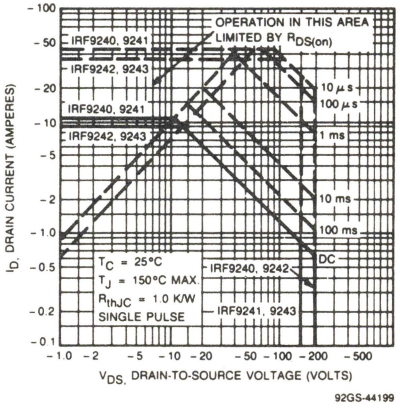


Fig. 4 - Maximum safe operating area.

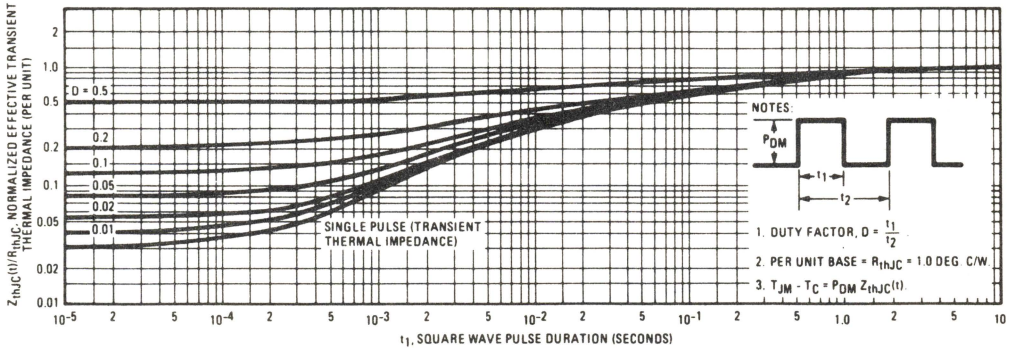


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

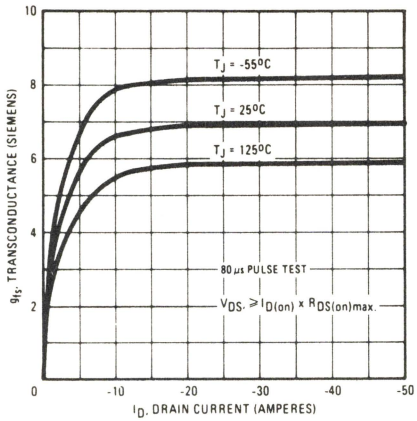


Fig. 6 - Typical transconductance vs. drain current.

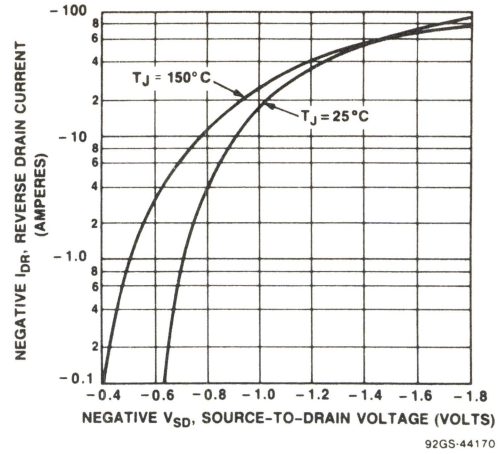


Fig. 7 - Typical source-drain diode forward voltage.

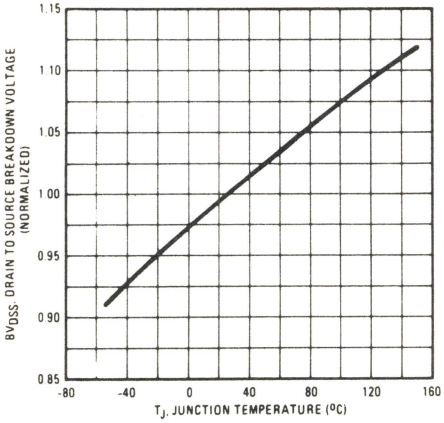


Fig. 8 - Breakdown voltage vs. temperature.

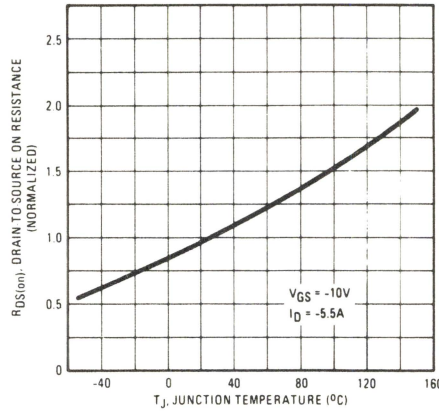


Fig. 9 - Normalized on-resistance vs. temperature.

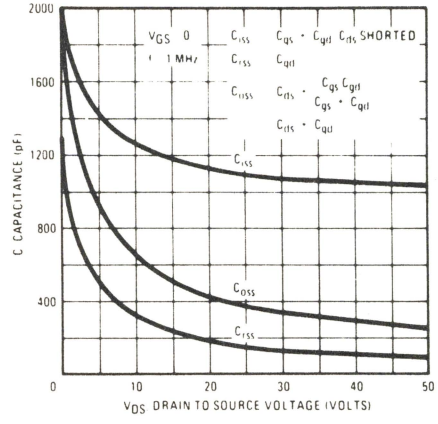


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

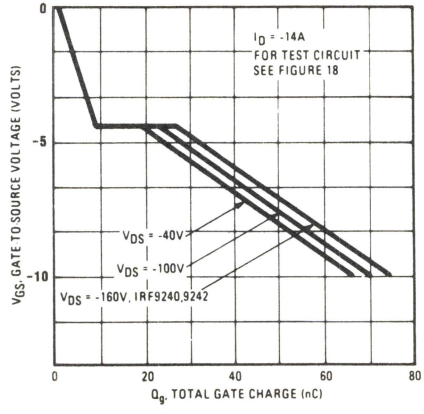


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

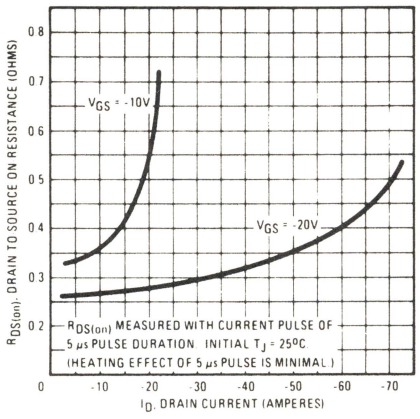


Fig. 12 - Typical on-resistance vs. drain current.

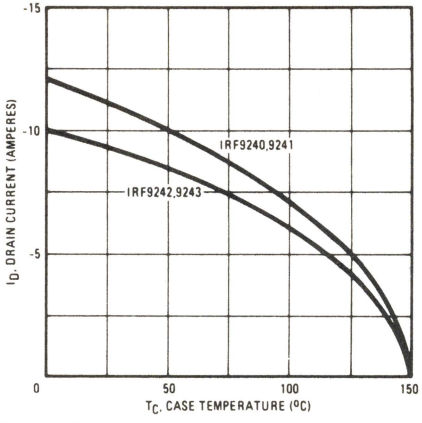


Fig. 13 - Maximum drain current vs. case temperature.

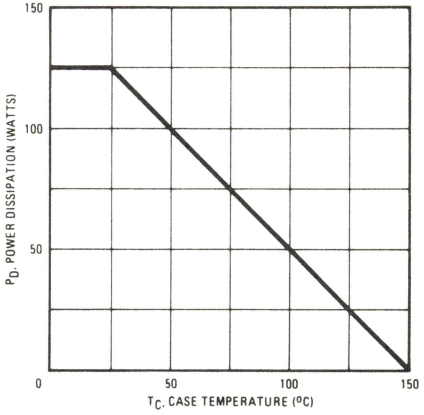


Fig. 14 - Power vs. temperature derating curve.

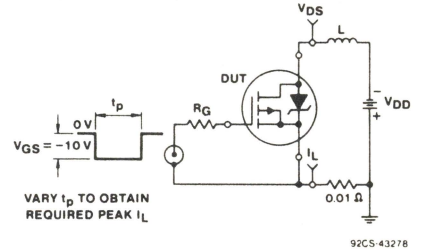


Fig. 15 - Unclamped inductive test circuit.

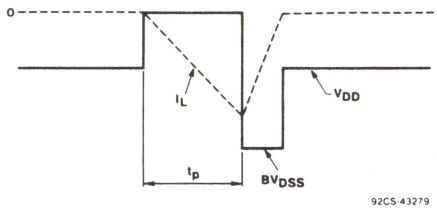


Fig. 16 - Unclamped inductive waveforms.

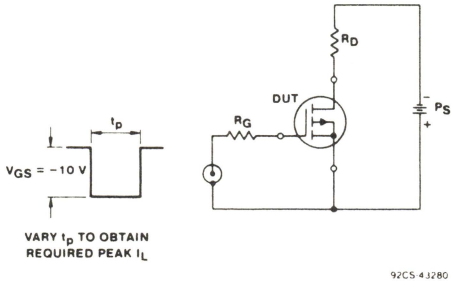


Fig. 17 - Switching time test circuit.

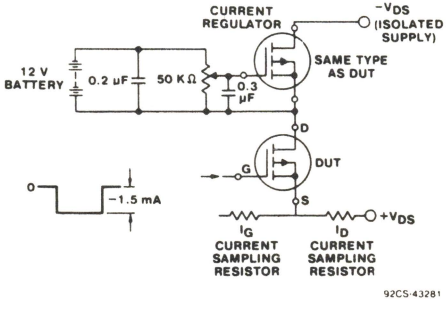


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9510, IRF9511 IRF9512, IRF9513

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -2.5A and -3.0A, -80V and -100V
- $r_{DS(ON)}$ = 1.2Ω and 1.6Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

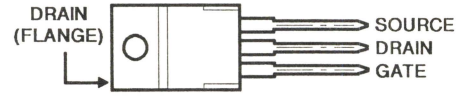
Description

The IRF9510, IRF9511, IRF9512 and IRF9513 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

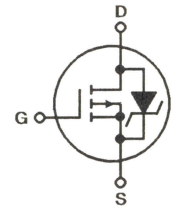
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9510	IRF9511	IRF9512	IRF9513	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-3.0	-3.0	-2.5	-2.5	A
T_C = 100°C ..... I_D	-2.0	-2.0	-1.5	-1.5	A
Pulsed Drain Current (3) ..... I_{DM}	-12	-12	-10	-10	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	20	20	20	20	W
Linear Derating Factor ..... (See Figure 14)	0.16	0.16	0.16	0.16	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	190	190	190	190	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 31.7mHμ, R_G = 25Ω, Peak I_L = 3.0A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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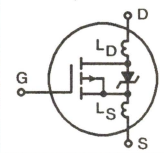
File Number **2214.1**

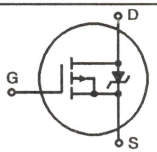
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9510, IRF9512	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9511, IRF9513			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9510, IRF9511	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-3.0	-	-	A
IRF9512, IRF9513			-2.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9510, IRF9511	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -1.5A	-	1.0	1.2	Ω
IRF9512, IRF9513			-	1.2	1.6	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -1.5A	0.8	1.1	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	180	-	pF
Output Capacitance	C_{OSS}		-	85	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -3.0A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	15	30	ns
Rise Time	t_r		-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	40	ns
Fall Time	t_f		-	20	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -3A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	8.5	11	nC
Gate-Source Charge	Q_{gs}		-	3.8	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4.7	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.4	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-3.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-12	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -3.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -3.0A, dI_F/dt = 100A/μs	-	120	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -3.0A, dI_F/dt = 100A/μs	-	6.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 31.7mH, R_G = 25Ω, Peak I_L = 3.0A (See Figures 15 and 16)

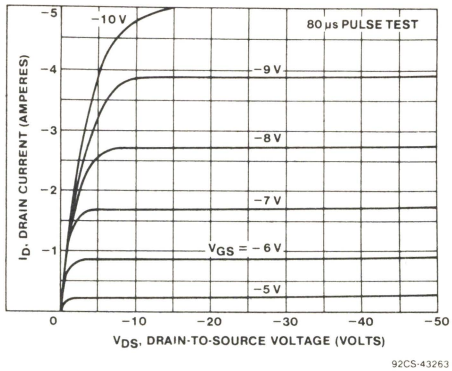


Fig. 1 - Typical Output Characteristics

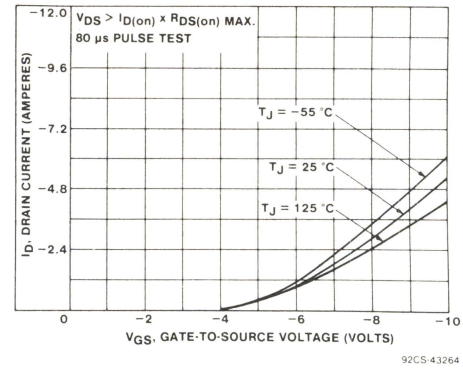


Fig. 2 - Typical Transfer Characteristics

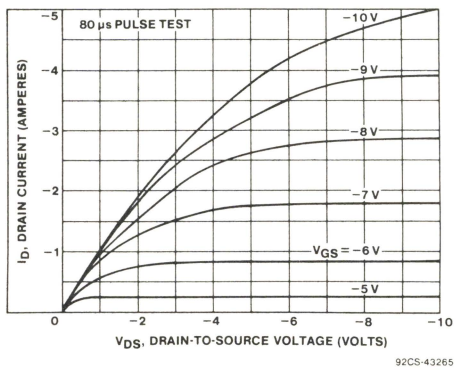
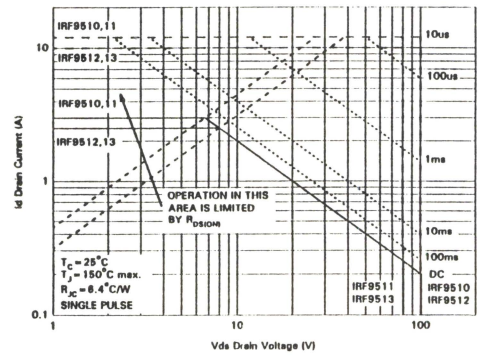


Fig. 3 - Typical saturation characteristic.



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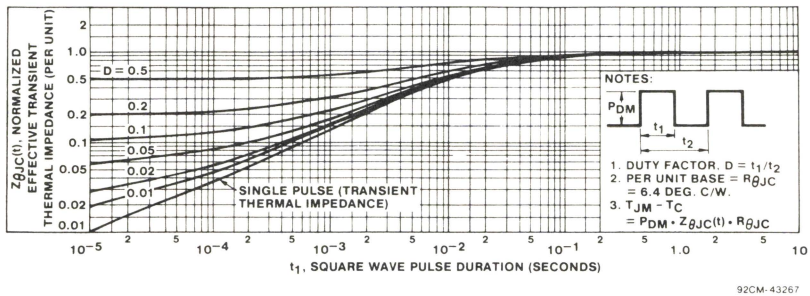


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

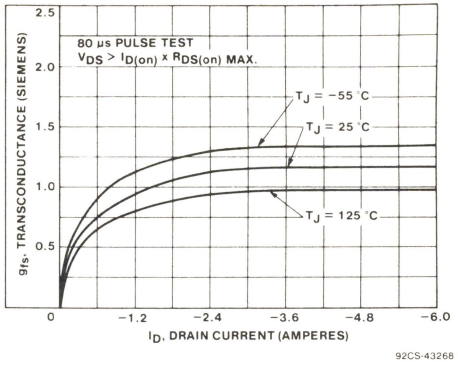


Fig. 6 - Typical transconductance vs. drain current.

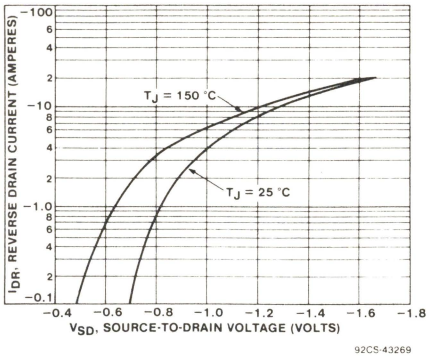


Fig. 7 - Typical source-drain diode forward voltage.

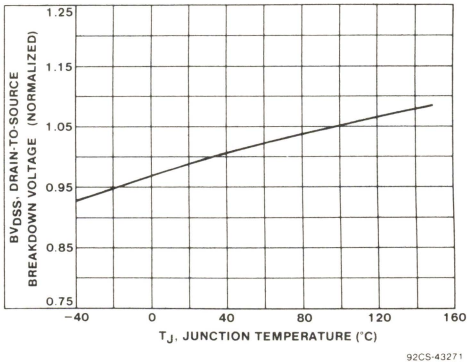


Fig. 8 - Breakdown voltage vs. temperature.

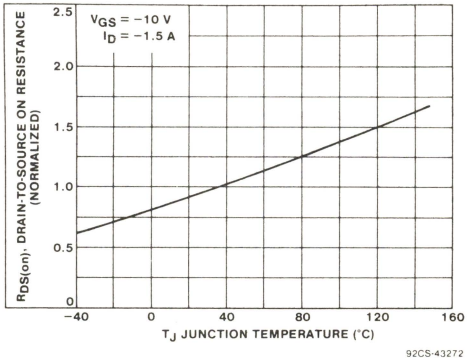


Fig. 9 - Normalized on-resistance vs. temperature.

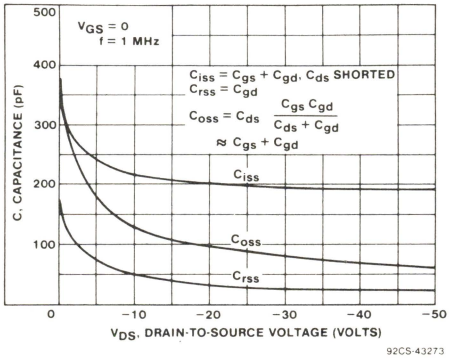


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

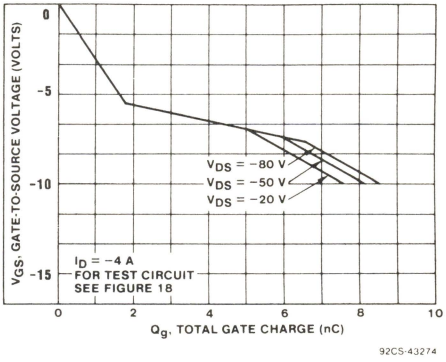
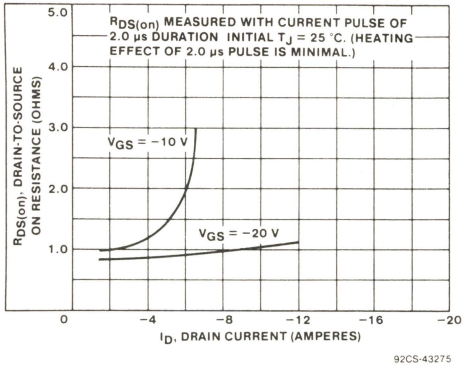


Fig. 11 - Typical gate charge vs. gate-to-source voltage.



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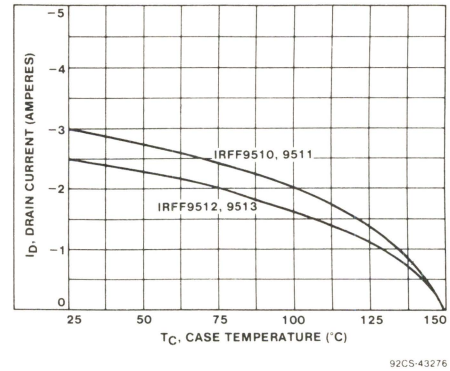
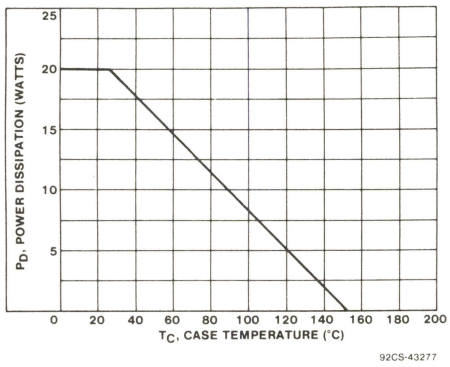


Fig. 13 - Maximum drain current vs. case temperature.



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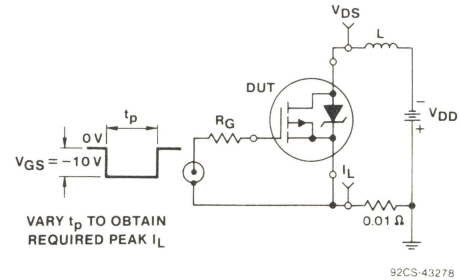
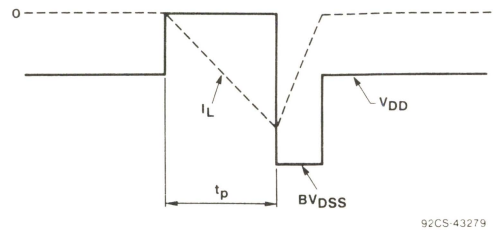


Fig. 15 - Unclamped inductive test circuit.



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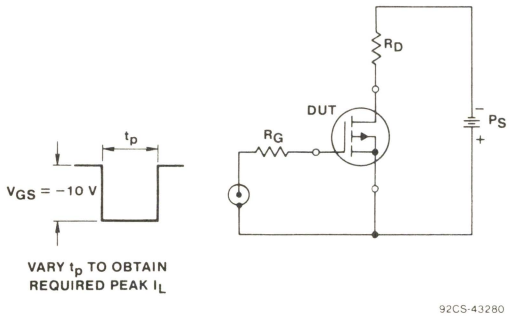

Fig. 17 - Switching time test circuit.

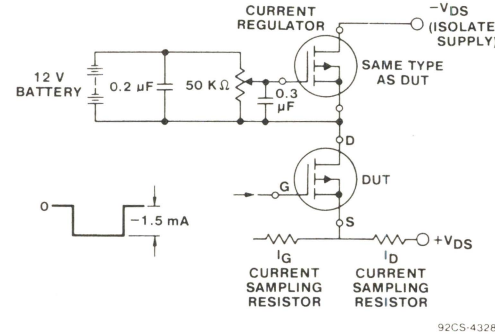

Fig. 18 - Gate charge test circuit.

HARRIS

IRF9520, IRF9521 IRF9522, IRF9523

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- High Input Impedance

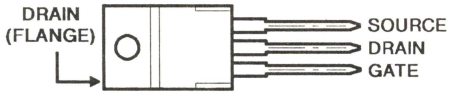
Description

The IRF9520, IRF9521, IRF9522 and IRF9523 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9520	IRF9521	IRF9522	IRF9523	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-6	-6	-5	-5	A
T_C = 100°C ..... I_D	-4	-4	-3.5	-3.5	A
Pulsed Drain Current (3) ..... I_{DM}	-24	-24	-20	-20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	40	40	40	40	W
Linear Derating Factor ..... (See Figure 14)	0.32	0.32	0.32	0.32	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	370	370	370	370	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 15.4mHμ, R_G = 25Ω, Peak I_L = 6.0A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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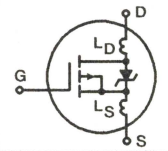
File Number 2281.1

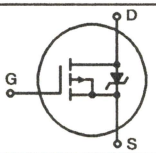
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9520, IRF9522	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9521, IRF9523			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9520, IRF9521	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6	-	-	A
IRF9522, IRF9523			-5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9520, IRF9521	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3.5A	-	0.5	0.6	Ω
IRF9522, IRF9523			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -3.5A	0.9	2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.0A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-6.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-24	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.0A, dI_F/dt = 100A/μs	-	230	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.0A, dI_F/dt = 100A/μs	-	1.3	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 15.4mH, R_G = 25Ω, Peak I_L = 6.0A (See Figures 15 and 16)

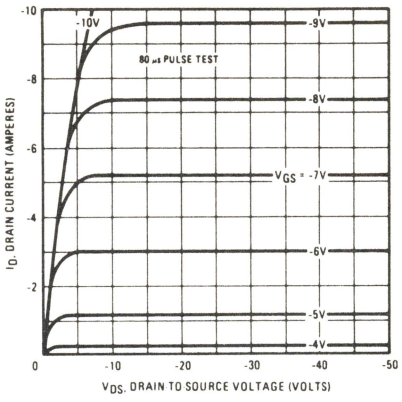


Fig. 1 - Typical output characteristics.

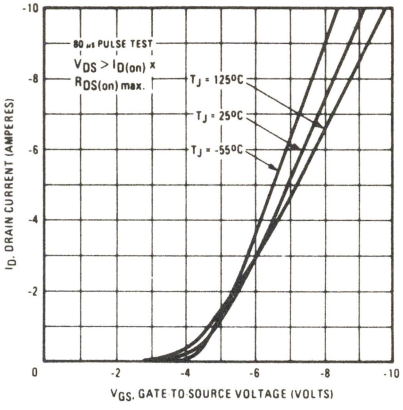


Fig. 2 - Typical transfer characteristics.

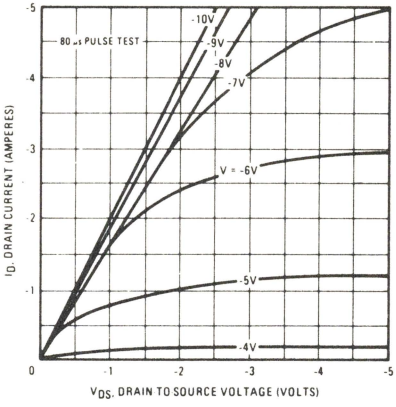


Fig. 3 - Typical saturation characteristics.

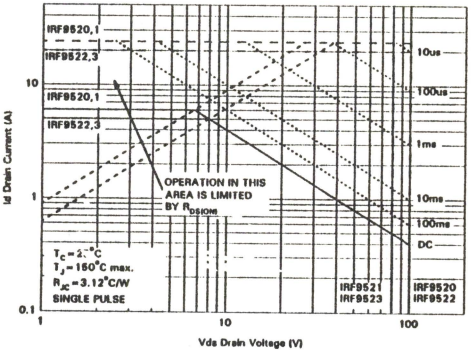


Fig. 4 - Maximum safe operating area.

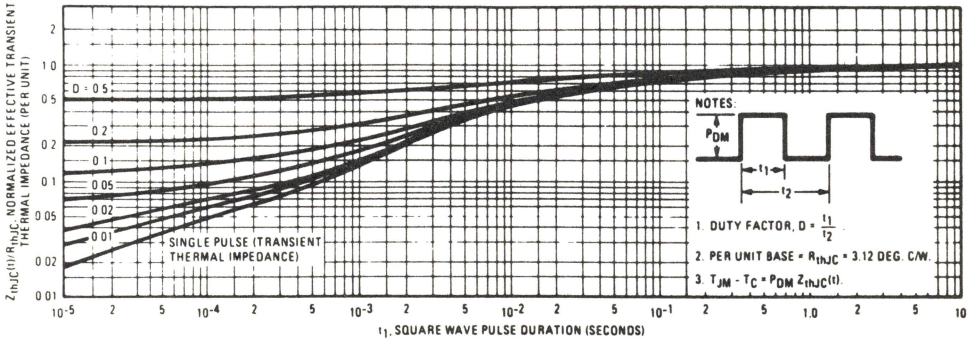


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

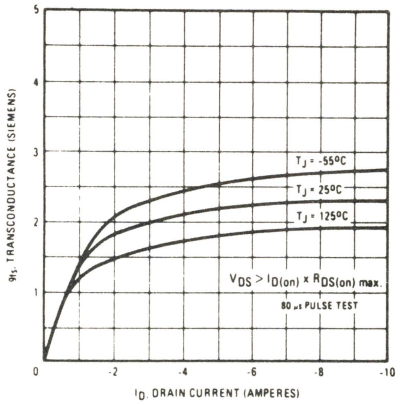


Fig. 6 - Typical transconductance vs. drain current.

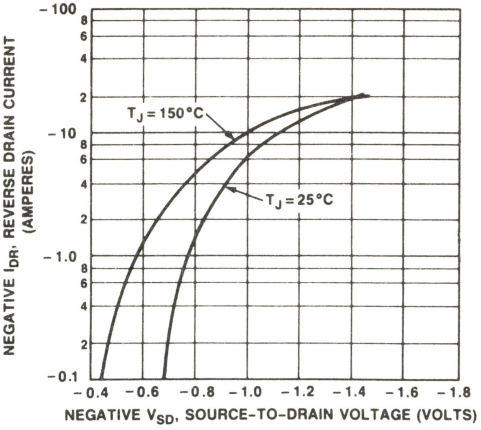


Fig. 7 - Typical source-drain diode forward voltage.

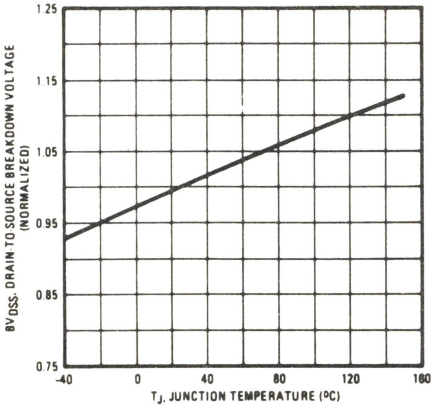


Fig. 8 - Breakdown voltage vs. temperature.

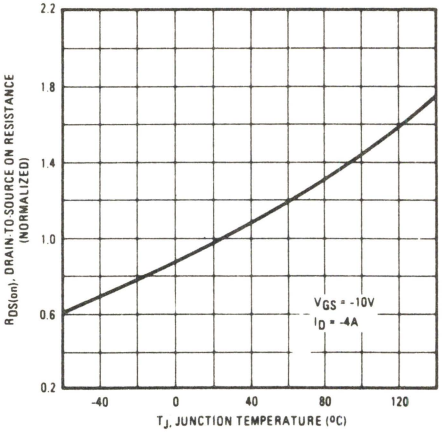


Fig. 9 - Normalized on-resistance vs. temperature.

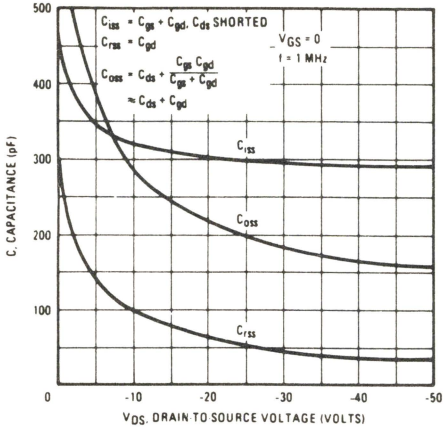


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

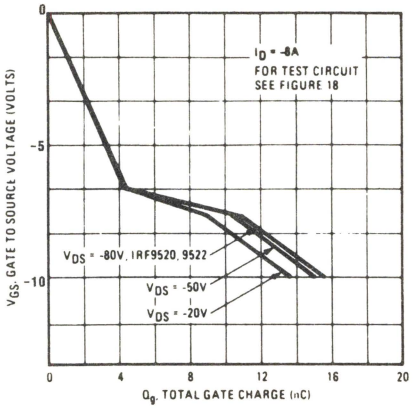


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

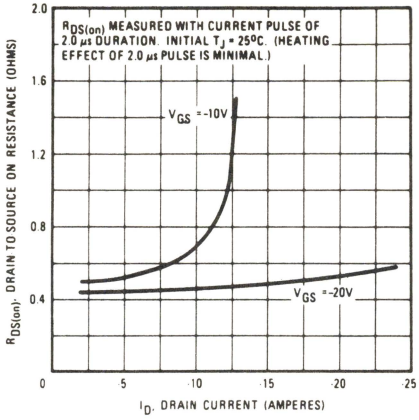


Fig. 12 - Typical on-resistance vs. drain current.

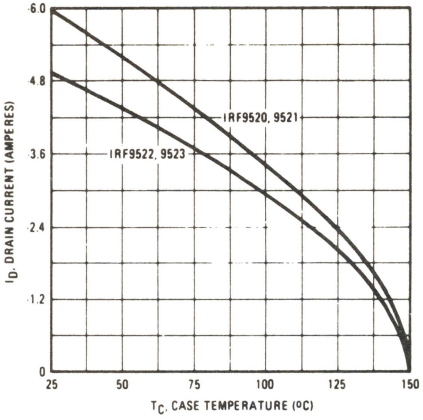


Fig. 13 - Maximum drain current vs. case temperature.

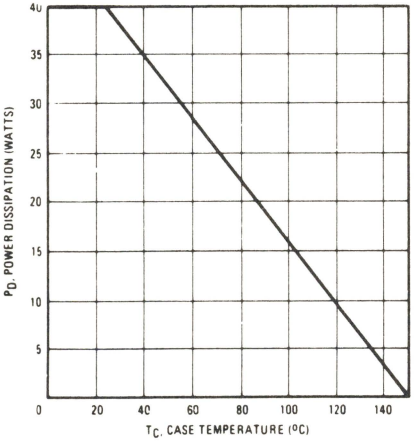


Fig. 14 - Power vs. temperature derating curve.

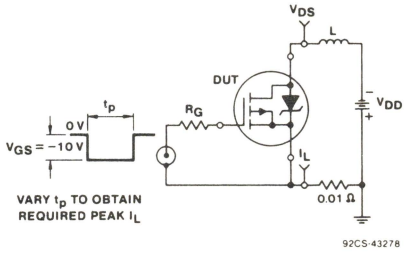


Fig. 15 - Unclamped inductive test circuit.

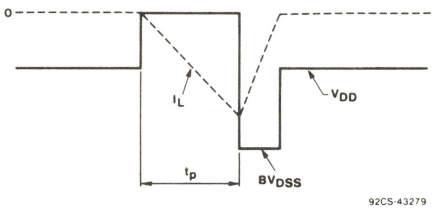


Fig. 16 - Unclamped inductive waveforms.

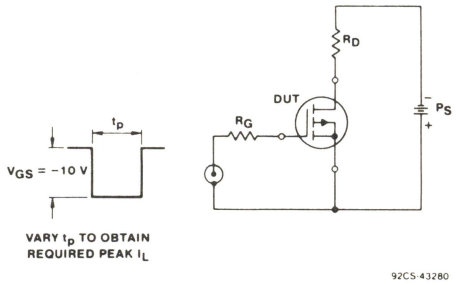


Fig. 17 - Switching time test circuit.

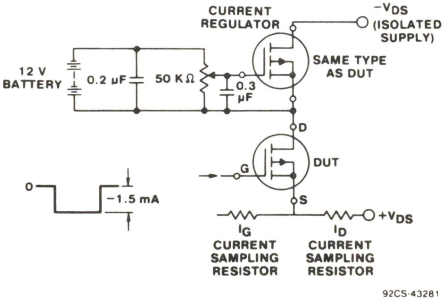


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9530, IRF9531 IRF9532, IRF9533

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -10A and -12A, -80V and -100V
- $r_{DS(ON)}$ = 0.3Ω and 0.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

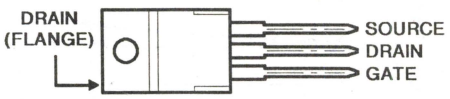
Description

The IRF9530, IRF9531, IRF9532 and IRF9533 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

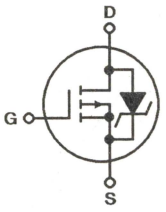
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRF9530	IRF9531	IRF9532	IRF9533	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current						
T_C = 25°C	I_D	-12	-12	-10	-10	A
T_C = 100°C	I_D	-7.5	-7.5	-6.5	-6.5	A
Pulsed Drain Current (3)	I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage	V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation (See Figure 14)	P_D	75	75	75	75	W
Linear Derating Factor (See Figure 14)		0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mHμ, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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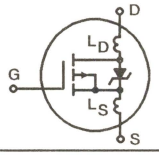
File Number 2221.1

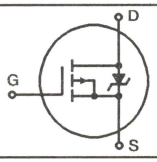
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9530, IRF9532	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9531, IRF9533			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9530, IRF9531	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-12	-	-	A
IRF9532, IRF9533			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9530, IRF9531	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6.5A	-	0.25	0.3	Ω
IRF9532, IRF9533			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 6.5A	2.0	3.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -12A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -12A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -12A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -12A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -12A, dI_F/dt = 100A/μs	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 5.2mH, R_G = 25Ω, Peak I_L = 12A (See Figures 15 and 16)

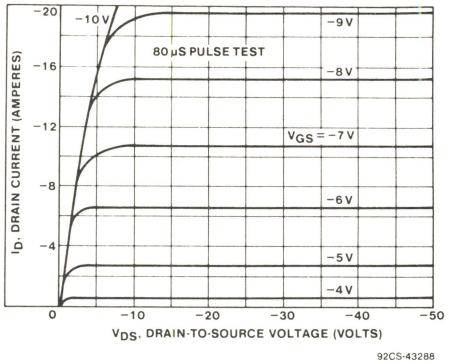


Fig. 1 - Typical Output Characteristics

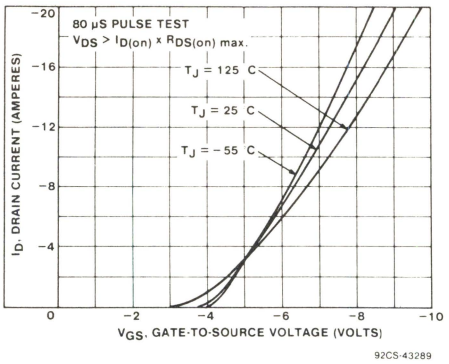


Fig. 2 - Typical Transfer Characteristics

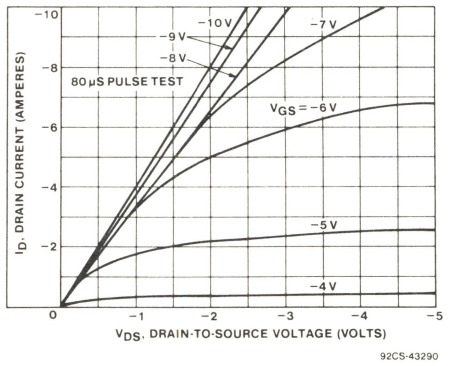


Fig. 3 - Typical saturation characteristic.

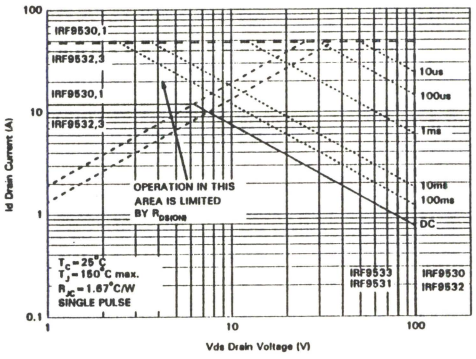


Fig. 4 - Maximum safe operating area.

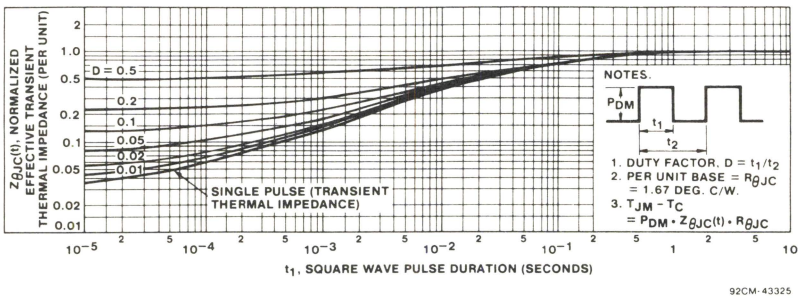


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

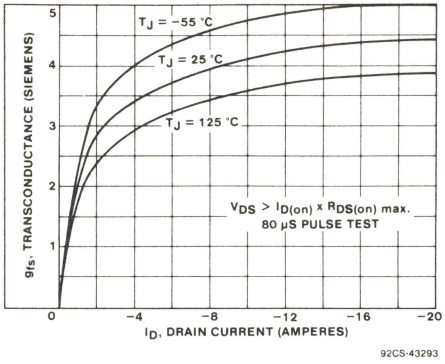


Fig. 6 - Typical transconductance vs. drain current.

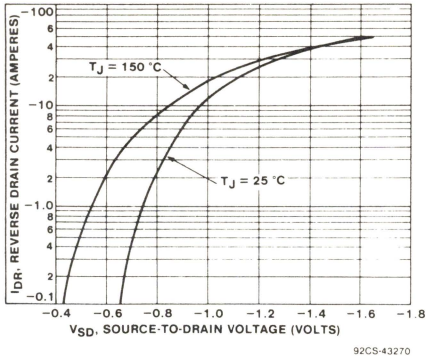


Fig. 7 - Typical source-drain diode forward voltage.

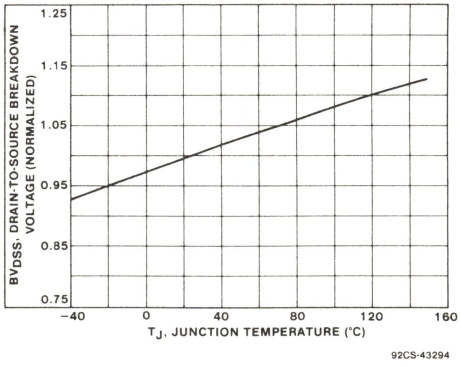


Fig. 8 - Breakdown voltage vs. temperature.

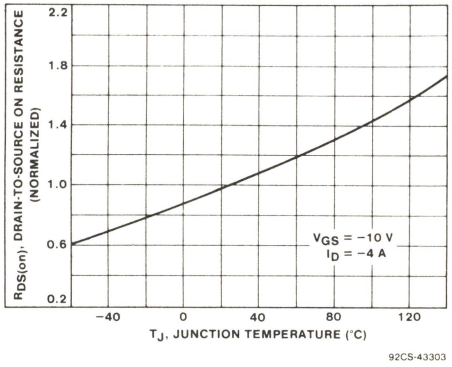


Fig. 9 - Normalized on-resistance vs. temperature.

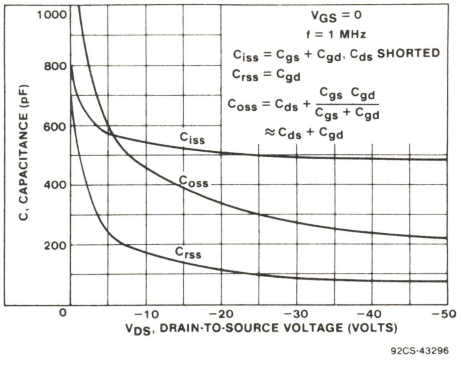


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

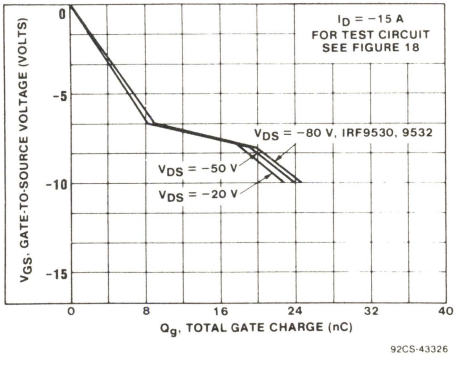


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

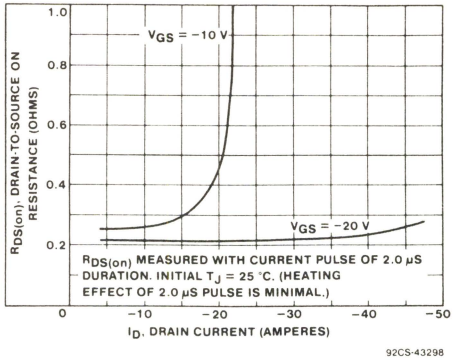


Fig. 12 - Typical on-resistance vs. drain current.

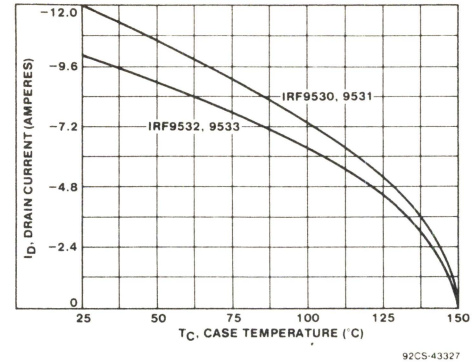


Fig. 13 - Maximum drain current vs. case temperature.

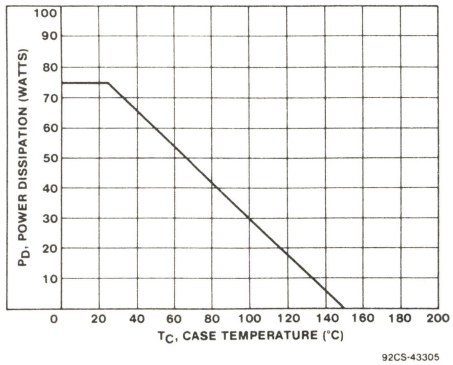


Fig. 14 - Power vs. temperature derating curve.

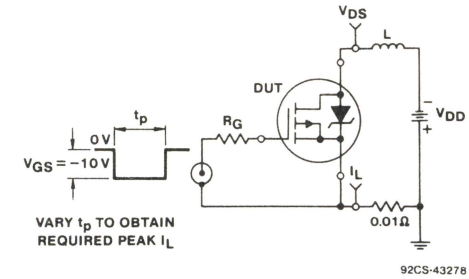


Fig. 15 - Unclamped inductive test circuit.

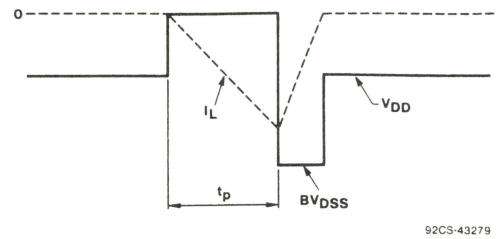


Fig. 16 - Unclamped inductive waveforms.

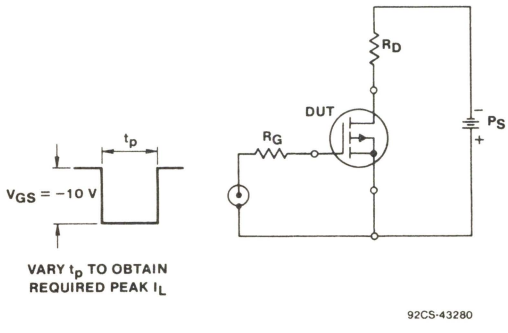


Fig. 17 - Switching time test circuit.

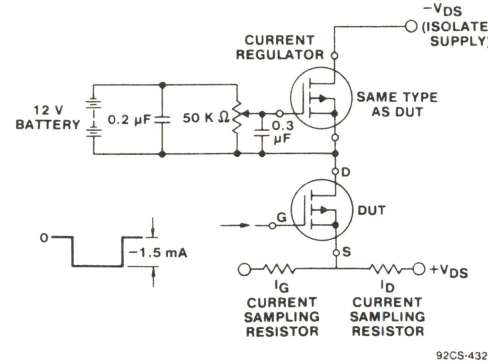


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9540, IRF9541 IRF9542, IRF9543

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -15A and -19A, -80V and -100V
- $r_{DS(ON)}$ = 0.20Ω and 0.30Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

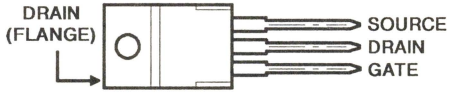
Description

The IRF9540, IRF9541, IRF9542 and IRF9543 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

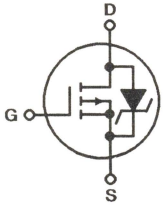
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9540	IRF9541	IRF9542	IRF9543	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-19	-19	-15	-15	A
T_C = 100°C ..... I_D	-12	-12	-10	-10	A
Pulsed Drain Current (3) ..... I_{DM}	-76	-76	-60	-60	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	125	125	125	125	W
Linear Derating Factor ..... (See Figure 14)	1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	960	960	960	960	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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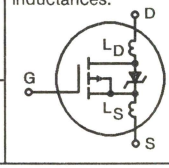
File Number 2282.2

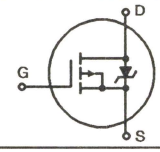
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9540, IRF9542	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRF9541, IRF9543			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9540, IRF9541	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-19	-	-	A
IRF9542, IRF9543			-15	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9540, IRF9541	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.15	0.20	Ω
IRF9542, IRF9543			-	0.22	0.30	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -6A	5	7	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1100	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	250	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -19A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	20	ns
Rise Time	t_r		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	t_f		-	28	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -19A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	90	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	56	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-19	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-76	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -19A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 19A, dI_F/dt = 100A/μs	-	170	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 19A, dI_F/dt = 100A/μs	-	0.8	0	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 4mH, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

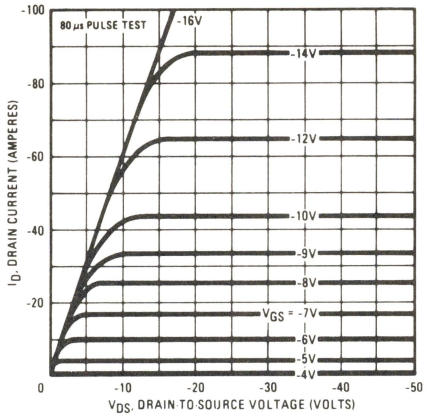


Fig. 1 - Typical output characteristics.

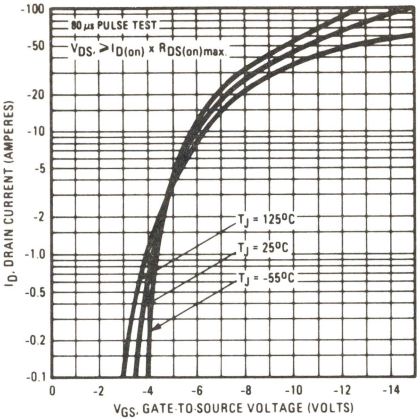


Fig. 2 - Typical transfer characteristics.

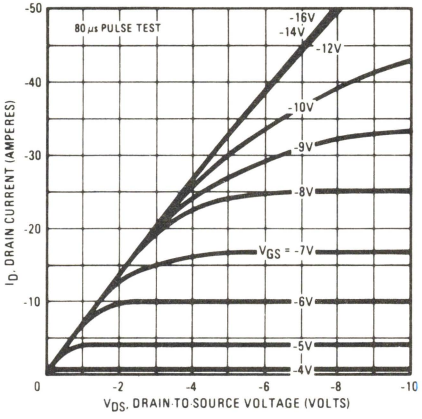


Fig. 3 - Typical saturation characteristics.

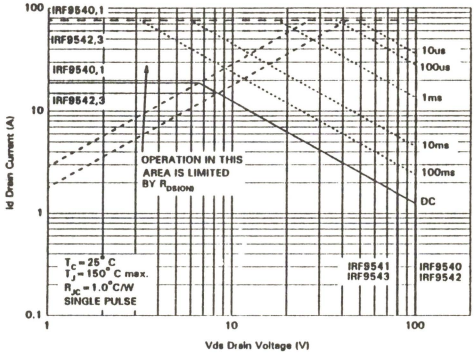


Fig. 4 - Maximum safe operating area.

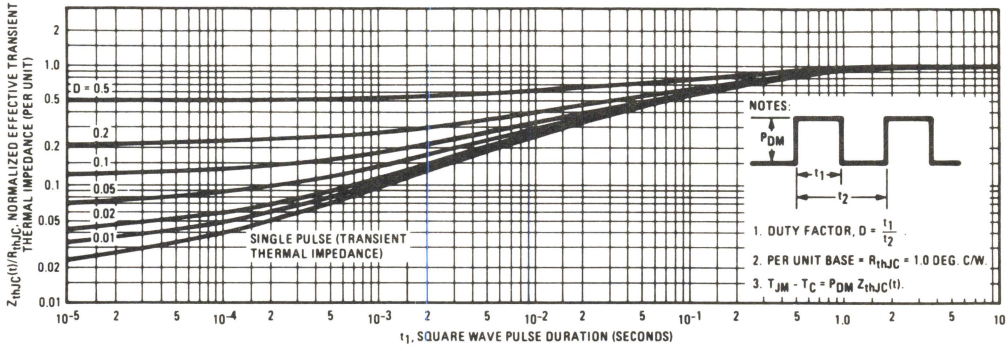


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

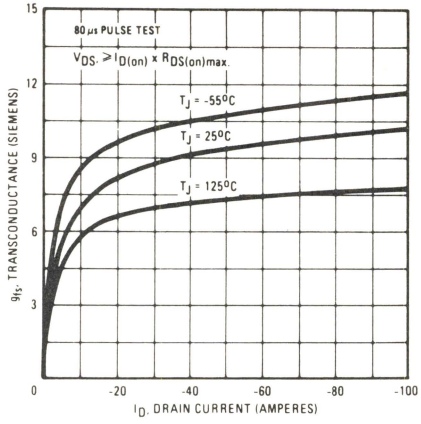


Fig. 6 - Typical transconductance vs. drain current.

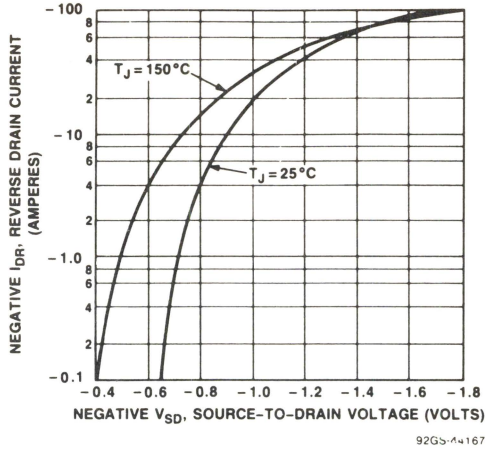


Fig. 7 - Typical source-drain diode forward voltage.

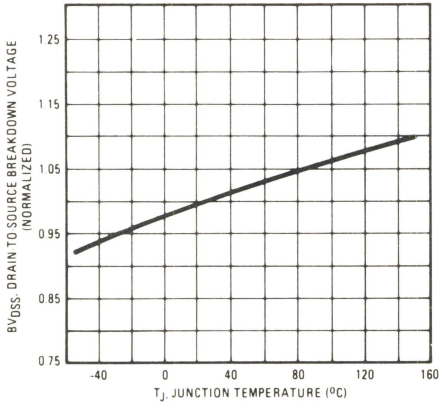


Fig. 8 - Breakdown voltage vs. temperature.

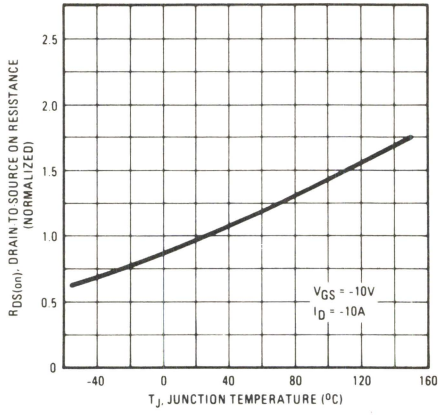


Fig. 9 - Normalized on-resistance vs. temperature.

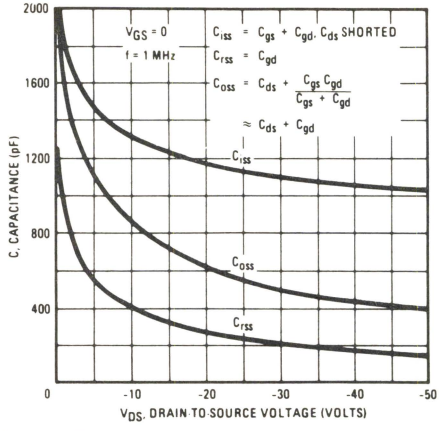


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

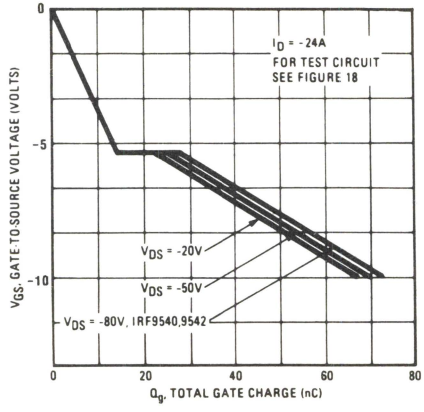


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

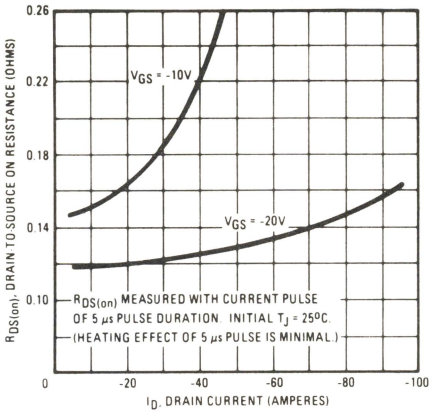


Fig. 12 - Typical on-resistance vs. drain current.

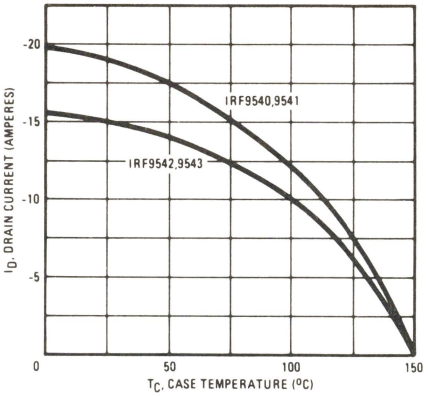


Fig. 13 - Maximum drain current vs. case temperature.

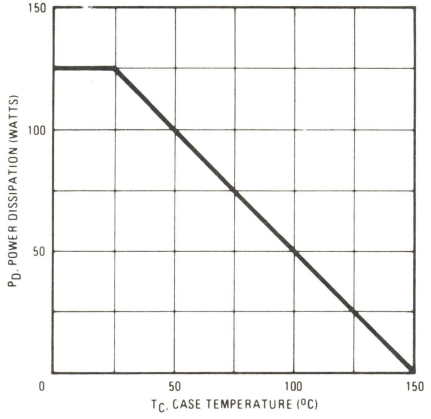


Fig. 14 - Power vs. temperature derating curve.

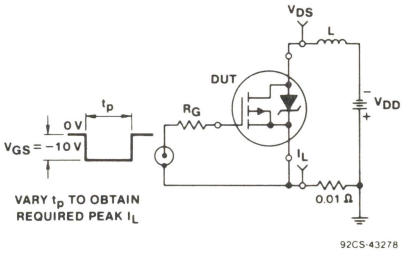


Fig. 15 - Unclamped inductive test circuit.

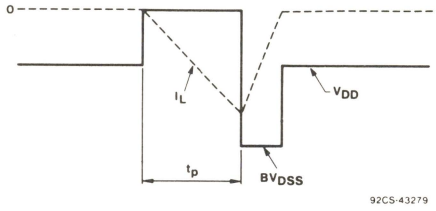


Fig. 16 - Unclamped inductive waveforms.

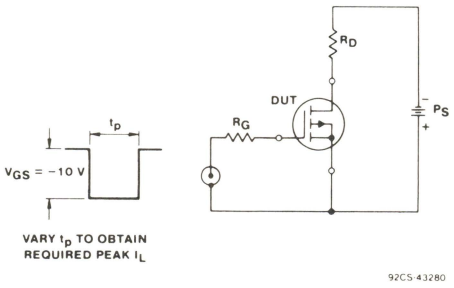


Fig. 17 - Switching time test circuit.

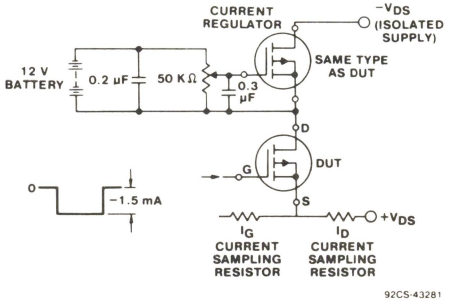


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9620, IRF9621 IRF9622, IRF9623

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -3A and -3.5A, -150V and -200V
- $r_{DS(ON)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

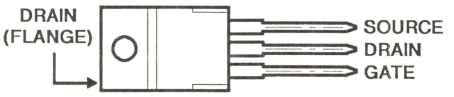
Description

The IRF9620, IRF9621, IRF9622 and IRF9623 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

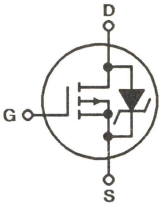
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9620	IRF9621	IRF9622	IRF9623	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-3.5	-3.5	-3	-3	A
T_C = 100°C ..... I_D	-2	-2	-1.5	-1.5	A
Pulsed Drain Current (3) ..... I_{DM}	-14	-14	-12	-12	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	40	40	40	40	W
Linear Derating Factor ..... (See Figure 14)	0.32	0.32	0.32	0.32	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	290	290	290	290	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 35.5mH, R_G = 25Ω, Peak I_L = 3.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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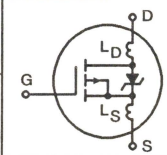
File Number **2283**

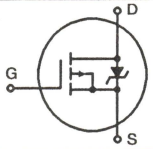
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9620, IRF9622	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9621, IRF9623			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9620, IRF9621	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-3.5	-	-	A
IRF9622, IRF9623			-3	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9620, IRF9621	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -1.5A	-	1.0	1.5	Ω
IRF9622, IRF9623			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.5A	1	1.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	350	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -3.5A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -3.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	3.12	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-3.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-14	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -3.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -3.5A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -3.5A, dI_F/dt = 100A/μs	-	1.9	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 35.5mH, R_G = 25Ω, Peak I_L = 3.5A (See Figures 15 and 16)

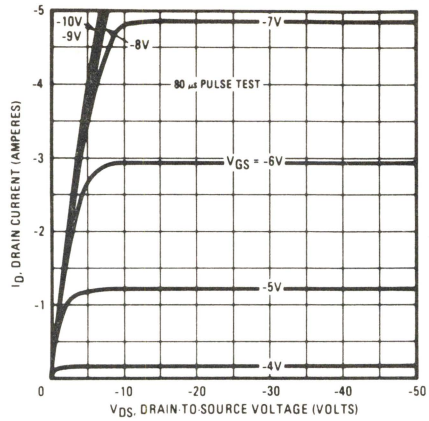


Fig. 1 - Typical output characteristics.

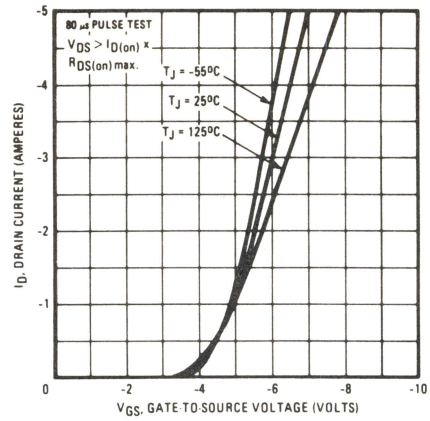


Fig. 2 - Typical transfer characteristics.

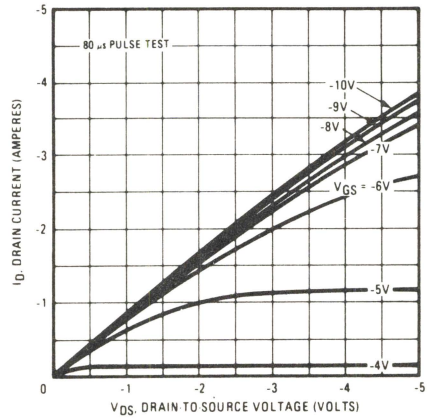


Fig. 3 - Typical saturation characteristics.

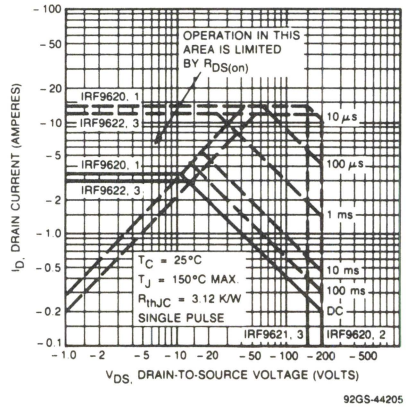


Fig. 4 - Maximum safe operating area.

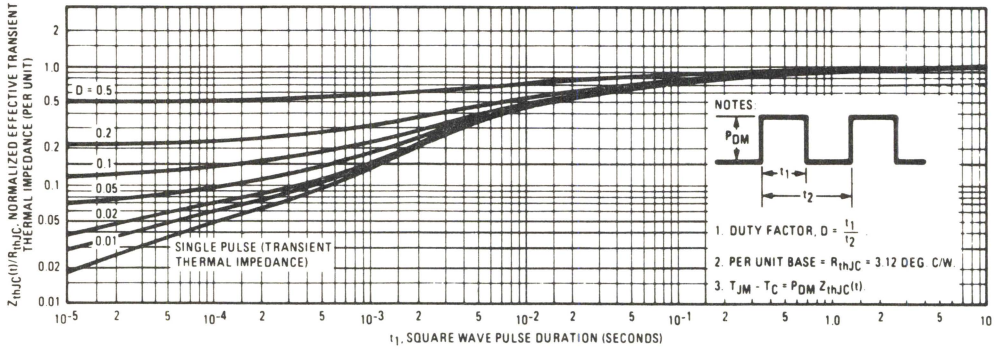


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

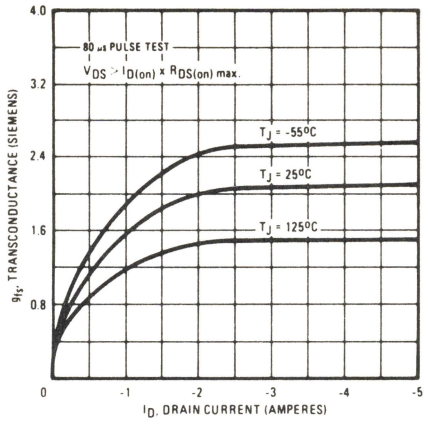


Fig. 6 - Typical transconductance vs. drain current.

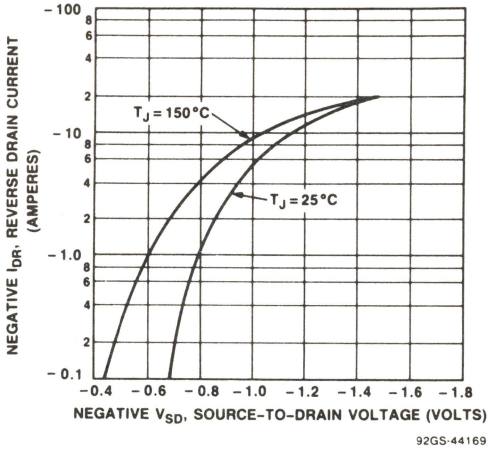


Fig. 7 - Typical source-drain diode forward voltage.

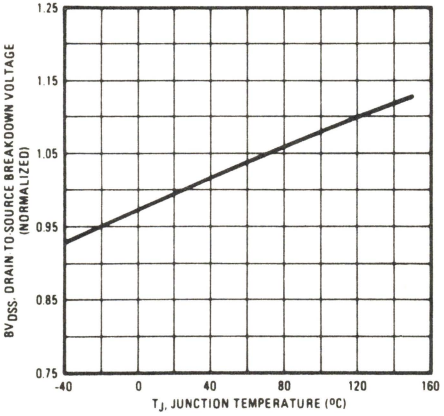


Fig. 8 - Breakdown voltage vs. temperature.

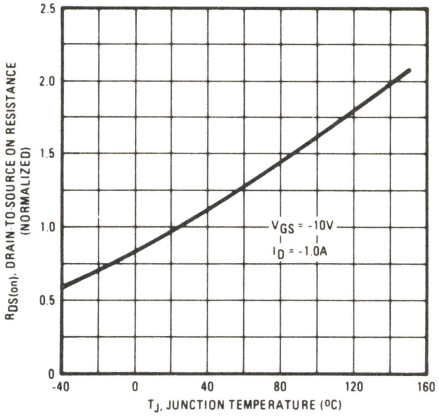


Fig. 9 - Normalized on-resistance vs. temperature.

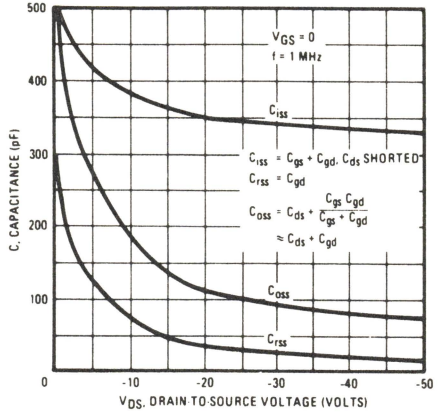


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

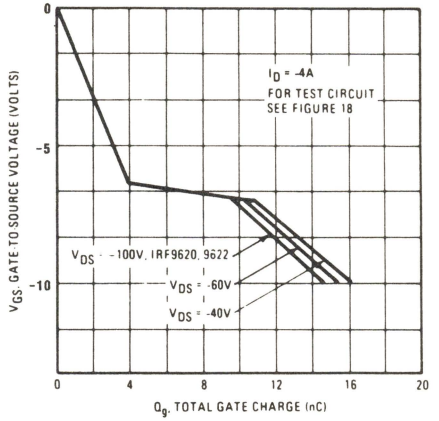


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

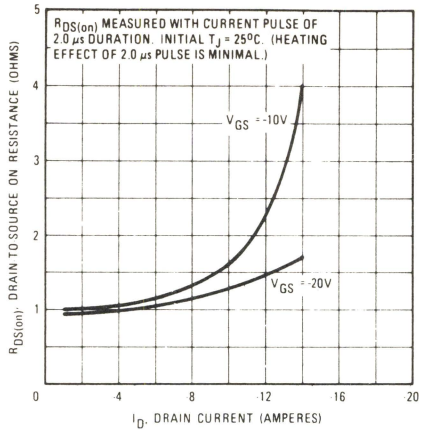


Fig. 12 - Typical on-resistance vs. drain current.

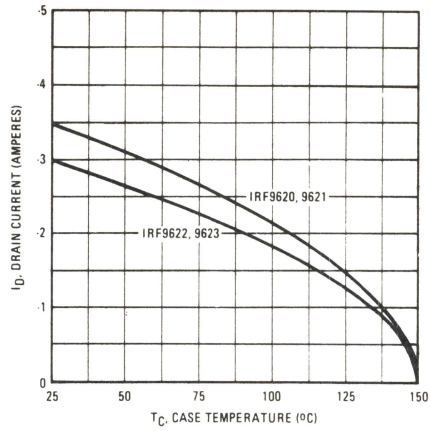


Fig. 13 - Maximum drain current vs. case temperature.

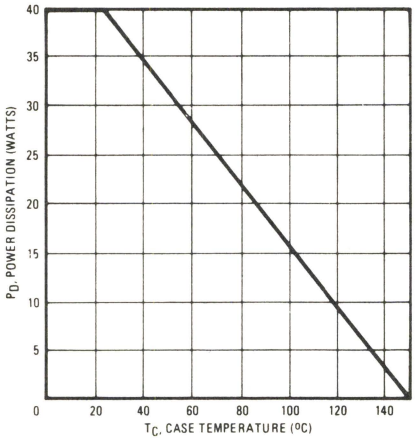


Fig. 14 - Power vs. temperature derating curve.

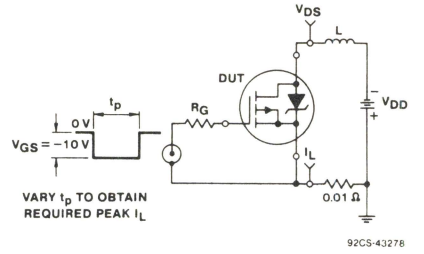


Fig. 15 - Unclamped inductive test circuit.

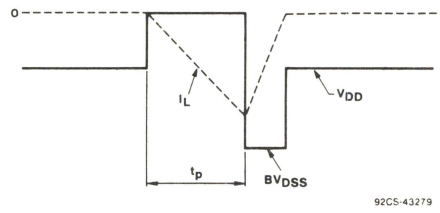


Fig. 16 - Unclamped inductive waveforms.

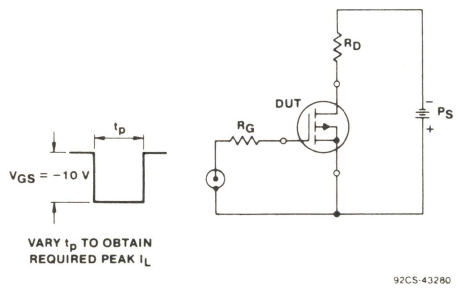


Fig. 17 - Switching time test circuit.

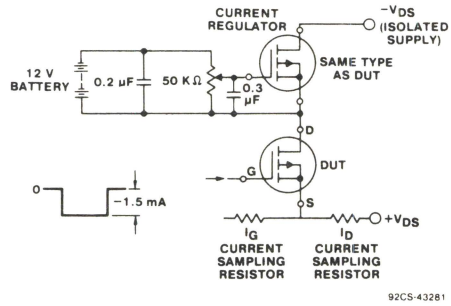


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9630, IRF9631 IRF9632, IRF9633

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -5.5A and -6.5A, -150V and -200V
- $r_{DS(ON)}$ = 0.8Ω and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

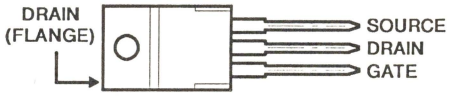
Description

The IRF9630, IRF9631, IRF9632 and IRF9633 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

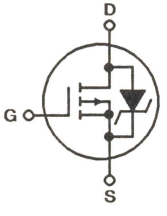
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9630	IRF9631	IRF9632	IRF9633	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-6.5	-6.5	-5.5	-5.5	A
T_C = 100°C ..... I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3) ..... I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	75	75	75	75	W
Linear Derating Factor ..... (See Figure 14)	0.6	0.6	0.6	0.6	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.55mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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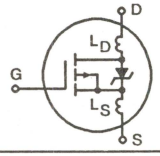
File Number 2224

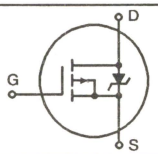
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9630, IRF9632	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9631, IRF9633			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9630, IRF9631	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6.5	-	-	A
IRF9632, IRF9633			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9630, IRF9631	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3.5A	-	0.5	0.8	Ω
IRF9632, IRF9633			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)\,Max}$, I_D = 3.5A	2.2	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	550	-	pF
Output Capacitance	C_{OSS}		-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, R_G = 50Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	13	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	400	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	2.6	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

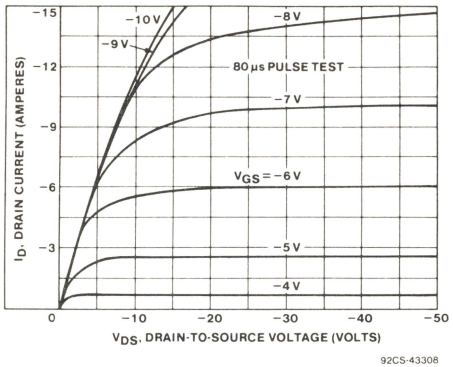


Fig. 1 - Typical output characteristics.

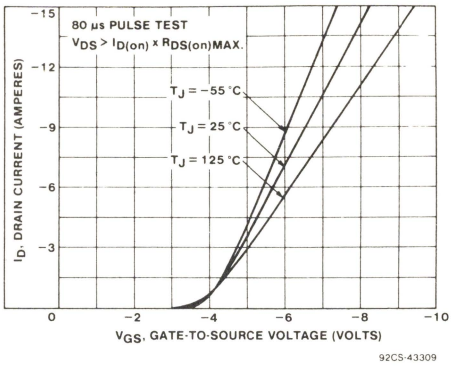


Fig. 2 - Typical transfer characteristics.

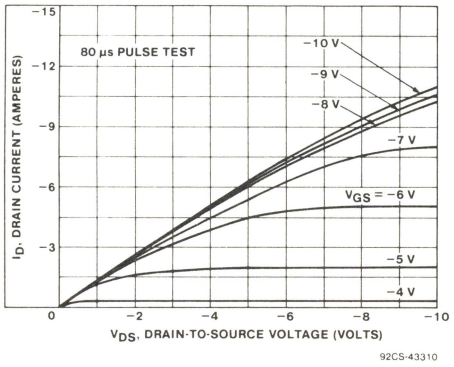


Fig. 3 - Typical saturation characteristics.

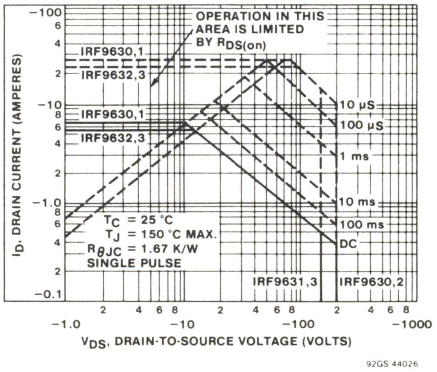


Fig. 4 - Maximum safe operating area.

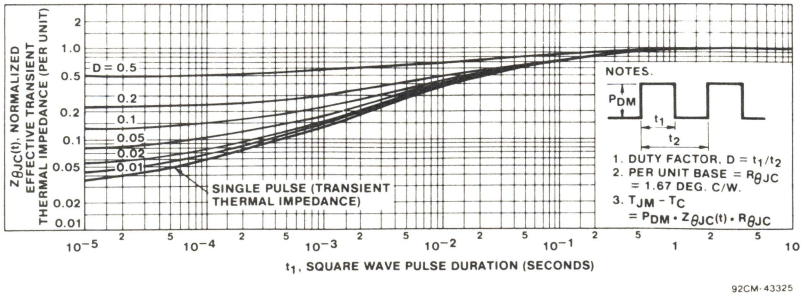


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

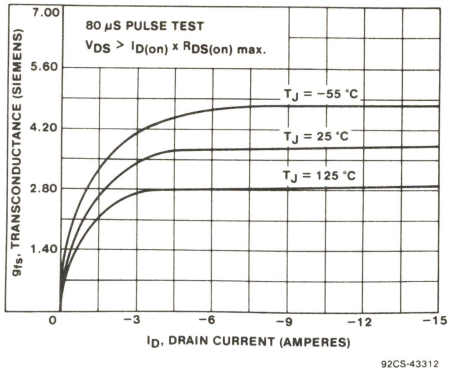


Fig. 6 - Typical transconductance vs. drain current.

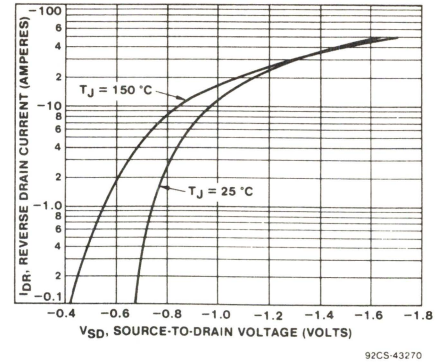


Fig. 7 - Typical source-drain diode forward voltage.

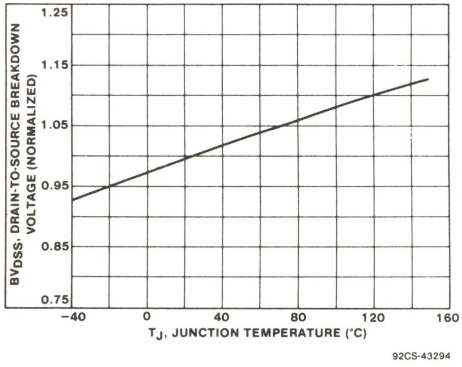


Fig. 8 - Breakdown voltage vs. temperature.

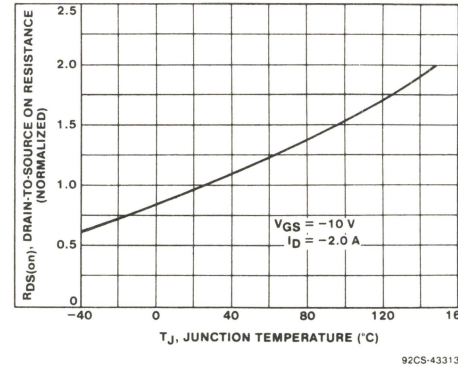


Fig. 9 - Normalized on-resistance vs. temperature.

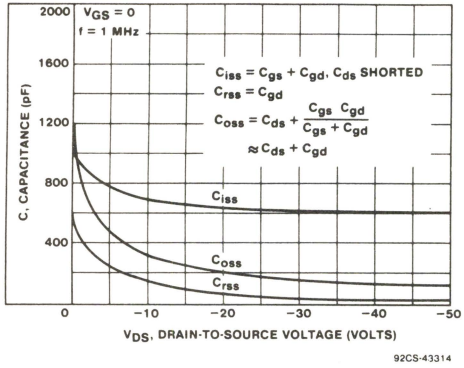


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

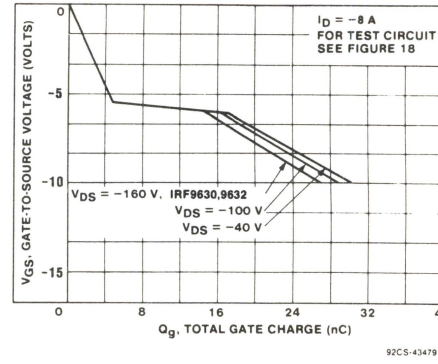


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

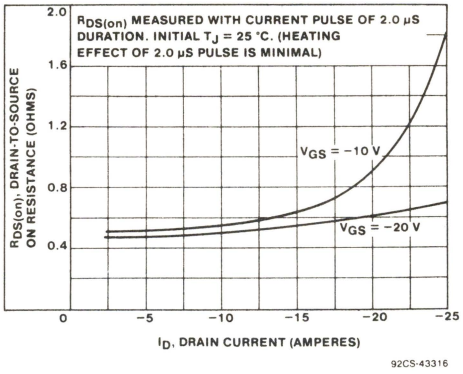


Fig. 12 - Typical on-resistance vs. drain current.

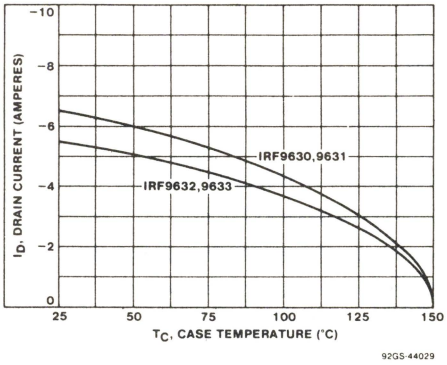


Fig. 13 - Maximum drain current vs. case temperature.

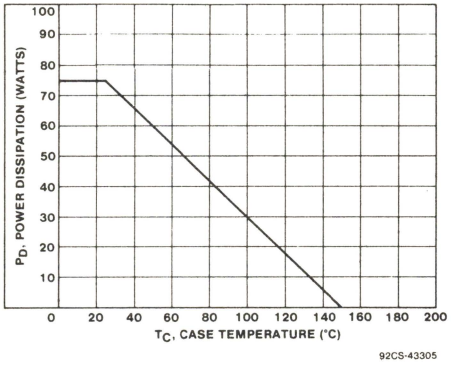


Fig. 14 - Power vs. temperature derating curve.

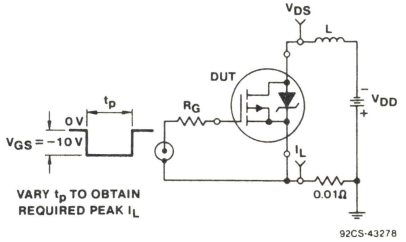


Fig. 15 - Unclamped inductive test circuit.

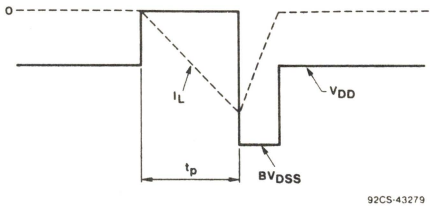


Fig. 16 - Unclamped inductive waveforms.

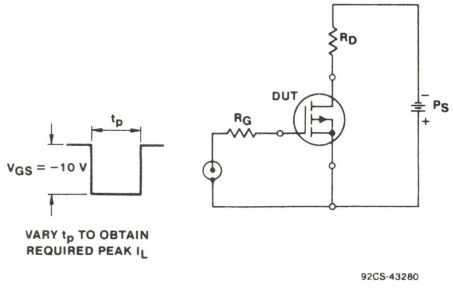


Fig. 17 - Switching time test circuit.

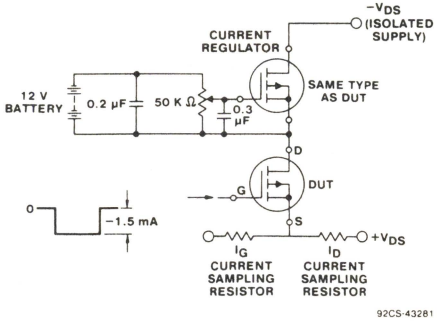


Fig. 18 - Gate charge test circuit.

HARRIS

IRF9640, IRF9641 IRF9642, IRF9643

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -9A and -11A, -150V and -200V
- $r_{DS(ON)}$ = 0.5Ω and 0.7Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

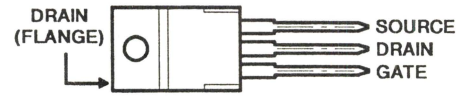
Description

The IRF9640, IRF9641, IRF9642 and IRF9643 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

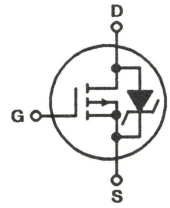
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRF9640	IRF9641	IRF9642	IRF9643	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-11	-11	-9	-9	A
T_C = 100°C ..... I_D	-7	-7	-6	-6	A
Pulsed Drain Current (3) ..... I_{DM}	-44	-44	-36	-36	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	125	125	125	125	W
Linear Derating Factor ..... (See Figure 14)	1	1	1	1	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	790	790	790	790	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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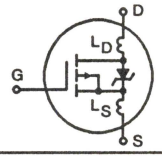
File Number **2284**

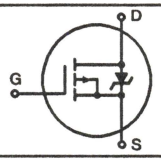
Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9640, IRF9642	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRF9641, IRF9643			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9640, IRF9641	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-11	-	-	A
IRF9642, IRF9643			-9	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9640, IRF9641	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6A	-	0.35	0.5	Ω
IRF9642, IRF9643			-	0.55	0.7	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -6A	4	6	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1100	-	pF
Output Capacitance	C_{OSS}		-	375	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	150	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -11A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	18	22	ns
Rise Time	t_r		-	45	68	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	90	ns
Fall Time	t_f		-	29	44	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -11A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	70	90	nC
Gate-Source Charge	Q_{gs}		-	55	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	15	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	°C/W



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-11	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-44	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -11A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -11A, dI_F/dt = 100A/μs	-	1.9	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-



NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 9.8mH, R_G = 25Ω, Peak I_L = 11A (See Figures 15 and 16)

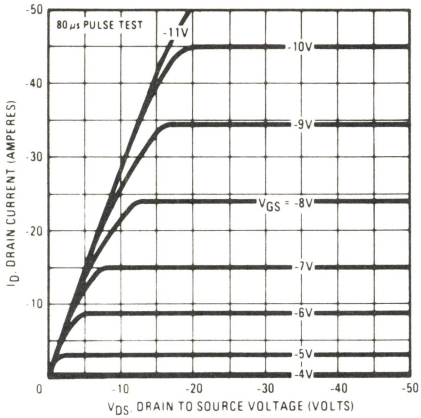


Fig. 1 - Typical output characteristics.

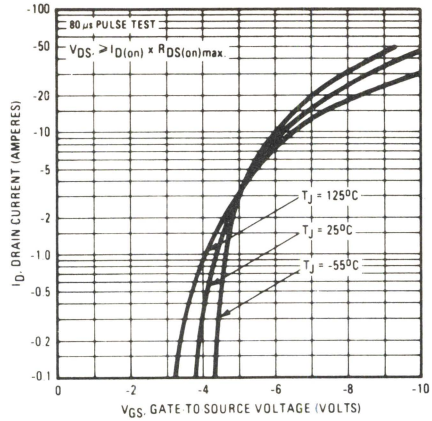


Fig. 2 - Typical transfer characteristics.

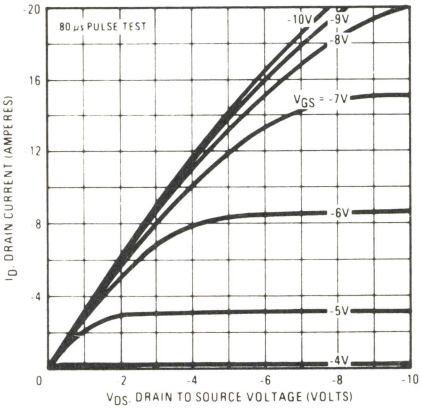


Fig. 3 - Typical saturation characteristics.

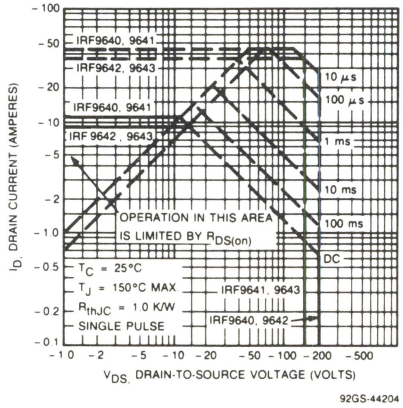


Fig. 4 - Maximum safe operating area.

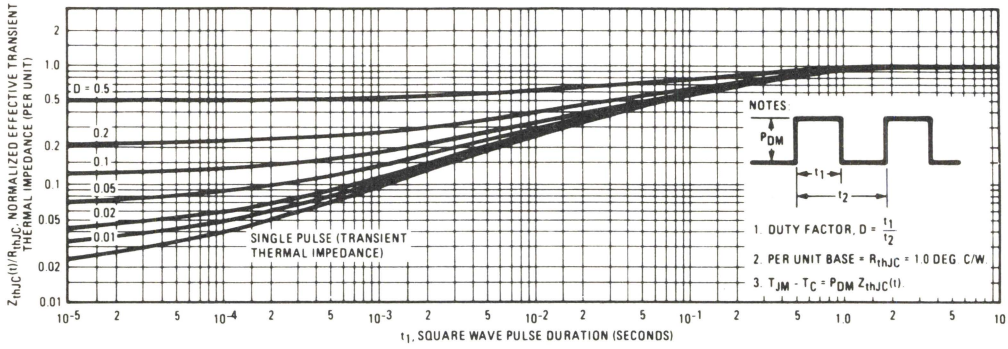


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

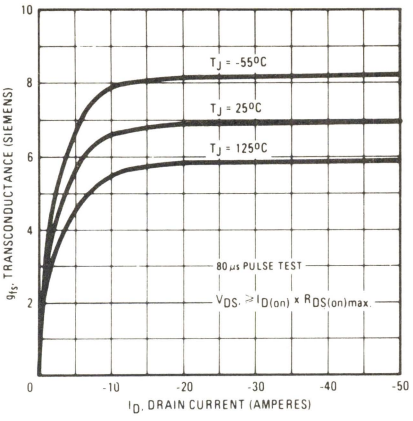


Fig. 6 - Typical transconductance vs. drain current.

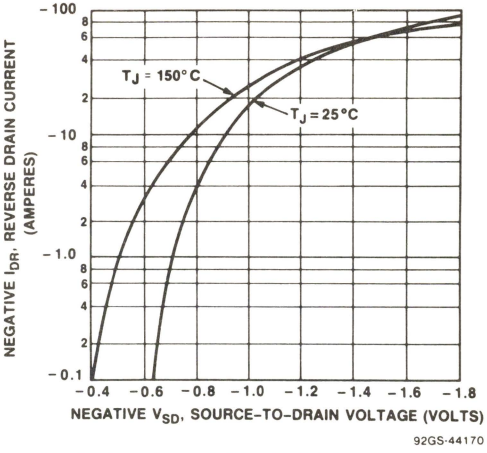


Fig. 7 - Typical source-drain diode forward voltage.

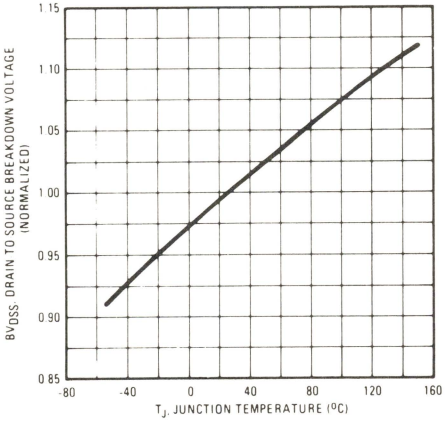


Fig. 8 - Breakdown voltage vs. temperature.

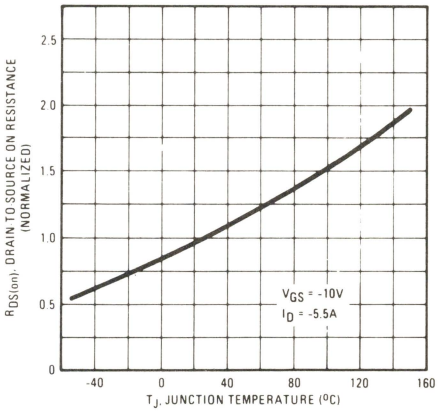


Fig. 9 - Normalized on-resistance vs. temperature.

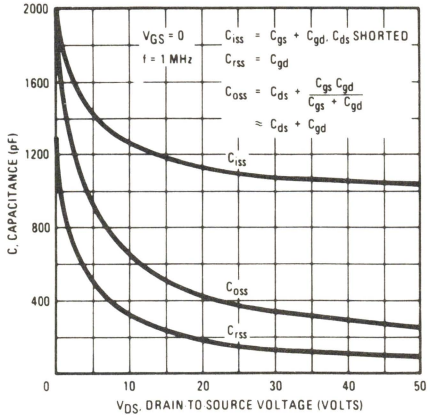


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

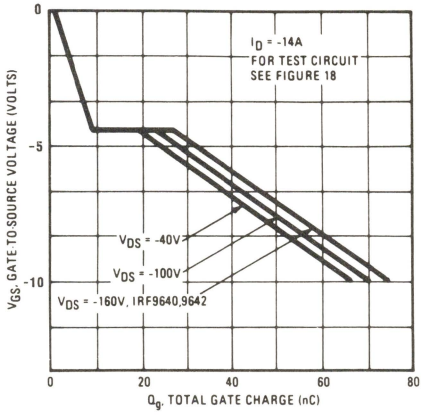


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

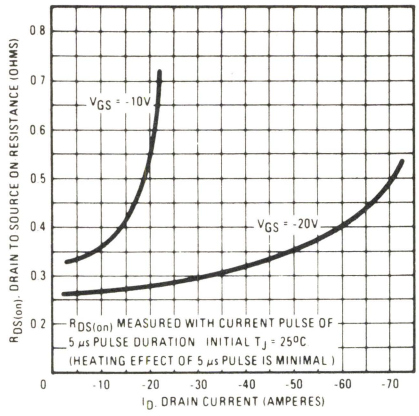


Fig. 12 - Typical on-resistance vs. drain current.

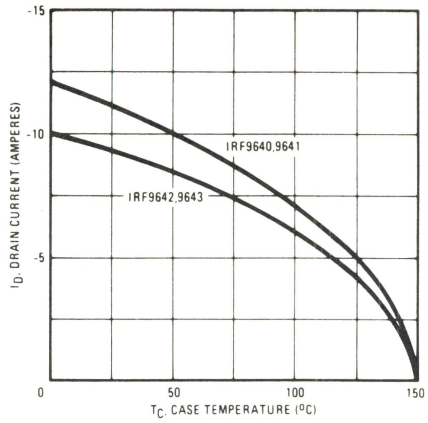


Fig. 13 - Maximum drain current vs. case temperature.

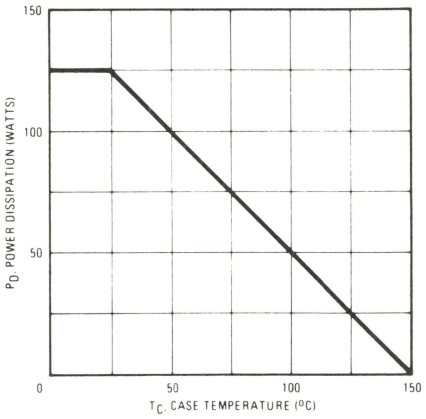


Fig. 14 - Power vs. temperature derating curve.

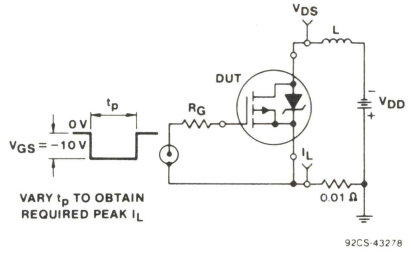


Fig. 15 - Unclamped inductive test circuit.

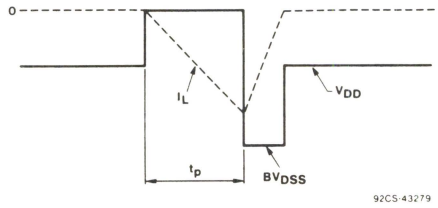


Fig. 16 - Unclamped inductive waveforms.

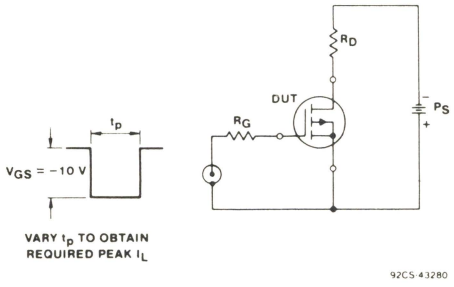


Fig. 17 - Switching time test circuit.

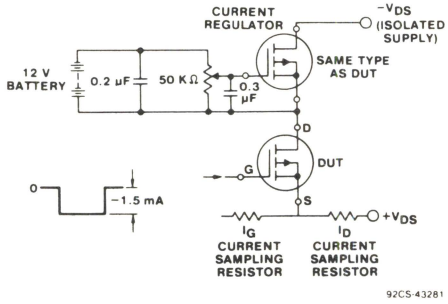


Fig. 18 - Gate charge test circuit.

HARRIS

IRFD9110
IRFD9113

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -0.6A and -0.7A, -80V and -100V
- $r_{DS(ON)}$ = 1.2Ω and 1.6Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFD9110 and IRFD9113 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-Pin dual-in-line plastic package.

Package

4-PIN DUAL-IN-LINE
TOP VIEW

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFD9110	IRFD9113	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-80	V
Continuous Drain Current T_C = 25°C	I_D	-0.7	-0.6	A
Pulsed Drain Current	I_{DM}	-3.0	-2.5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 13)	P_D	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating (3)	E_{as}	190	190	mJ
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. T_J = 25°C to 150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, Start T_J = +25°C, L = 582mh, R_G = 25Ω, Peak I_L = 0.7A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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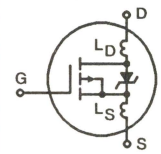
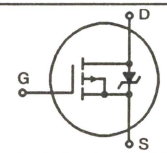
File Number 2215.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD9110	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFD9113			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFD9110	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-0.7	-	-	A
IRFD9113			-0.6	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD9110	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -0.3A	-	1.0	1.2	Ω
IRFD9113			-	1.2	1.6	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \leq$ 50V, I_D = -0.6A	0.59	0.88	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 9	-	180	-	pF
Output Capacitance	C_{OSS}		-	85	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5, I_D = 0.7A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature.)	-	15	30	ns
Rise Time	t_r		-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	40	ns
Fall Time	t_f		-	20	40	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -0.7A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	11	15	nC
Gate-Source Charge	Q_{gs}		-	5.7	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	5.3	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from header to source bonding pad. 	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-0.7	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-3.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -0.7A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -0.7A, dI_F/dt = 100A/μs	-	120	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -0.7A, dI_F/dt = 100A/μs	-	6.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

3. V_{DD} = 25V, Start T_J = +25°C, L = 582mH, R_G = 25Ω, Peak I_L = 0.7A (See Figures 14 and 15)

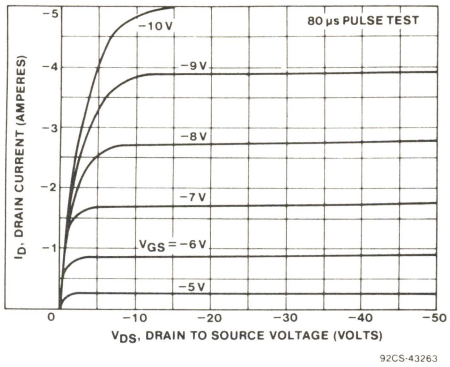


Fig. 1 - Typical Output Characteristics

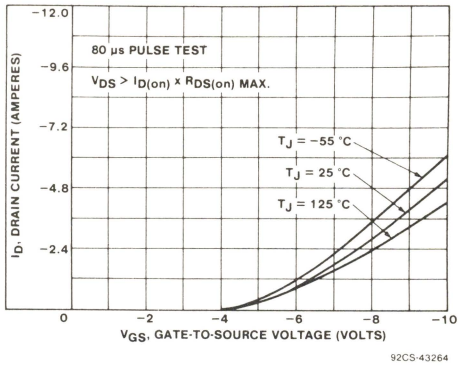


Fig. 2 - Typical Transfer Characteristics

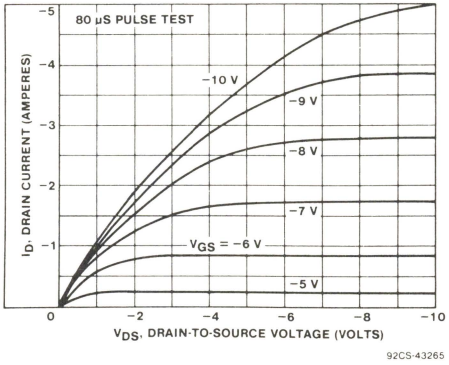


Fig. 3 - Typical Saturation Characteristics

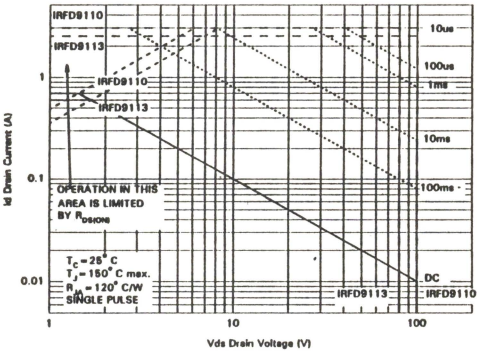


Fig. 4 - Maximum Safe Operating Area

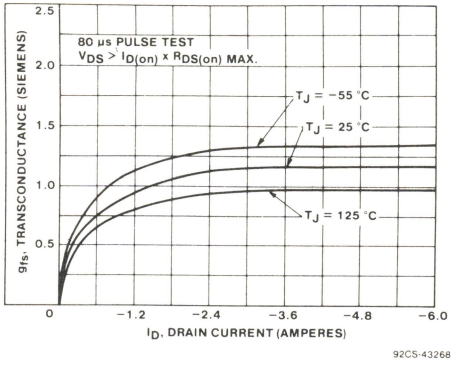


Fig. 5 - Typical Transconductance Vs. Drain Current

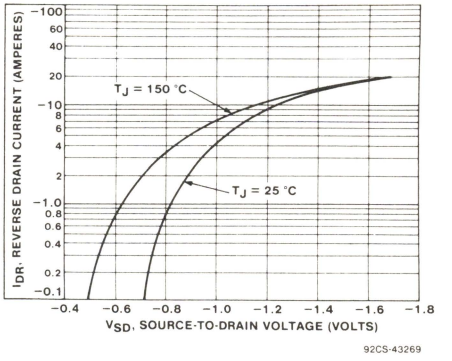


Fig. 6 - Typical Source-Drain Diode Forward Voltage

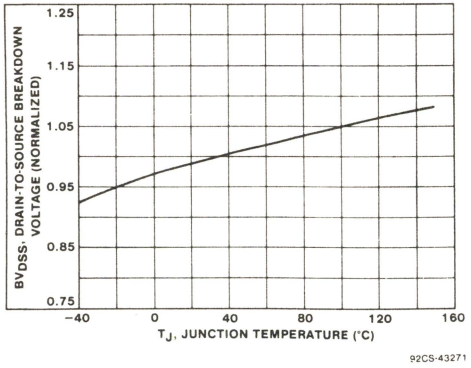


Fig. 7 - Breakdown Voltage Vs. Temperature

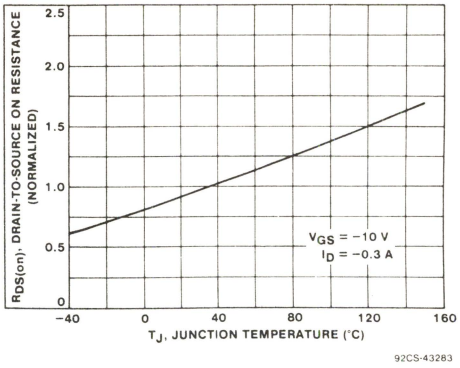


Fig. 8 - Normalized On-Resistance Vs. Temperature

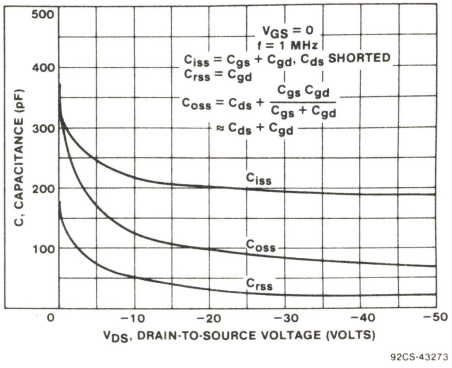


Fig. 9 - Typical Capacitance Vs. Drain-to-Source Voltage

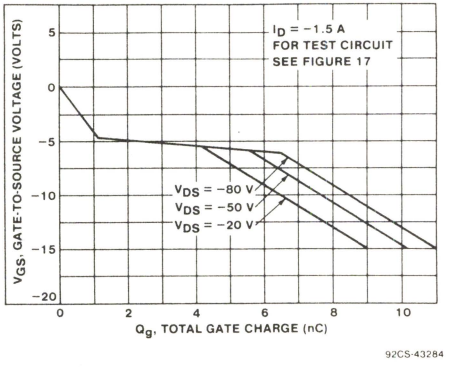


Fig. 10 - Typical Gate Charge Vs. Gate-to-Source Voltage

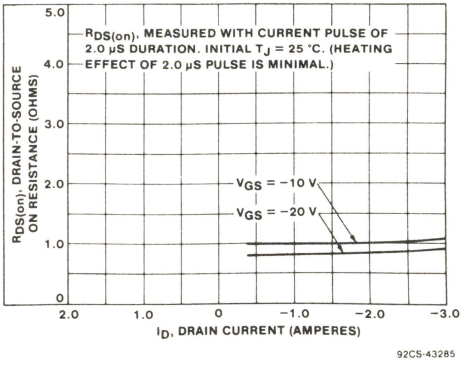


Fig. 11 - Typical On-Resistance Vs. Drain Current

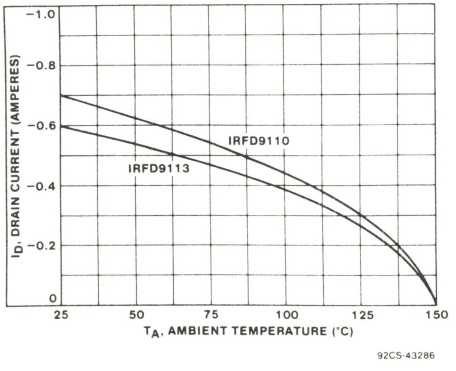


Fig. 12 - Maximum Drain Current Vs. Case Temperature

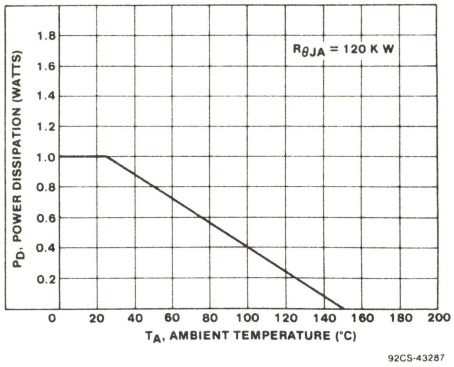


Fig. 13 - Power Vs. Temperature Derating Curve

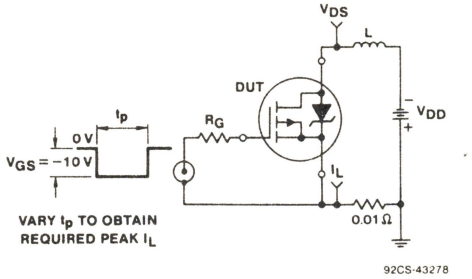


Fig. 14 - Unclamped Inductive Test Circuit

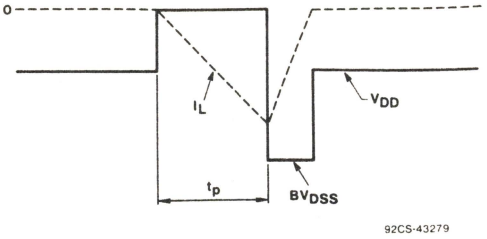


Fig. 15 - Unclamped Inductive Waveforms

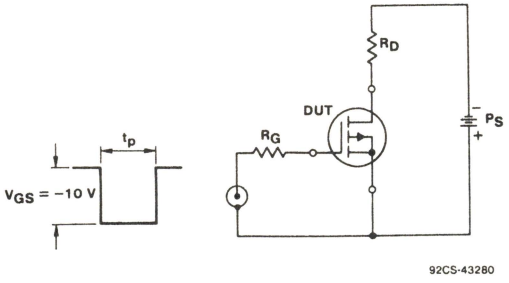


Fig. 16 - Switching Time Test Circuit

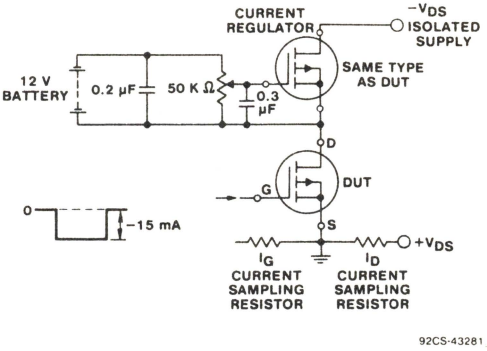


Fig. 17 - Gate Charge Test Circuit

HARRIS

IRFD9120
IRFD9123

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -1.0A and -0.8A, -80V and -100V
- $r_{DS(ON)}$ = 0.6Ω and 0.8Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

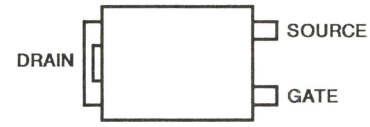
Description

The IRFD9120 and IRFD9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-Pin dual-in-line plastic package.

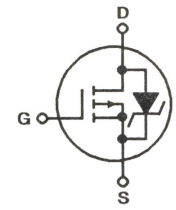
Package

4-PIN DUAL-IN-LINE
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFD9120	IRFD9123	UNITS
Drain-Source Voltage (1)	V_{DS}	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-100	-80	V
Continuous Drain Current T_C = 25°C	I_D	-1.0	-0.8	A
Pulsed Drain Current (3)	I_{DM}	-8.0	-6.4	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 13)	P_D	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	370	370	mJ
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

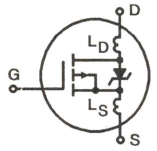
NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 555mH, R_G = 25Ω, Peak I_L = 1.0A (See Figures 14 and 15)

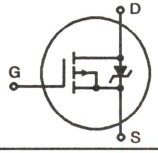
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
Copyright © Harris Corporation 1994

File Number **2285.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD9120	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFD9123			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFD9120	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-1.0	-	-	A
IRFD9123			-0.8	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD9120	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -0.8A	-	0.5	0.6	Ω
IRFD9123			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} < 50V, I_D = -0.8A	0.8	1.2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 9	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5, I_D = 1.0A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature.)	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -1.0A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	20	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from header to source bonding pad. 	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-1.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-8.0	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -1.0A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	150	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	-	0.9	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 555mH, R_G = 25Ω, Peak I_L = 1.0A (See Figures 14 and 15)

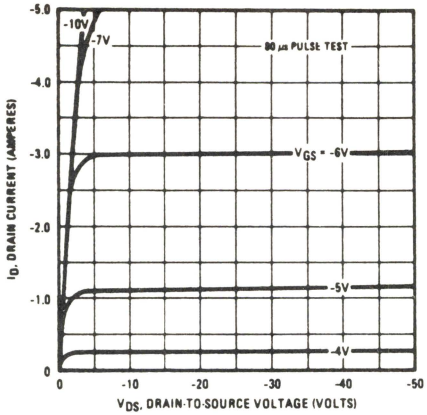


Fig. 1 - Typical output characteristics.

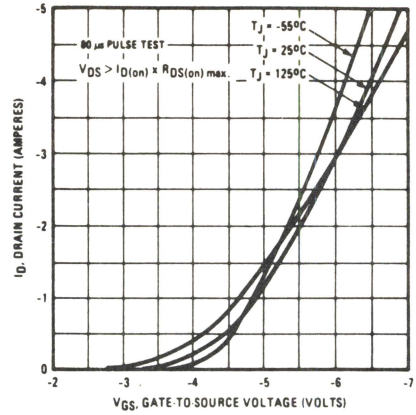


Fig. 2 - Typical transfer characteristics.

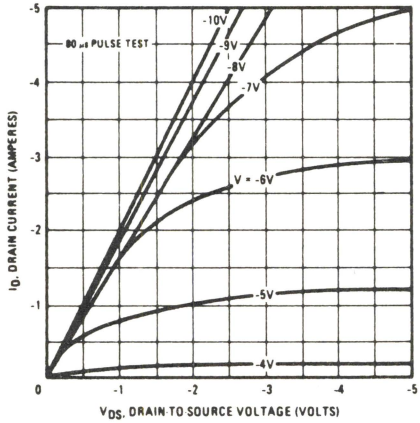


Fig. 3 - Typical saturation characteristics.

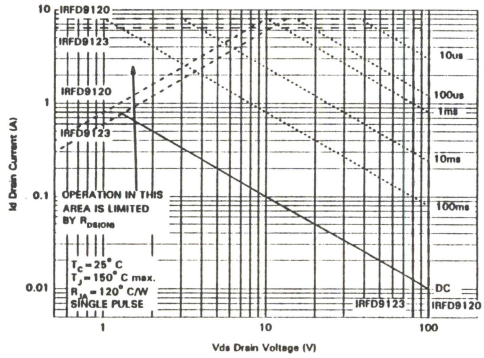


Fig. 4 - Maximum safe operating area.

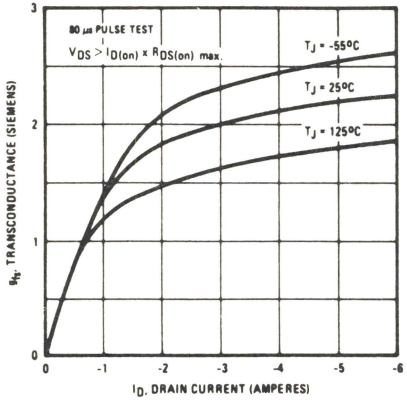


Fig. 5 - Typical transconductance vs. drain current.

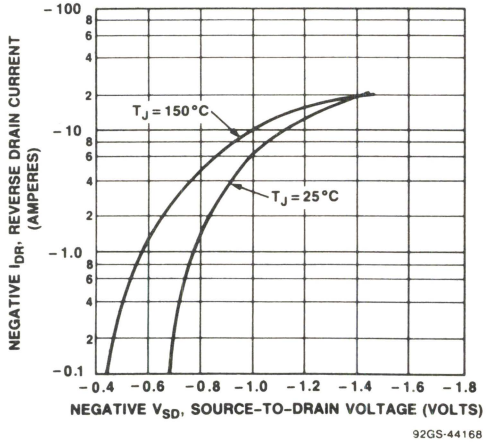


Fig. 6 - Typical source-drain diode forward voltage.

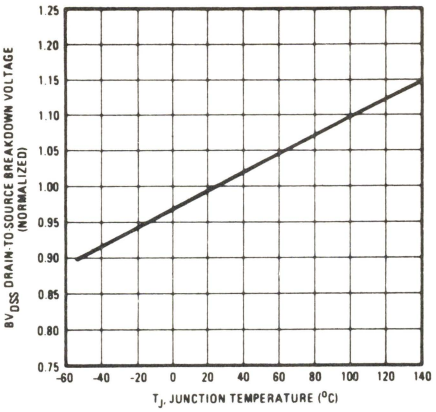


Fig. 7 - Breakdown voltage vs. temperature.

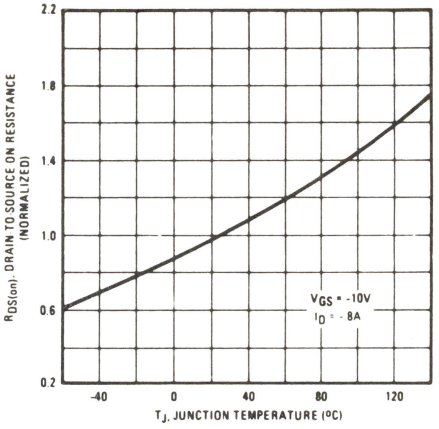


Fig. 8 - Normalized on-resistance vs. temperature.

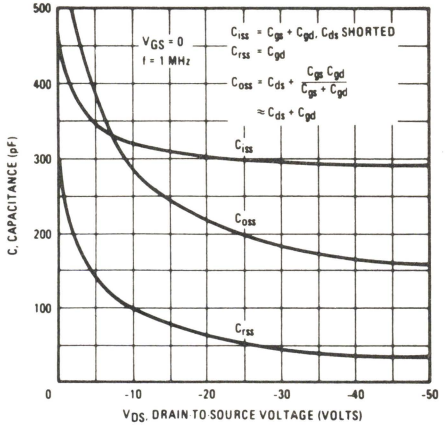


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

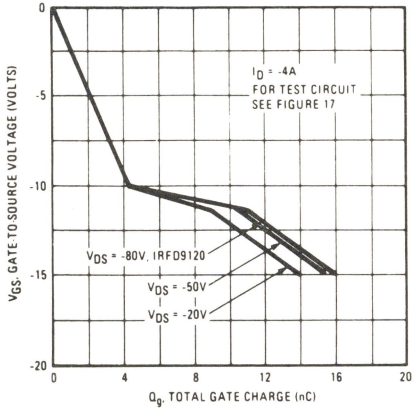


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

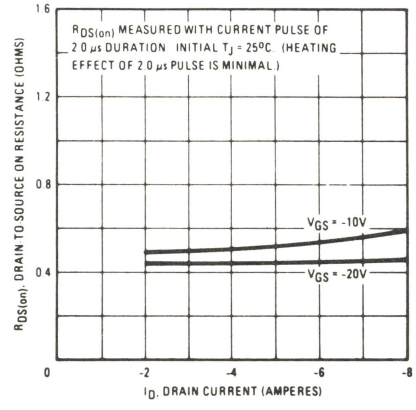


Fig. 11 - Typical on-resistance vs. drain current.

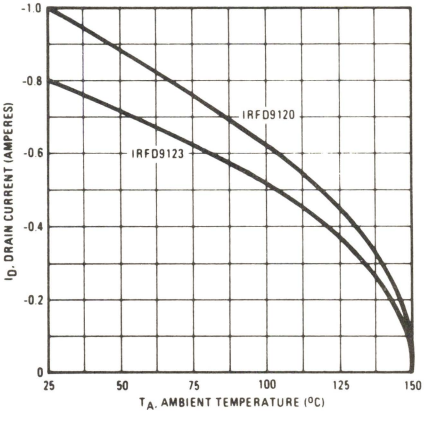


Fig. 12 - Maximum drain current vs. case temperature.

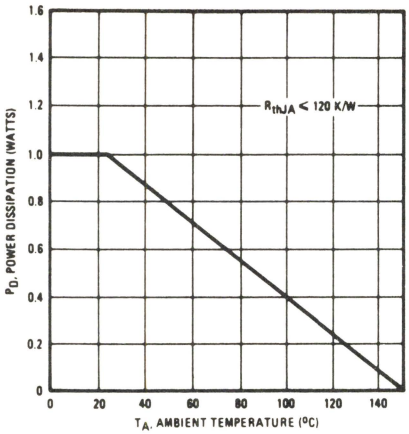


Fig. 13 - Power vs. temperature derating curve.

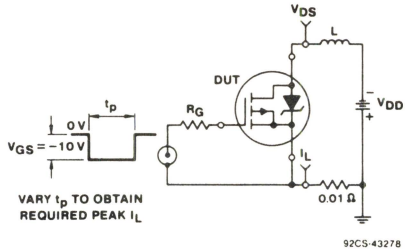


Fig. 14 - Unclamped inductive test circuit.

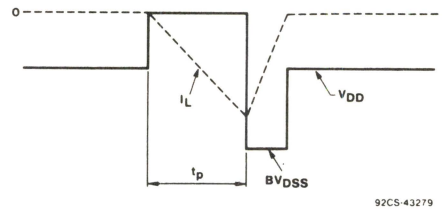


Fig. 15 - Unclamped inductive waveforms.

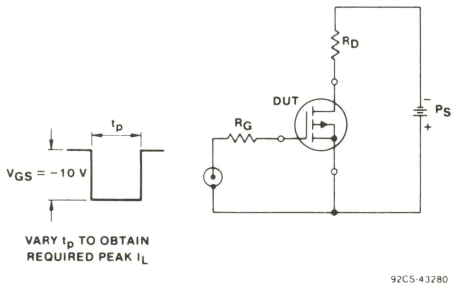


Fig. 16 - Switching time test circuit.

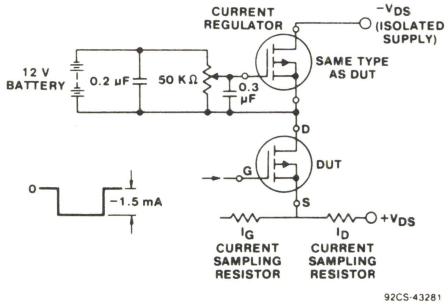


Fig. 17 - Gate charge test circuit.

HARRIS

IRFD9220
IRFD9223

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -0.45A and -0.6A, -150V and -200V
- $r_{DS(ON)}$ = 1.5Ω and 2.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

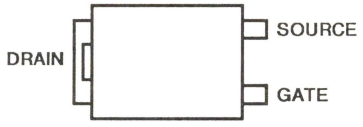
Description

The IRFD9220 and IRFD9223 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-Pin dual-in-line plastic package.

Package

4-PIN DUAL-IN-LINE
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		IRFD9220	IRFD9223	UNITS
Drain-Source Voltage (1)	V_{DS}	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1)	V_{DGR}	-200	-150	V
Continuous Drain Current T_C = 25°C	I_D	-0.6	-0.45	A
Pulsed Drain Current (3)	I_{DM}	-4.8	-3.6	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 13)	P_D	1.0	1.0	W
Linear Derating Factor (See Figure 13)		0.008	0.008	W/°C
Single Pulse Avalanche Energy Rating (4)	E_{as}	290	290	mJ
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 1210mH, R_G = 25Ω, Peak I_L = 0.6A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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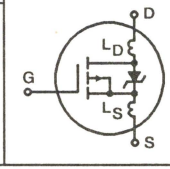
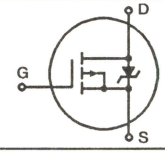
File Number 2286.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD9220	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRFD9223			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFD9220	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-0.6	-	-	A
IRFD9223			-0.45	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD9220	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -0.3A	-	1.0	1.5	Ω
IRFD9223			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≤ 50V, I_D = -0.3A	0.6	1.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 9	-	350	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5, I_D = 0.6A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature.)	-	15	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -0.6A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	10	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	4	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from header to source bonding pad. 	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-0.6	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-4.8	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -0.6A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -0.6A, dI_F/dt = 100A/μs	-	150	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -0.6A, dI_F/dt = 100A/μs	-	0.5	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 1210mH, R_G = 25Ω, Peak I_L = 0.6A (See Figures 14 and 15)

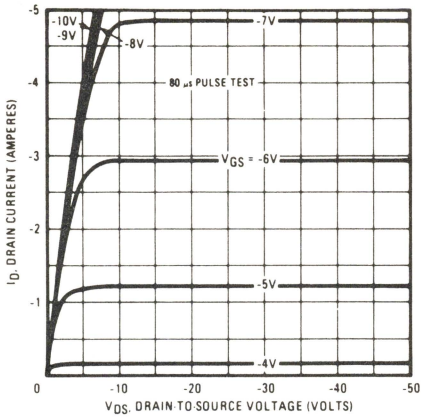


Fig. 1 - Typical output characteristics.

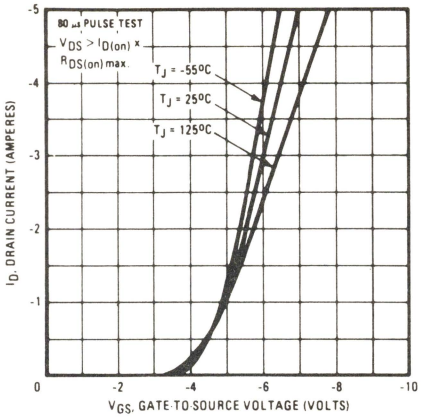


Fig. 2 - Typical transfer characteristics.

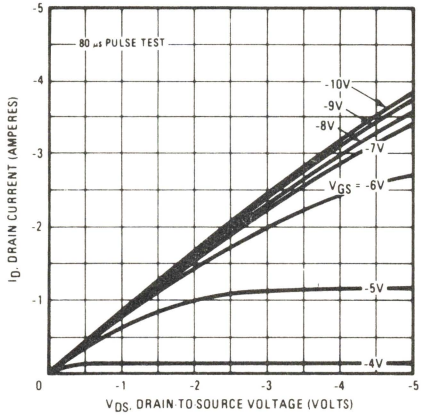


Fig. 3 - Typical saturation characteristics.

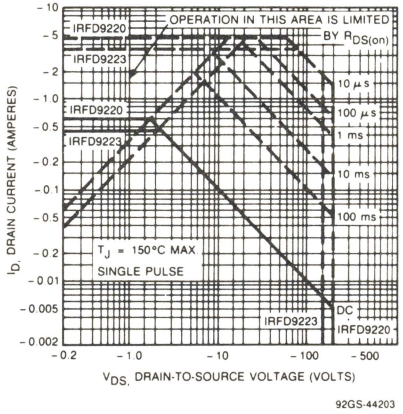


Fig. 4 - Maximum safe operating area.

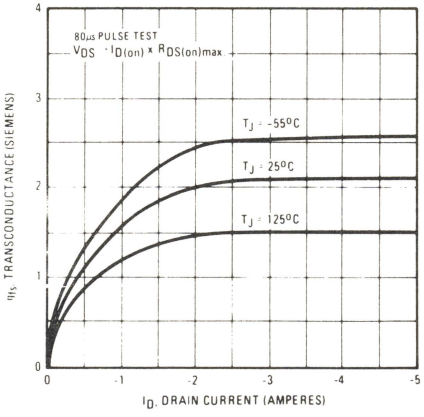


Fig. 5 - Typical transconductance vs. drain current.

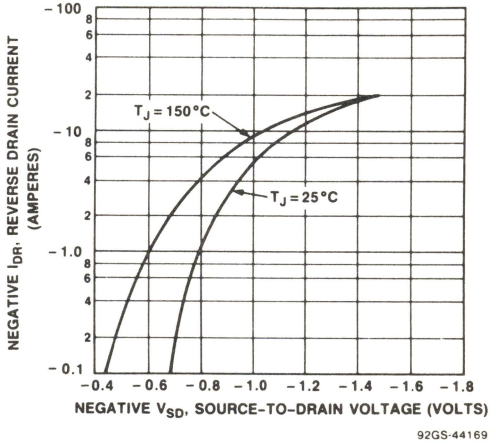


Fig. 6 - Typical source-drain diode forward voltage.

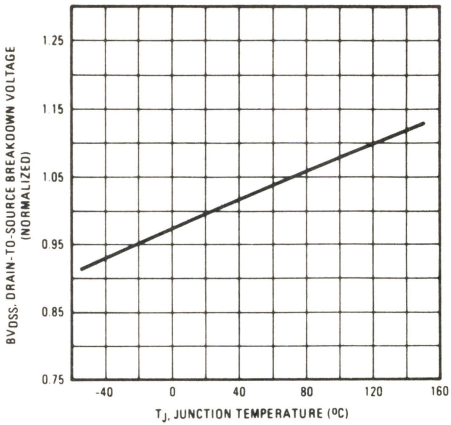


Fig. 7 - Breakdown voltage vs. temperature.

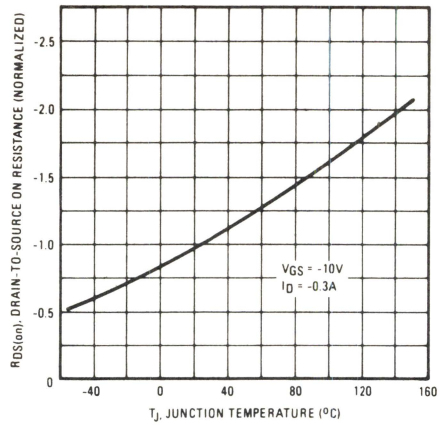


Fig. 8 - Normalized on-resistance vs. temperature.

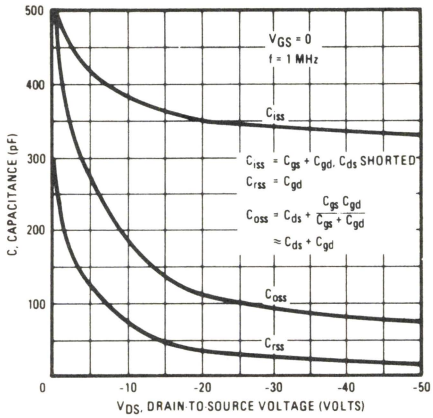


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

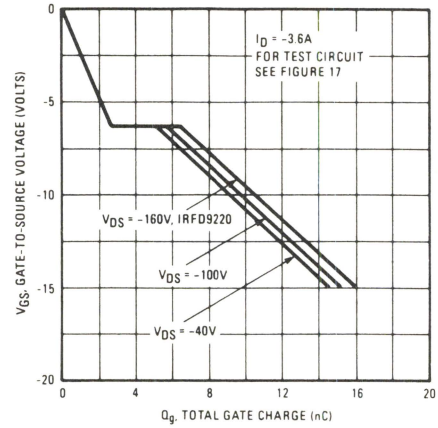


Fig. 10 - Typical gate charge vs. gate-to-source voltage.

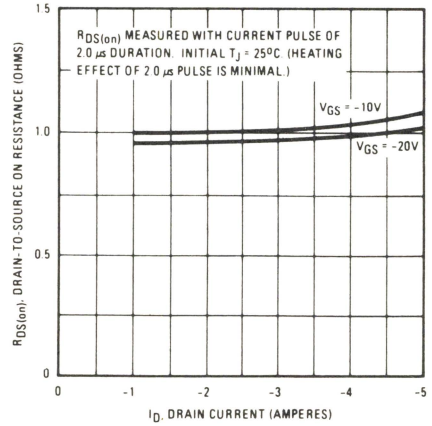


Fig. 11 - Typical on-resistance vs. drain current.

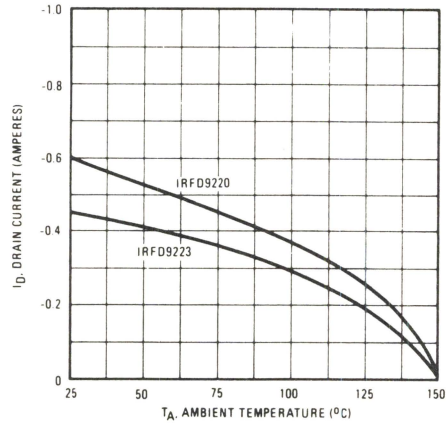


Fig. 12 - Maximum drain current vs. case temperature.

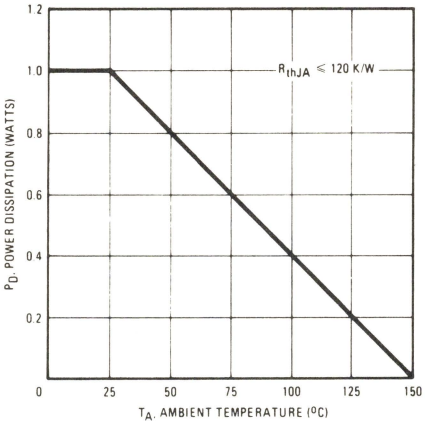


Fig. 13 - Power vs. temperature derating curve.

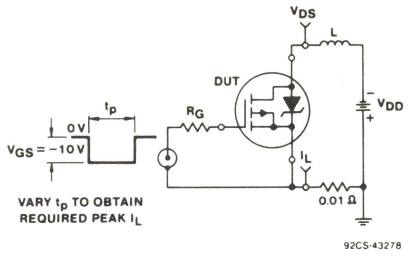


Fig. 14 - Unclamped inductive test circuit.

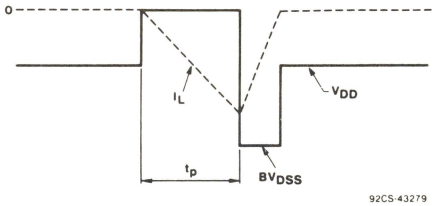


Fig. 15 - Unclamped inductive waveforms.

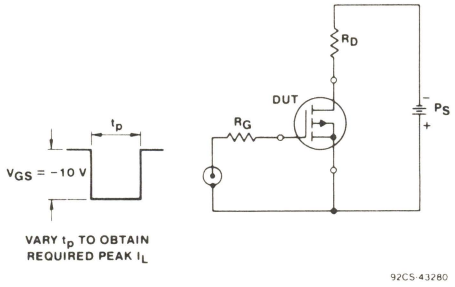


Fig. 16 - Switching time test circuit.

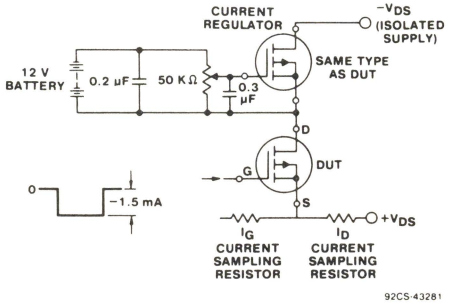


Fig. 17 - Gate charge test circuit.

HARRIS

IRFF9120, IRFF9121 IRFF9122, IRFF9123

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -3.5A and -4A, -80V and -100V
- $r_{DS(ON)}$ = 0.60Ω and 0.80Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

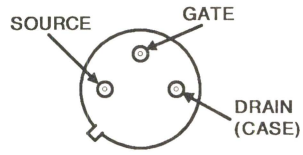
Description

The IRFF9120, IRFF9121, IRFF9122 and IRFF9123 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

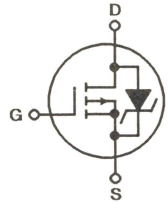
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFF9120	IRFF9121	IRFF9122	IRFF9123	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current T_C = 25°C ..... I_D	-4	-4	-3.5	-3.5	A
Pulsed Drain Current (3) ..... I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	20	20	20	20	W
Linear Derating Factor ..... (See Figure 14)	0.16	0.16	0.16	0.16	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	370	370	370	370	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 34.7mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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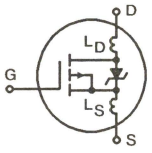
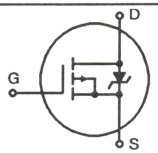
File Number **2287.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9120, IRFF9122	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFF9121, IRFF9123			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9120, IRFF9121	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-4	-	-	A
IRFF9122, IRFF9123			-3.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9120, IRFF9121	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -2A	-	0.5	0.6	Ω
IRFF9122, IRFF9123			-	0.6	0.8	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -2A	1.25	2	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	300	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -4A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	25	50	ns
Rise Time	t_r		-	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	50	100	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -4A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-4	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-16	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -4A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 4A, dI_F/dt = 100A/μs	-	230	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4A, dI_F/dt = 100A/μs	-	1.3	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 34.7mH, R_G = 25Ω, Peak I_L = 4A (See Figures 15 and 16)

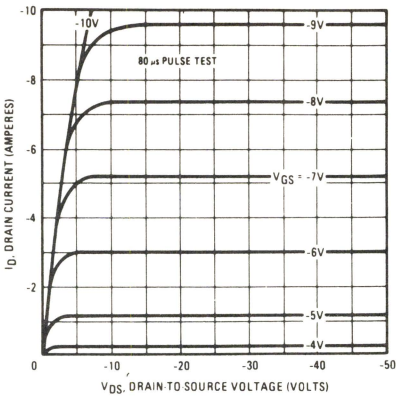


Fig. 1 - Typical output characteristics.

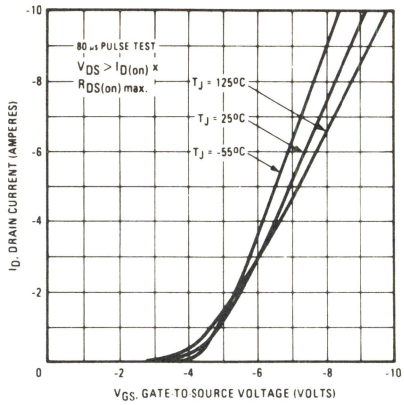


Fig. 2 - Typical transfer characteristics.

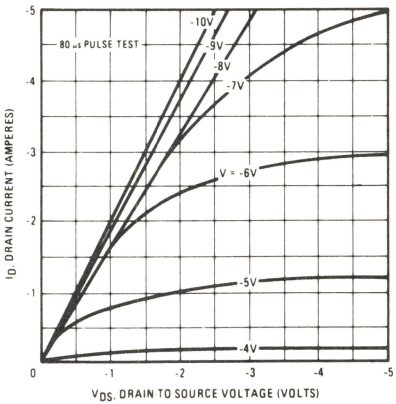


Fig. 3 - Typical saturation characteristics.

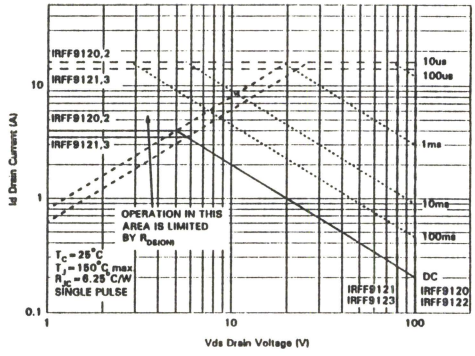


Fig. 4 - Maximum safe operating area.

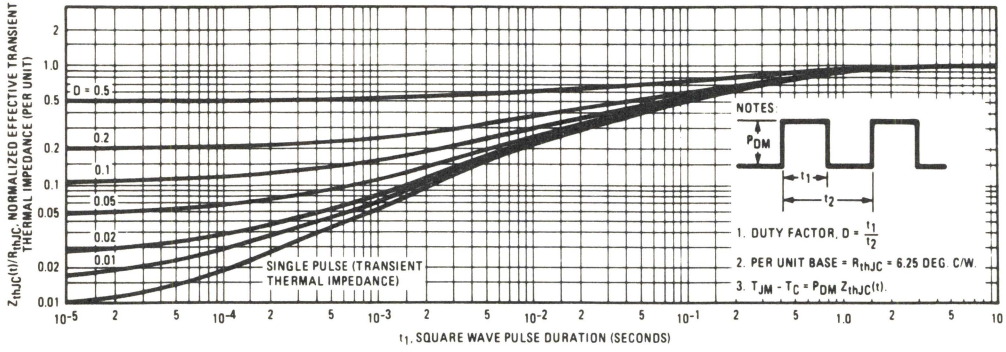


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

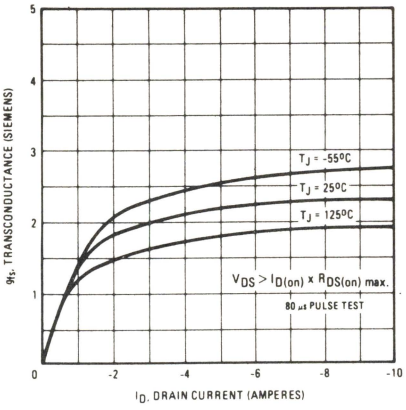


Fig. 6 - Typical transconductance vs. drain current.

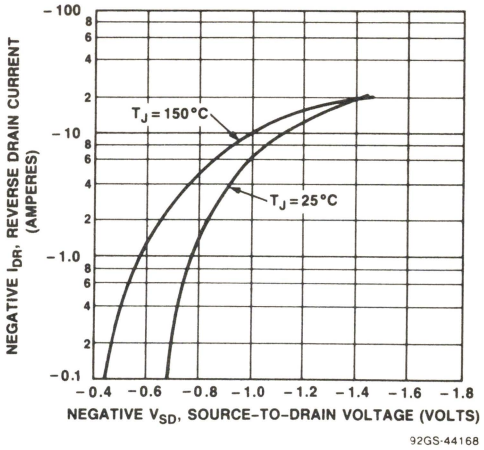


Fig. 7 - Typical source-drain diode forward voltage.

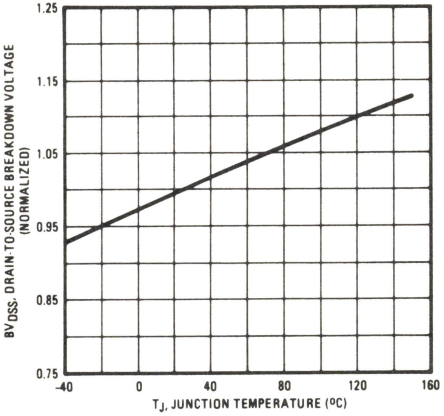


Fig. 8 - Breakdown voltage vs. temperature.

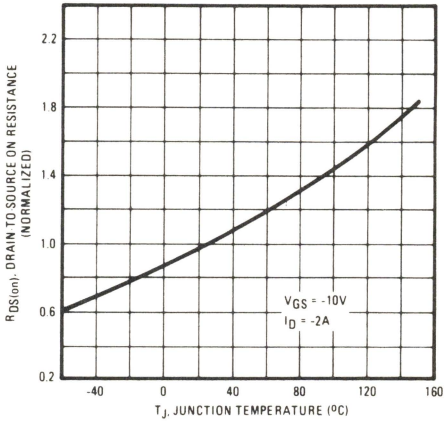


Fig. 9 - Normalized on-resistance vs. temperature.

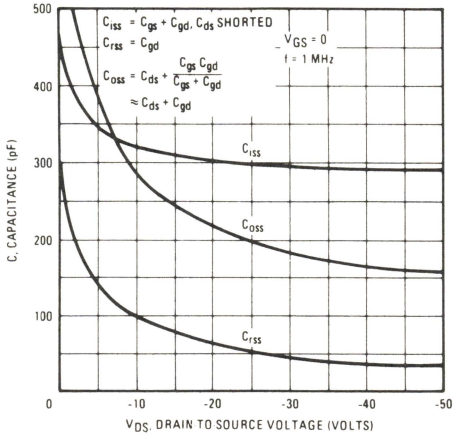


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

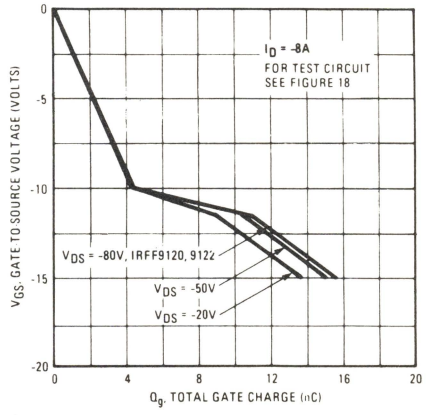


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

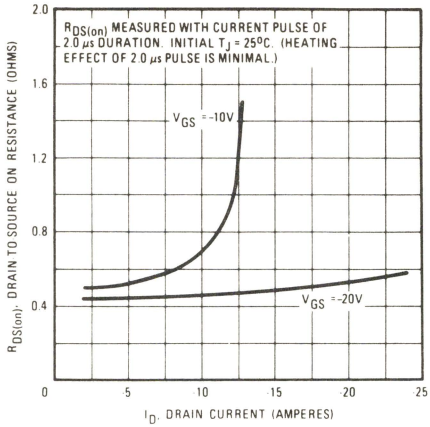


Fig. 12 - Typical on-resistance vs. drain current.

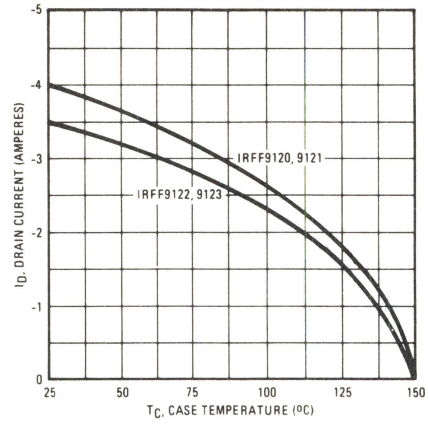


Fig. 13 - Maximum drain current vs. case temperature.

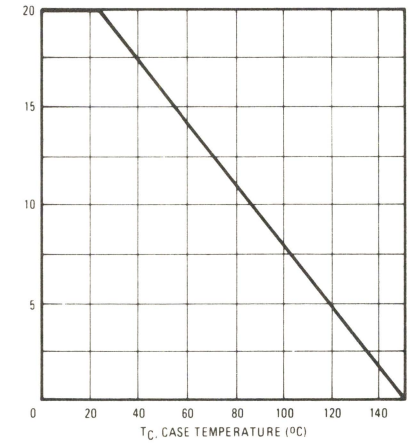


Fig. 14 - Power vs. temperature derating curve.

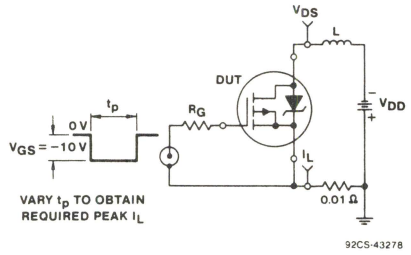


Fig. 15 - Unclamped inductive test circuit.

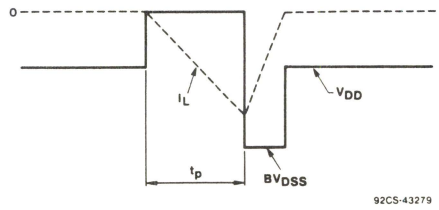


Fig. 16 - Unclamped inductive waveforms.

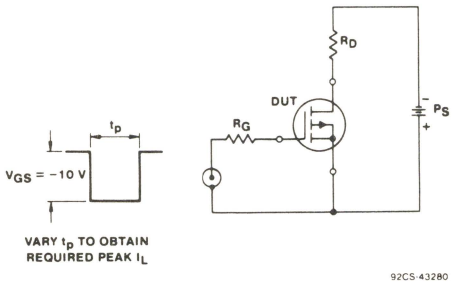


Fig. 17 - Switching time test circuit.

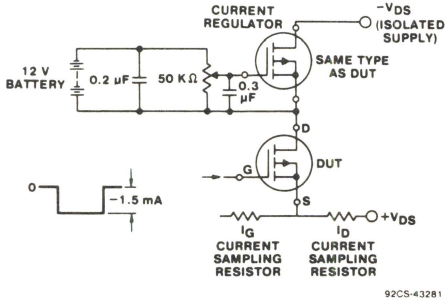


Fig. 18 - Gate charge test circuit.

IRFF9130, IRFF9131 IRFF9132, IRFF9133

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -5.5A and -6.5A, -80V and -100V
- $r_{DS(ON)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

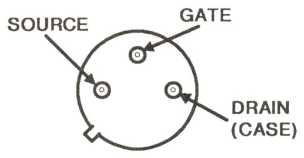
Description

The IRFF9130, IRFF9131, IRFF9132 and IRFF9133 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFF9130	IRFF9131	IRFF9132	IRFF9133	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current T_C = 25°C ..... I_D	-6.5	-6.5	-5.5	-5.5	A
Pulsed Drain Current (3) ..... I_{DM}	-26	-26	-22	-22	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	25	25	25	25	W
Linear Derating Factor ..... (See Figure 14)	0.2	0.2	0.2	0.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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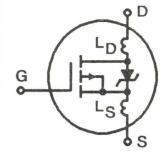
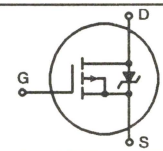
File Number 2216.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9130, IRFF9132	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFF9131, IRFF9133			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9130, IRFF9131	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-6.5	-	-	A
IRFF9132, IRFF9133			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9130, IRFF9131	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -3A	-	0.25	0.3	Ω
IRFF9132, IRFF9133			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -3A	2.5	3.5	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	500	-	pF
Output Capacitance	C_{OSS}		-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -6.5A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	60	ns
Rise Time	t_r		-	70	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -6.5A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -6.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -6.5A, dI_F/dt = 100A/μs	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 25V, Start T_J = +25°C, L = 17.75mH, R_G = 25Ω, Peak I_L = 6.5A (See Figures 15 and 16)

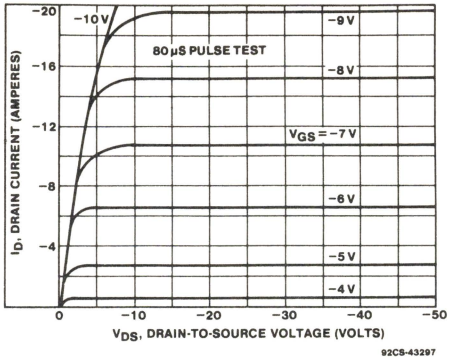


Fig. 1 - Typical Output Characteristics

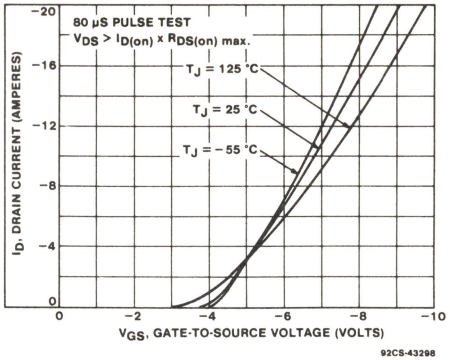


Fig. 2 - Typical Transfer Characteristics

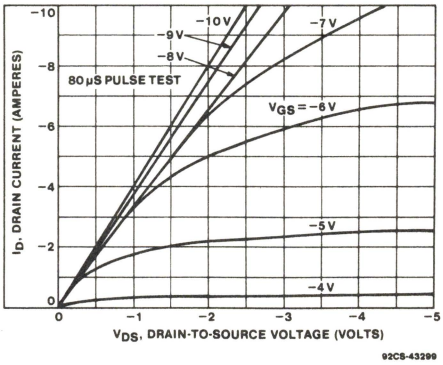


Fig. 3 - Typical Saturation Characteristics

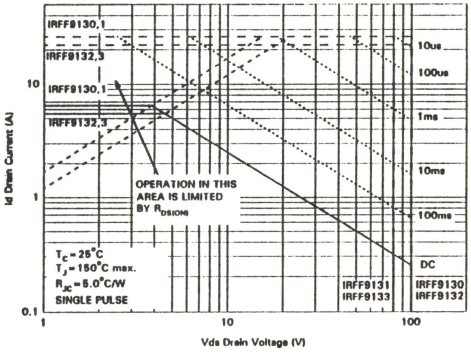


Fig. 4 - Maximum Safe Operating Area

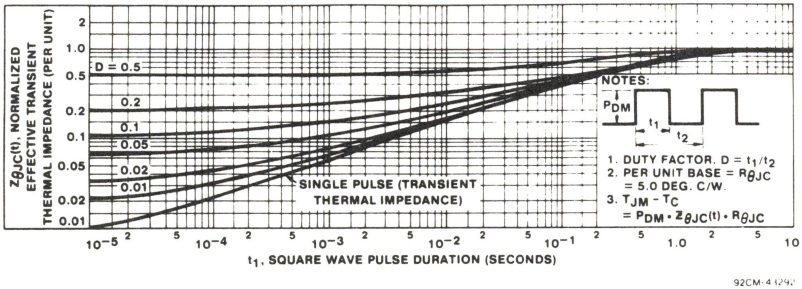


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

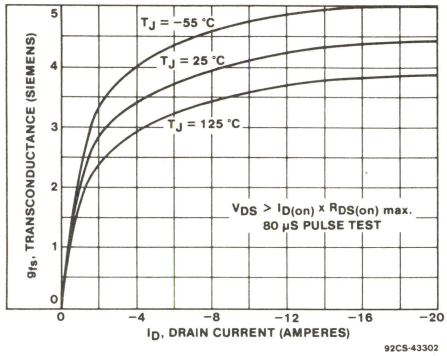


Fig. 6 - Typical Transconductance Vs. Drain Current

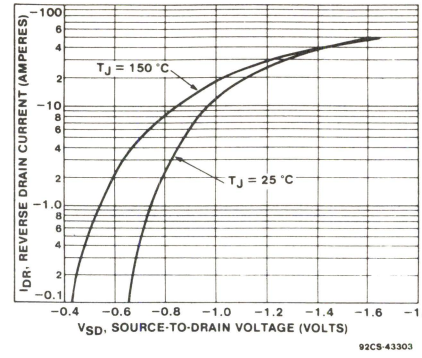


Fig. 7 - Typical Source-Drain Diode Forward Voltage

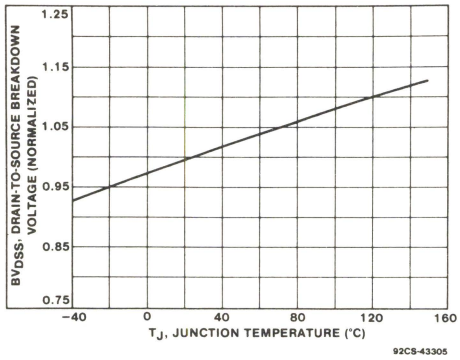


Fig. 8 - Breakdown Voltage Vs. Temperature

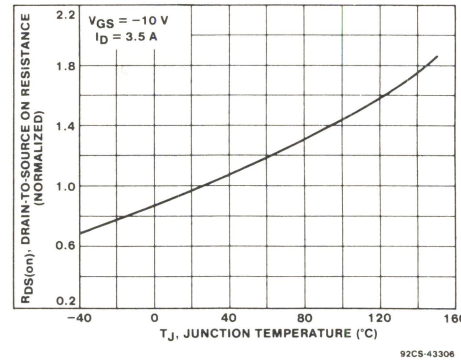


Fig. 9 - Normalized On-Resistance Vs. Temperature

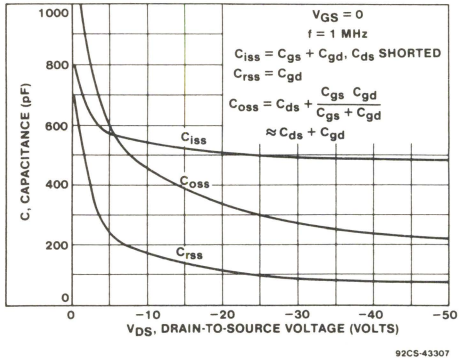


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

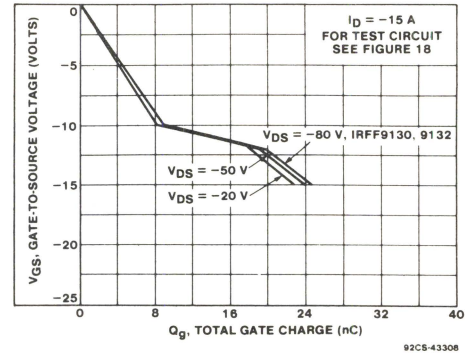


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

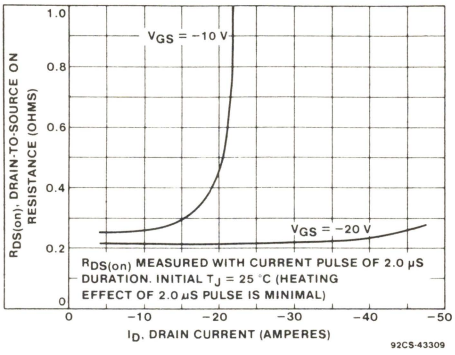


Fig. 12 - Typical On-Resistance Vs. Drain Current

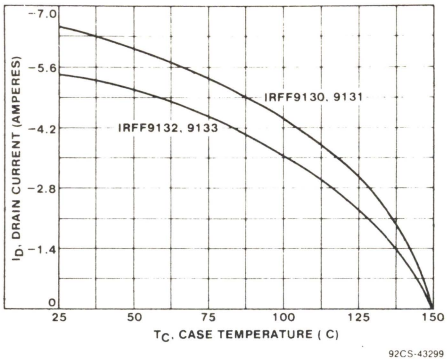


Fig. 13 - Maximum Drain Current Vs. Case Temperature

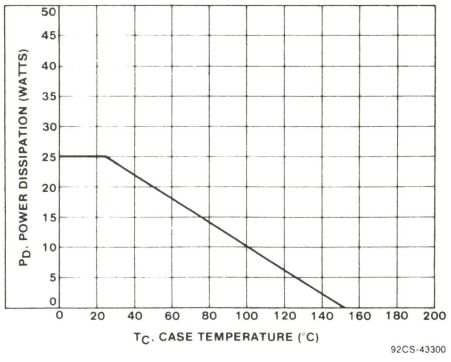


Fig. 14 - Power Vs. Temperature Derating Curve

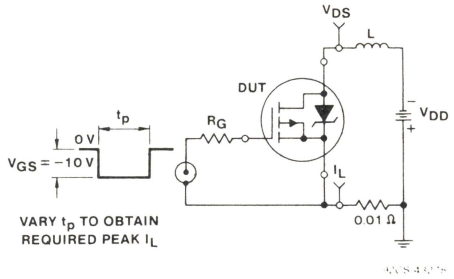


Fig. 15 - Unclamped Inductive Test Circuit

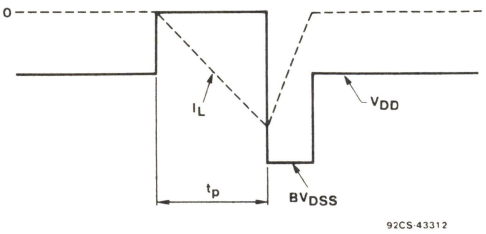


Fig. 16 - Unclamped Inductive Waveforms

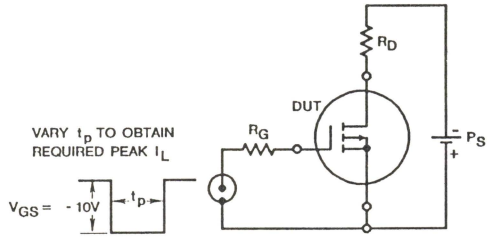


Fig. 17 - Switching Time Test Circuit

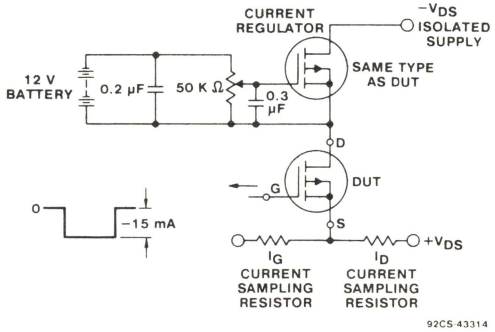


Fig. 18 - Gate Charge Test Circuit

HARRIS

IRFF9220, IRFF9221 IRFF9222, IRFF9223

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -2A and -2.5A, -150V and -200V
- $r_{DS(ON)}$ = 1.50Ω and 2.40Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

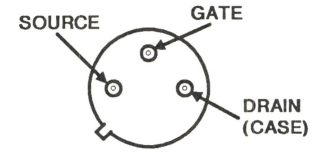
Description

The IRFF9220, IRFF9221, IRFF9222 and IRFF9223 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

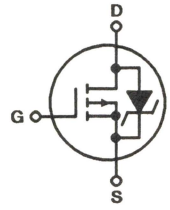
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFF9220	IRFF9221	IRFF9222	IRFF9223	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current T_C = 25°C ..... I_D	-2.5	-2.5	-2.0	-2.0	A
Pulsed Drain Current (3) ..... I_{DM}	-10	-10	-8	-8	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	20	20	20	20	W
Linear Derating Factor ..... (See Figure 14)	0.16	0.16	0.16	0.16	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	290	290	290	290	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 69.6mH, R_G = 25Ω, Peak I_L = 2.5A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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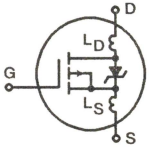
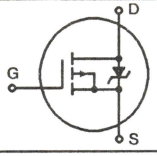
File Number **2288**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9220, IRFF9222	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRFF9221, IRFF9223			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFF9220, IRFF9221	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-2.5	-	-	A
IRFF9222, IRFF9223			-2.0	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFF9220, IRFF9221	$r_{DS(ON)}$	V_{GS} = -10V, I_D = 1.5A	-	1.0	1.5	Ω
IRFF9222, IRFF9223			-	1.5	2.4	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 1.5A	1	1.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	350	-	pF
Output Capacitance	C_{OSS}		-	100	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -2.5A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	15	40	ns
Rise Time	t_r		-	25	50	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -2.5V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	16	22	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	7	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	-	15	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	6.25	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-2.5	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-10	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -2.5A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -2.5A, dI_F/dt = 100A/μs	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -2.5A, dI_F/dt = 100A/μs	-	1.9	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 69.6mH, R_G = 25Ω, Peak I_L = 2.5A (See Figures 15 and 16)

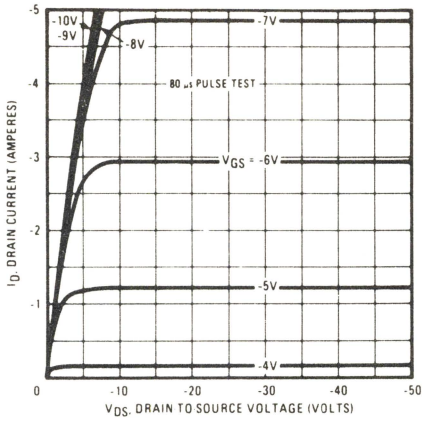


Fig. 1 - Typical output characteristics.

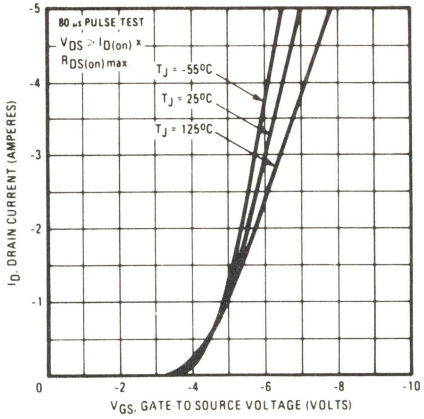


Fig. 2 - Typical transfer characteristics.

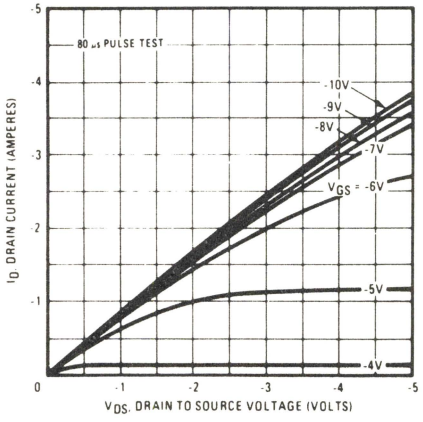


Fig. 3 - Typical saturation characteristics.

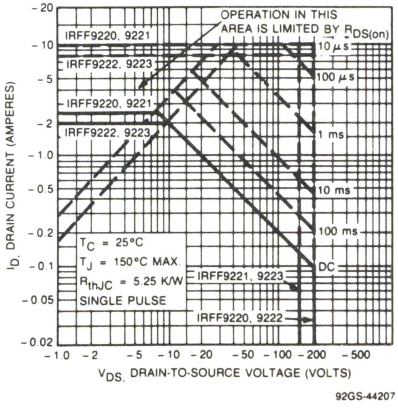


Fig. 4 - Maximum safe operating area.

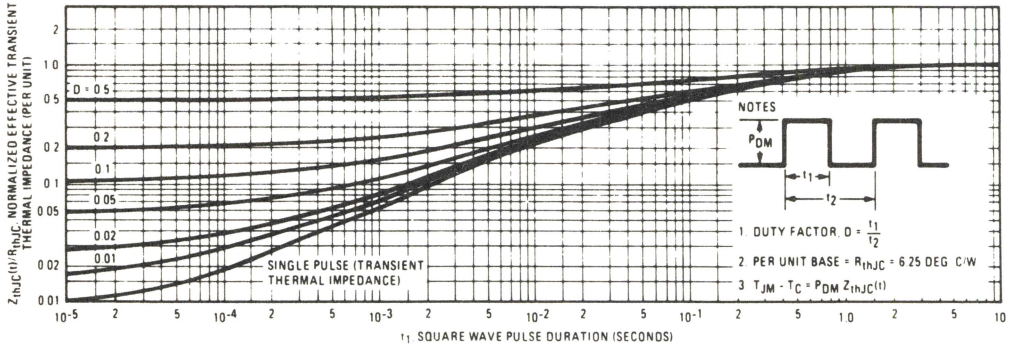


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

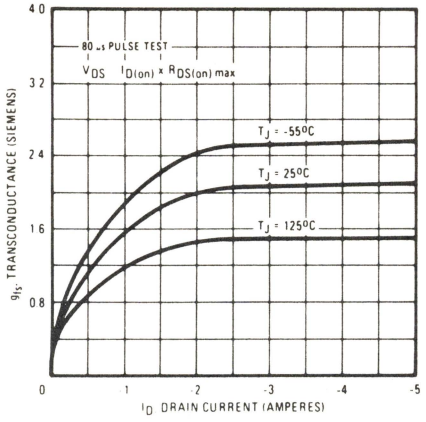


Fig. 6 - Typical transconductance vs. drain current.

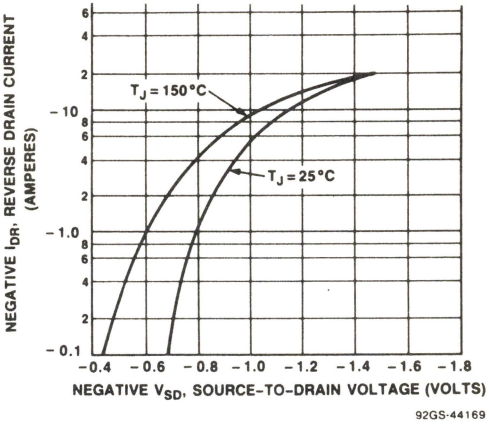


Fig. 7 - Typical source-drain diode forward voltage.

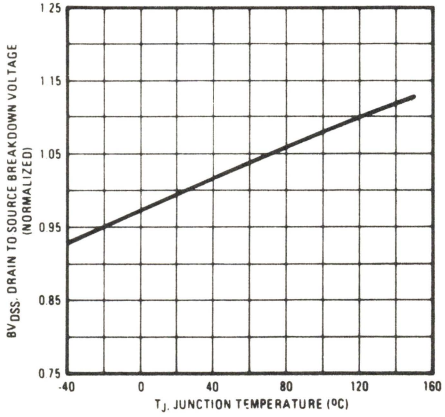


Fig. 8 - Breakdown voltage vs. temperature.

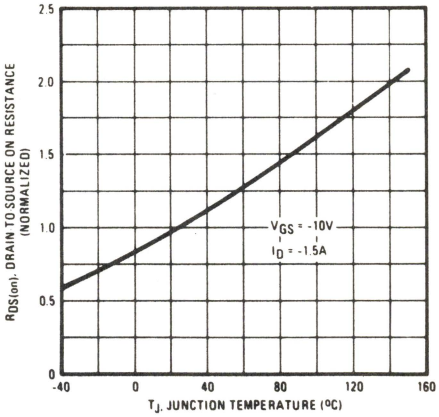


Fig. 9 - Normalized on-resistance vs. temperature.

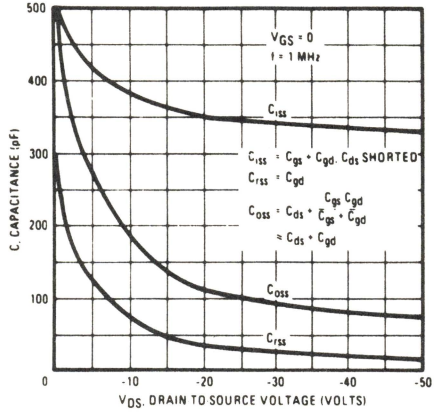


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

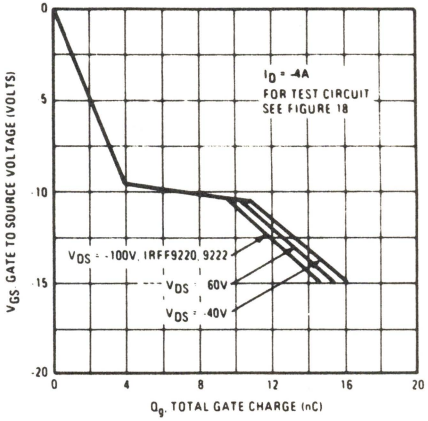


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

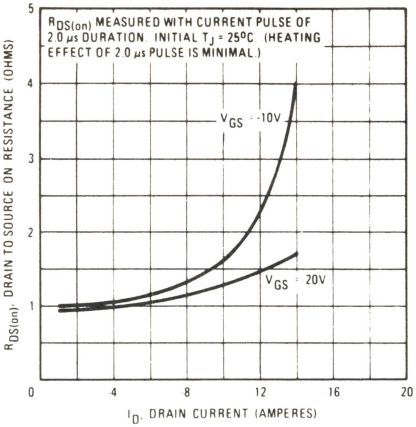


Fig. 12 - Typical on-resistance vs. drain current.

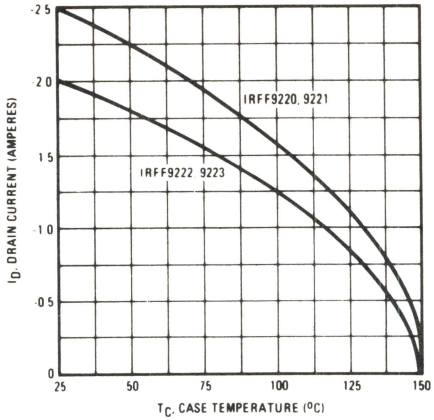


Fig. 13 - Maximum drain current vs. case temperature.

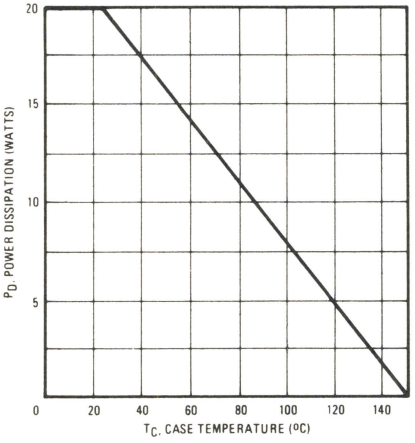


Fig. 14 - Power vs. temperature derating curve.

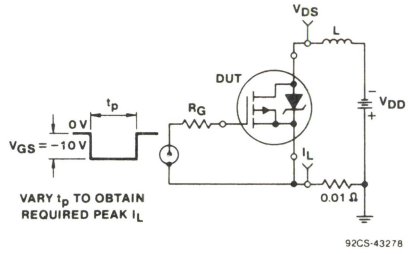


Fig. 15 - Unclamped inductive test circuit.

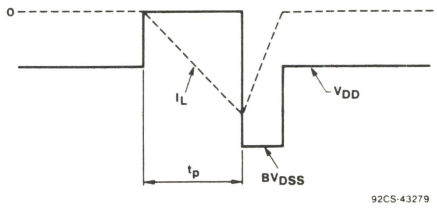


Fig. 16 - Unclamped inductive waveforms.

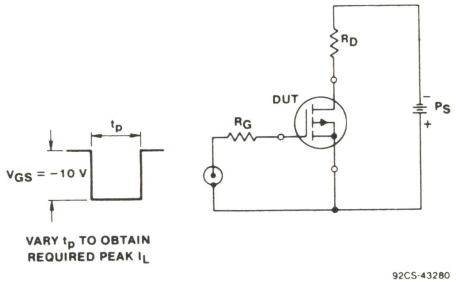


Fig. 17 - Switching time test circuit.

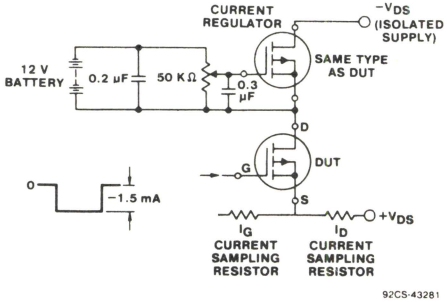


Fig. 18 - Gate charge test circuit.

IRFF9230, IRFF9231 IRFF9232, IRFF9233

Avalanche Energy Rated P-Channel Power MOSFETs

August 1991

Features

- -3.5A and -4.0A, -150V and -200V
- $r_{DS(ON)}$ = 0.8Ω and 1.20Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

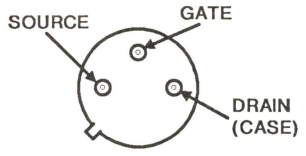
Description

The IRFF9230, IRFF9231, IRFF9232 and IRFF9233 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF types are supplied in the JEDEC TO-205AF (Low Profile TO-39) metal package.

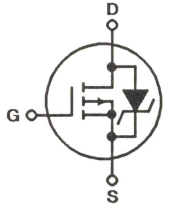
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	IRFF9230	IRFF9231	IRFF9232	IRFF9233	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current T_C = 25°C ..... I_D	-4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3) ..... I_{DM}	-16	-16	-14	-14	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	25	25	25	25	W
Linear Derating Factor ..... (See Figure 14)	0.2	0.2	0.2	0.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	500	500	500	500	mJ
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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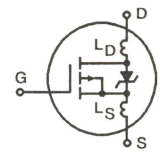
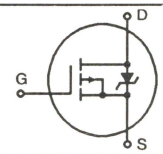
File Number 2225

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFF9230, IRFF9232	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	–	–	V
IRFF9231, IRFF9233			-150	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	–	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	–	–	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	–	–	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	–	–	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	–	–	-1000	μA
On-State Drain Current (Note 2) IRFF9230, IRFF9231	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-4.0	–	–	A
IRFF9232, IRFF9233			-3.5	–	–	A
Static Drain-Source On-State Resistance (Note 2) IRFF9230, IRFF9231	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -2.0A	–	0.5	0.8	Ω
IRFF9232, IRFF9233			–	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = -2.0A	2.2	3.5	–	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	–	550	–	pF
Output Capacitance	C_{OSS}		–	170	–	pF
Reverse Transfer Capacitance	C_{RSS}		–	50	–	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} =0.5 BV_{DSS}, I_D = -4.0A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	–	30	50	ns
Rise Time	t_r		–	50	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		–	50	100	ns
Fall Time	t_f		–	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -4.0V$_{DS}$ = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	–	31	45	nC
Gate-Source Charge	Q_{gs}		–	18	–	nC
Gate-Drain ("Miller") Charge	Q_{gd}		–	13	–	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 5mm (0.2") from header to center of die. Modified MOSFET symbol showing the internal device inductances.	–	5.0	–	nH
Internal Source Inductance	L_S	Measured from the source lead, 5mm (0.2") from header to source bonding pad. 	–	15	–	nH
Junction-to-Case	$R_{\theta JC}$		–	–	5.0	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	–	–	175	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	–	–	-4.0	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		–	–	-16	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = -4.0A, V_{GS} = 0V	–	–	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	–	400	–	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = -4.0A, dI_F/dt = 100A/μs	–	2.6	–	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	–	–	–	–

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 46.9mH, R_G = 25Ω, Peak I_L = 4.0A (See Figures 15 and 16)

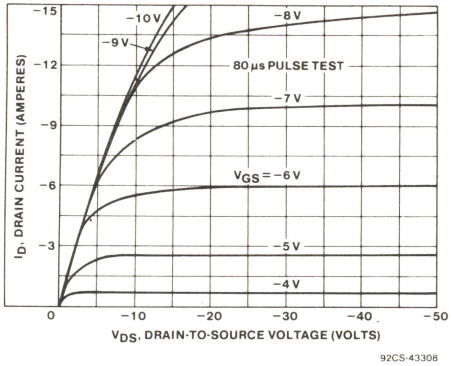


Fig. 1 - Typical output characteristics.

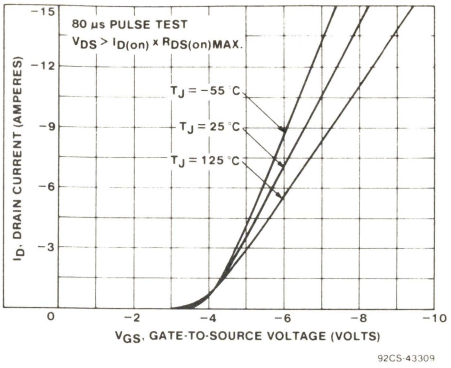


Fig. 2 - Typical transfer characteristics.

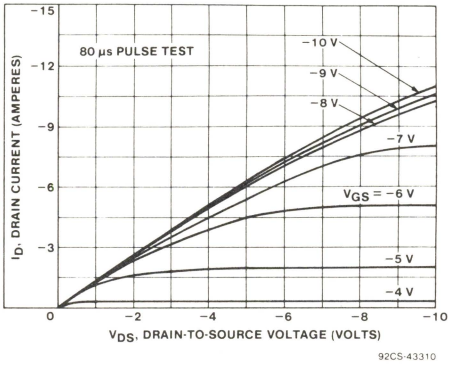


Fig. 3 - Typical saturation characteristics.

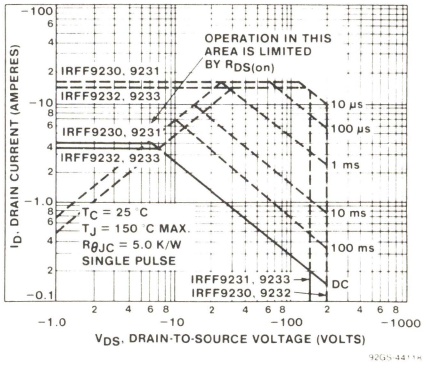


Fig. 4 - Maximum safe operating area.

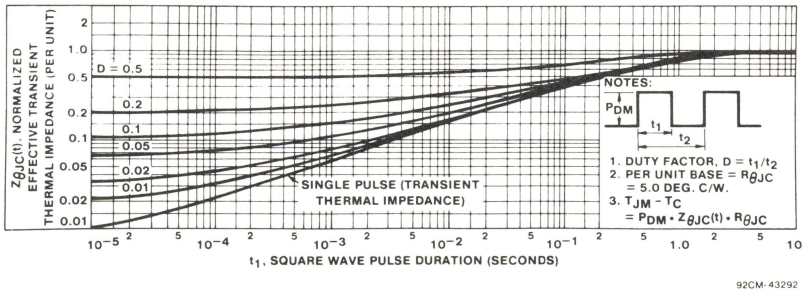


Fig. 5 - Maximum effective transient thermal impedance, junction-

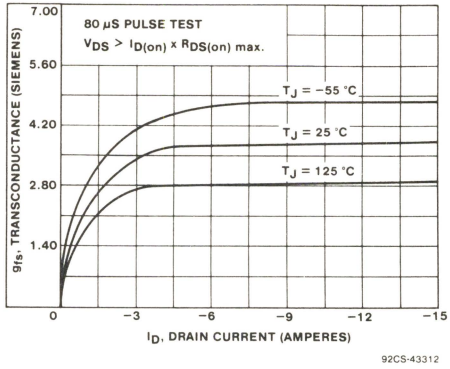


Fig. 6 - Typical transconductance vs. drain current.

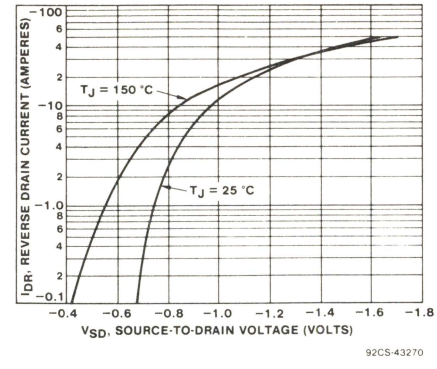


Fig. 7 - Typical source-drain diode forward voltage.

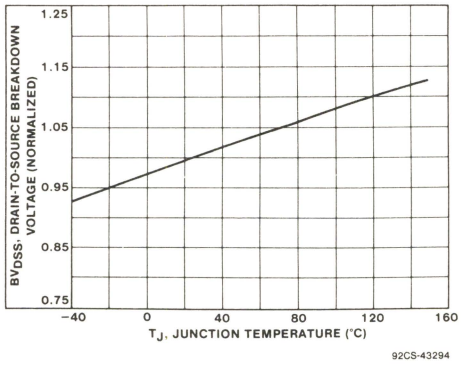


Fig. 8 - Breakdown voltage vs. temperature.

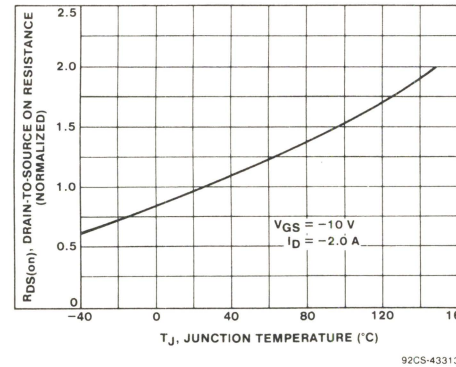


Fig. 9 - Normalized on-resistance vs. temperature.

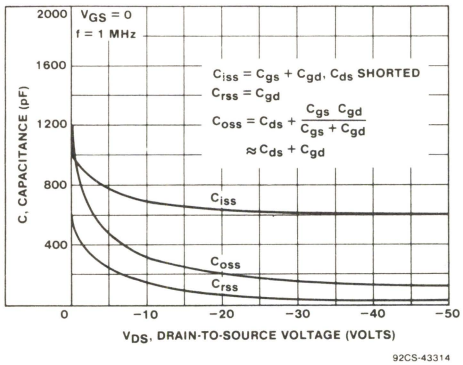


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

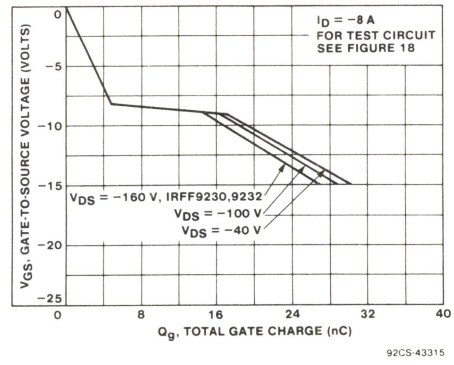


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

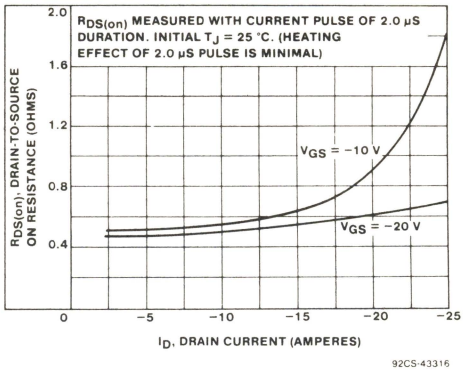


Fig. 12 - Typical on-resistance vs. drain current.

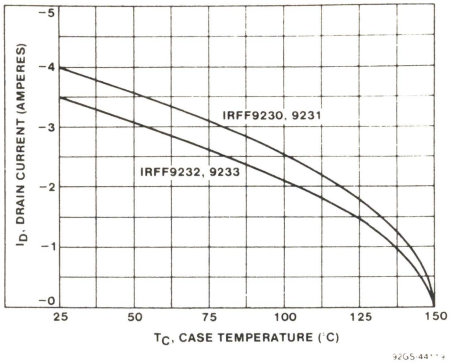


Fig. 13 - Maximum drain current vs. case temperature.

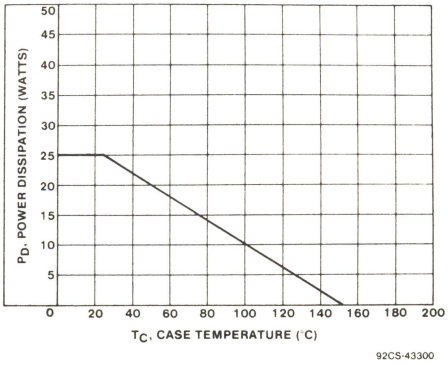


Fig. 14 - Power vs. temperature derating curve.

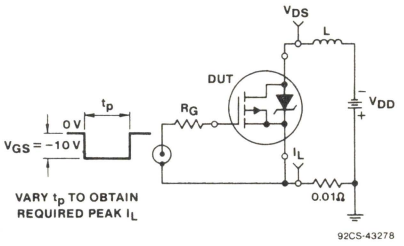


Fig. 15 - Unclamped inductive test circuit.

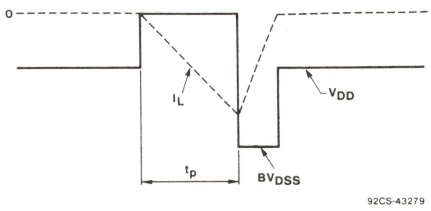


Fig. 16 - Unclamped inductive waveforms.

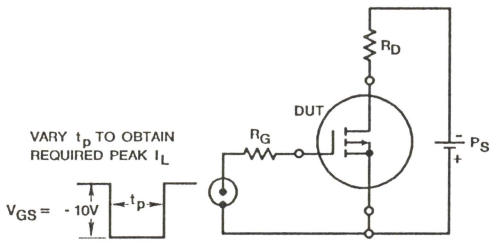


Fig. 17 - Switching time test circuit.

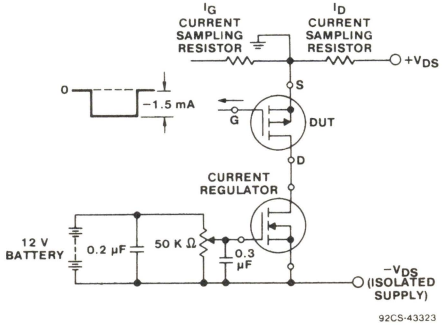


Fig. 18 - Gate charge test circuit.

HARRIS

IRFP9140/P9141
IRFP9142/P9143

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -19A and -16A, -80V and -100V
- $r_{DS(ON)}$ = 0.20Ω and 0.30Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

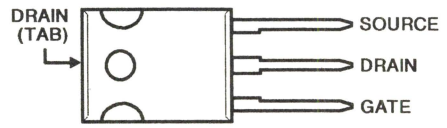
Description

The IRFP9140, IRFP9141, IRFP9142 and IRFP9143 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP9140	IRFP9141	IRFP9142	IRFP9143	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-100	-80	-100	-80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-100	-80	-100	-80	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-19	-19	-16	-16	A
T_C = 100°C ..... I_D	-12	-12	-10	-10	A
Pulsed Drain Current (3) ..... I_{DM}	-76	-76	-64	-64	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	150	150	150	150	W
Linear Derating Factor ..... (See Figure 14)	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	960	960	960	960	mJ
Operating and Storage Junction ..... TJ, TSTG Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.2mHμ, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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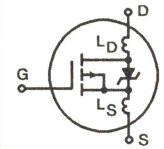
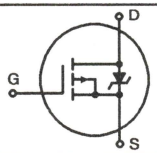
File Number 2292.2

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP9140, IRFP9142	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFP9141, IRFP9143			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	μA
On-State Drain Current (Note 2) IRFP9140, IRFP9141	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = -10V	-19	-	-	A
IRFP9142, IRFP9143			-16	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP9140, IRFP9141	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.14	0.20	Ω
IRFP9142, IRFP9143			-	0.20	0.30	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≤ -50V, I_D = -10A	5.3	7.9	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1200	-	pF
Output Capacitance	C_{OSS}		-	570	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -50V, I_D = -19A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	20	ns
Rise Time	t_r		-	65	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	70	ns
Fall Time	t_f		-	28	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -19A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	37	55	nC
Gate-Source Charge	Q_{gs}		-	8.7	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	22	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-19	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-76	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = -19A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = -18A, dI_F/dt = 100A/μs	-	210	-	ns
Reverse Recovered Charge	Q_{RR}		-	2.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 4.2mHμ, R_G = 25Ω, Peak I_L = 19A (See Figures 15 and 16)

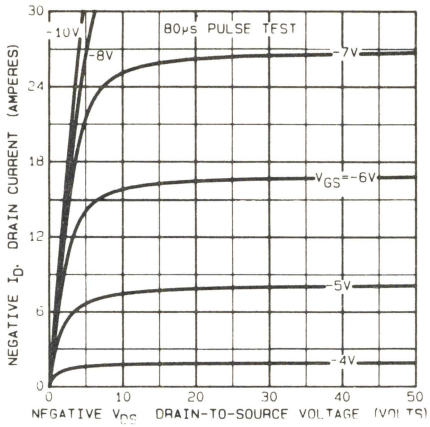


Fig. 1 - Typical output characteristics.

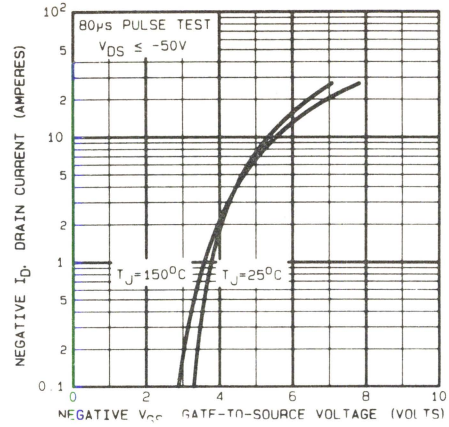


Fig. 2 - Typical transfer characteristics.

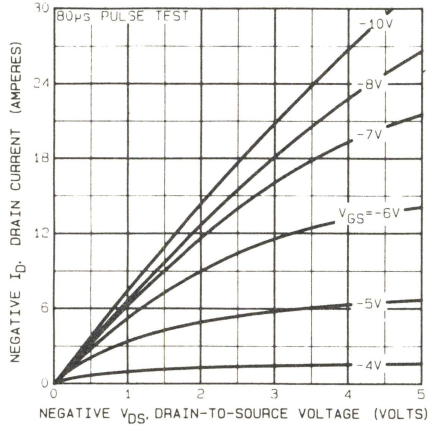


Fig. 3 - Typical saturation characteristics.

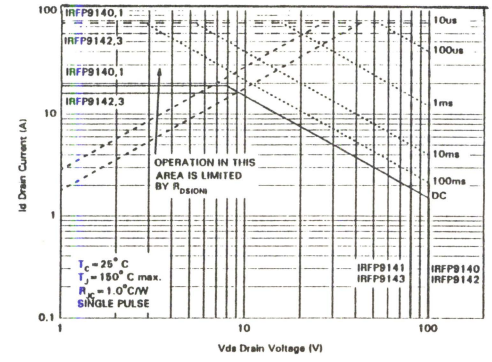


Fig. 4 - Maximum safe operating area.

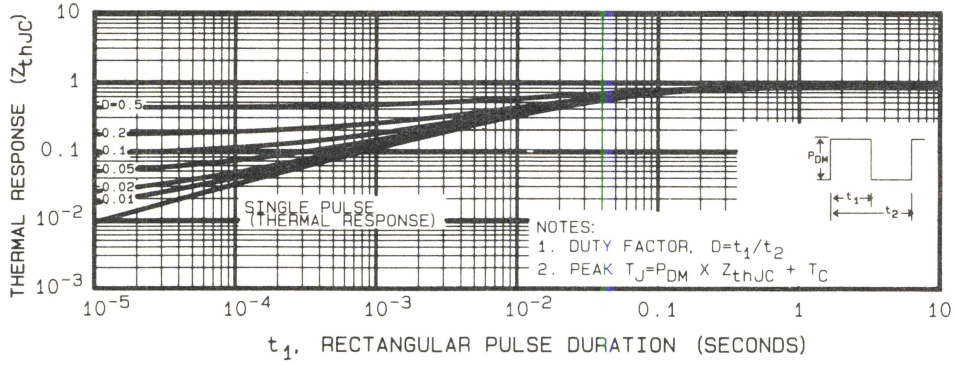


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

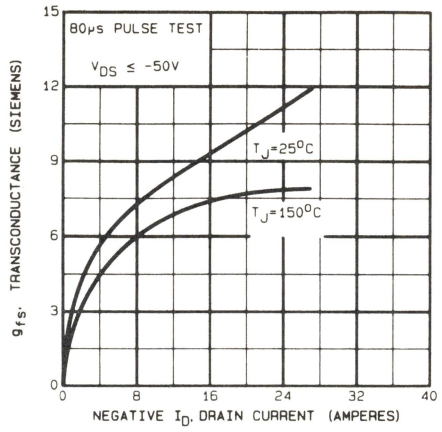


Fig. 6 - Typical transconductance vs. drain current.

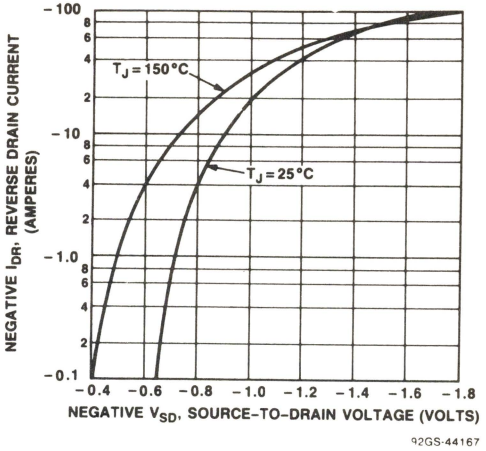


Fig. 7 - Typical source-drain diode forward voltage.

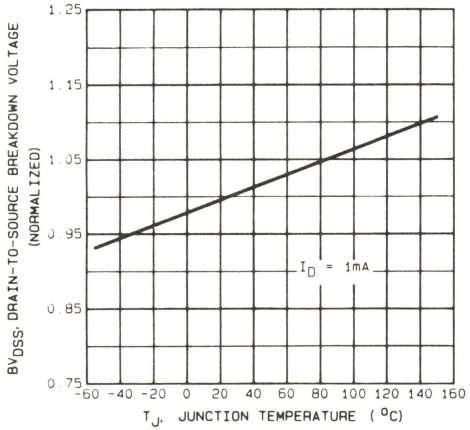


Fig. 8 - Breakdown voltage vs. temperature.

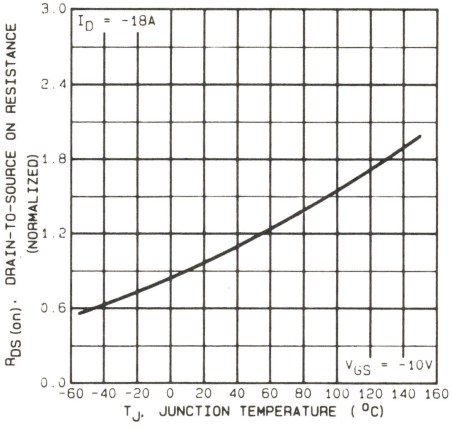


Fig. 9 - Normalized on-resistance vs. temperature.

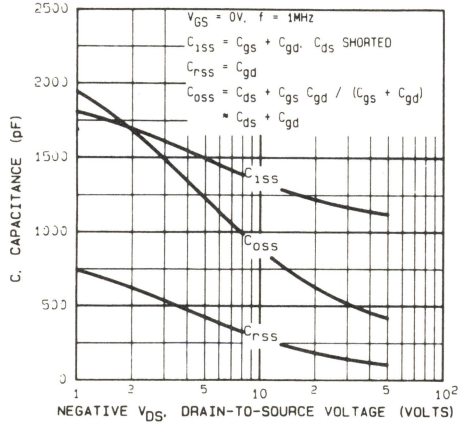


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

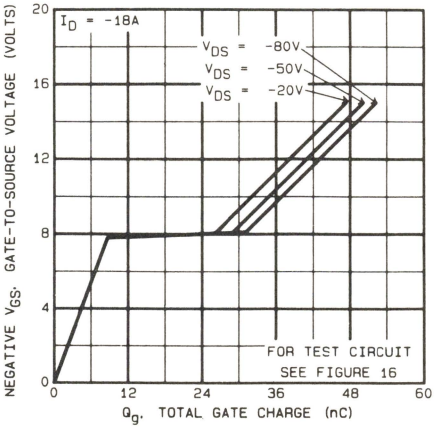


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

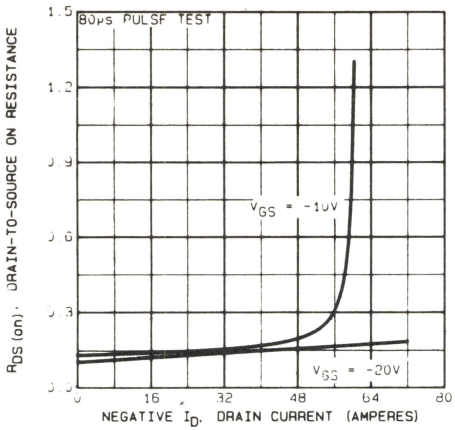


Fig. 12 - Typical on-resistance vs. drain current.

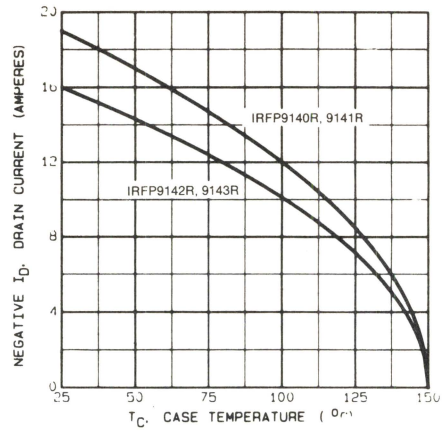


Fig. 13 - Maximum drain current vs. case temperature.

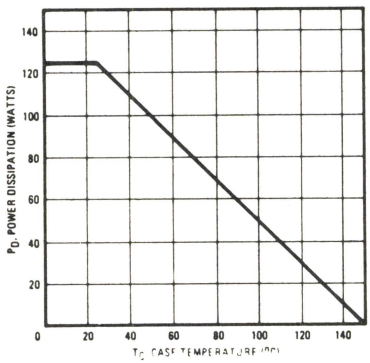


Fig. 14 - Power vs. temperature derating curve.

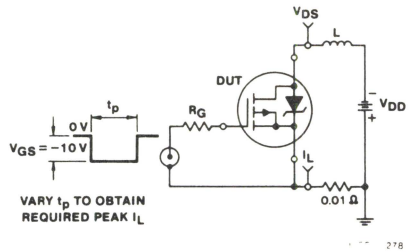


Fig. 15 - Unclamped inductive test circuit.

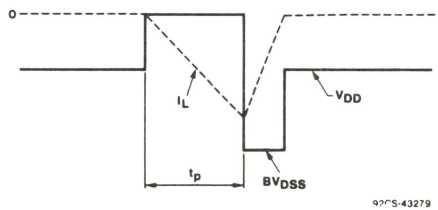


Fig. 16 - Unclamped inductive waveforms.

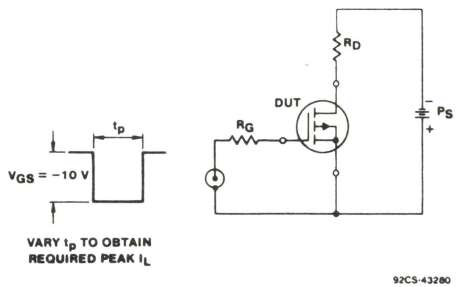


Fig. 17 - Switching time test circuit.

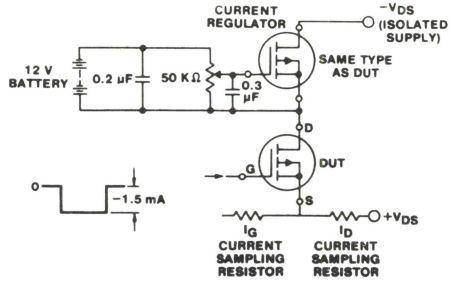


Fig. 18 - Gate charge test circuit.

HARRIS

IRFP9150
IRFP9151

Avalanche Energy Rated P-Channel Power MOSFETs

January 1994

Features

- -25A, -80V and -100V
- $r_{DS(ON)} = 0.150\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

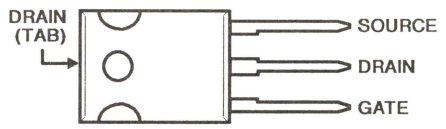
The IRFP9150 and IRFP9151 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRFP9150 is an approximate electrical complement to the N-channel IRF150.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

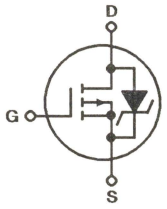
Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



5 P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

		IRFP9150	IRFP9151	UNITS
Drain-Source Voltage	V_{DS}	-100	-80	V
Continuous Drain Current				
$T_C = 25^oC$	I_D	-25	-25	A
$T_C = 100^oC$	I_D	-18	-18	A
Pulsed Drain Current	I_{DM}	-100	-100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 18)	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	1300	1300	mJ
Avalanche Current (Repetitive or Nonrepetitive)	I_{AR}	-25	-25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Pulse Test: Pulse width $\leq$ 300μs, Duty Cycle $\leq$ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 25A (See Figures 14 and 15)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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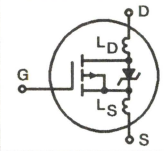
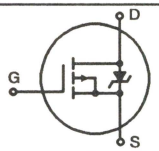
File Number 2293.1

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP9150	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100	-	-	V
IRFP9151			-80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	μA
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	-25	-	-	A
Static Drain-Source On-State Resistance (Note 1)	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.09	0.15	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = -10V, I_D = -12.5A	4	10	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	2400	-	pF
Output Capacitance	C_{OSS}		-	850	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	400	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -50V, I_D = -25A, R_G = 6.8Ω, R_D = 2Ω. See Figures 16 and 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	24	ns
Rise Time	t_r		-	110	160	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	65	100	ns
Fall Time	t_f		-	46	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -25A, V_{DS} = 0.8 Max Rating. See Figures 11 & 19 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	82	120	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	42	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-100	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 25A, V_{GS} = 0V	-	-0.9	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	-	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/μs	0.3	0.7	1.5	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 25A (See Figures 14 and 15)

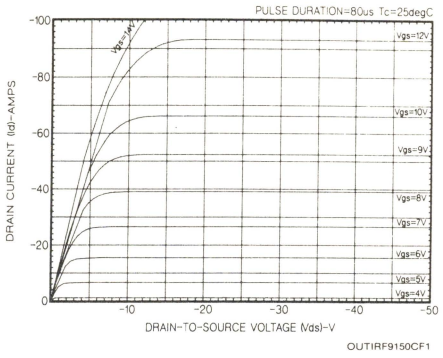


Fig. 1 - Typical output characteristics.

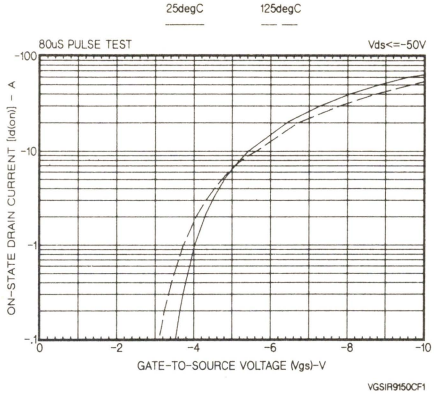


Fig. 2 - Typical transfer characteristics.

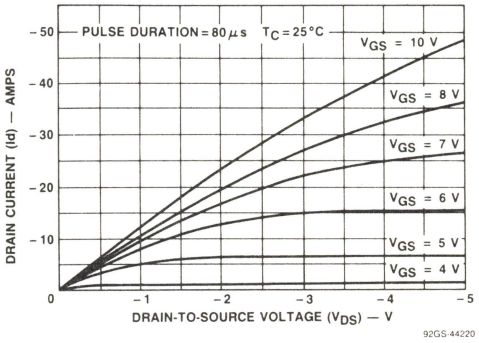


Fig. 3- Typical saturation characteristics.

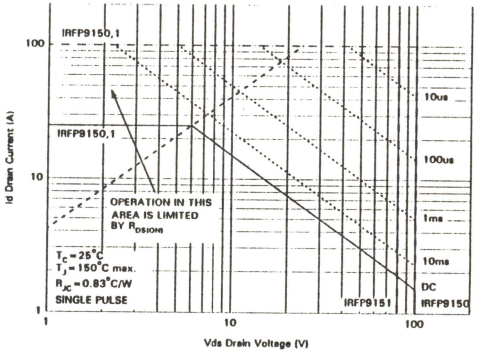


Fig. 4 - Maximum safe operating area.

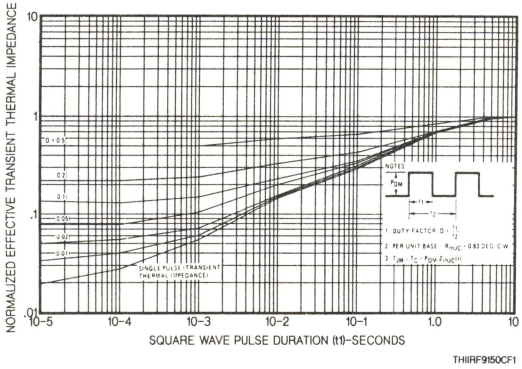


Fig. 5 - Maximum effective transient thermal impedance.

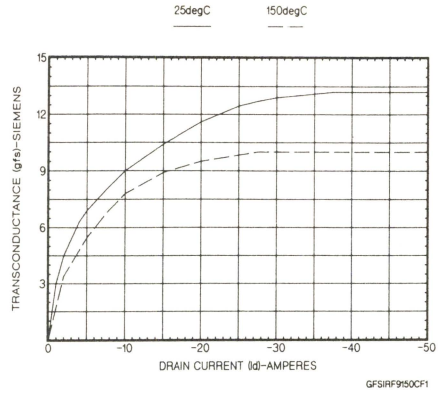


Fig. 6 - Typical transconductance vs. drain current.

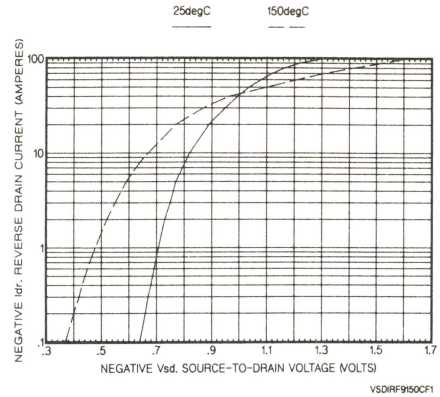


Fig. 7 - Typical source-drain diode forward voltage.

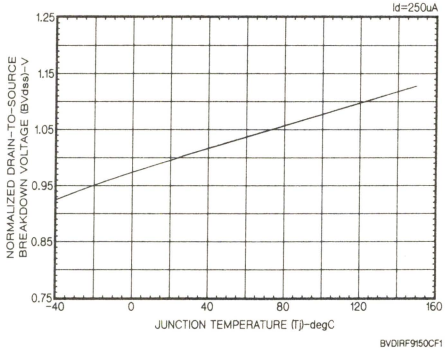


Fig. 8 - Normalized breakdown voltage vs. temperature.

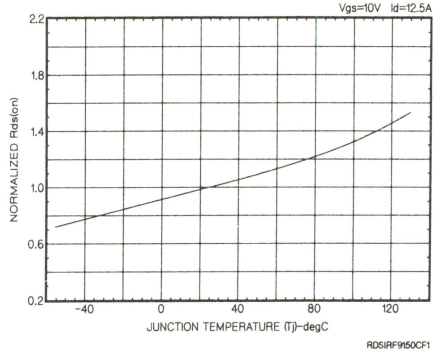


Fig. 9 - Normalized on-resistance vs. temperature.

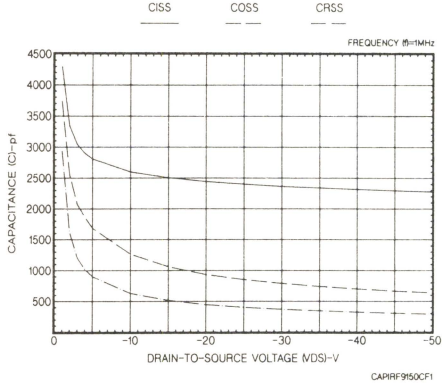


Fig. 10 - Typical capacitance vs. drain-to source voltage.

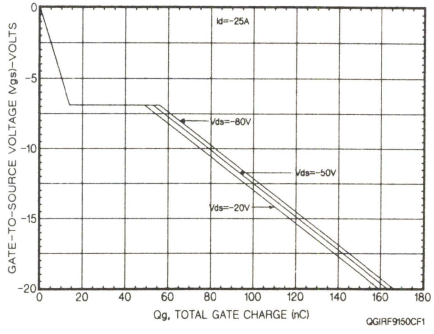


Fig. 11 - Typical gate charge vs. gate-to source voltage.

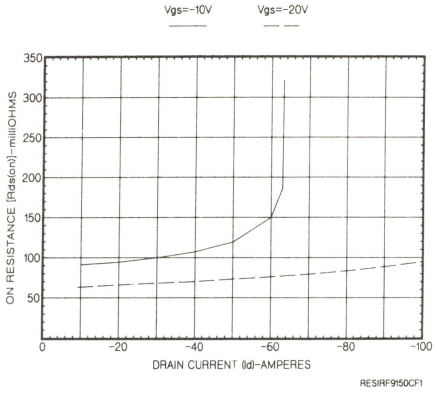


Fig. 12 - Typical on-resistance vs. drain current.

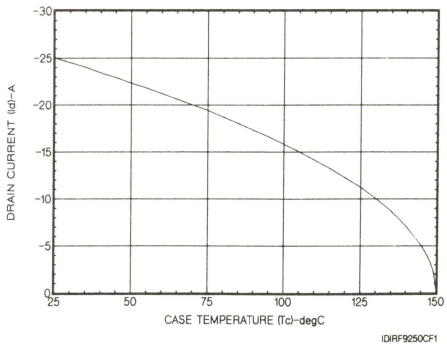


Fig. 13 - Maximum drain current vs. case temperature.

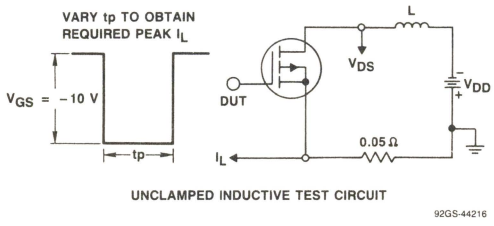


Fig. 14 - Unclamped inductive test circuit.

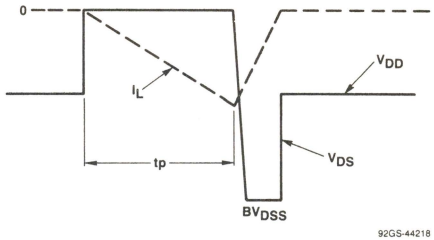


Fig. 15 - Unclamped inductive waveforms.

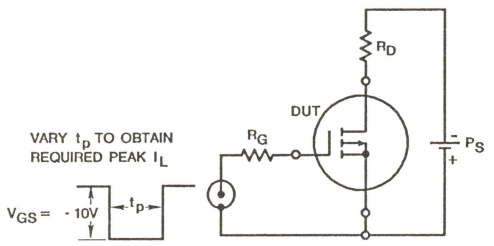


Fig. 16 - Switching time test circuit.

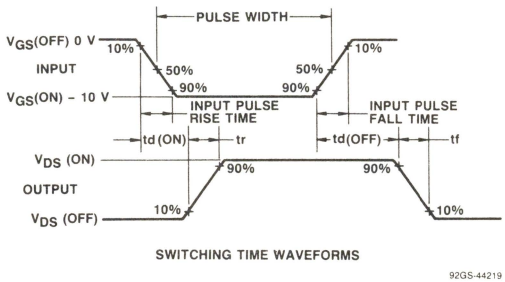


Fig. 17 - Switching time waveforms.

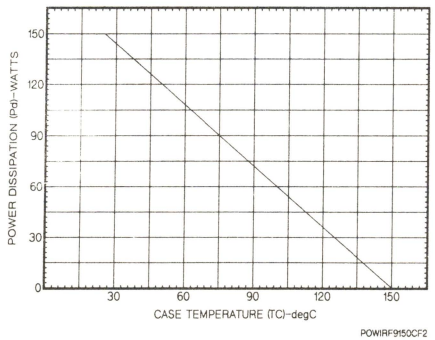


Fig. 18 - Power vs. temperature derating curve.

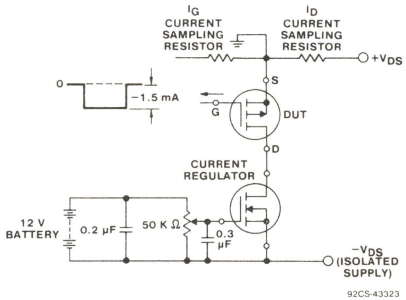


Fig. 19 - Gate charge test circuit.

HARRIS

IRFP9240/P9241
IRFP9242/P9243

Avalanche Energy Rated P-Channel Power MOSFETs

May 1992

Features

- -10A and -12A, -200V and -150V
- $r_{DS(ON)}$ = 0.50Ω and 0.7Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

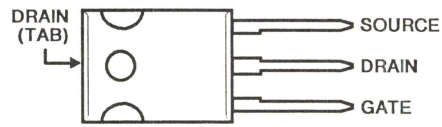
Description

The IRFP9240, IRFP9241, IRFP9242 and IRFP9243 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

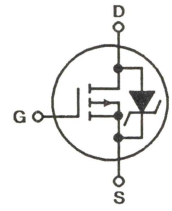
Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFP9240	IRFP9241	IRFP9242	IRFP9243	UNITS
Drain-Source Voltage (1) ..... V_{DS}	-200	-150	-200	-150	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	-200	-150	-200	-150	V
Continuous Drain Current					
T_C = 25°C ..... I_D	-12	-12	-10	-10	A
T_C = 100°C ..... I_D	-7.5	-7.5	-6.3	-6.3	A
Pulsed Drain Current (3) ..... I_{DM}	-48	-48	-40	-40	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation ..... P_D (See Figure 14)	150	150	150	150	W
Linear Derating Factor ..... (See Figure 14)	1.2	1.2	1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (4) ..... E_{as}	790	790	790	790	mJ
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s) ..... T_L	300	300	300	300	°C

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 8.2mH, R_G = 50Ω, Peak I_L = 12A (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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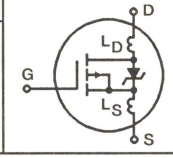
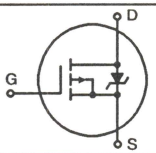
File Number **2294.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP9240, IRFP9242	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-200	-	-	V
IRFP9241, IRFP9243			-150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250μA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	μA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	-1000	μA
On-State Drain Current (Note 2) IRFP9240, IRFP9241	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)}$ Max, V_{GS} = -10V	-12	-	-	A
IRFP9242, IRFP9243			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP9240, IRFP9241	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -6.3A	-	0.38	0.50	Ω
IRFP9242, IRFP9243			-	0.50	0.70	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \leq$ -50V, I_D = -6.3A	3.8	5.7	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	1400	-	pF
Output Capacitance	C_{OSS}		-	350	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	140	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -100V, I_D = -12A, R_G = 9.1Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	18	22	ns
Rise Time	t_r		-	45	68	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	75	90	ns
Fall Time	t_f		-	29	44	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -12A, V_{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	57	nC
Gate-Source Charge	Q_{gs}		-	8.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	21	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = -12A, V_{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = -11A, dI_F/dt = 100A/μs	-	210	-	ns
Reverse Recovered Charge	Q_{RR}		-	2.0	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 8.2mHμ, R_G = 50Ω, Peak I_L = 12A (See Figures 15 and 16)

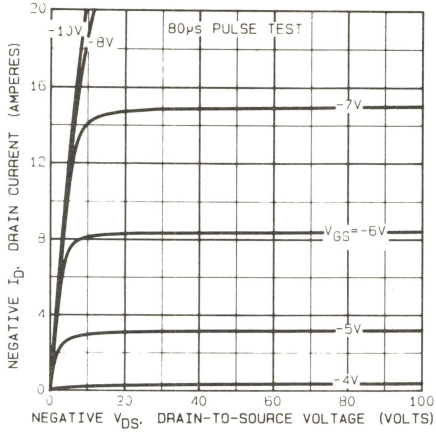


Fig. 1 - Typical output characteristics.

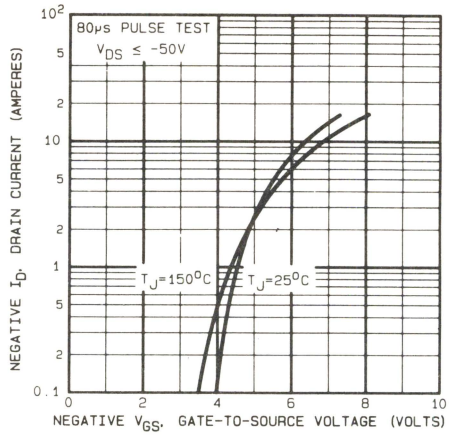


Fig. 2 - Typical transfer characteristics.

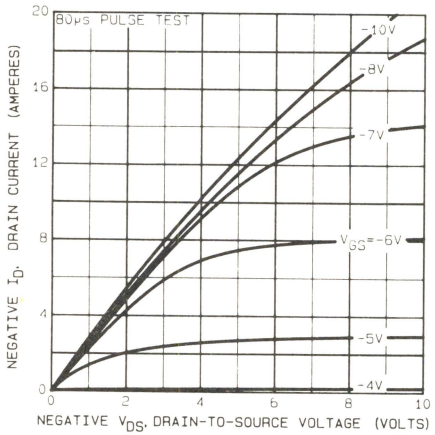


Fig. 3 - Typical saturation characteristics.

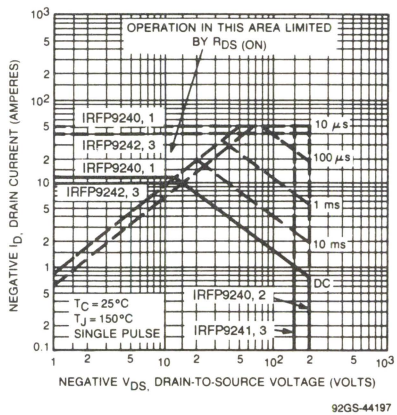


Fig. 4 - Maximum safe operating area.

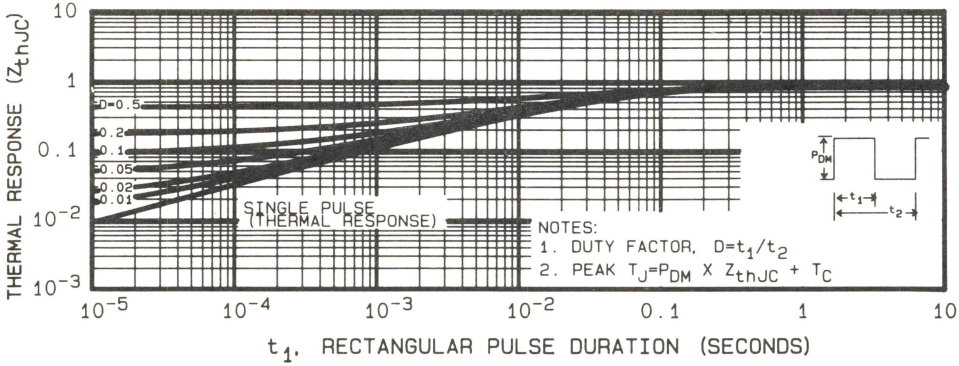


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

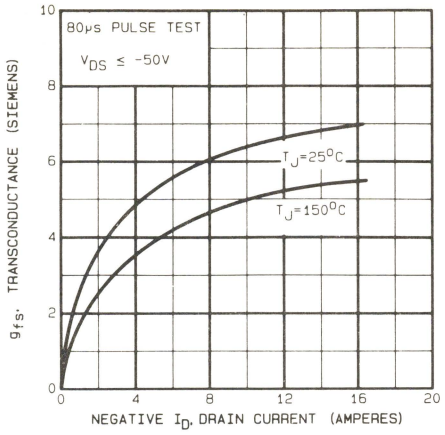


Fig. 6 - Typical transconductance vs. drain current.

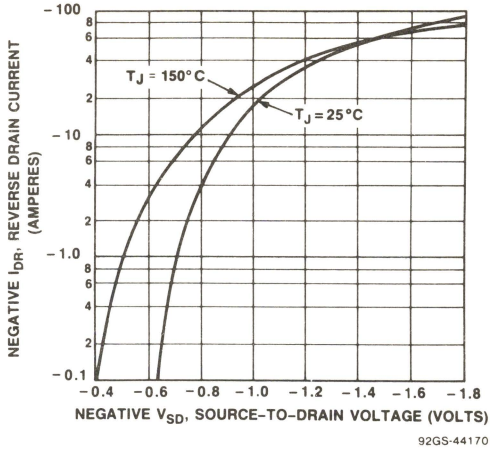


Fig. 7 - Typical source-drain diode forward voltage.

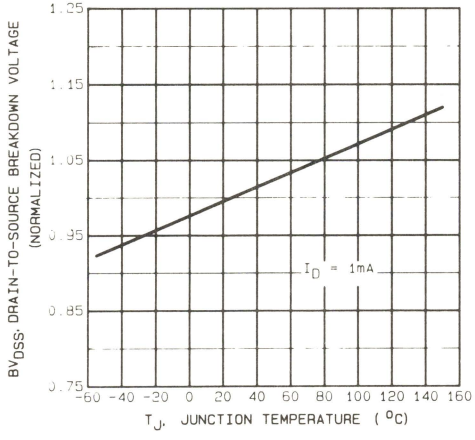


Fig. 8 - Breakdown voltage vs. temperature.

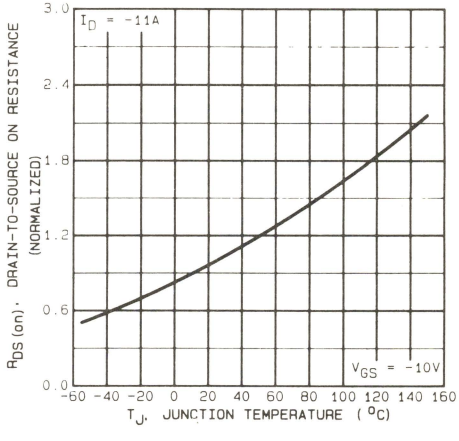


Fig. 9 - Normalized on-resistance vs. temperature.

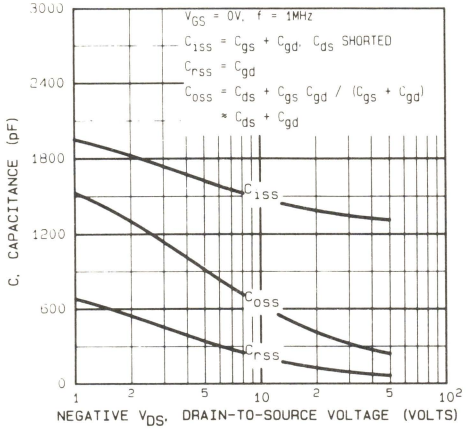


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

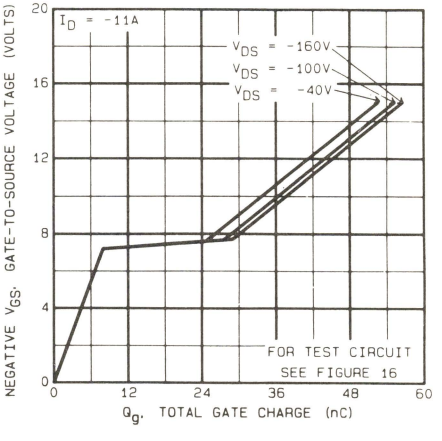


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

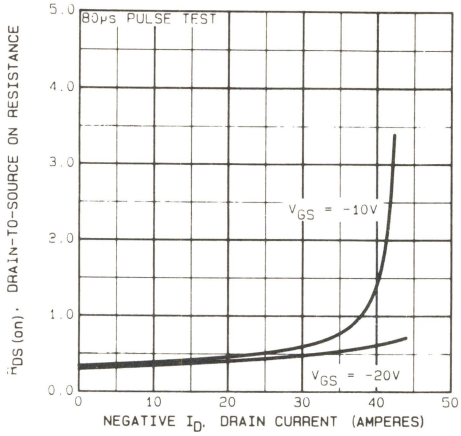


Fig. 12 - Typical on-resistance vs. drain current.

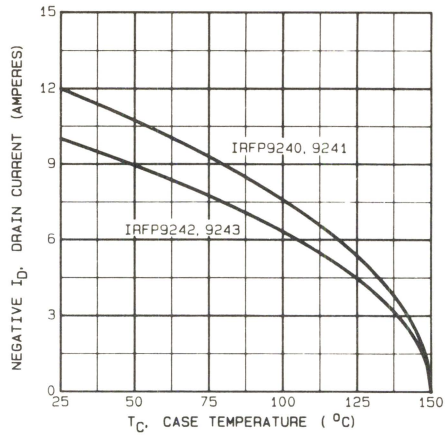


Fig. 13 - Maximum drain current vs. case temperature.

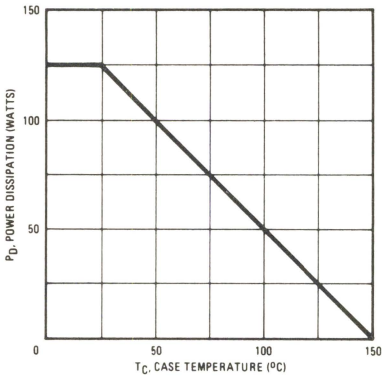


Fig. 14 - Power vs. temperature derating curve.

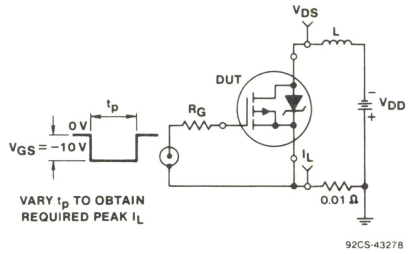


Fig. 15 - Unclamped inductive test circuit.

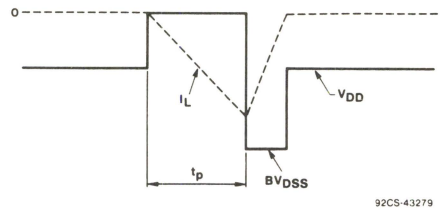


Fig. 16 - Unclamped inductive waveforms.

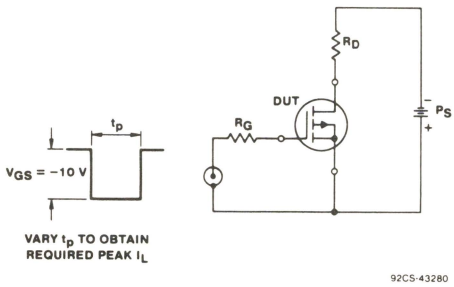


Fig. 17 - Switching time test circuit.

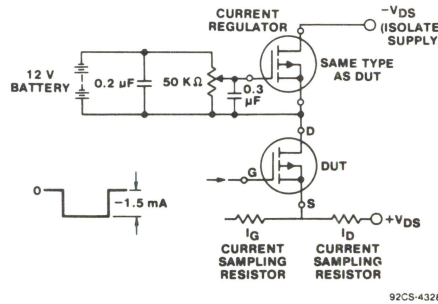


Fig. 18 - Gate charge test circuit.

HARRIS

RFL1P08
RFL1P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 1A, -80V and -100V
- $r_{DS(ON)} = 3.65\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

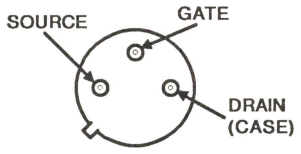
Description

The RFL1P08 and RFL1P10 are P-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

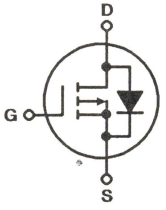
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		RFL1P08	RFL1P10	UNITS
Drain-Source Voltage	V_{DS}	-80	-100	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	-80	-100	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	8.33	8.33	W
Above T_C = +25°C, Derate Linearly		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1535.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1P08		RFL1P10		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	-80	–	-100	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65V	–	-1	–	–	μA
		V_{DS} = -80V	–	–	–	-1	μA
		T_C = +125°C V_{DS} = -65V	–	-50	–	–	μA
		V_{DS} = -80V	–	–	–	-50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	±100	–	±100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	–	-3.65	–	-3.65	V
		I_D = 2A, V_{GS} = -10V	–	-9.3	–	-9.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	–	3.65	–	3.65	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = -10V	200	–	200	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V f = 1MHz	–	150	–	150	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	30	–	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = -50V R_{GEN} = R_{GS} = 50Ω V_{GS} = -10V	7 (typ)	25	7 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		14 (typ)	45	14 (typ)	45	ns
Fall Time	t_f		11 (typ)	25	11 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1P08		RFL1P10		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	-1.4	–	-1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A d_{IF}/dt = 50A/μs	–	135 (typ)	–	135 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

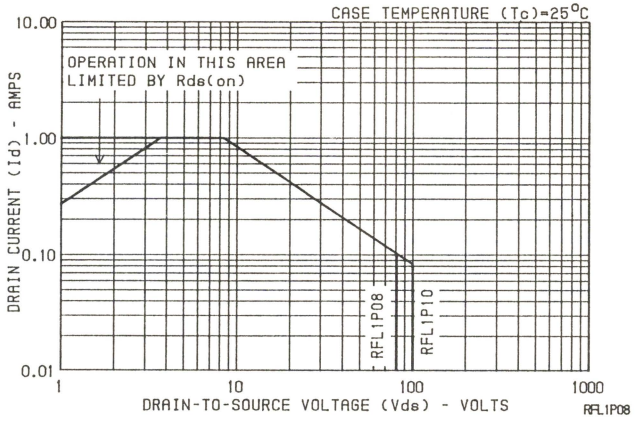


Fig. 1 - Maximum operating areas for all types.

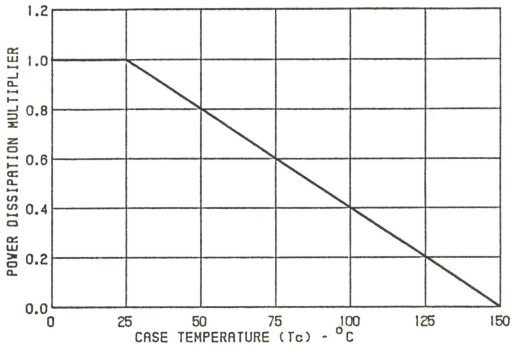


Fig. 2 - Normalized power dissipation vs temperature derating curve.

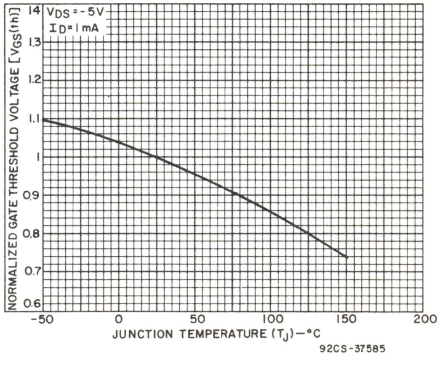


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

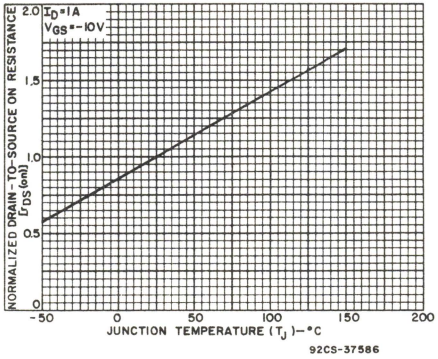


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

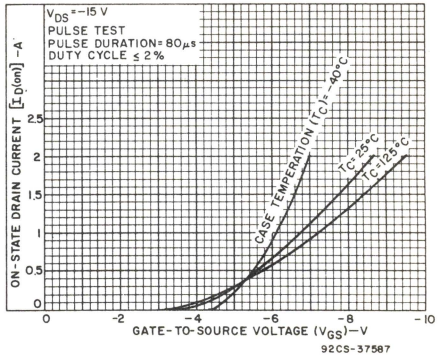


Fig. 5 - Typical transfer characteristics for all types.

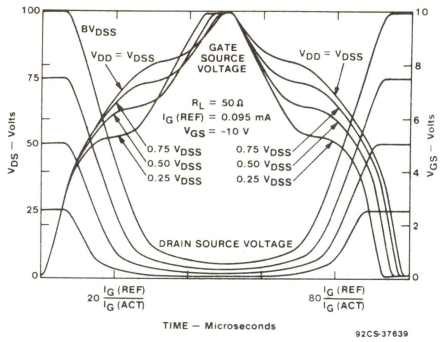


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

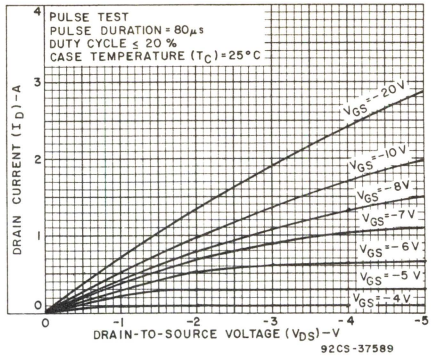


Fig. 7 - Typical saturation characteristics for all types.

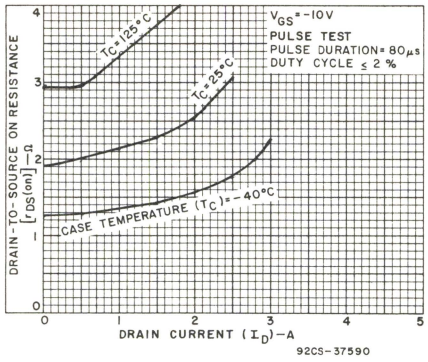


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

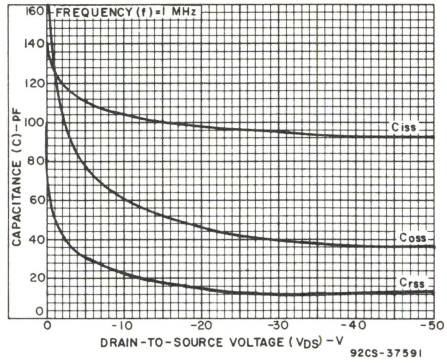


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

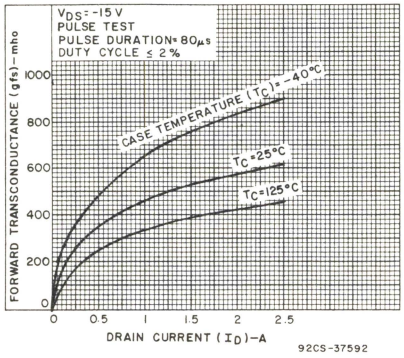


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

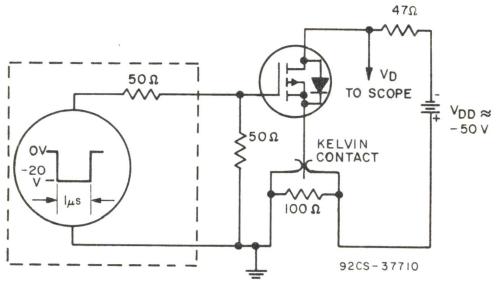


Fig. 11 - Switching time test circuit.

HARRIS

RFP2P08
RFP2P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -2A, -80V and -100V
- $r_{DS(ON)} = 3.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

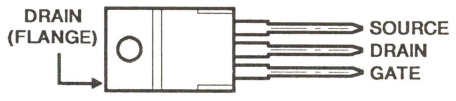
Description

The RFP2P08 and RFP2P10 are P-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

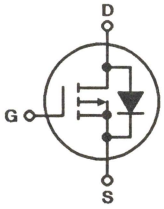
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

		RFP2P08	RFP2P10	UNITS
Drain-Source Voltage	V_{DS}	-80	-100	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	-80	-100	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	25	25	W
Above T_C = +25°C, Derate Linearly		0.2	0.2	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2870

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2P08		RFP2P10		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	-80	-	-100	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 1mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65V	-	-1	-	-	μA
		V_{DS} = -80V	-	-	-	-1	μA
		T_C = +125°C, V_{DS} = -65V	-	-50	-	-	μA
		V_{DS} = -80V	-	-	-	-50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	±100	-	±100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	-	-3.5	-	-3.5	V
		I_D = 2A, V_{GS} = -10V	-	-9.0	-	-9.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = -10V	-	3.5	-	3.5	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = -10V	200	-	200	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz	-	150	-	150	pF
Output Capacitance	C_{OSS}		-	80	-	80	pF
Reverse Transfer Capacitance	C_{RSS}		-	30	-	30	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = -50V, $R_{GEN} = R_{GS}$ = 50Ω, V_{GS} = -10V	7 (typ)	25	7 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		14 (typ)	45	14 (typ)	45	ns
Fall Time	t_f		11 (typ)	25	11 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	5	-	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2P08		RFP2P10		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	-	-1.4	-	-1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	-	135 (typ)	-	135 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

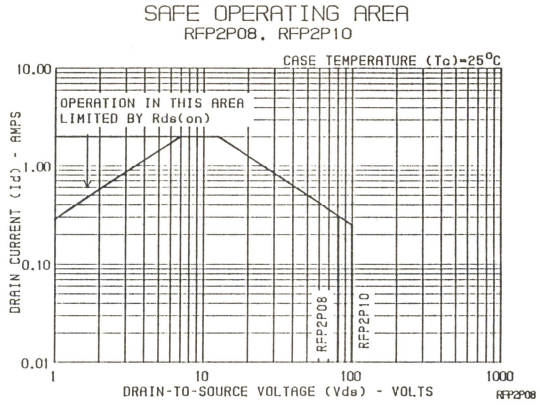


Fig. 1 - Maximum operating areas for all types.

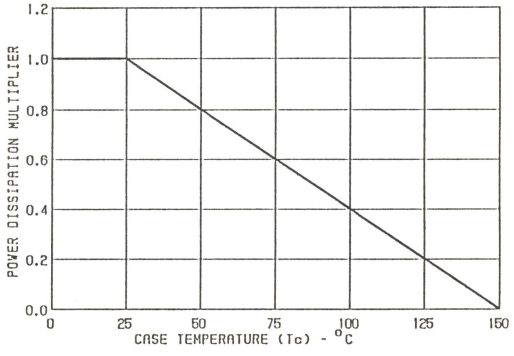


Fig. 2 – Normalized power dissipation vs temperature derating curve.

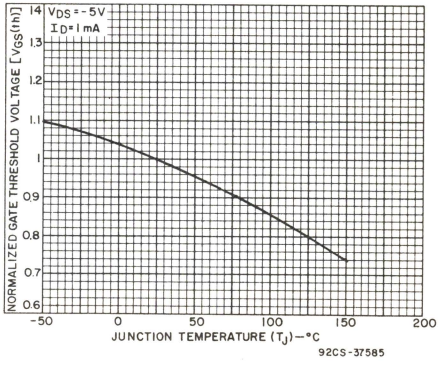


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

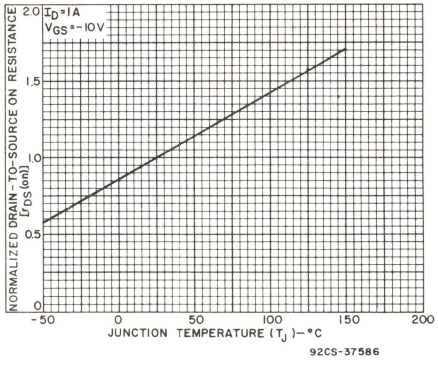


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

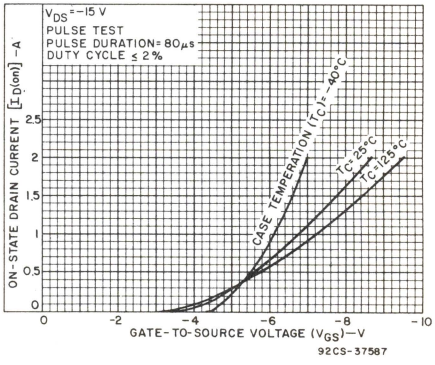


Fig. 5 - Typical transfer characteristics for all types.

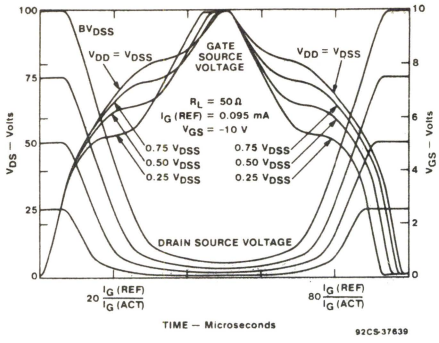


Fig. 6 - Normalized switching waveforms for constant gate-current.

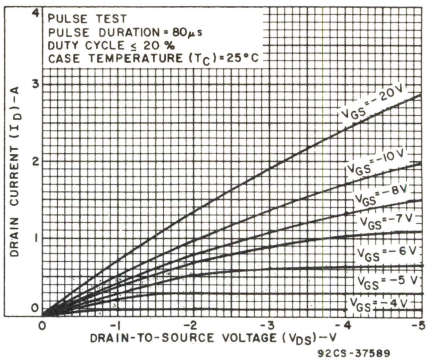


Fig. 7 - Typical saturation characteristics for all types.

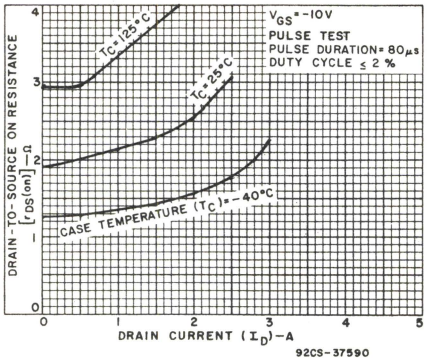


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

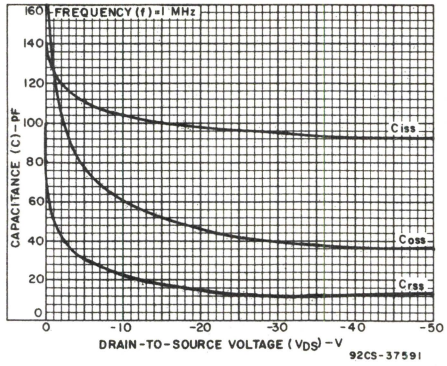


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

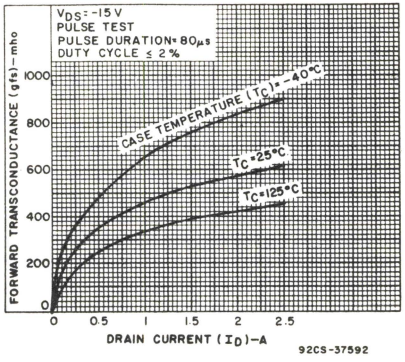


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

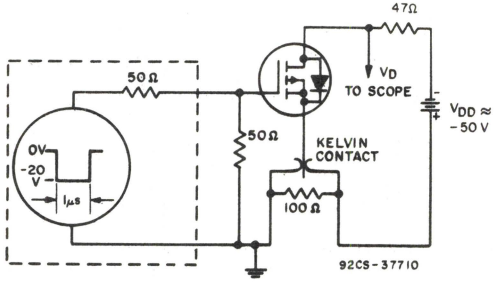


Fig. 11 - Switching time test circuit.

HARRIS

RFM5P12/5P15
RFP5P12/5P15

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -5A, -120V and -150V
- $r_{DS(on)} = 1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

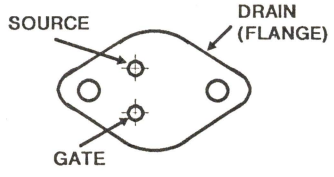
Description

The RFM5P12 and RFM5P15 and the RFP5P12 and RFP5P15 are p-channel enhancement-mode silicon gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

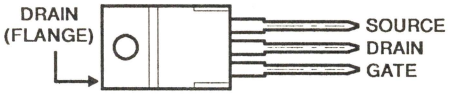
The RFM series types are supplied in the JEDEC TO-204AA metal package and the RFP series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate zener diode.

Packages

TO-204AA
BOTTOM VIEW

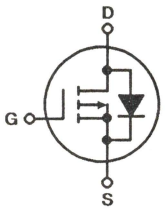


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	RFM5P12	RFM5P15	RFP5P12	RFP5P15	UNITS
Drain-Source Voltage ..... V_{DS}	-120	-150	-120	-150	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	-120	-150	-120	-150	V
Continuous Drain Current					
RMS Continuous ..... I_D	5	5	5	5	A
Pulsed Drain Current ..... I_{DM}	15	15	15	15	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	60	60	W
Above T_C = +25°C, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 1463

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V	—	1	—	—	μA
		V_{DS} = -120 V	—	—	—	1	
		T_C = 125°C V_{DS} = -100 V	—	50	—	—	
		V_{DS} = -120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 2.5 A V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 5A V_{GS} = -10 V	—	-8	—	-8	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 2.5 A V_{GS} = -10 V	—	1	—	1	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 2.5 A	0.75	—	0.75	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	700	—	700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1/2 BV_{DSS}	20(typ.)	60	20(typ.)	60	ns
Rise Time	t_r	I_D = 2.5 A	36(typ.)	100	36(typ.)	100	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = R_{gs} = 50Ω	63(typ.)	150	63(typ.)	150	
Fall Time	t_f	V_{GS} = 10 V	40(typ.)	100	40(typ.)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM5P12, RFM5P15	—	1.67	—	1.67	°C/W
		RFP5P12, RFP5P15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max,	
Diode Forward Voltage	V_{SD}	I_{SD} = 2.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	300(typ.)		300(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

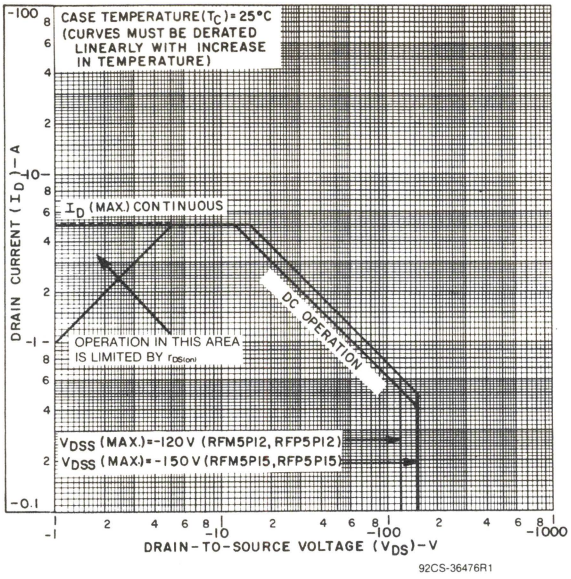


Fig. 1 - Maximum safe operating areas for all types.

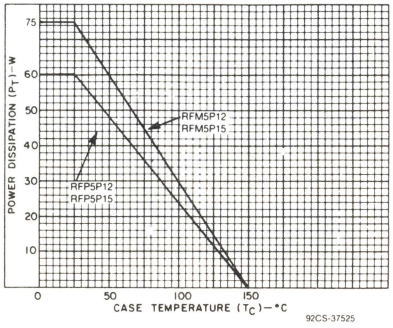


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

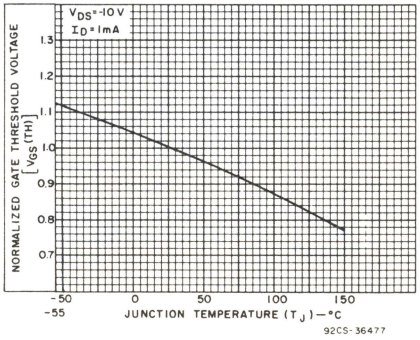


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

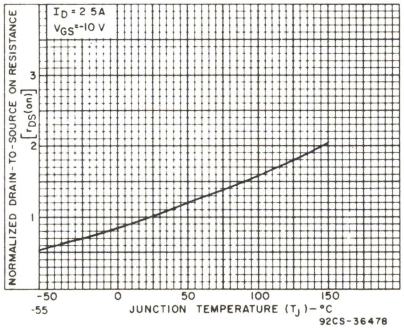


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

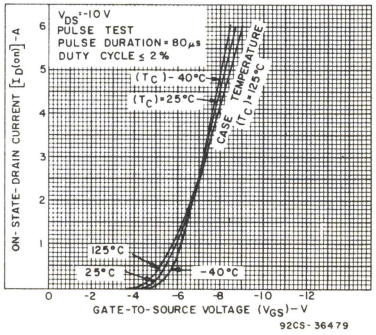


Fig. 5 - Typical transfer characteristics for all types.

5 P-CHANNEL POWER MOSFETs

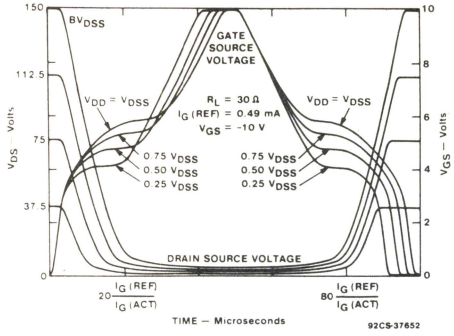


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

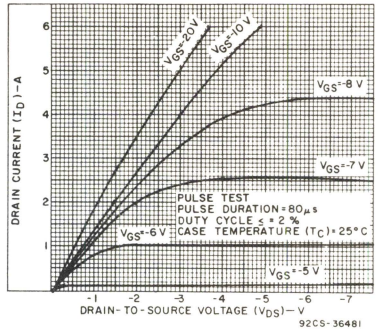


Fig. 7 - Typical saturation characteristics for all types.

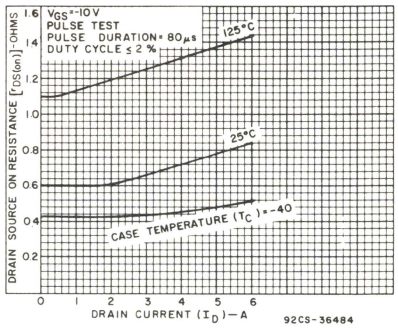


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

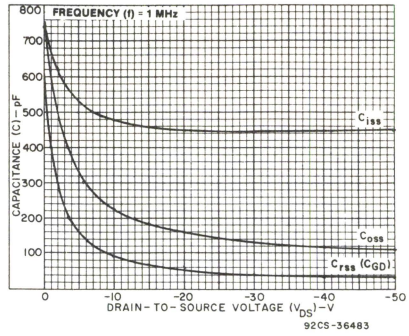


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

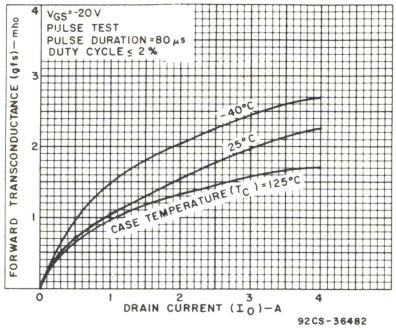


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

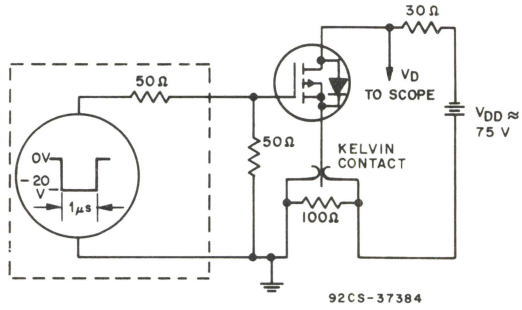


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM6P08/6P10
RFP6P08/6P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -6A, -80V and -100V
- $r_{DS(on)} = 0.6\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

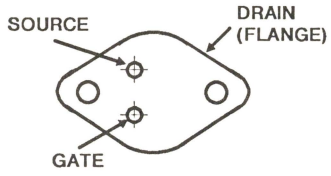
Description

The RFM6P08 and RFM6P10 and the RFP6P08 and RFP6P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

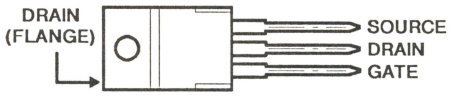
The RFM series types are supplied in the JEDEC TO-204AA metal package and the RFP series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate zener diode.

Packages

TO-204AA
BOTTOM VIEW



TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFM6P08	RFM6P10	RFP6P08	RFP6P10	UNITS
Drain-Source Voltage ..... V_{DS}	80	100	80	100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	6	6	6	6	A
Pulsed Drain Current ..... I_{DM}	20	20	20	20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1490

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=6 A V_{GS}=-10 V	—	-6	—	-6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	800	—	800	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	350	—	350	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	150	—	150	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	11(typ)	60	11(typ)	60	ns
Rise Time	t_r	I_D=3 A	48(typ)	100	48(typ)	100	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	102(typ)	150	102(typ)	150	ns
Fall Time	t_f	V_{GS}=10 V	70(typ)	100	70(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6P08, RFM6P10	—	1.67	—	1.67	°C/W
		RFP6P08, RFP6P10	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=3 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=50 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

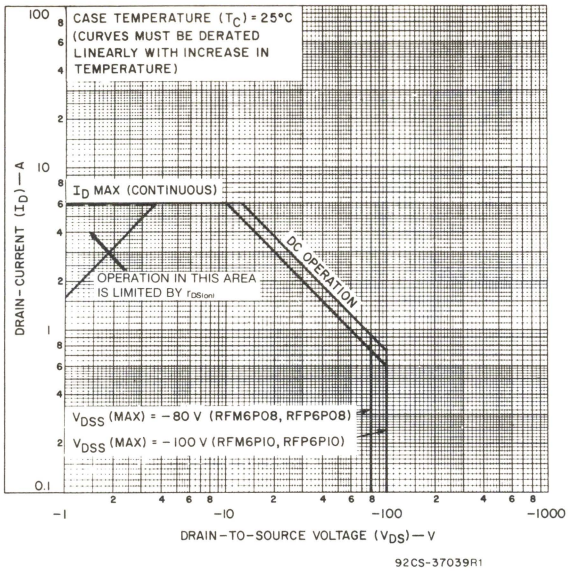


Fig. 1 — Maximum safe operating areas for all types.

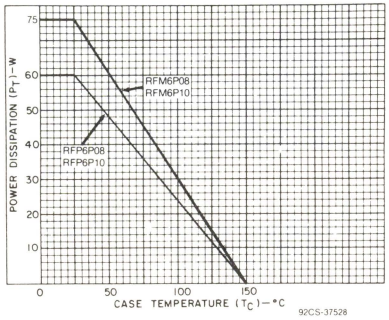


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

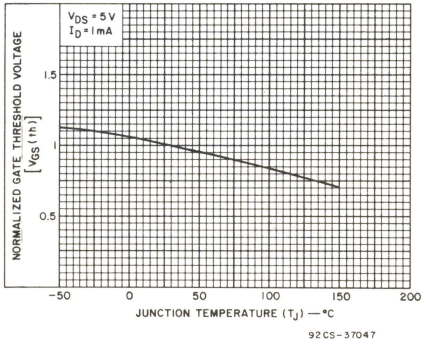


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

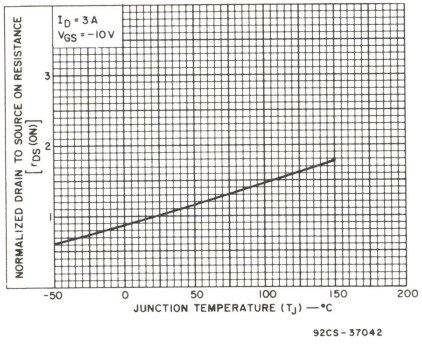


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

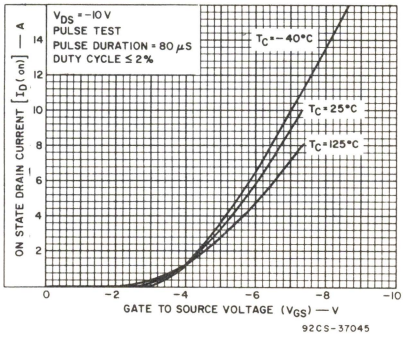


Fig. 5 — Typical transfer characteristics for all types.

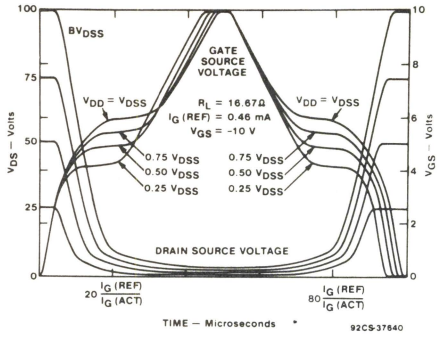


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

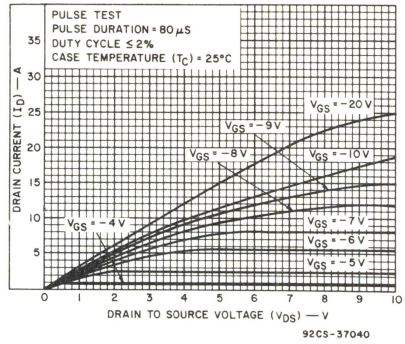


Fig. 7 — Typical saturation characteristics for all types.

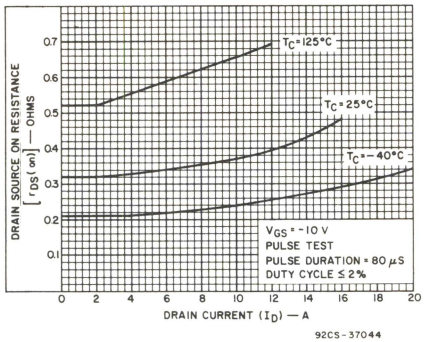


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

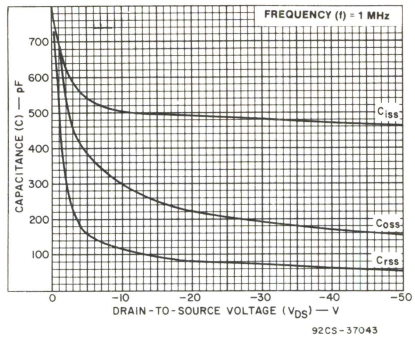


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

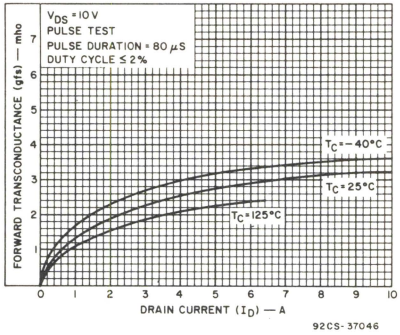


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

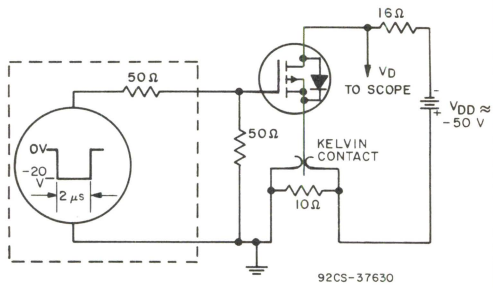


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFD8P05/05SM RFP8P05

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

August 1991

Features

- -8A, -50V
- $r_{DS(on)} = 0.300\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

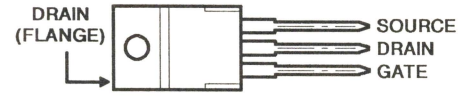
Description

The RFD8P05, RFD8P05SM and RFP8P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

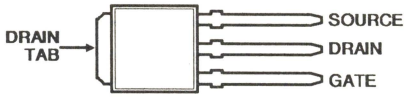
The RFD8P05 is supplied in the JEDEC TO-251AA plastic package and the RFD8P05SM in the TO-252AA plastic package. The RFP8P05 is supplied in the JEDEC TO-220AB plastic package.

Packages

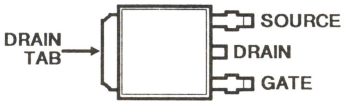
TO-220AB
TOP VIEW



TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings ($T_C = 25^oC$), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} ..... -50V
Drain-Gate Voltage, ($R_{GS} = 1M\Omega$), V_{DGR} ..... -50V
Gate-Source Voltage, V_{GS} ..... ±20V
Drain Current:
  RMS Continuous, I_D ..... -8A
  Pulsed, I_{DM} ..... -20A
Avalanche Current, I_{AS} ..... See Figure 2
Power Dissipation, P_D:
  $T_C = +25^oC$ 48W
  Derate Above $T_C = +25^oC$ ..... 0.27W/^{o}C
Operating and Storage Junction
Temperature Range, T_J, T_{STG} ..... -55^oC to $+175^oC$

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number **2384**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C			50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 8A, V_{GS} = -10V		-	0.300	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 4A Ig1 = Ig2 = 0.2A V_{GS} (clamp): -10V, +0.6V R_L = 6.25Ω (See Figure 12)		-	60	ns
Turn-On Delay Time	$t_{d(on)}$			-	16 (typ)	ns
Rise Time	t_r			-	30 (typ)	ns
Turn-Off Delay Time	$t_{d(off)}$			-	42 (typ)	ns
Fall Time	t_f				20 (typ)	ns
Turn-Off Time	$t_{(off)}$			-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -40V	-	80	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 8A	-	40	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 5Ω	-	2	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 8A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 4A, R_L = 6.25Ω L = 0.2µH, Ig1 = Ig2 = 0.2A V_{GS} (clamp): -10V, +0.6V		-	8	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-220AB		-	80	°C/W
		TO-251AA, TO-252AA		-	100	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 8A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 8A, d_{ISD}/dt = 100A/µs	-	125	ns

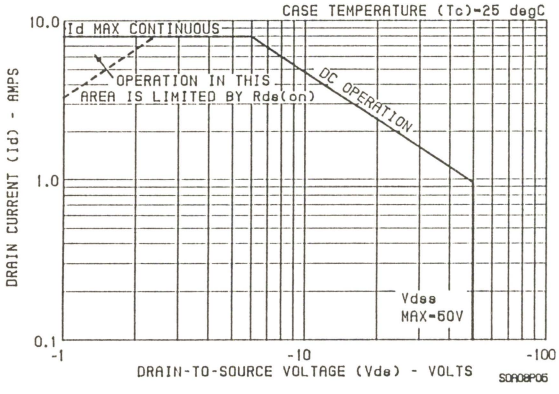


Figure 1 – Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

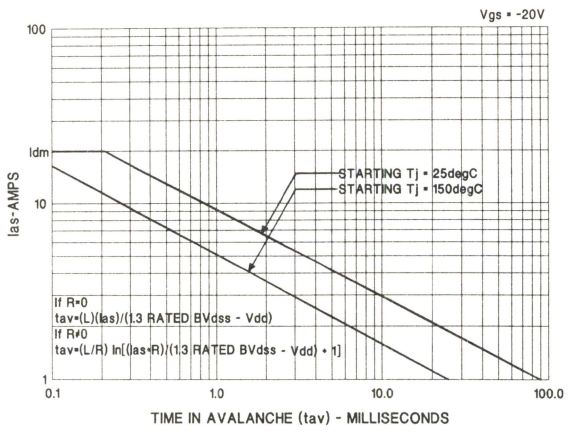


Figure 2 – Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

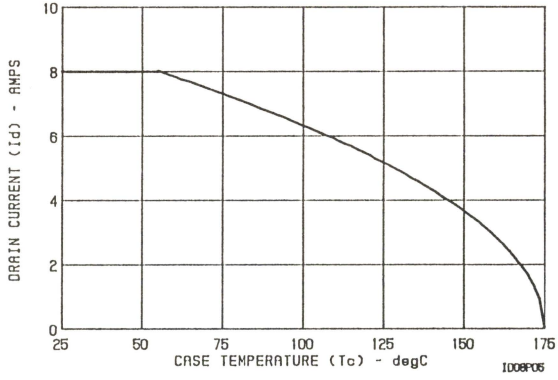


Figure 3 - Maximum continuous drain current vs. temperature.

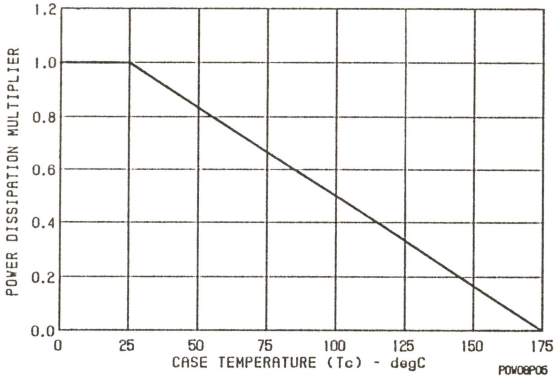


Figure 4 - Normalized power dissipation vs temperature derating curve.

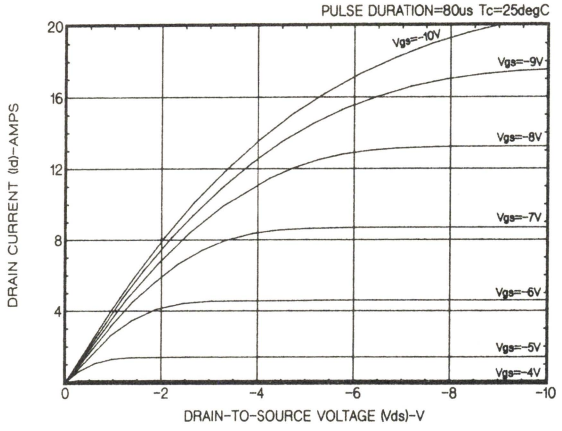


Figure 5 - Typical saturation characteristics.

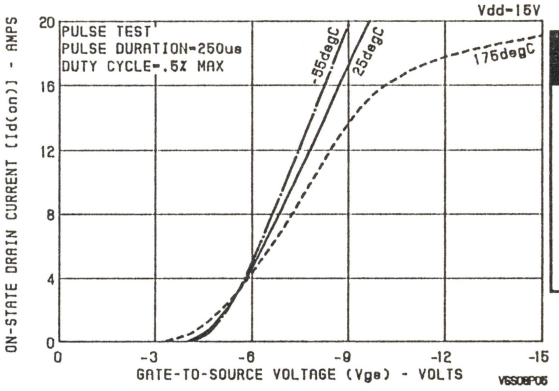


Figure 6 - Typical transfer characteristics.

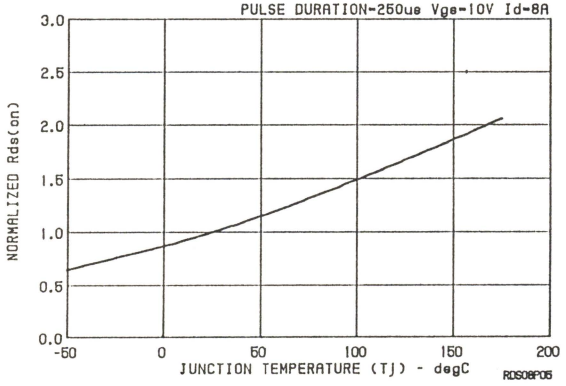


Figure 7 - Normalized rDS(on) vs junction temperature.

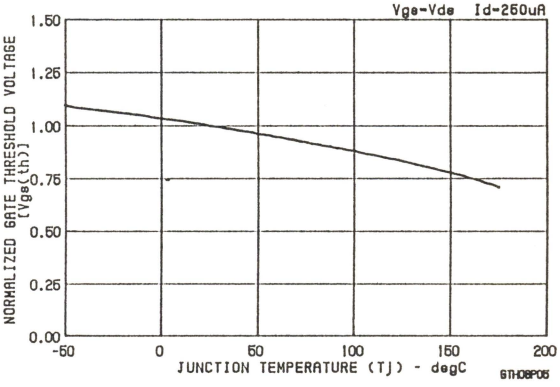


Figure 8 - Normalized gate threshold voltage.

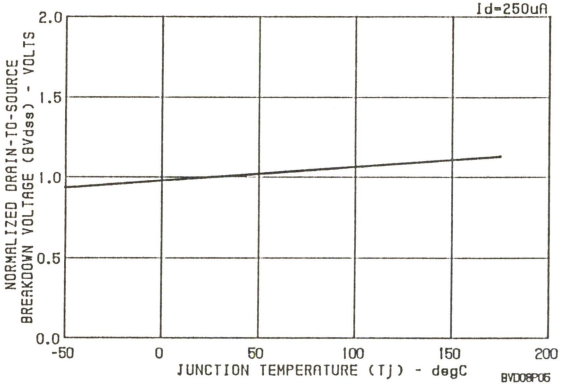


Figure 9 - Normalized drain source breakdown voltage vs temperature.

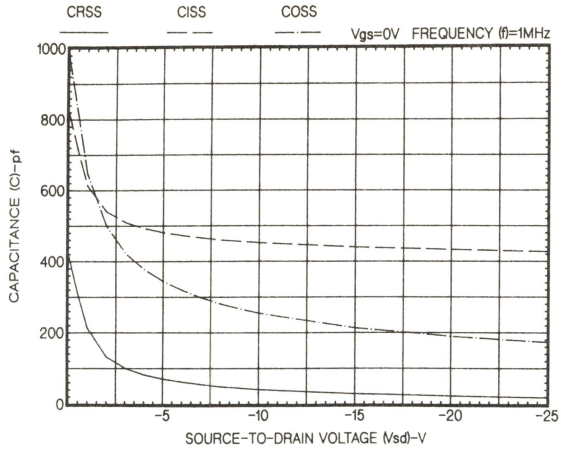


Figure 10 - Typical capacitance vs voltage.

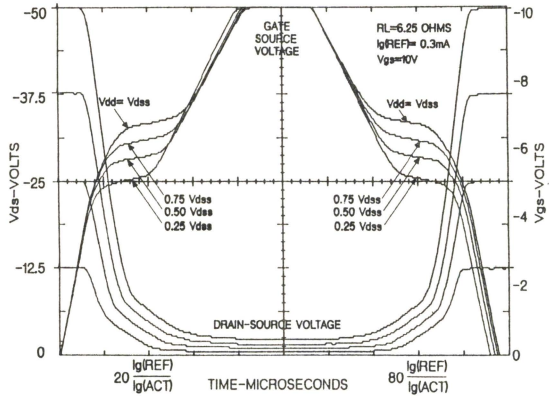
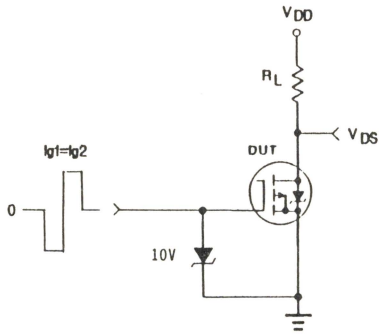
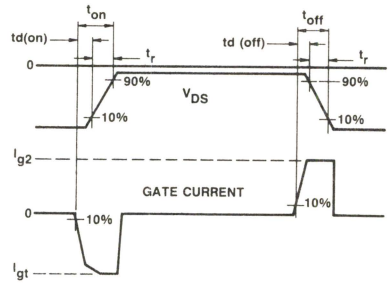


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.



Switching Test Circuit



Switching Waveforms

Figure 12 - Resistive switching.

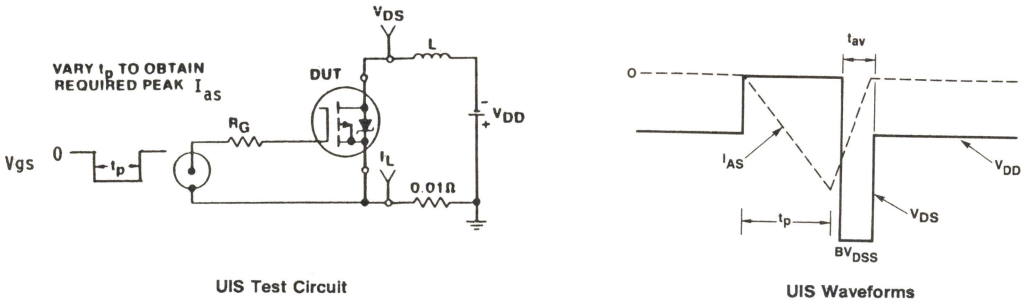


Figure 13 – Unclamped-inductive-switching test.

HARRIS

RFM8P08/8P10
RFP8P08/8P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -8A, -80V and -100V
- $r_{DS(on)} = 0.4\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

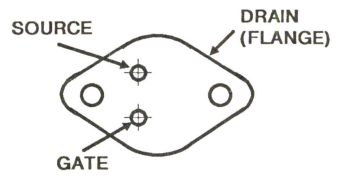
Description

The RFM8P08 and RFM8P10 and the RFP8P08 and RFP8P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

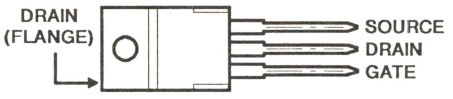
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

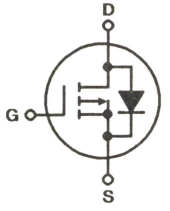


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	RFM8P08	RFM8P10	RFP8P08	RFP8P10	UNITS
Drain-Source Voltage ..... V_{DS}	-80	-100	-80	-100	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	-80	-100	-80	-100	V
Continuous Drain Current					
RMS Continuous ..... I_D	8	8	8	8	A
Pulsed Drain Current ..... I_{DM}	20	20	20	20	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	100	100	75	75	W
Above T_C = +25°C, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1496**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	-1.6	—	-1.6	V
		I_D=8 A V_{GS}=-10 V	—	-4.0	—	-4.0	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	.4	—	.4	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=4 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	1500	—	1500	pF
Output Capacitance	C_{oss}		—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}		—	300	—	300	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V I_D=4 A R_{gen}=R_{gs}=50 Ω V_{GS}=-10 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r		70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		166(typ)	275	166(typ)	275	ns
Fall Time	t_f		94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8P08, RFM8P10	—	1.25	—	1.25	°C/W
		RFP8P08, RFP8P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

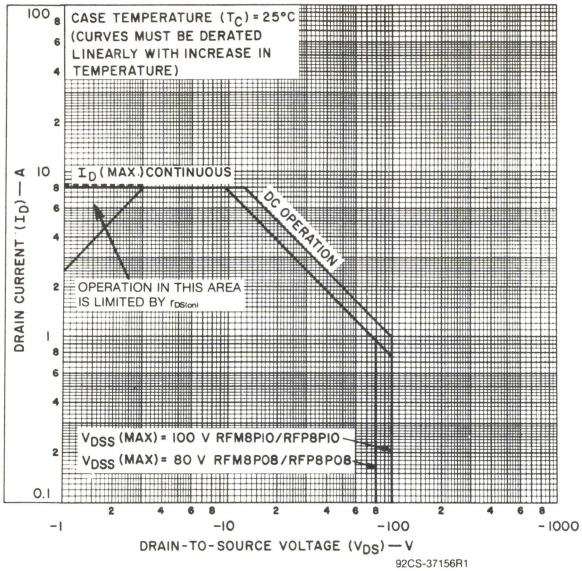


Fig. 1 — Maximum operating areas for all types.

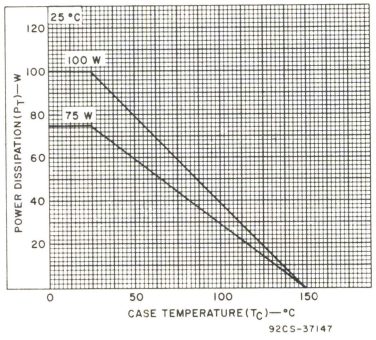


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

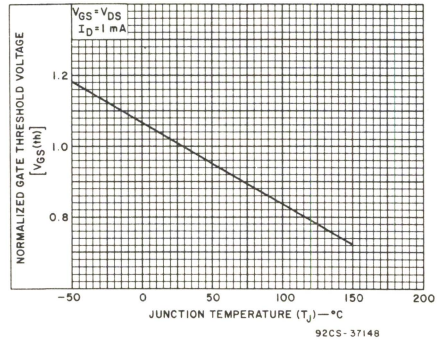


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

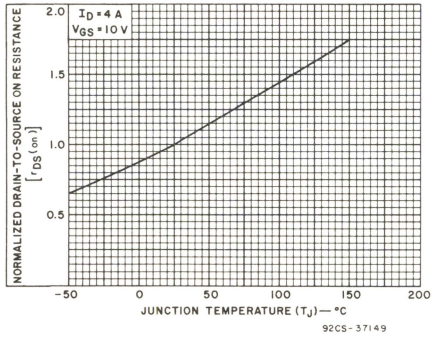


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

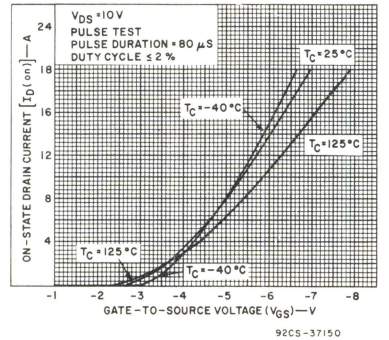


Fig. 5 — Typical transfer characteristics for all types.

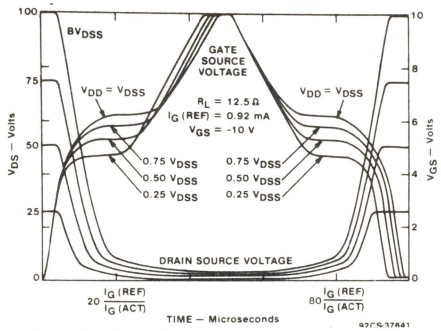


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

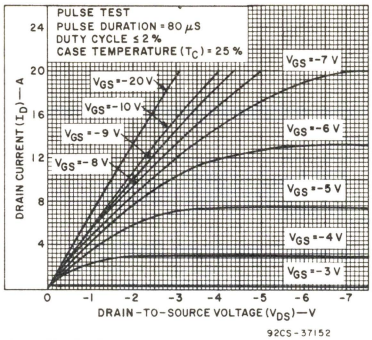


Fig. 7 — Typical saturation characteristics for all types.

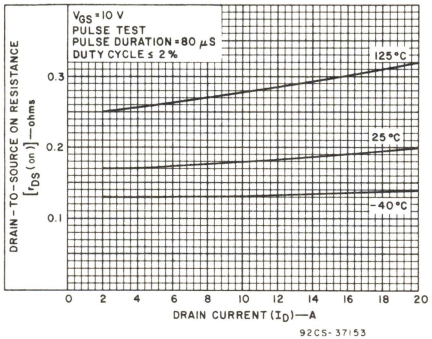


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

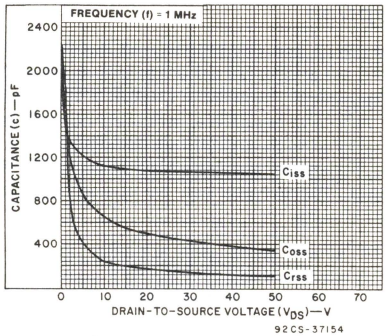


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

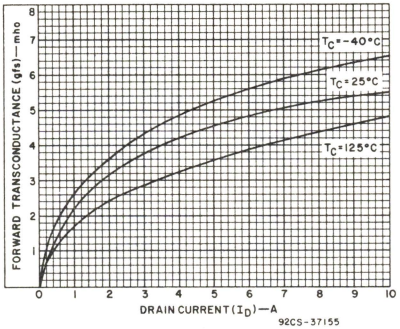


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

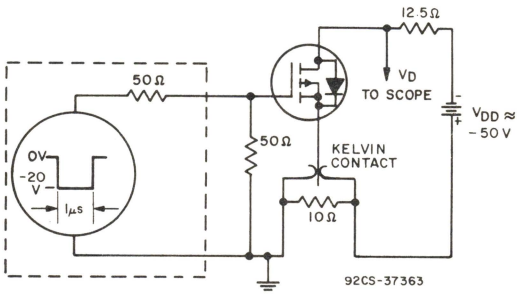


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFM10P12/10P15
RFP10P12/10P15

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -10A, -120V and -150V
- $r_{DS(on)} = 0.5\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

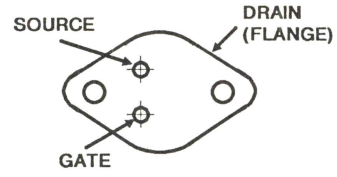
Description

The RFM10P12 and RFM10P15 and the RFP10P12 and RFP10P15 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

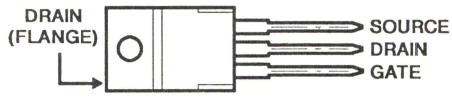
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW



TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	RFM10P12	RFM10P15	RFP10P12	RFP10P15	UNITS
Drain-Source Voltage ..... V_{DS}	-120	-150	-120	-150	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	-120	-150	-120	-150	V
Continuous Drain Current					
RMS Continuous ..... I_D	10	10	10	10	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	100	100	75	75	W
Above T_C = +25°C, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1595**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V V_{DS} = -120 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = -100 V V_{DS} = -120 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 10 A V_{GS} = -10 V	—	-6.0	—	-6.0	V
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V	—	1700	—	1700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	350	—	350	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -75 V	24(typ)	50	24(typ)	50	ns
Rise Time	t_r	I_D = 5 A	74(typ)	150	74(typ)	150	ns
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = R_{gs} = 50 Ω	138(typ)	225	138(typ)	225	ns
Fall Time	t_f	V_{GS} = -10 V	61(typ)	100	61(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10P12, RFM10P15	—	1.25	—	1.25	°C/W
		RFP10P12, RFP10P15	—	1.67	—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, dI_F/d_t = 100 A/μs	210 (typ.)		210 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

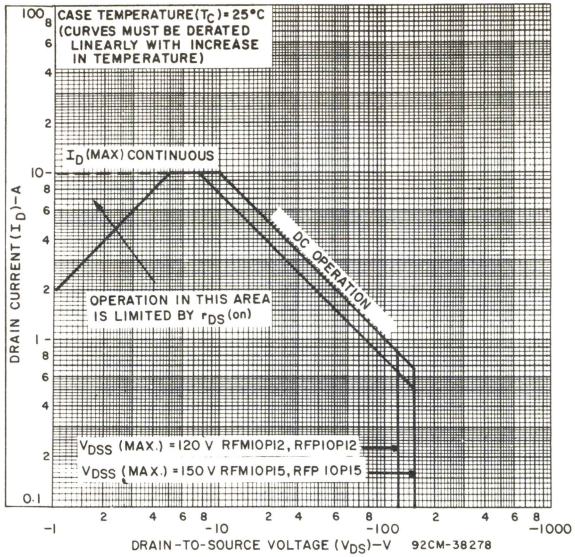


Fig. 1 - Maximum safe operating areas for all types.

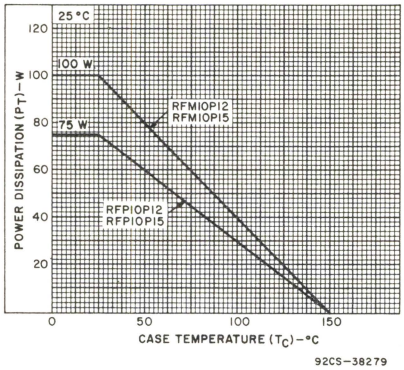


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

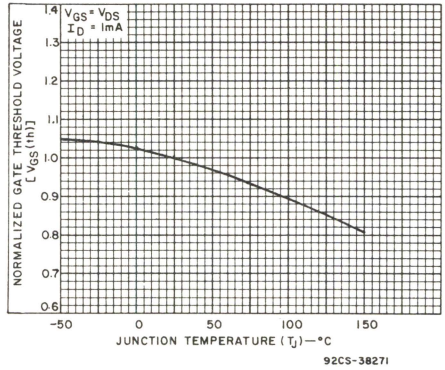


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

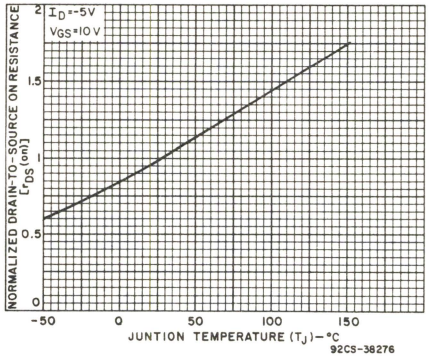


Fig. 4 - Normalized drain-to-source on resistance as as function of junction temperature for all types.

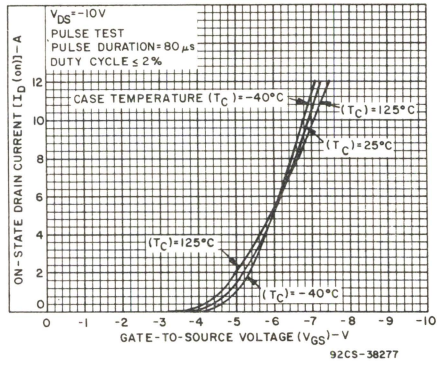


Fig. 5 - Typical transfer characteristics for all types.

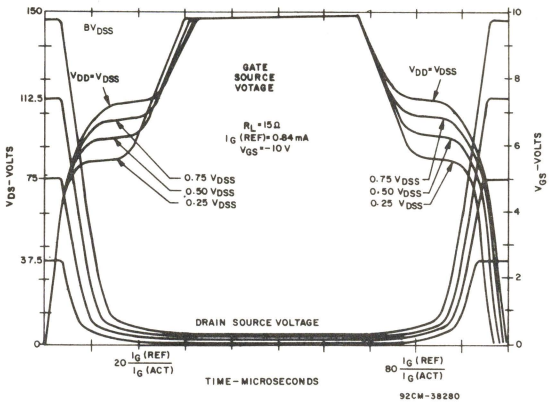


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

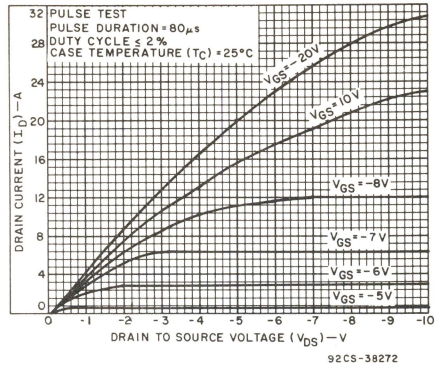


Fig. 7 - Typical saturation characteristics for all types.

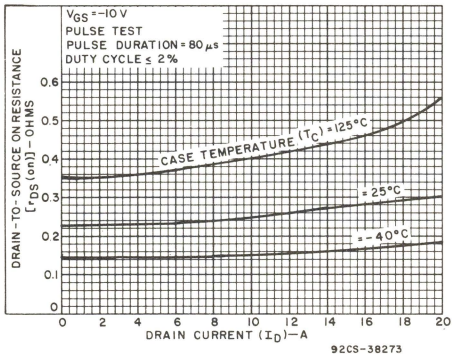


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

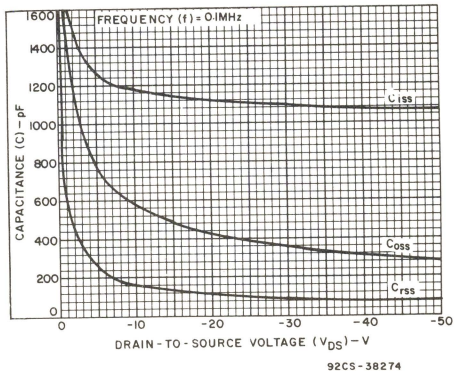


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

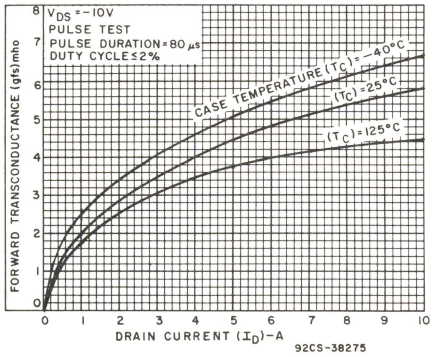


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

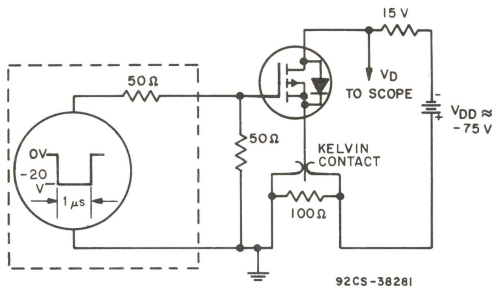


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFM12P08/12P10
RFP12P08/12P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -12A, -80V and -100V
- $r_{DS(on)} = 0.3\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

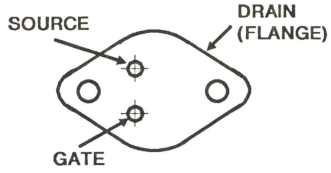
Description

The RFM12P08 and RFM12P10 and the RFP12P08 and RFP12P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

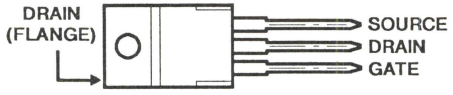
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Packages

TO-204AA
BOTTOM VIEW

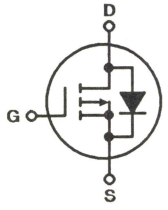


TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

	RFM12P08	RFM12P10	RFP12P08	RFP12P10	UNITS
Drain-Source Voltage ..... V_{DS}	-80	-100	-80	-100	V
Drain-Gate Voltage (R_{GS} = 1mΩ) ..... V_{DGR}	-80	-100	-80	-100	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	100	100	75	75	W
Above T_C = +25°C, Derate Linearly	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1495**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=12 A V_{GS}=-10 V	—	-4.8	—	-4.8	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	.3	—	.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	300	—	300	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=6 A	90(typ)	175	90(typ)	175	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	144(typ)	275	144(typ)	275	ns
Fall Time	t_f	V_{GS}=-10 V	94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12P08, RFM12P10	—	1.25	—	1.25	°C/W
		RFP12P08, RFP12P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

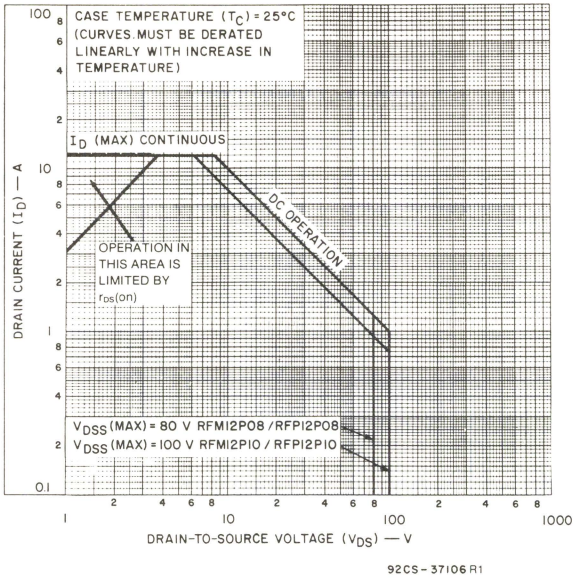


Fig. 1 — Maximum safe operating areas for all types.

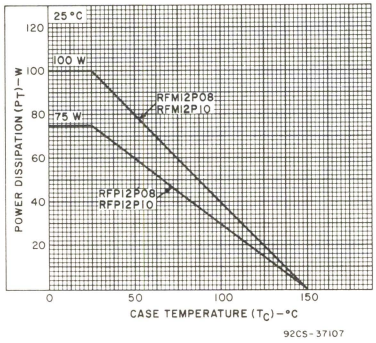


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

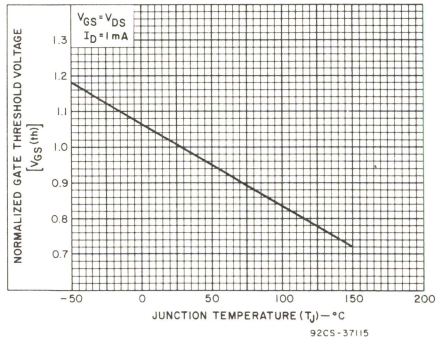


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

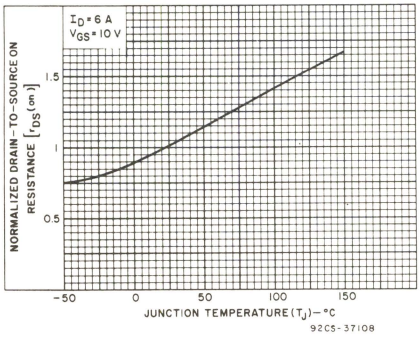


Fig. 4 — Normalized drain-to-source on resistance as a function of junction temperature for all types.

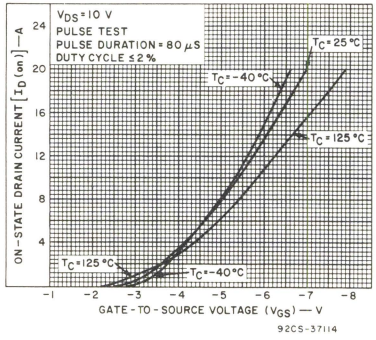


Fig. 5 — Typical transfer characteristics for all types.

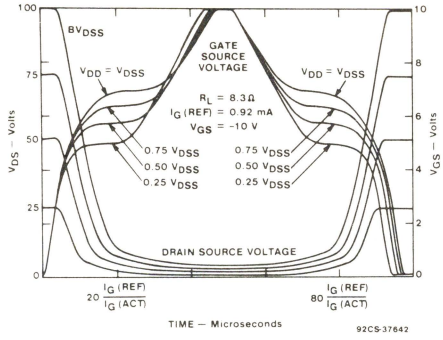


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

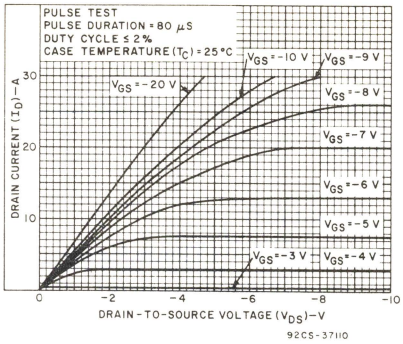


Fig. 7 — Typical saturation characteristics for all types.

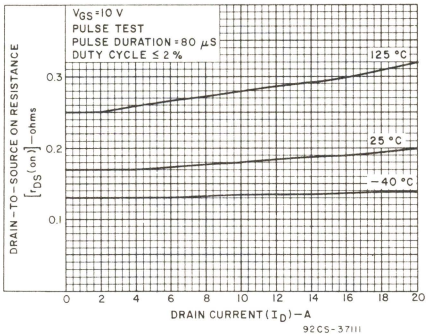


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

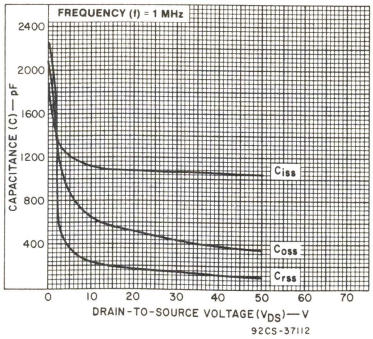


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

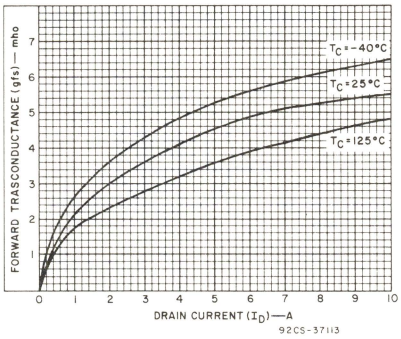


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

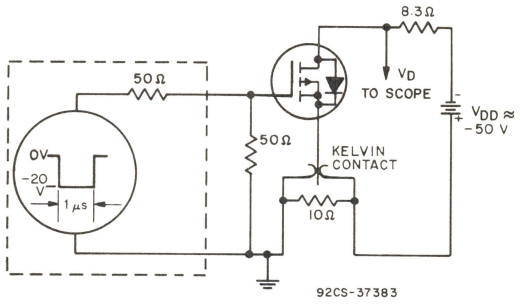


Fig. 11 — Switching Time Test Circuit

HARRIS

RFD15P05/05SM
RFP15P05

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

May 1992

Features

- -15A, -50V
- $r_{DS(on)} = 0.150\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

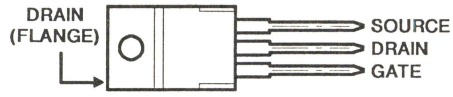
Description

The RFD15P05, RFD15P05SM and RFP15P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

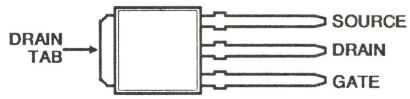
The RFD15P05 is supplied in the JEDEC TO-251AA plastic package and the RFD15P05SM in the TO-252AA plastic package. The RFP15P05 is supplied in the JEDEC TO-220AB plastic package.

Packages

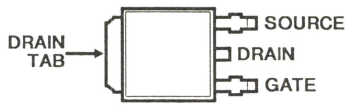
TO-220AB
TOP VIEW



TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-50V
Drain-Gate Voltage, (R_{GS} = 1MΩ), V_{DGR}	-50V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	-15A
Pulsed, I_{DM}	-40A
Avalanche Current, I_{AS}	See Figure 2
Power Dissipation, P_D:	
T_C = +25°C	80W
Derate Above T_C = +25°C	0.533W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55°C to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

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File Number **2387.1**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C			50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 15A, V_{GS} = -10V		-	0.150	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 7.5A Ig1 = Ig2 = 0.4A V_{GS} (clamp): -10V, +0.6V R_L = 3.3Ω (See Figure 12)		-	60	ns
Turn-On Delay Time	$t_{d(on)}$			-	16 (typ)	ns
Rise Time	t_r			-	30 (typ)	ns
Turn-Off Delay Time	$t_{d(off)}$			-	50 (typ)	ns
Fall Time	t_f				20 (typ)	ns
Turn-Off Time	$t_{(off)}$			-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -40V	-	150	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 15A	-	75	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 2.67Ω	-	3.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 15A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 7.5A, R_L = 3.33Ω L = 0.2µH, Ig1 = Ig2 = 0.4A V_{GS} (clamp): -10V, +0.6V		-	17	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$	TO-220AB, TO-251AA, TO-252AA		-	1.875	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA		-	100	°C/W
		TO-220AB		-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 15A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 15A, d_{ISD}/dt = 100A/µs	-	125	ns

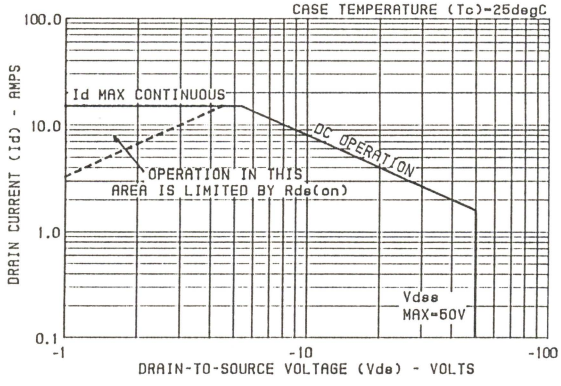


Figure 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

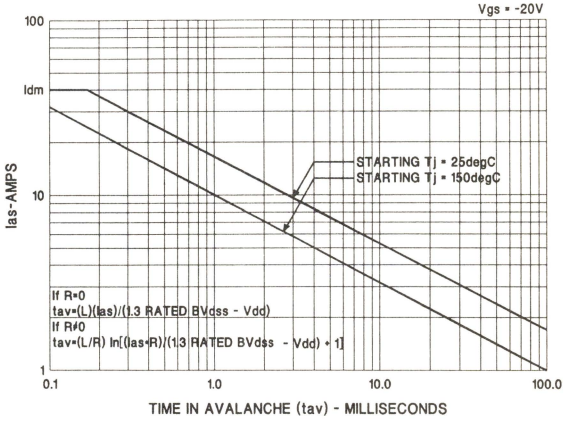


Figure 2 - Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

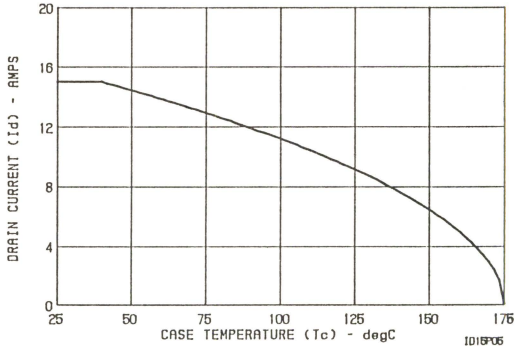


Figure 3 – Maximum continuous drain current vs. temperature.

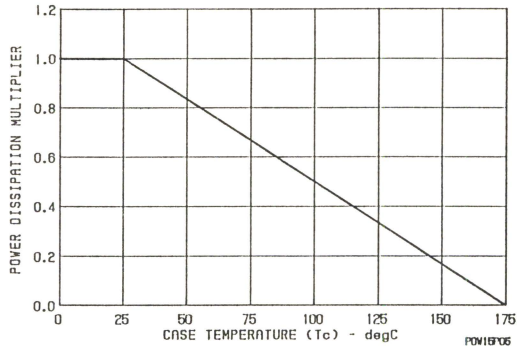


Figure 4 – Normalized power dissipation vs temperature derating curve.

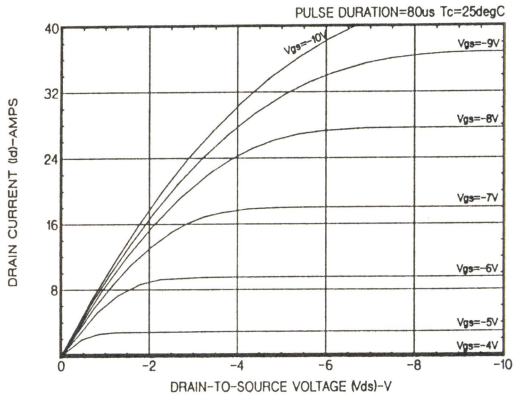


Figure 5 – Typical saturation characteristics.

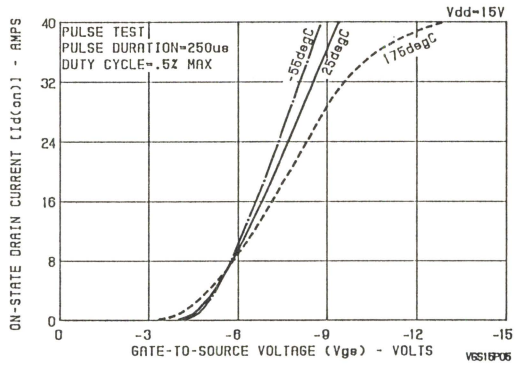


Figure 6 – Typical transfer characteristics.

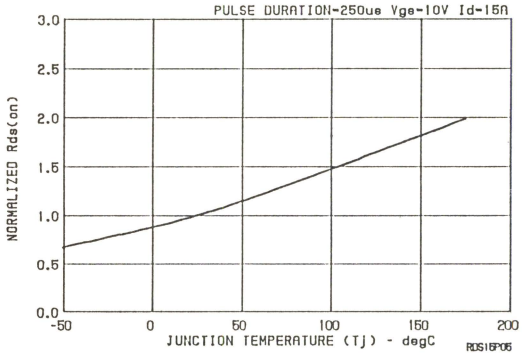


Figure 7 – Normalized rDS(on) vs junction temperature.

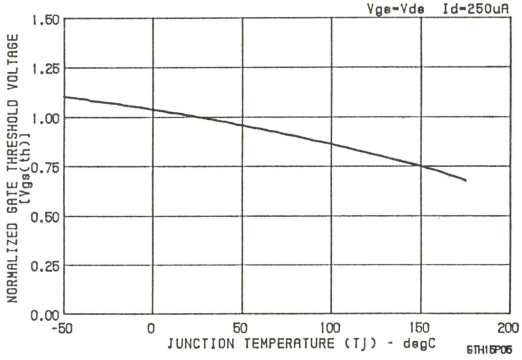


Figure 8 – Normalized gate threshold voltage.

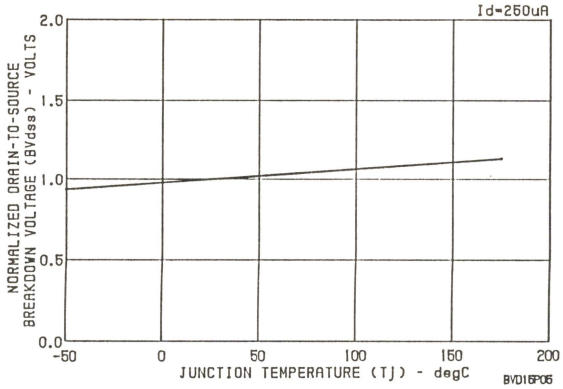


Figure 9 - Normalized drain source breakdown voltage vs temperature.

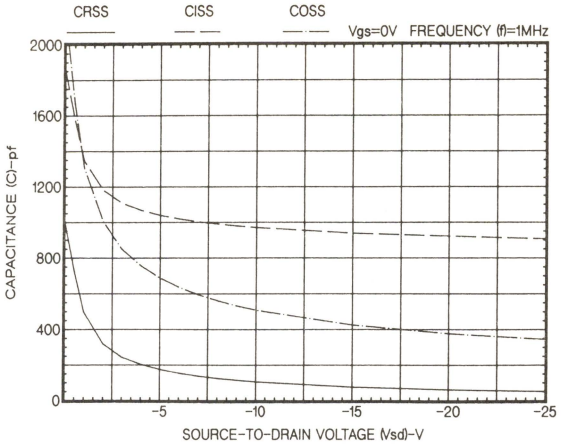


Figure 10 - Typical capacitance vs voltage.

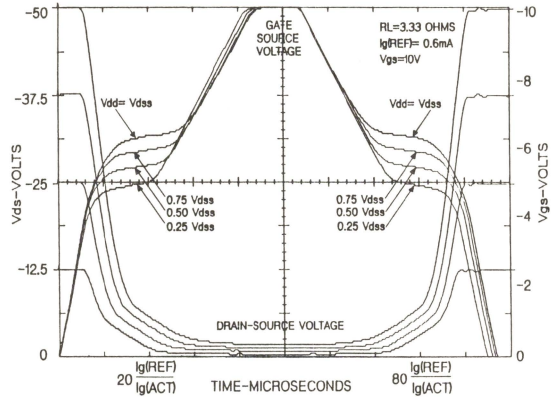
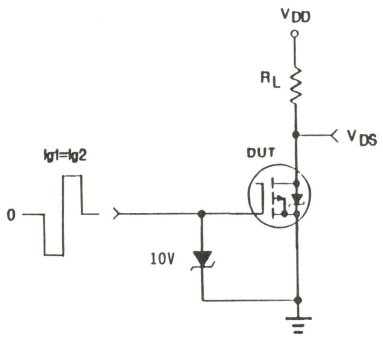
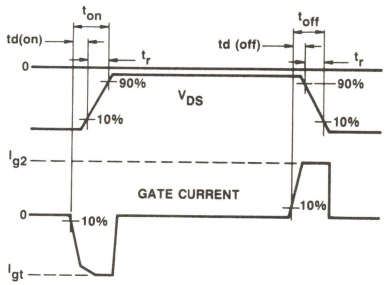


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.



Switching Test Circuit



Switching Waveforms

Figure 12 - Resistive switching.

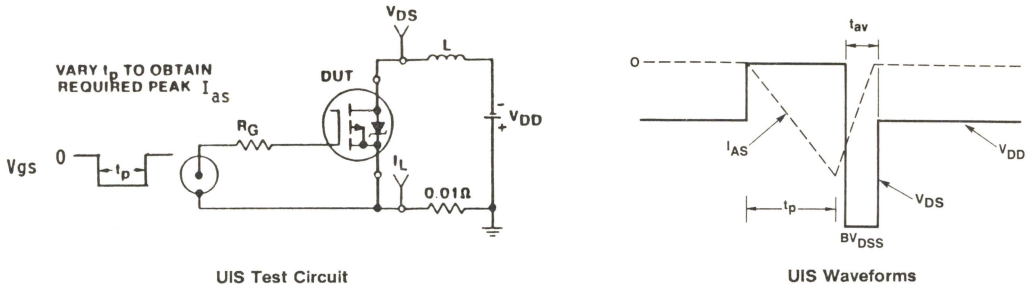


Figure 13 - Unclamped-inductive-switching test.

HARRIS

RFH25P08/25P10
RFK25P08/25P10

P-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- -25A, -100V and -80V
- $r_{DS(on)} = 0.15\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

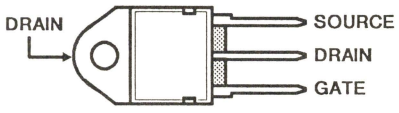
Description

The RFH25P08 and RFH25P10 and the RFK25P08 and RFK25P10 are p-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

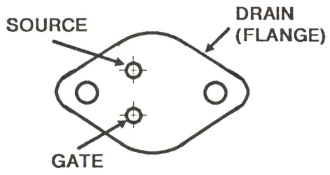
The RFH series types are supplied in the JEDEC TO-218AC plastic package and the RFK series types in the JEDEC TO-204AE steel package.

Packages

TO-218AC
TOP VIEW



TO-204AE
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

	RFH25P08	RFH25P10	RFK25P08	RFK25P10	UNITS
Drain-Source Voltage ..... V_{DS}	-80	-100	-80	-100	V
Drain-Gate Voltage ($R_{GS} = 1m\Omega$) ..... V_{DGR}	-80	-100	-80	-100	V
Continuous Drain Current					
RMS Continuous ..... I_D	-25	-25	-25	-25	A
Pulsed Drain Current ..... I_{DM}	-60	-60	-60	-60	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	150	150	150	150	W
Above $T_C = +25^oC$, Derate Linearly	1.2	1.2	1.2	1.2	W/°C
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **1632**

Electrical Characteristics (T_C = 25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFH25P08 RFK25P08		RFH25P10 RFK25P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1.0mA, V_{GS} = 0	-80	-	-100	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65V	-	-1	-	-	μA
		V_{DS} = -80V	-	-	-	-1	μA
		T_C = 125°C V_{DS} = -65V	-	-50	-	-	μA
		V_{DS} = -80V	-	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	100	-	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 12.5A, V_{GS} = -10V	-	-1.88	-	-1.88	V
		I_D = 25A, V_{GS} = -10V	-	-4.5	-	-4.5	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 12.5A, V_{GS} = -10V	-	0.15	-	0.15	Ω
Forward Transconductance	g_{ts}*	I_D = 12.5A, V_{DS} = -10V	4	-	4	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V f = 1MHz	-	3000	-	3000	pF
Output Capacitance	C_{OSS}		-	1500	-	1500	pF
Reverse Transfer Capacitance	C_{RSS}		-	600	-	600	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 12.5A, V_{DS} = -50V R_{GEN} = R_{GS} = 50Ω V_{GS} = -10V	35 (typ)	50	35 (typ)	50	ns
Rise Time	t_r		165 (typ)	250	165 (typ)	250	ns
Turn-Off Delay Time	$t_{d(off)}$		270 (typ)	400	270 (typ)	400	ns
Fall Time	t_f		165 (typ)	250	165 (typ)	250	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK25P08, RFK25P10	-	0.83	-	0.83	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFH25P08 RFK25P08		RFH25P10 RFK25P10		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}**	I_{SD} = -12.5A	-	1.4	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/dt = 100A/μs	-	300 (typ)	-	300 (typ)	ns

** Pulsed test: Width ≤ 300μs, duty cycle ≤ 2%.

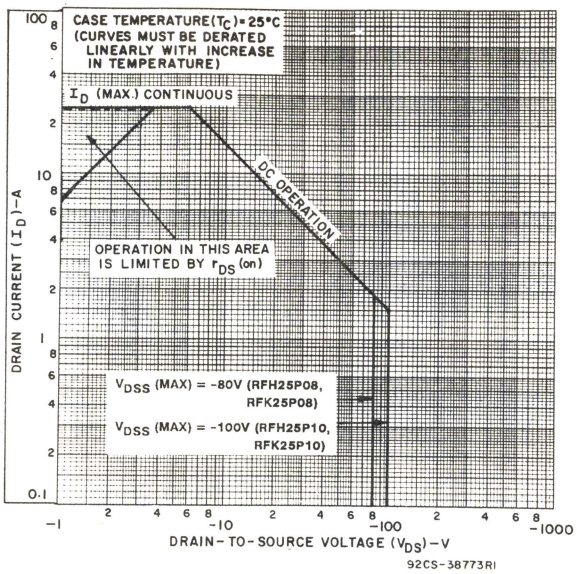


Fig. 1 - Maximum safe operating areas for all types.

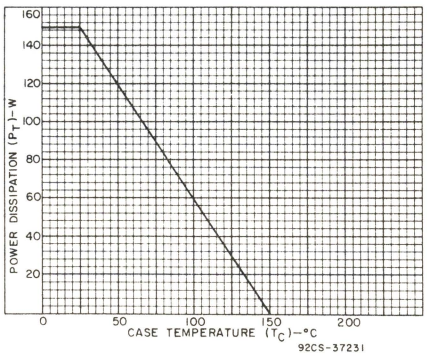


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

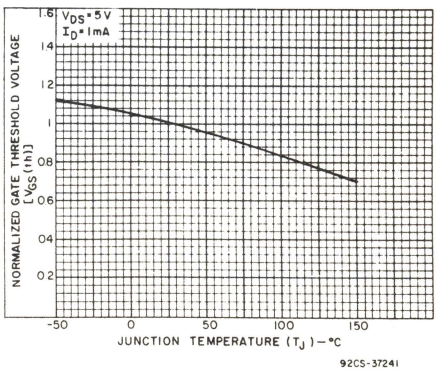


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

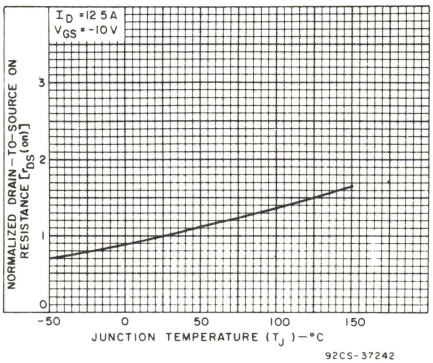


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

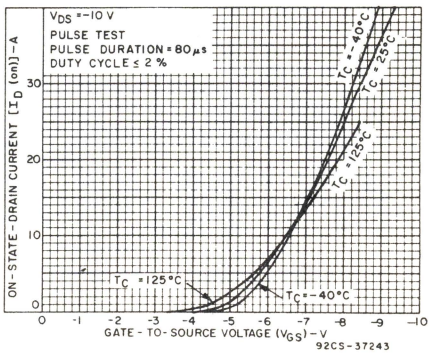


Fig. 5 - Typical transfer characteristics for all types.

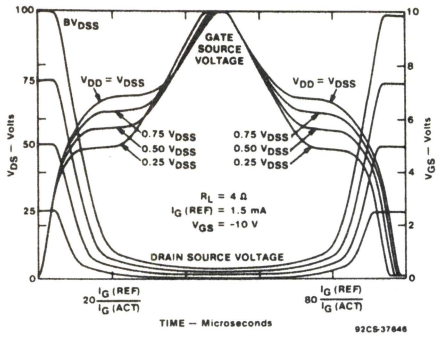


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

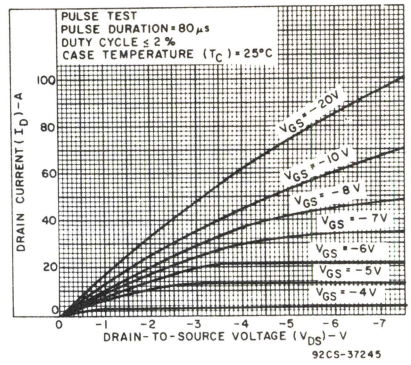


Fig. 7 - Typical saturation characteristics for all types.

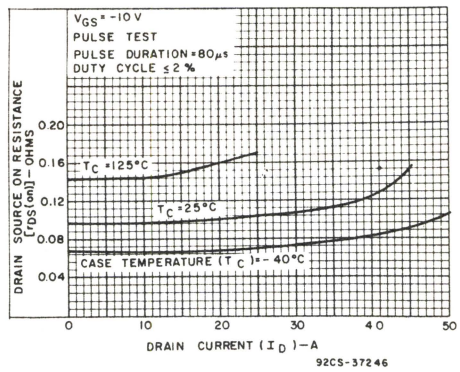


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

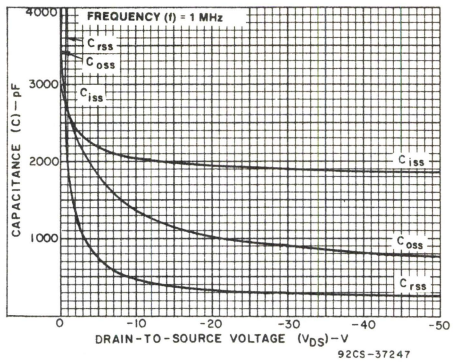


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

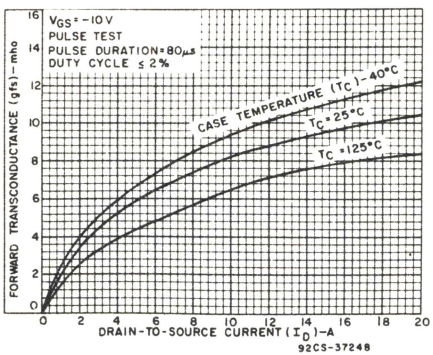


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

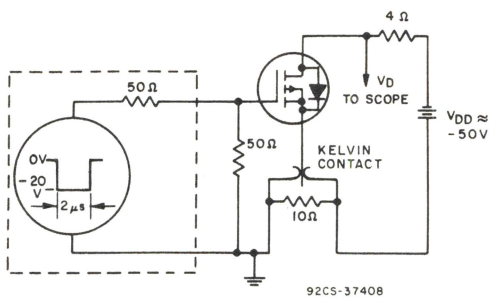


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFG30P05
RFP30P05

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

August 1991

Features

- -30A, -50V
- $r_{DS(on)} = 0.065\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

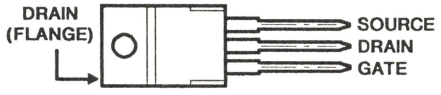
Description

The RFG30P05 and RFP30P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

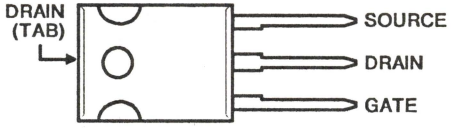
The RFG30P05 is supplied in the JEDEC TO-247 plastic package and the RFP30P05 in the TO-220AB plastic package.

Packages

TO-220AB
TOP VIEW

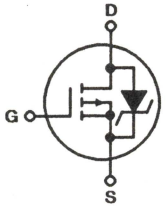


TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} ..... -50V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR} ..... -50V
Gate-Source Voltage, V_{GS} ..... ±20V
Drain Current:
  RMS Continuous, I_D ..... -30A
  Pulsed, I_{DM} ..... -75A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve
Power Dissipation, P_D:
  T_C = +25°C 120W
  Derate Above T_C = +25°C ..... 0.8W/°C
Operating and Storage Junction
Temperature Range, T_J, T_{STG} ..... -55 to +175°C

5 P-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.
Copyright © Harris Corporation 1991

File Number 2436

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C			50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 30A, V_{GS} = -10V		-	0.0.65	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 15A Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V R_L = 1.67Ω		-	80	ns
Turn-On Delay Time	$t_{d(on)}$			15 (typ)	-	ns
Rise Time	t_r			23 (typ)	-	ns
Turn-Off Delay Time	$t_{d(off)}$			28 (typ)	-	ns
Fall Time	t_f			18 (typ)	-	ns
Turn-Off Time	$t_{(off)}$			-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -40V	-	200	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 40A	-	100	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 1.33Ω	-	2	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 30A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 15A, R_L = 1.67Ω L = 0.2µH, Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V		-	75	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	1.25	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 30A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 30A, dI_{SD}/dt = 100A/µs	-	150	ns

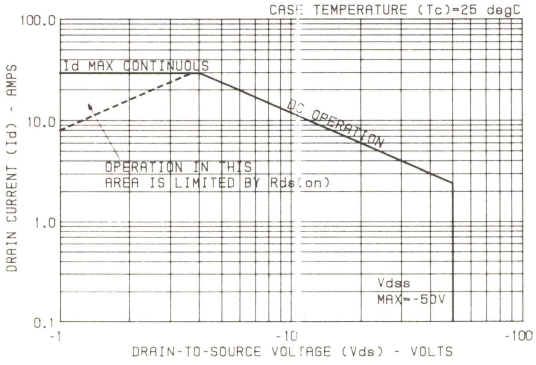


Figure 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

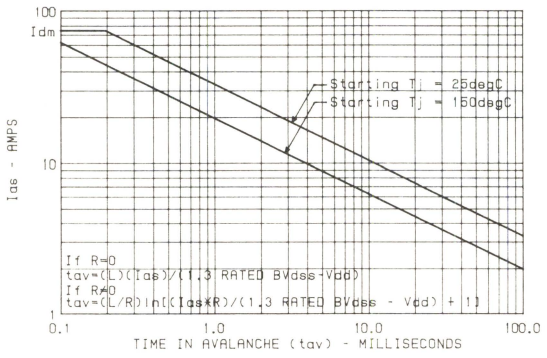


Figure 2 - Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

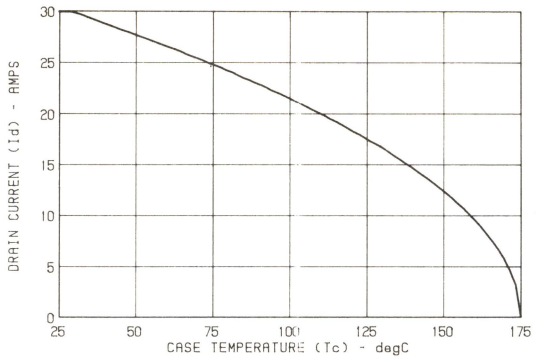


Figure 3 - Maximum continuous drain current vs case temperature.

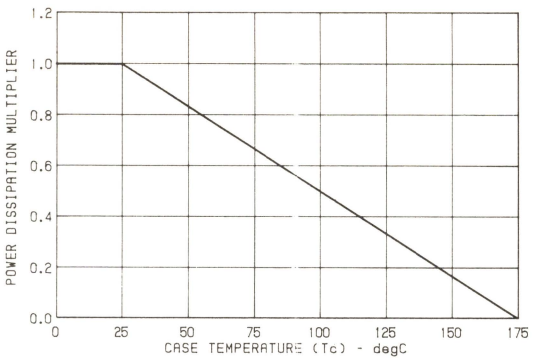


Figure 4 - Normalized power dissipation vs case temperature.

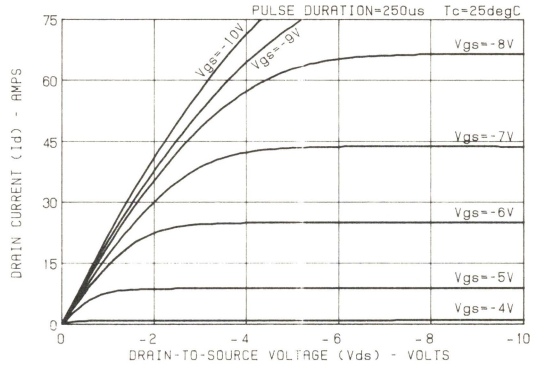


Figure 5 - Typical saturation characteristics.

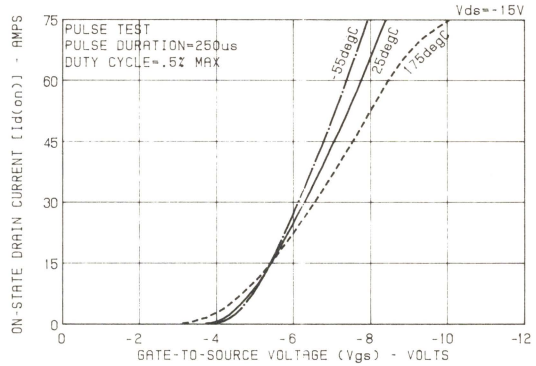


Figure 6 - Typical transfer characteristics.

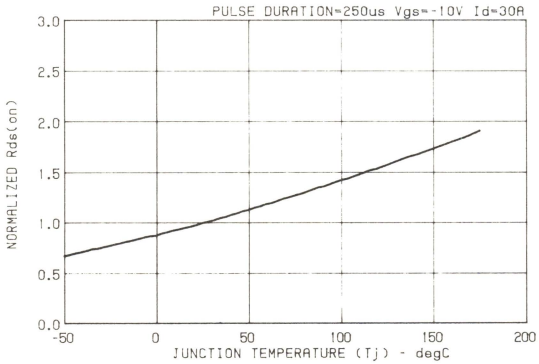


Figure 7 - Normalized on-state resistance vs junction temperature.

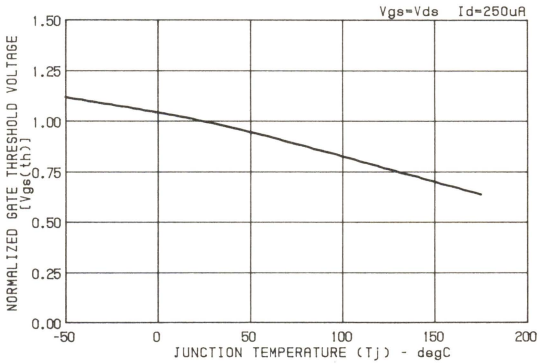


Figure 8 - Normalized gate threshold voltage vs junction temperature.

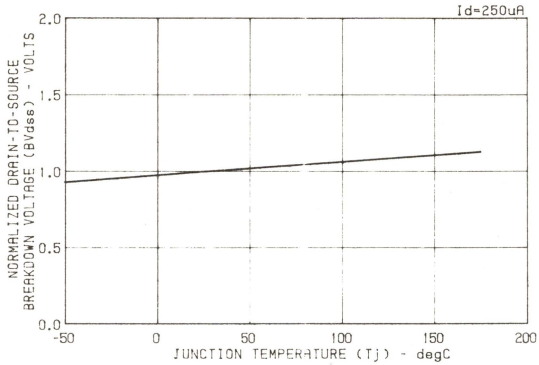


Figure 9 - Normalized drain source breakdown voltage vs junction temperature.

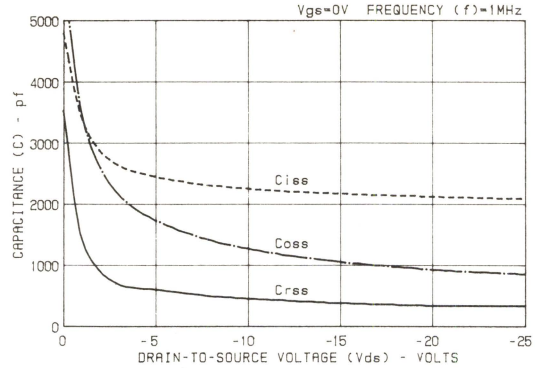


Figure 10 - Typical capacitance vs voltage.

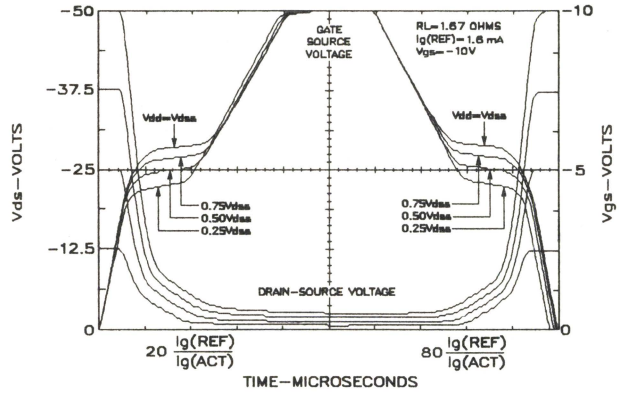
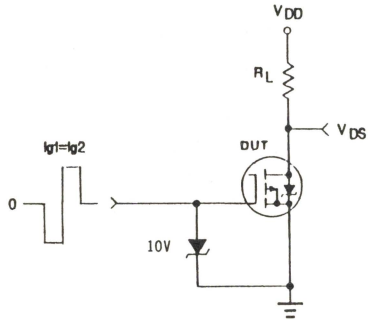
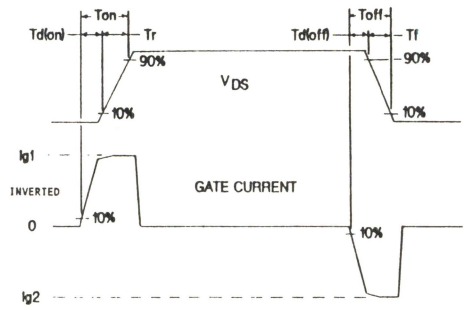


Figure 11 - Normalized switching waveforms for constant gate current. (Refer to application notes AN-7254 and AN-7260.)

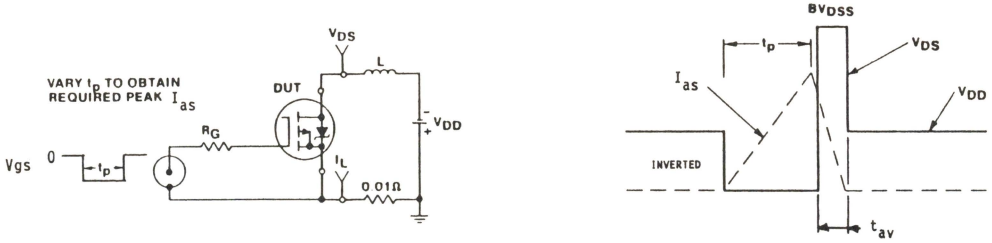


Switching Test Circuit



Switching Waveforms

Figure 12 - Resistive switching.



UIS Test Circuit **UIS Waveforms**

Figure 13 – Unclamped-inductive-switching test.

HARRIS

RFG30P06
RFP30P06

P-Channel Enhancement Mode Power Field Effect Transistors (MegaFETs)

August 1991

Features

- -30A, -60V
- $r_{DS(on)} = 0.075\ \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

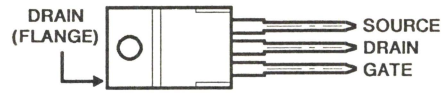
Description

The RFG30P06 and RFP30P06 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

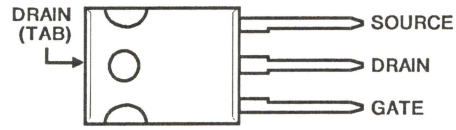
The RFG30P06 is supplied in the JEDEC TO-247 plastic package and the RFP30P06 in the TO-220AB plastic package.

Packages

TO-220AB
TOP VIEW



TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-60V
Drain-Gate Voltage, (R_{GS} = 1mΩ), V_{DGR}	-60V
Gate-Source Voltage, V_{GS}	±20V
Drain Current:	
RMS Continuous, I_D	-30A
Pulsed, I_{DM}	-75A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve	
Power Dissipation, P_D:	
T_C = +25°C	135W
Derate Above T_C = +25°C	0.9W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

Copyright © Harris Corporation 1991

File Number **2437**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-60	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C			50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 30A, V_{GS} = -10V		-	0.075	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -30V, I_D = 15A Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V R_L = 2.0Ω		-	60	ns
Turn-On Delay Time	$t_{d(on)}$			15 (typ)	-	ns
Rise Time	t_r			23 (typ)	-	ns
Turn-Off Delay Time	$t_{d(off)}$			28 (typ)	-	ns
Fall Time	t_f			18 (typ)	-	ns
Turn-Off Time	$t_{(off)}$			-	100	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -48V	-	200	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 30A	-	100	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 1.6Ω	-	7	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 30A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -30V, I_D = 15A, R_L = 2.0Ω L = 0.2µH, Ig1 = Ig2 = 0.8A V_{GS} (clamp): -10V, +0.6V		-	75	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	1.11	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 30A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 30A, d_{ISD}/dt = 100A/µs	-	150	ns

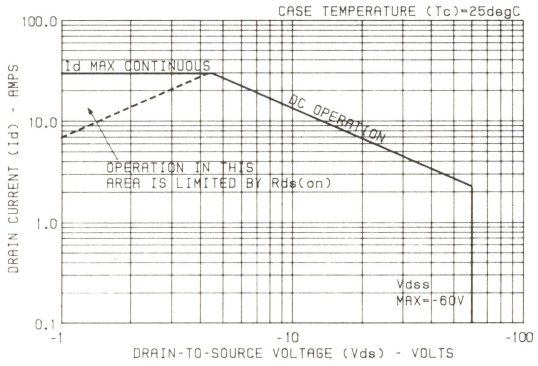


Figure 1 – Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

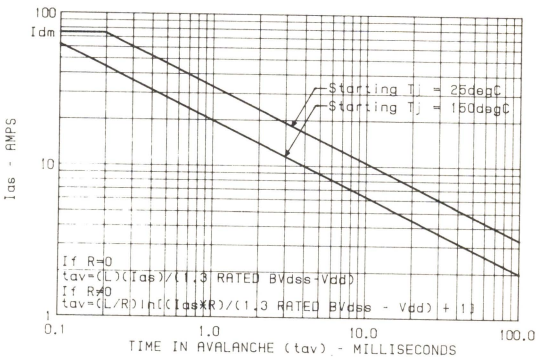


Figure 2 – Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

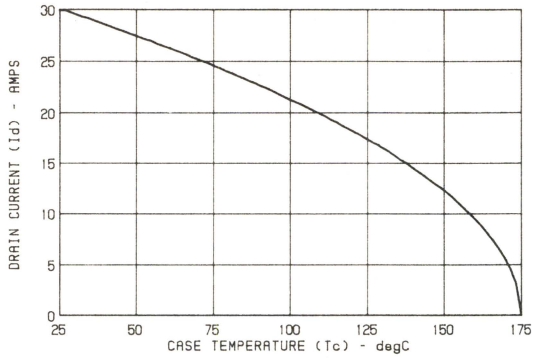


Figure 3 - Maximum continuous drain current vs case temperature.

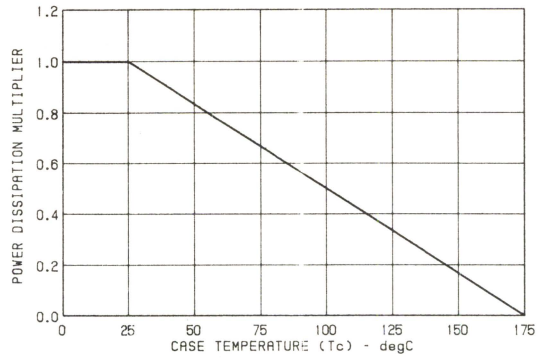


Figure 4 - Normalized power dissipation vs case temperature.

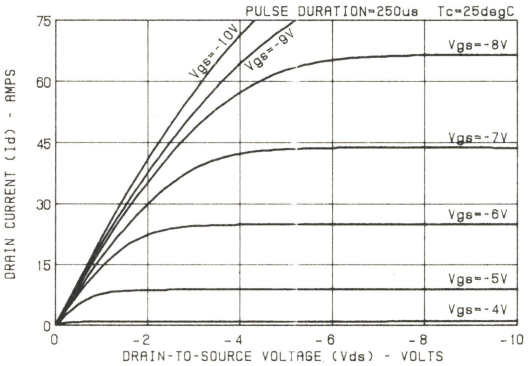


Figure 5 - Typical saturation characteristics.

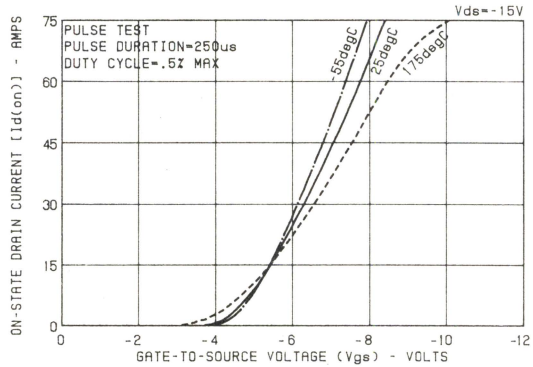


Figure 6 - Typical transfer characteristics.

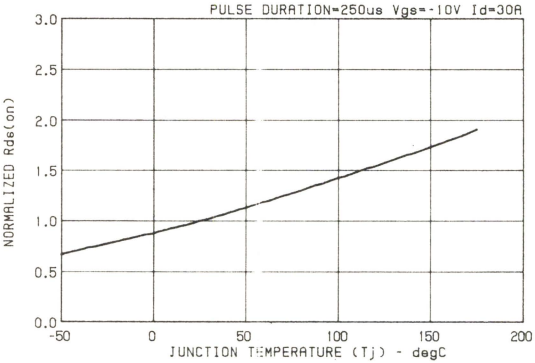


Figure 7 - Normalized on-state resistance vs junction temperature.

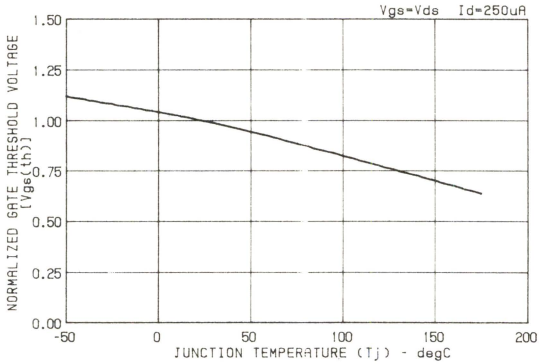


Figure 8 - Normalized gate threshold voltage vs junction temperature.

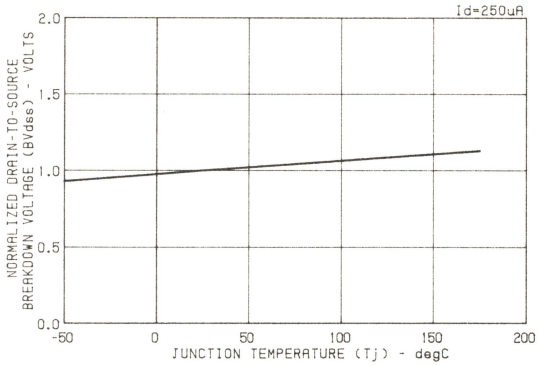


Figure 9 – Normalized drain source breakdown voltage vs junction temperature.

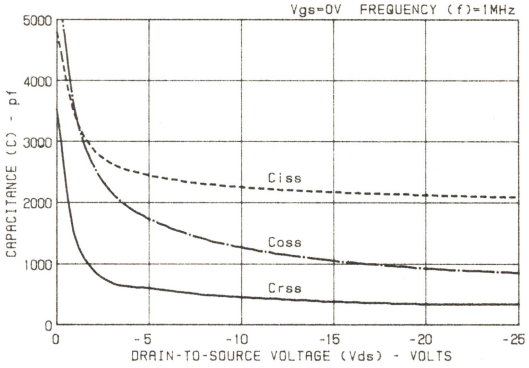


Figure 10 – Typical capacitance vs voltage.

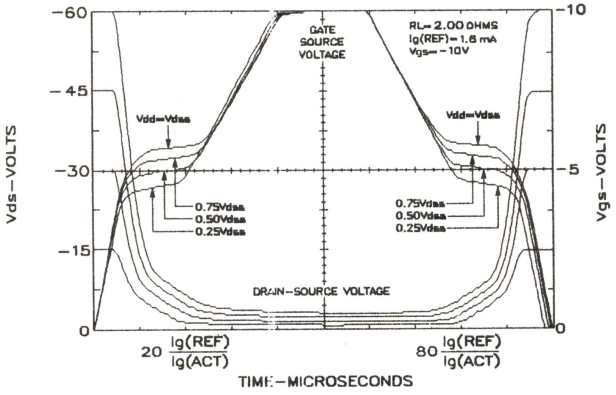


Figure 11 – Normalized switching waveforms for constant gate current.
(Refer to application notes AN-7254 and AN-7260.)

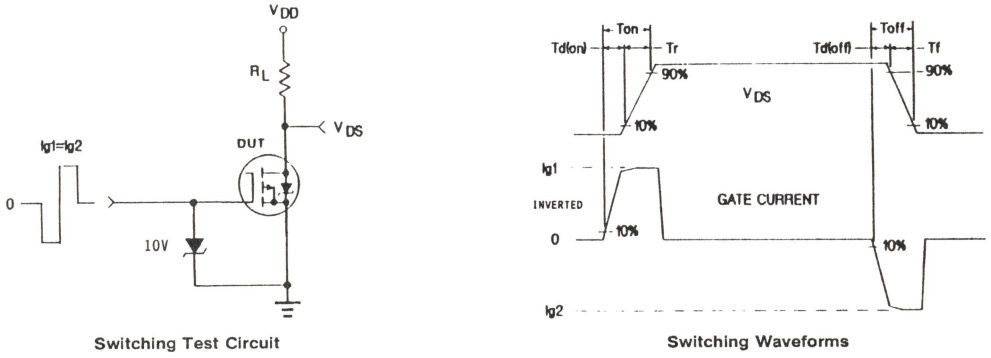
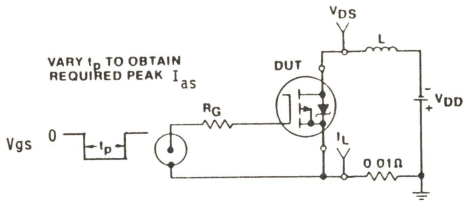
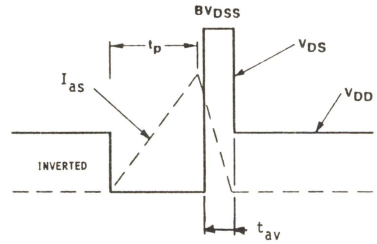


Figure 12 – Resistive switching.



UIS Test Circuit



UIS Waveforms

Figure 13 - Unclamped-inductive-switching test.

HARRIS

RFG60P05E
RFG60P06E

P-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

January 1994

Features

- RFG60P05E = -60A, -50V, $r_{DS(on)}$ = 0.026Ω
- RFG60P06E = -60A, -60V, $r_{DS(on)}$ = 0.030Ω
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

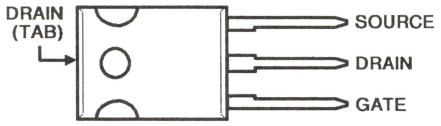
Description

The RFG60P05E and RFG60P06E p-channel ESD rated power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFG60P05E and RFG60P06E are supplied in the JEDEC TO-247 plastic package.

Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE

Absolute Maximum Ratings (T_C = 25°C), Unless Otherwise Specified

		RFG60P05E	RFG60P06E	UNITS
Drain-Source Voltage	V_{DSS}	-50	-60	V
Drain-Gate Voltage (R_{GS} = 1mΩ)	V_{DGR}	-50	-60	V
Continuous Drain Current				
RMS Continuous	I_D	-60	-60	A
Pulsed Drain Current	I_{DM}	-150	-150	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	E_{SD}	2	2	KV
Single Pulse Avalanche Rating (Refer to UIS SOA Curve)				
Maximum Power Dissipation				
T_C = +25°C	P_D	190	215	W
Above T_C = +25°C, Derate Linearly		1.27	1.43	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **2745.2**

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-50	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V		-	1	µA
		T_C = 150°C		-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 60A, V_{GS} = -10V		-	0.026	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -25V, I_D = 30A Ig1 = Ig2 = 2.0A $V_{GS\ (clamp)}$: -10V, +0.6V R_L = 0.83Ω		-	125	ns
Turn-On Delay Time	$t_{d(on)}$			20 (typ)	-	ns
Rise Time	t_r			70 (typ)	-	ns
Turn-Off Delay Time	$t_{d(off)}$			65 (typ)	-	ns
Fall Time	t_f			20 (typ)	-	ns
Turn-Off Time	$t_{(off)}$			-	125	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -40V	-	450	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 60A	-	225	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 0.67Ω	-	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 60A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -25V, I_D = 30A, R_L = 0.83Ω L = 0.2µH, Ig1 = Ig2 = 2.0A $V_{GS\ (clamp)}$: -10V, +0.6V		-	300	µJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	0.79	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 60A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 60A, d_{ISD}/dt = 100A/µs	-	200	ns

Electrical Characteristics (T_C = +25°C) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0V		-60	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25 mA		-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48V, V_{GS} = 0V		-	1	μA
		T_C = 150°C		-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20V		-	100	nA
Static Drain-Source on Resistance	$r_{DS(on)}$	I_D = 60A, V_{GS} = -10V		-	0.030	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = -30V, I_D = 30A Ig1 = Ig2 = 2.0A $V_{GS(clamp)}$: -10V, +0.6V R_L = 1.0Ω		-	125	ns
Turn-On Delay Time	$t_{d(on)}$			20 (typ)	-	ns
Rise Time	t_r			60 (typ)	-	ns
Turn-Off Delay Time	$t_{d(off)}$			65 (typ)	-	ns
Fall Time	t_f			20 (typ)	-	ns
Turn-Off Time	$t_{(off)}$			-	125	ns
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to -20V	V_{DD} = -48V	-	450	nC
Gate Charge at -10V	$Q_{g(-10V)}$	V_{GS} = 0 to -10V	I_D = 60A	-	225	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to -2V	R_L = 0.8Ω	-	15	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 60A, V_{DS} = -15V		-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = -30V, I_D = 30A, R_L = 1.0Ω L = 0.2μH, Ig1 = Ig2 = 2.0A $V_{GS(clamp)}$: -10V, +0.6V		-	300	μJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	0.70	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 60A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 60A, d_{ISD}/dt = 100A/μs	-	200	ns

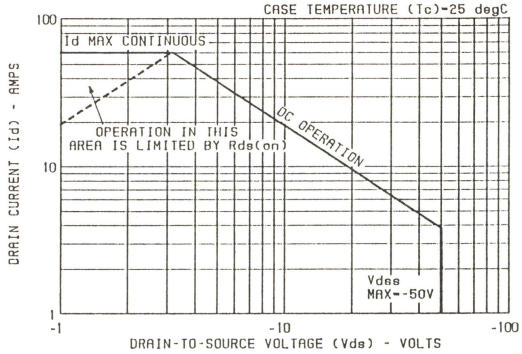

FIGURE 1. RFG60P05E - SAFE OPERATING AREA CURVE

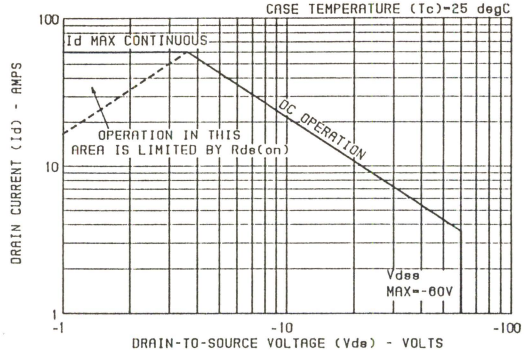

FIGURE 2. RFG60P06E - SAFE OPERATING AREA CURVE

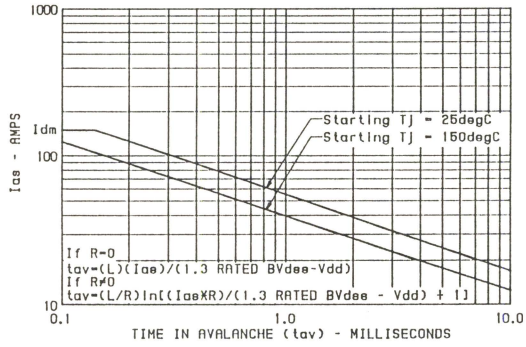

FIGURE 3. RFG60P05E - UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

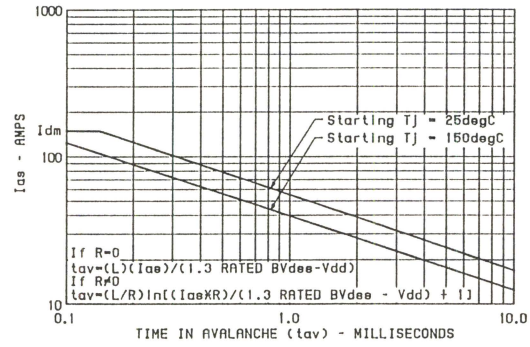

FIGURE 4. RFG60P06E - UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

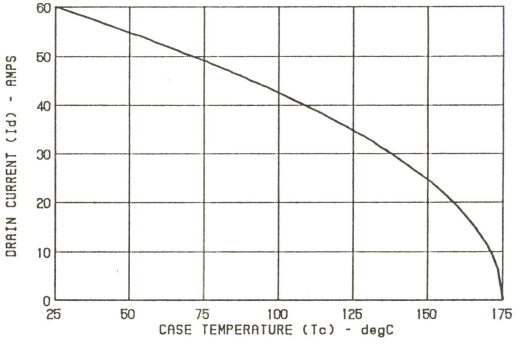

FIGURE 5. MAXIMUM CONTINUOUS DRAIN CURRENT VS TEMPERATURE

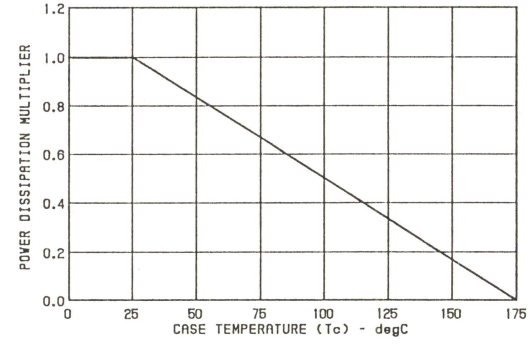

FIGURE 6. NORMALIZED POWER DISSIPATION VS TEMPERATURE

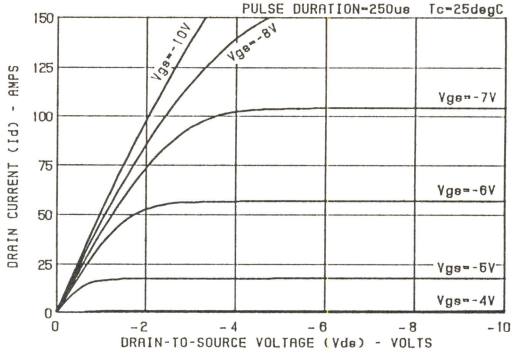

FIGURE 7. RFG60P05E - TYPICAL SATURATION CHARACTERISTICS

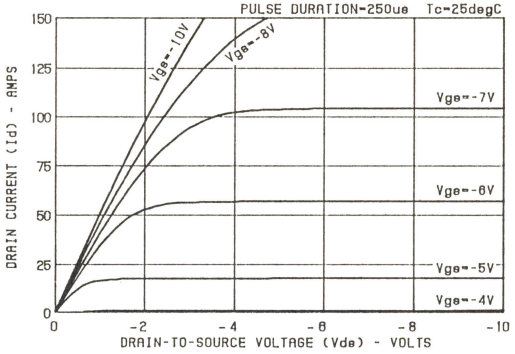

FIGURE 8. RFG60P06E - TYPICAL SATURATION CHARACTERISTICS

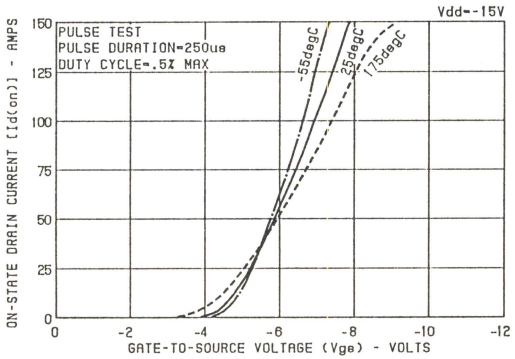

FIGURE 9. RFG60P05E - TYPICAL TRANSFER CHARACTERISTICS

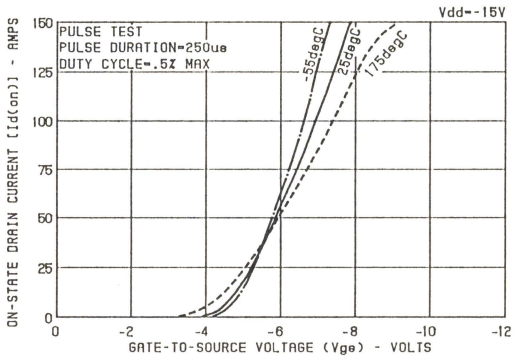

FIGURE 10. RFG60P06E - TYPICAL TRANSFER CHARACTERISTICS

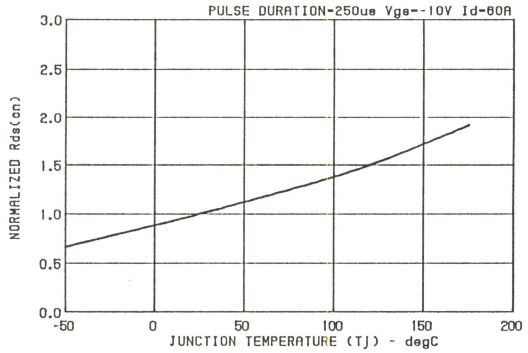

FIGURE 11. NORMALIZED $r_{DS(ON)}$ VS JUNCTION TEMPERATURE

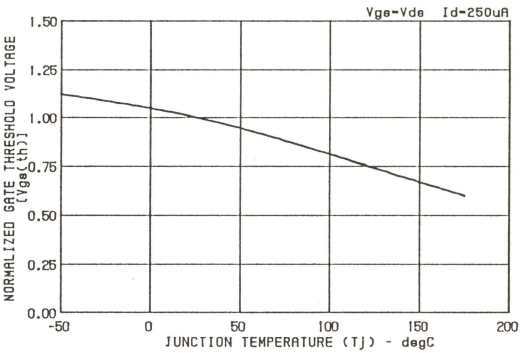

FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE

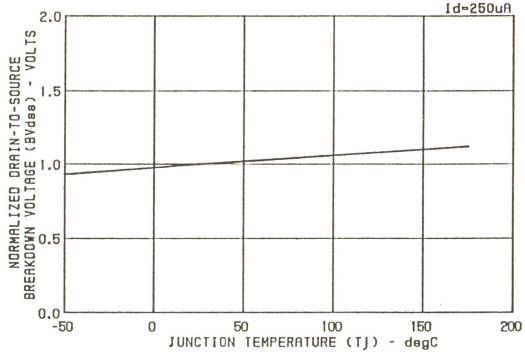

FIGURE 13. DRAIN SOURCE BREAKDOWN VOLTAGE VS TEMPERATURE

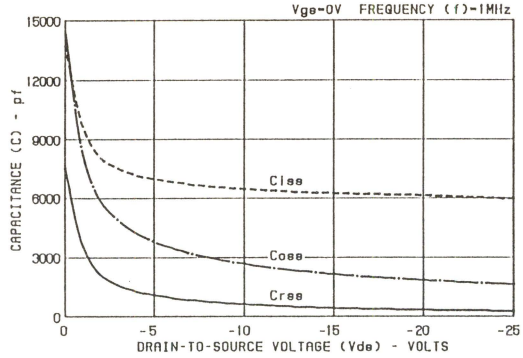

FIGURE 14. TYPICAL CAPACITANCE VS VOLTAGE

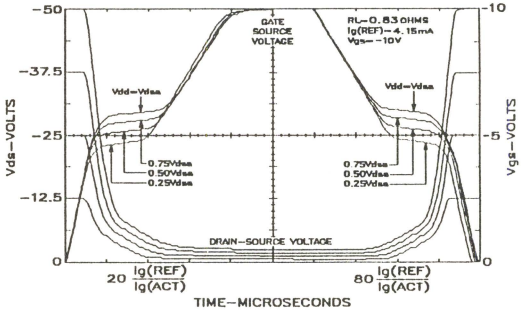

FIGURE 15. RFG60P05E - NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT

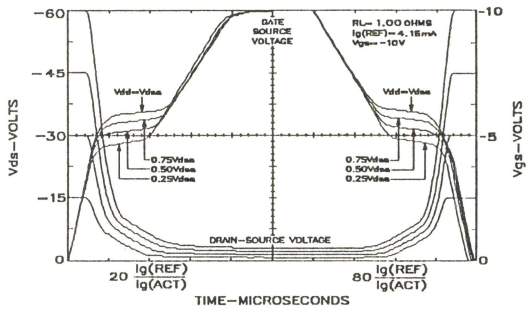

FIGURE 16. RFG60P06E - NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT

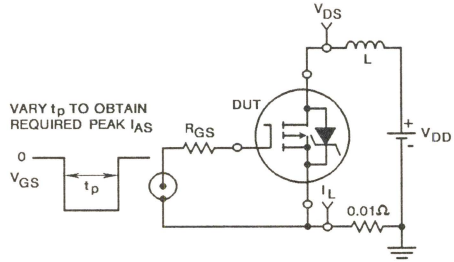

FIGURE17a. UIS TEST CIRCUIT

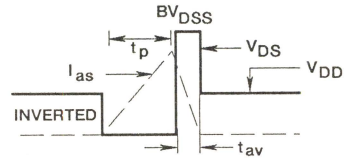

FIGURE 17b. UIS WAVEFORMS

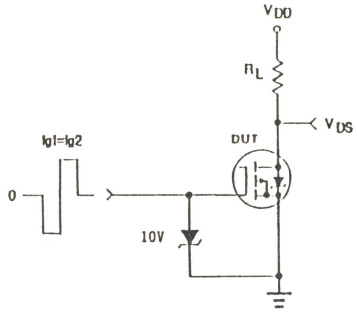

FIGURE 18a. SWITCHING TEST CIRCUIT

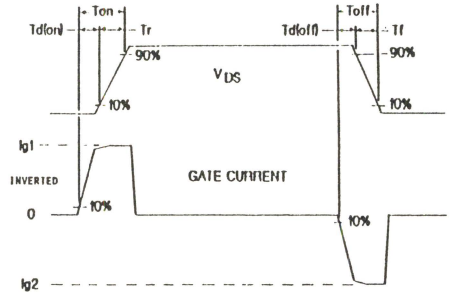

FIGURE 18b. SWITCHING WAVEFORMS

POWER MOSFETs 6

LOGIC LEVEL POWER MOSFETs

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RFL1N08L, RFL1N10L	N-Channel Logic Level Power Field-Effect Transistors (L^2FET)	6-19
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RFL1N18L, RFL1N20L	N-Channel Logic Level Power Field-Effect Transistors (L^2FET)	6-27
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RFM8N18L/20L, RFP8N18L/20L	N-Channel Logic Level Power Field-Effect Transistors (L^2FET)	6-62
RFM10N12L/15L, RFP10N12L/15L	N-Channel Logic Level Power Field-Effect Transistors (L^2FET)	6-66
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RFD14N05L/05LSM, RFP14N05L	N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors	6-79
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RFD16N06LE, RFD16N06LESM	16A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)	6-93
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RFP25N06L	N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor (L^2FET)	6-108
RFP30N06LE	30A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFET (MegaFET)	6-113
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HARRIS

2N6901

August 1991

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

Features

- 1.69A, 100V
- $r_{DS(on)} = 1.4\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

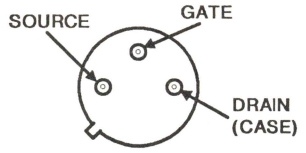
Description

The 2N6901 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6901 is supplied in the JEDEC TO-205AF metal package.

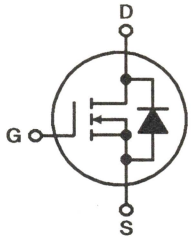
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6901	UNITS
Drain-Source Voltage	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	1.69*	A
Pulsed Drain Current	I_{DM}	5*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	8.33*	W
Above T_C = +25°C, Derate Linearly		0.0667*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering	T_L	260*	°C
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1877.1

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25° C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V	—	1	μA
			T_C = 125°C, V_{DS} = 80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 1.07 A, V_{GS} = 5 V	—	1.5	V
			I_D = 1.69 A, V_{GS} = 5 V	—	2.4	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 1.07 A, V_{GS} = 5 V	—	1.4	Ω
			T_C = 125°C, I_D = 1.07 A, V_{GS} = 5 V	—	2.6	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 1.07 A	500	2000	mmho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	50	200	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	20	80	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	5	20	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	—	25	ns
*	Rise Time	t_r	I_D = 1.07 A	—	45	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	45	
*	Fall Time	t_f	V_{GS} = 5 V	—	80	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1.69 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 1 A, d_{IF}/dt = 50 A/μs	—	250	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

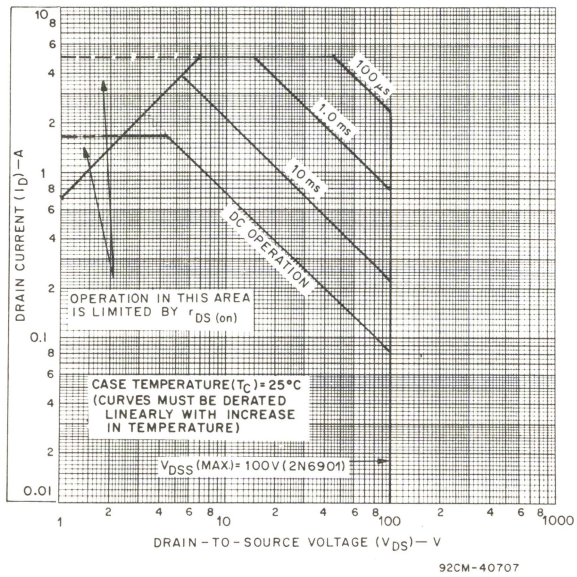


Fig. 1 - Maximum operating areas.

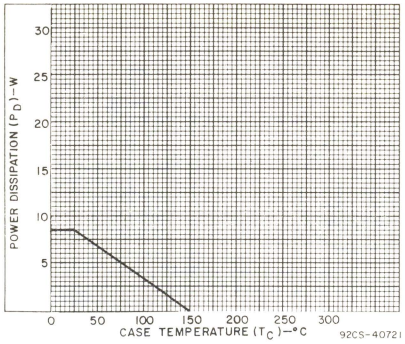


Fig. 2 - Power dissipation vs. temperature derating curve.

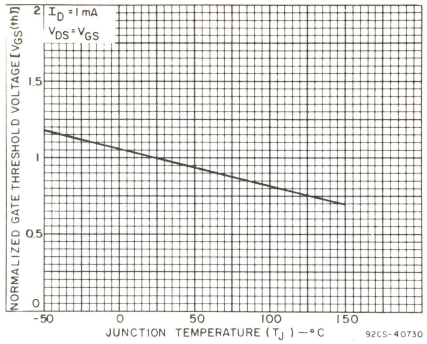


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

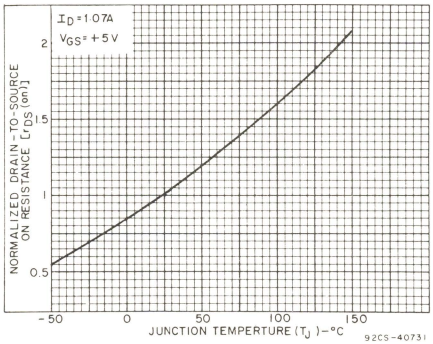


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

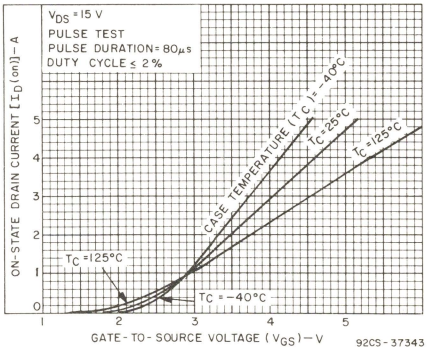


Fig. 5 - Typical transfer characteristics.

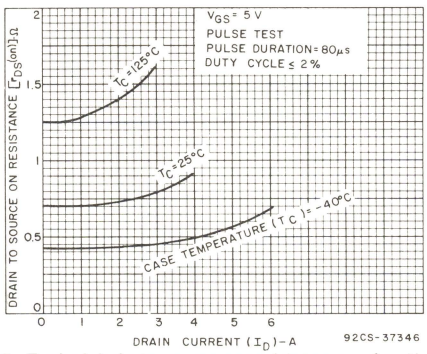


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

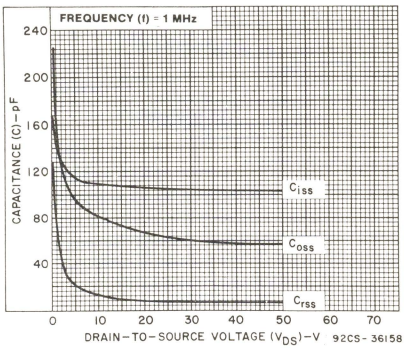


Fig. 7 - Capacitance as a function of drain-to-source voltage.

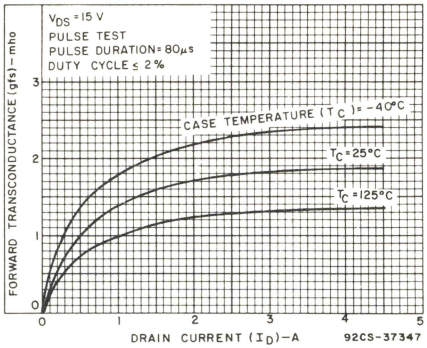


Fig. 8 - Typical forward transconductance as a function of drain current.

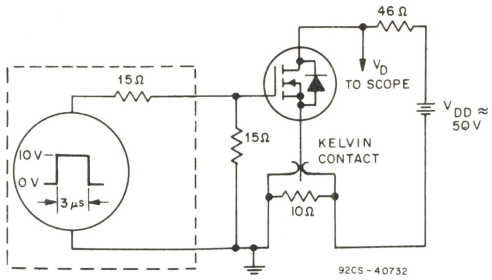


Fig. 9 - Switching time test circuit.

HARRIS

2N6902

August 1991

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

Features

- 12A, 100V
- $r_{DS(on)} = 0.2\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

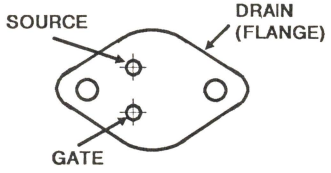
Description

The 2N6901 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6902 is supplied in the JEDEC TO-204AA steel package.

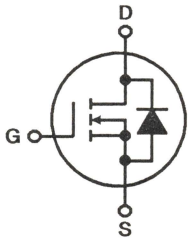
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6902	UNITS
Drain-Source Voltage	V_{DS}	100*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	100*	V
Continuous Drain Current			
T_C = +25°C	I_D	12*	A
Pulsed Drain Current	I_{DM}	30*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75*	W
Above T_C = +25°C, Derate Linearly		0.6*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering	T_L	260*	°C
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1878.1

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C = 25° C) unless otherwise specified

	CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
				MIN.	MAX.	
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V	—	1	μA
			T_C = 125° C, V_{DS} = 80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.6 A, V_{GS} = 5 V	—	1.52	V
			I_D = 12 A, V_{GS} = 5 V	—	3.3	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.6 A	—	0.2	Ω
			T_C=125° C, I_D=7.6 A, V_{GS}=5 V	—	0.32	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 7.6 A	3	12	mho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	350	900	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	100	325	
*	Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	25	100	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	—	50	ns
*	Rise Time	t_r	I_D = 7.6 V	—	150	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	130	
*	Fall Time	t_f	V_{GS} = 5 V	—	150	
*	Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 12 A	0.8	1.6	V
Reverse Recovery Time	t_{rr}	I_F = 4 A d_{IF}/d_t = 100 A/μs	—	375	ns

* In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs, max., duty cycle = 2%.

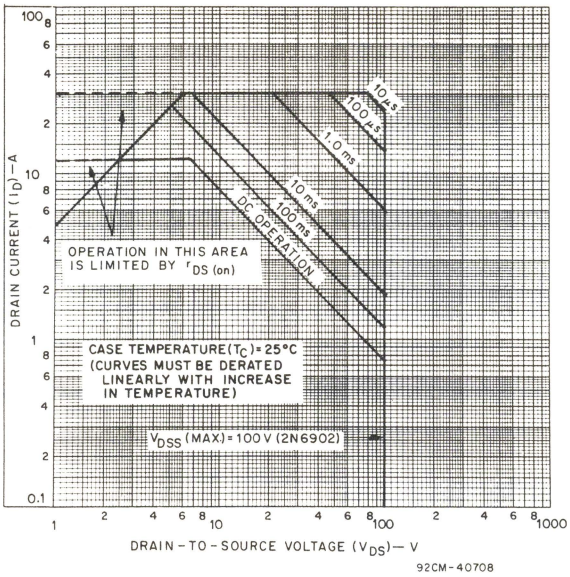


Fig. 1 - Maximum safe operating areas.

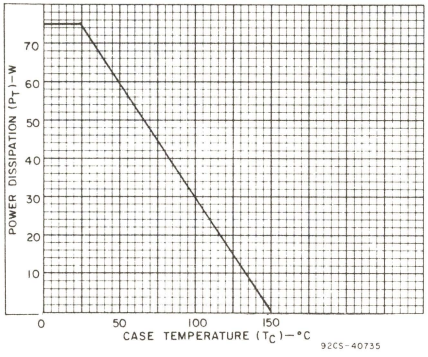


Fig. 2 - Power dissipation vs. temperature derating curve.

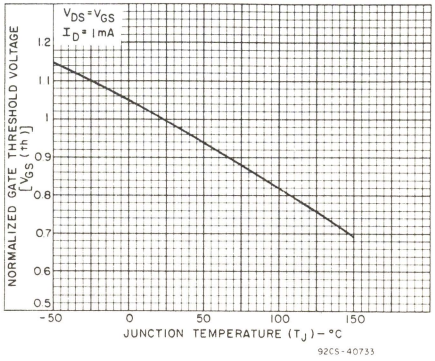


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

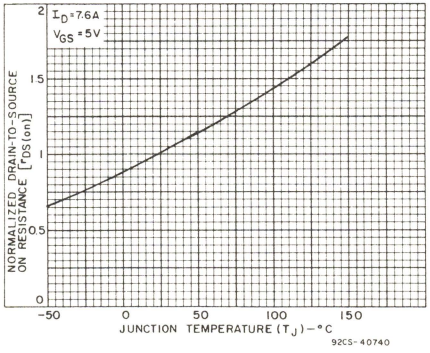


Fig. 4 - Typical normalized drain-to-source on resistance to

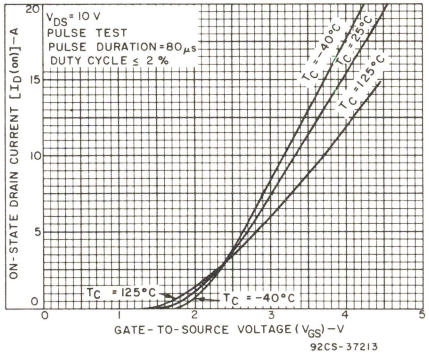


Fig. 5 - Typical transfer characteristics.

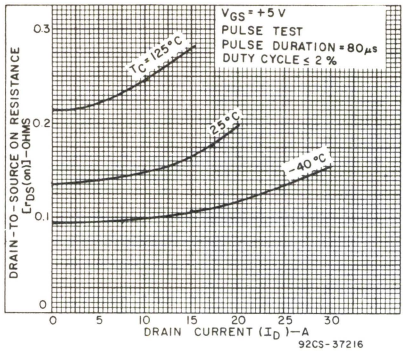


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

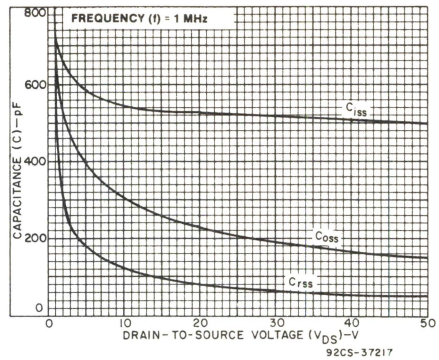


Fig. 7 - Capacitance as a function of drain-to-source voltage.

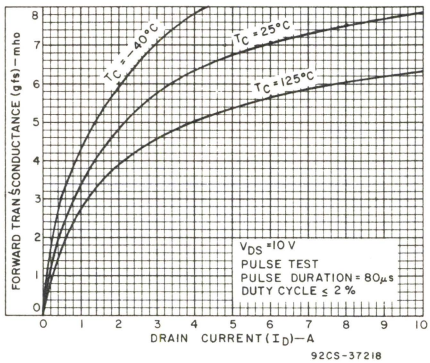


Fig. 8 - Typical forward transconductance as a function of drain current.

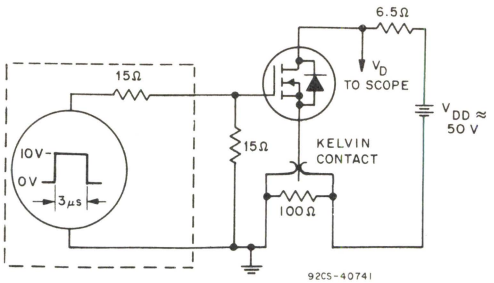


Fig. 9 - Switching time test circuit.

HARRIS

2N6903

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

January 1994

Features

- 0.98A, 200V
- $r_{DS(on)} = 3.65\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

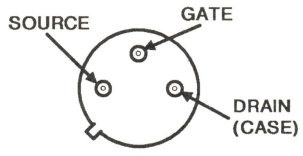
Description

The 2N6903 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6903 is supplied in the JEDEC TO-205AF metal package.

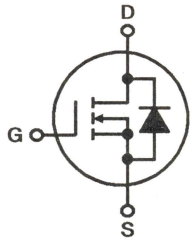
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6903	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	200*	V
Continuous Drain Current			
T_C = +25°C	I_D	0.98*	A
Pulsed Drain Current	I_{DM}	4*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	8.33*	W
Above T_C = +25°C, Derate Linearly		0.0667*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering	T_L	260*	°C
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1879.2

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	200	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V	—	1	μA
			T_C = 125°C, V_{DS} = 160 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 0.62 A, V_{GS} = 5 V	—	2.26	V
			I_D = 0.98 A, V_{GS} = 5 V	—	6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 0.62 A, V_{GS} = 5 V	—	3.65	Ω
			T_C = 125°C, I_D = 0.62 A, V_{GS} = 5 V	—	7.7	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 0.62 A	500	2000	mmho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	50	200	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	15	60	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	2	20	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V	—	25	ns
*	Rise Time	t_r	I_D = 0.62 A	—	30	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	40	
*	Fall Time	t_f	V_{GS} = 5 V	—	80	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 0.98 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 1 A, d_{IF}/dt = 50 A/μs	—	500	ns

*In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

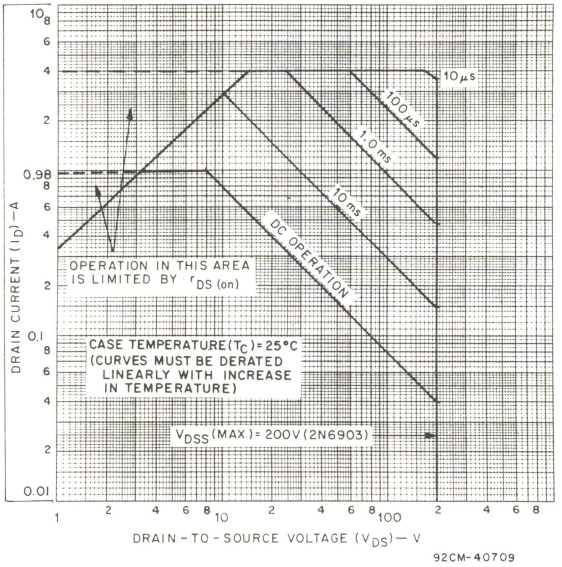


Fig. 1 - Maximum operating areas.

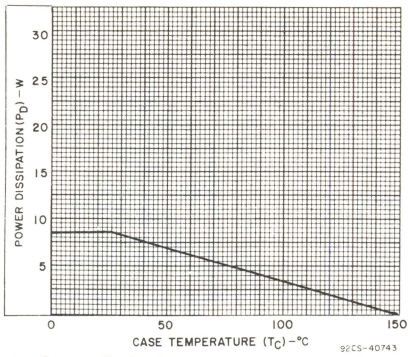


Fig. 2 - Power dissipation vs. temperature derating curve.

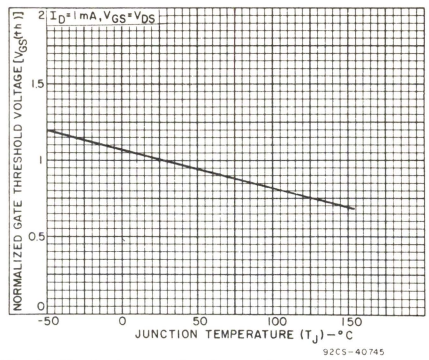


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.

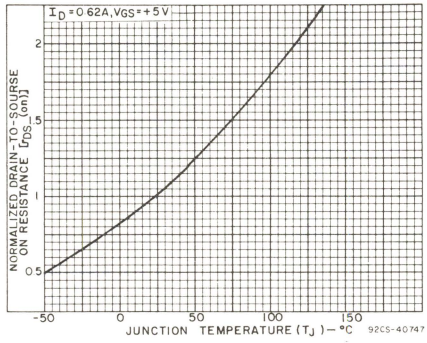


Fig. 4 - Typical normalized drain-to-source on resistance to junction temperature.

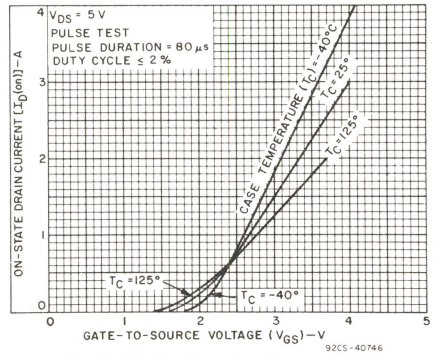


Fig. 5 - Typical transfer characteristics.

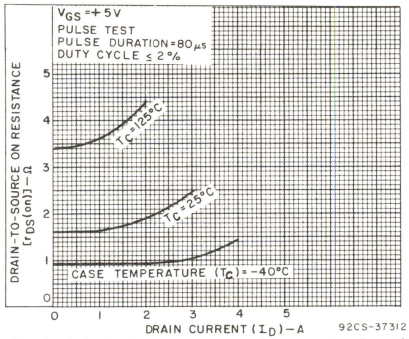


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

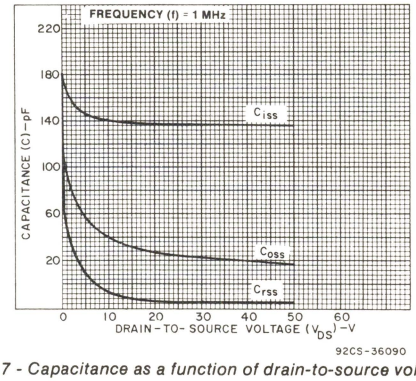


Fig. 7 - Capacitance as a function of drain-to-source voltage.

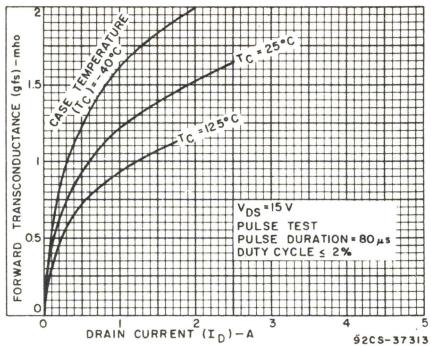


Fig. 8 - Typical forward transconductance as a function of drain current.

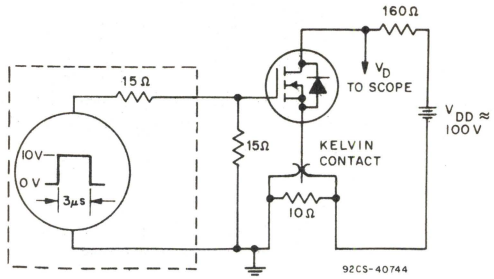


Fig. 9 - Switching time test circuit.

HARRIS

2N6904

N-Channel Logic Level Power MOS Field-Effect Transistors (L^2FET)

August 1991

Features

- 8A, 200V
- $r_{DS(on)} = 0.6\Omega$
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

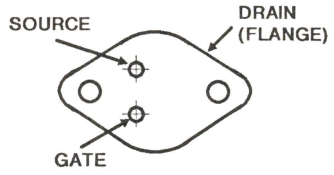
Description

The 2N6904 is an N-channel enhancement-mode silicon-gate power MOS field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, therefore facilitating true on-off power control directly from logic circuit supply voltages.

The 2N6904 is supplied in the JEDEC TO-204AA steel package.

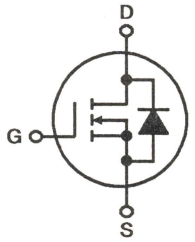
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		2N6904	UNITS
Drain-Source Voltage	V_{DS}	200*	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	200*	V
Continuous Drain Current			
T_C = +25°C	I_D	8*	A
Pulsed Drain Current	I_{DM}	20*	A
Gate-Source Voltage	V_{GS}	±10*	V
Maximum Power Dissipation			
T_C = +25°C	P_D	75*	W
Above T_C = +25°C, Derate Linearly		0.6*	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	°C
Maximum Lead Temperature for Soldering	T_L	260*	°C
At distance > 1/8 in. (3.17mm) from seating plane for 10s max			

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1880.1

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C = 25° C) unless otherwise specified

	CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
				MIN.	MAX.	
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	200	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1 mA	1	2	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V	—	1	μA
			T_C = 125° C, V_{DS} = 160 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5.1 A, V_{GS} = 5 V	—	3.06	V
			I_D = 8 A, V_{GS} = 5 V	—	5.5	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5.1 A	—	0.6	Ω
			T_C=125° C, I_D=5.1 A, V_{GS}=5 V	—	1.11	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = 5 V, I_D = 5.1 A	3	12	mho
*	Input Capacitance	C_{iss}	V_{DS} = 25 V	350	900	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	75	250	
*	Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	20	100	
*	Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V	—	45	ns
*	Rise Time	t_r	I_D = 5.1 A	—	150	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 15 Ω	—	135	
*	Fall Time	t_f	V_{GS} = 5 V	—	150	
*	Thermal Resistance Junction-to-Case	$R\theta_{JC}$		—	1.67	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
				MIN.	MAX.	
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 8 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A d_{IF}/d_t = 100 A/μs	—	625	ns

* In accordance with JEDEC registration data.

[a]Pulsed: Pulse duration = 300 μs, max., duty cycle = 2%.

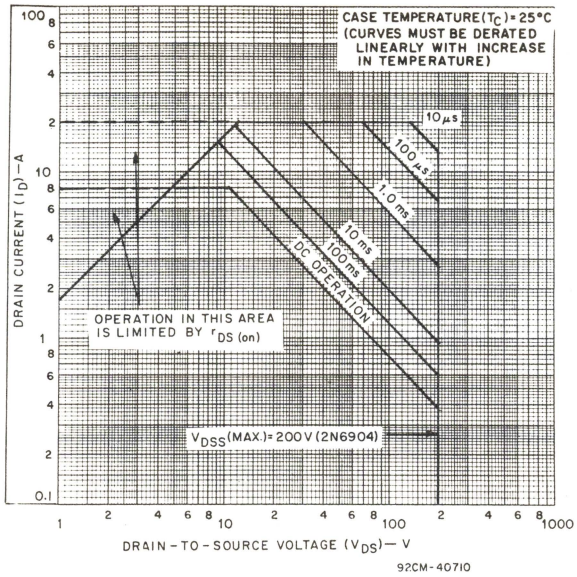


Fig. 1 - Maximum safe operating areas.

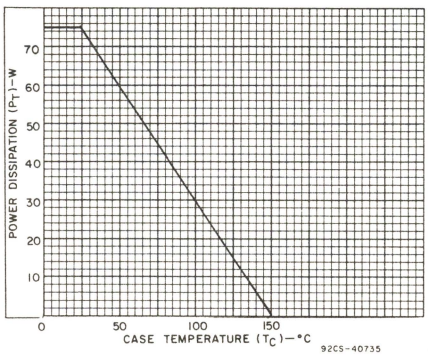


Fig. 2 - Power dissipation vs. temperature derating curve.

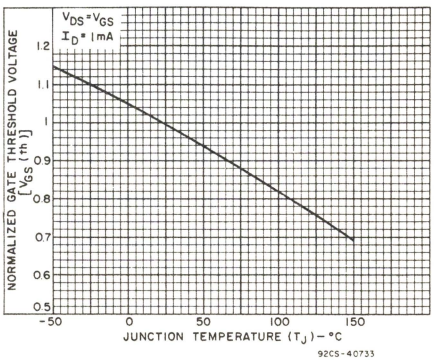
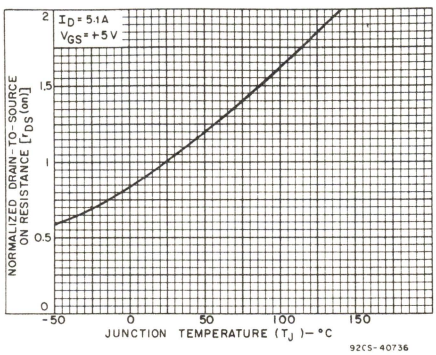
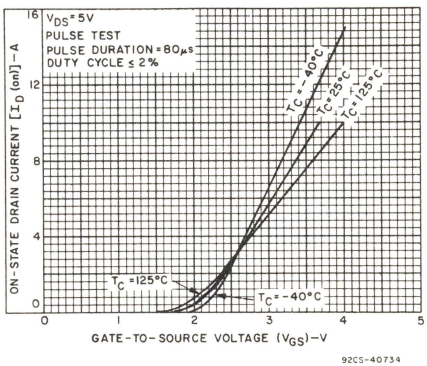


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature.





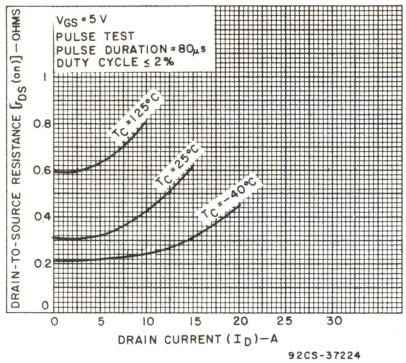


Fig. 6 - Typical drain-to-source on resistance as a function of drain current.

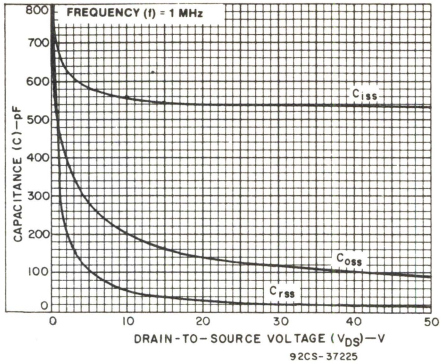


Fig. 7 - Capacitance as a function of drain-to-source voltage.

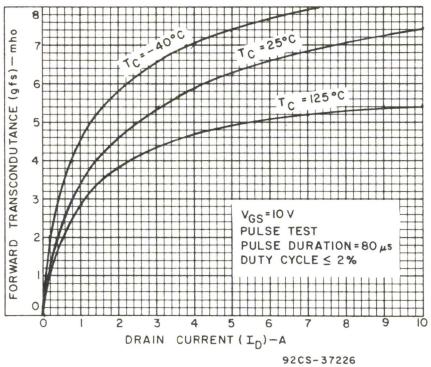


Fig. 8 - Typical forward transconductance as a function of drain current.

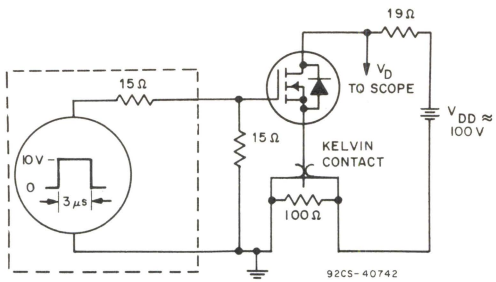


Fig. 9 - Switching time test circuit.

HARRIS

RFL1N08L
RFL1N10L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 1A, 80V and 100V
- $r_{DS(ON)} = 1.2\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

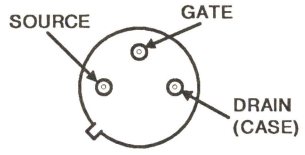
Description

The RFL1N08L and RFL1N10L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL series types are supplied in the JEDEC TO-205AF steel package.

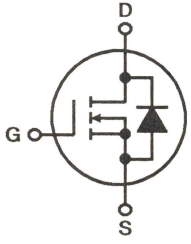
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFL1N08L	RFL1N10L	UNITS
Drain-Source Voltage	V_{DS}	80	100	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	80	100	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	8.33	8.33	W
Above $T_C = +25^oC$, Derate Linearly		0.0667	0.0667	W/^{o}C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **1510.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08L		RFL1N10L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	-	100	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	-	1	-	-	μA
		V_{DS} = 80V	-	-	-	1	μA
		T_C = +125°C, V_{DS} = 65V	-	50	-	-	μA
		V_{DS} = 80V	-	-	-	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	-	100	-	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	-	1.2	-	1.2	V
		I_D = 2A, V_{GS} = 5V	-	2.9	-	2.9	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	-	1.2	-	1.2	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	-	800	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	200	-	200	pF
Output Capacitance	C_{OSS}		-	80	-	80	pF
Reverse Transfer Capacitance	C_{RSS}		-	35	-	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	45	25 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	15	-	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08L		RFL1N10L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	-	1.4	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

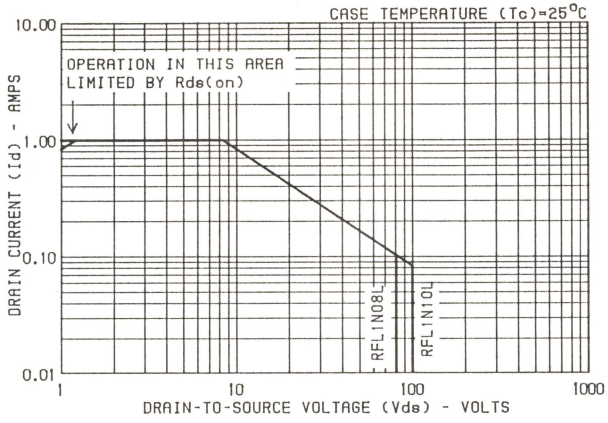


Fig. 1 — Maximum operating areas for all types.

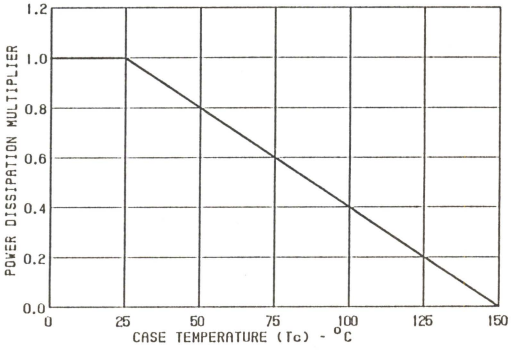


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

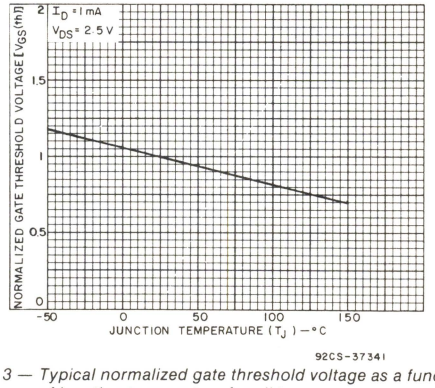


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

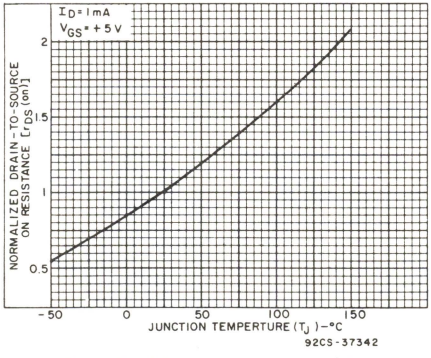


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

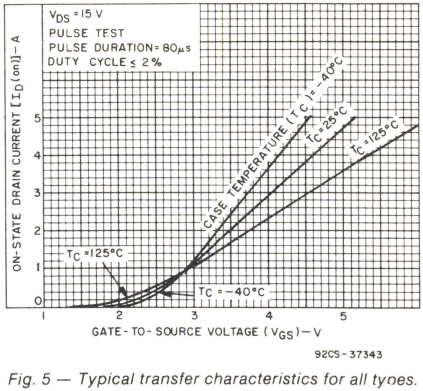


Fig. 5 — Typical transfer characteristics for all types.

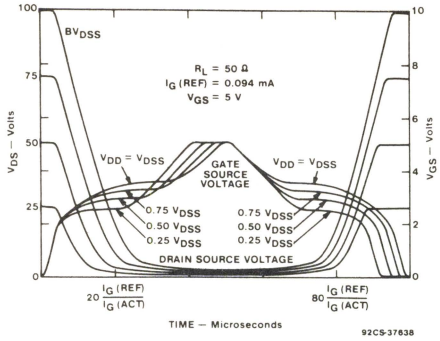


Fig 6. - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

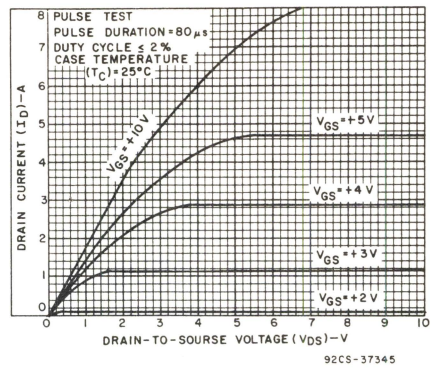


Fig. 7 — Typical saturation characteristics for all types.

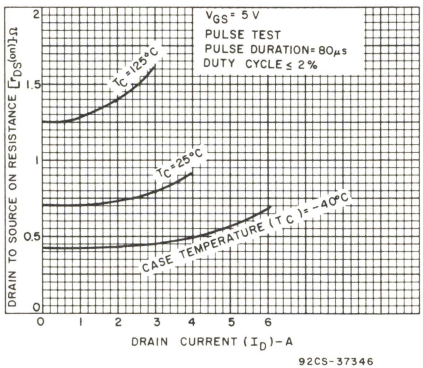


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

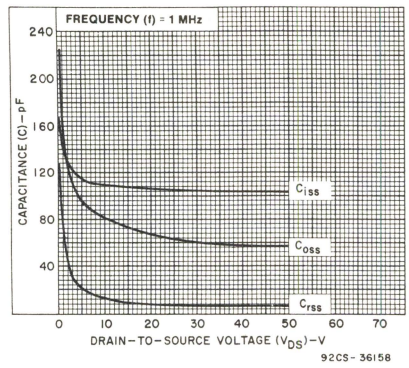


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

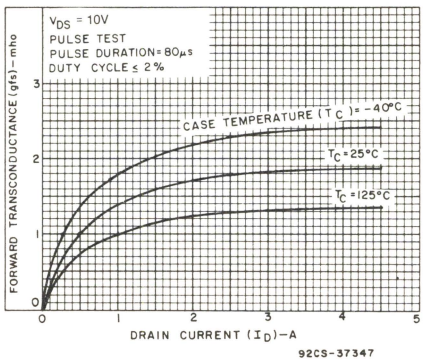


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

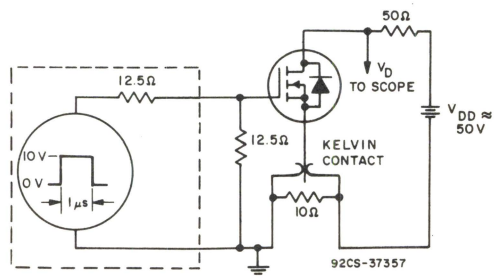


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFL1N12L
RFL1N15L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 1A, 120V and 150V
- $r_{DS(ON)} = 1.9\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

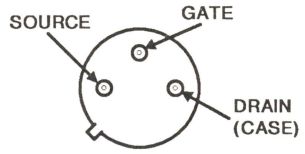
Description

The RFL1N12L and RFL1N15L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

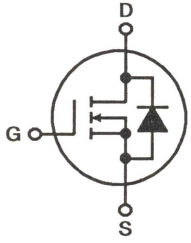
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		RFL1N12L	RFL1N15L	UNITS
Drain-Source Voltage	V_{DS}	120	150	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	120	150	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
T_C = +25°C	P_D	8.33	8.33	W
Above T_C = +25°C, Derate Linearly		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1513.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N12L		RFL1N15L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	–	150	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	–	1	–	–	μA
		V_{DS} = 120V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 100V	–	50	–	–	μA
		V_{DS} = 120V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.9	–	1.9	V
		I_D = 2A, V_{GS} = 5V	–	4.6	–	4.6	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.9	–	1.9	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V, R_{GEN} = ∞, R_{GS} = 6.25Ω, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	45	10 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		24 (typ)	45	24 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	R_{0JC}		–	15	–	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N12L		RFL1N15L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

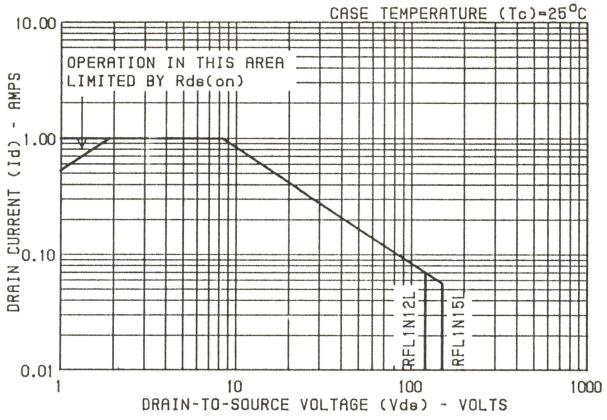


Fig. 1 — Maximum operating areas for all types.

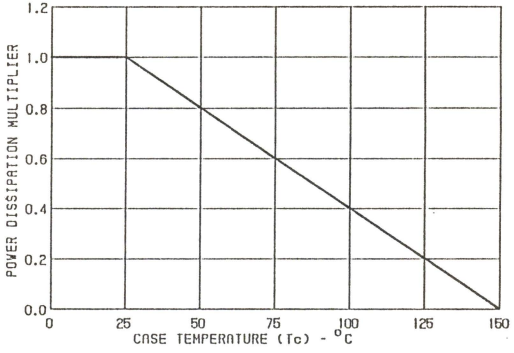


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

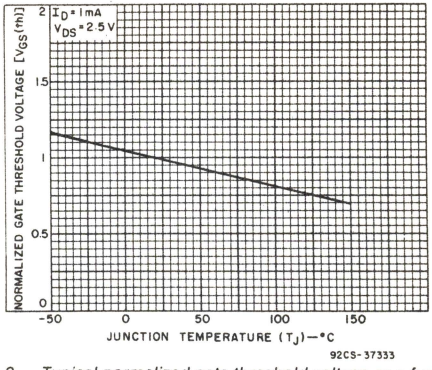


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

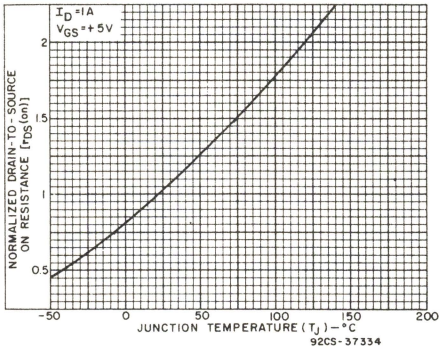


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

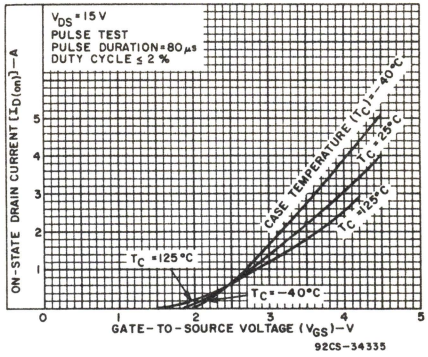


Fig. 5 — Typical transfer characteristics for all types.

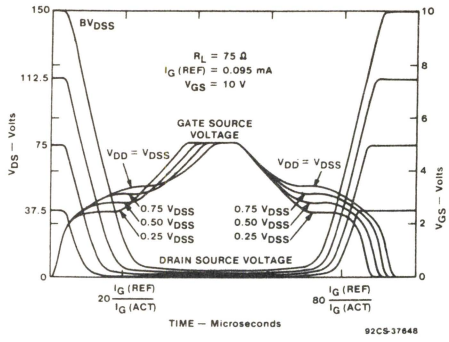


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

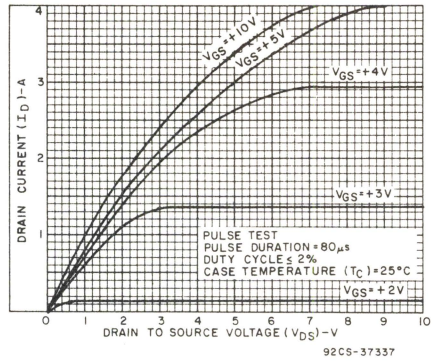


Fig. 7 — Typical saturation characteristics for all types.

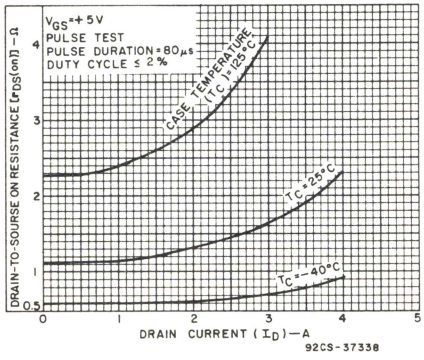


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

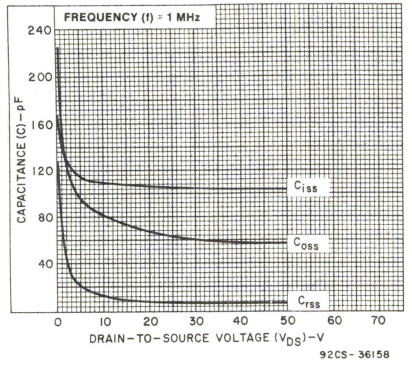


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

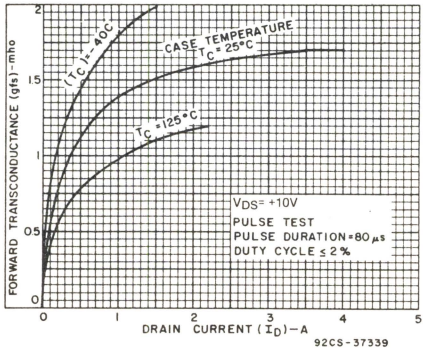


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

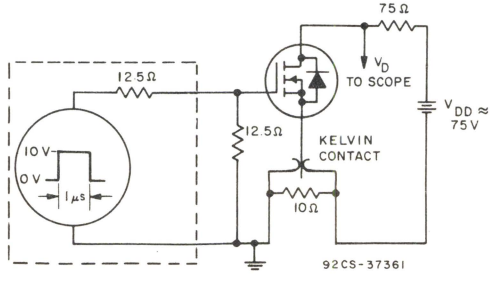


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFL1N18L
RFL1N20L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 1A, 180V and 200V
- $r_{DS(ON)} = 3.65\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

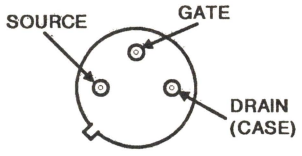
Description

The RFL1N18L and RFL1N20L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

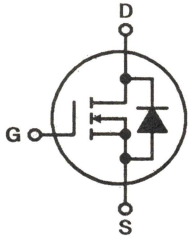
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFL1N18L	RFL1N20L	UNITS
Drain-Source Voltage	V_{DS}	180	200	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	180	200	V
Continuous Drain Current				
RMS Continuous	I_D	1	1	A
Pulsed Drain Current	I_{DM}	4	4	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	8.33	8.33	W
Above $T_C = +25^oC$, Derate Linearly		0.0667	0.0667	W/^{o}C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1511.1

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18L		RFL1N20L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	-	200	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	-	1	-	-	μA
		V_{DS} = 160V	-	-	-	1	μA
		T_C = +125°C V_{DS} = 145V	-	50	-	-	μA
		V_{DS} = 160V	-	-	-	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	-	100	-	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	-	3.65	-	3.65	V
		I_D = 2A, V_{GS} = 5V	-	9.3	-	9.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	-	3.65	-	3.65	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	-	800	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V f = 1MHz	-	200	-	200	pF
Output Capacitance	C_{OSS}		-	60	-	60	pF
Reverse Transfer Capacitance	C_{RSS}		-	35	-	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	30	10 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	15	-	15	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18L		RFL1N20L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	-	1.4	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A d_{IF}/dt = 50A/μs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

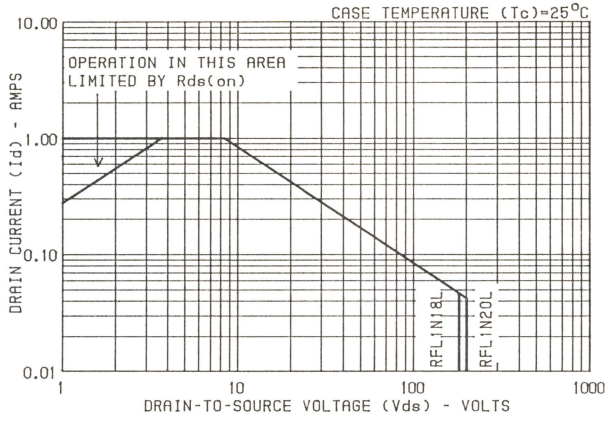


Fig. 1 — Maximum operating areas for all types.

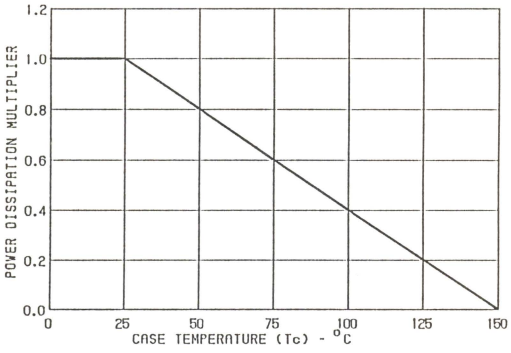


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

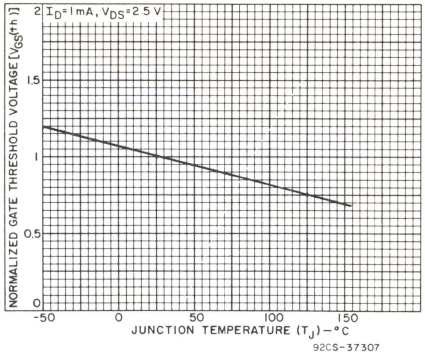


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

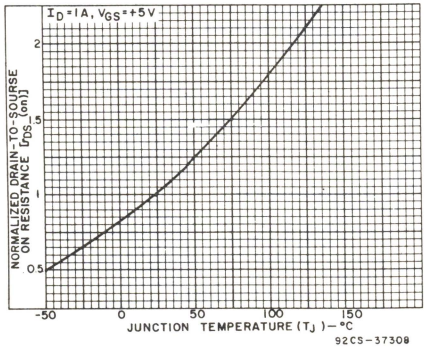


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

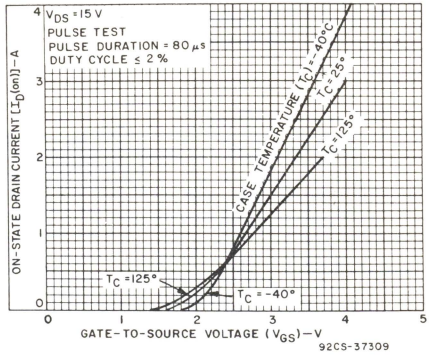


Fig. 5 — Typical transfer characteristics for all types.

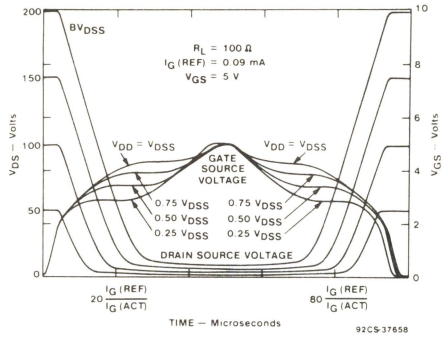


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

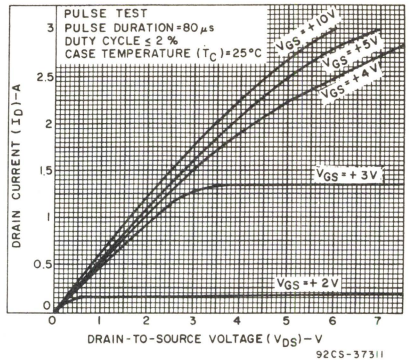


Fig. 7 — Typical saturation characteristics for all types.

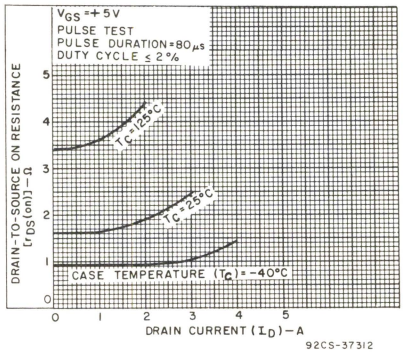


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

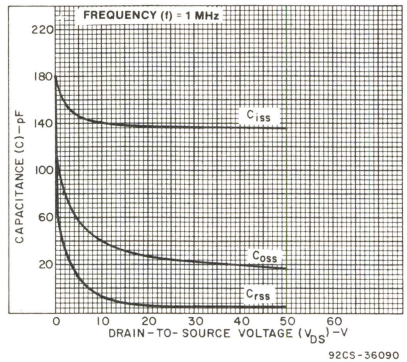


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

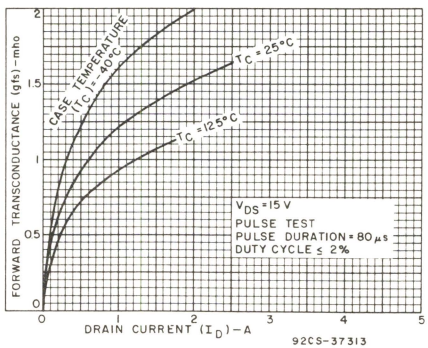


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

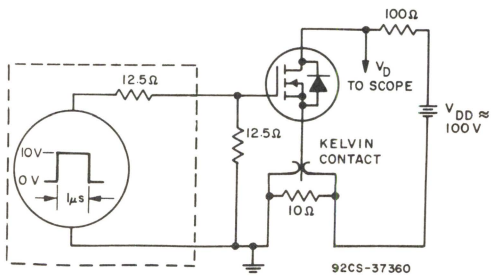


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFL2N05L
RFL2N06L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 50V and 60V
- $r_{DS(ON)} = 0.95\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

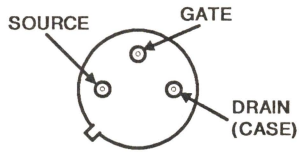
Description

The RFL2N05L and RFL2N06L are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL series types are supplied in the JEDEC TO-205AF metal package.

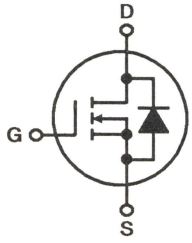
Package

TO-205AF
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFL2N05L	RFL2N06L	UNITS
Drain-Source Voltage	V_{DS}	50	50	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	50	60	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	10	10	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	8.33	8.33	W
Above $T_C = +25^oC$, Derate Linearly		0.0667	0.0667	W/^{o}C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **1560.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05L		RFL2N06L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.95	–	0.95	V
		I_D = 2A, V_{GS} = 5V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 7.5V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.95	–	0.95	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	225	–	225	pF
Output Capacitance	C_{OSS}		–	100	–	100	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	40	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	20	10 (typ)	20	ns
Rise Time	t_r		65 (typ)	130	65 (typ)	130	ns
Turn-Off Delay Time	$t_{d(off)}$		20 (typ)	40	20 (typ)	40	ns
Fall Time	t_f		30 (typ)	60	30 (typ)	60	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05L		RFL2N06L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 100A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

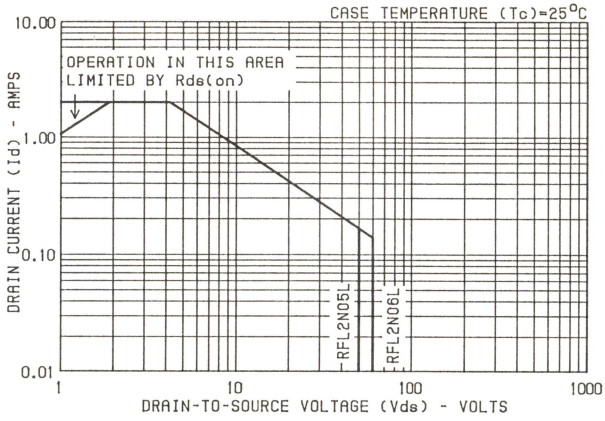


Fig. 1 - Maximum operating areas for all types.

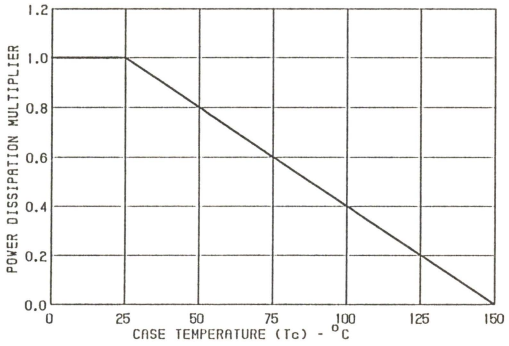


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

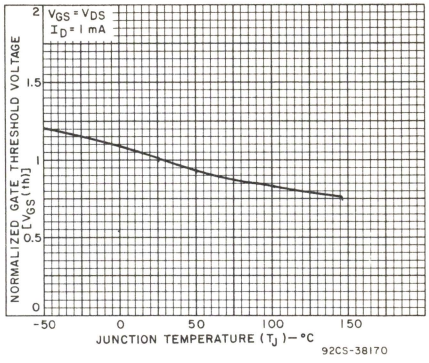


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

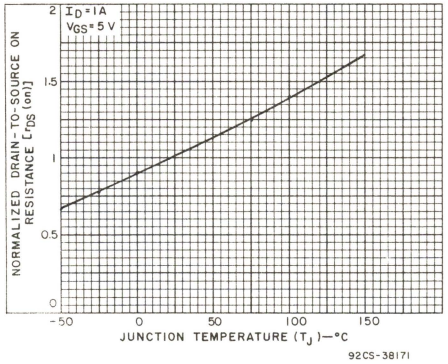


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

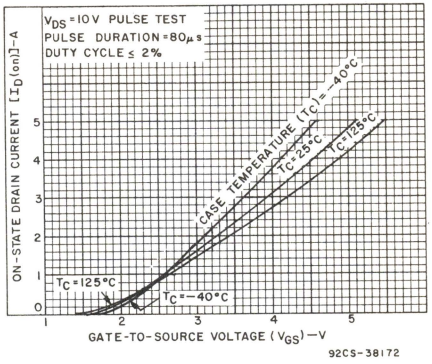


Fig. 5 - Typical transfer characteristics for all types.

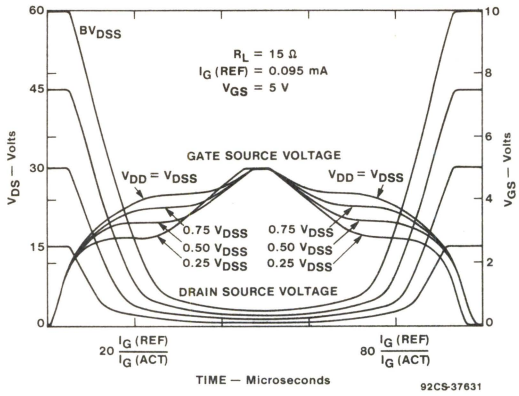


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

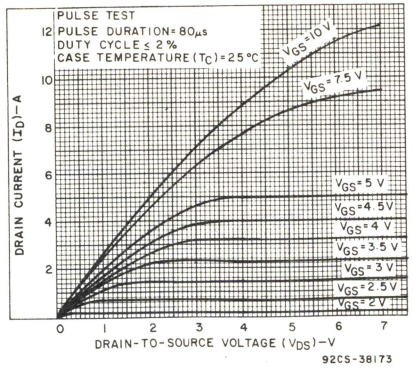


Fig. 7 - Typical saturation characteristics for all types.

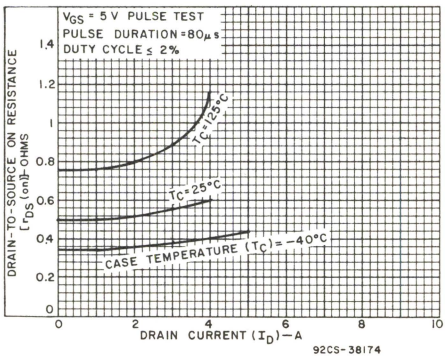


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

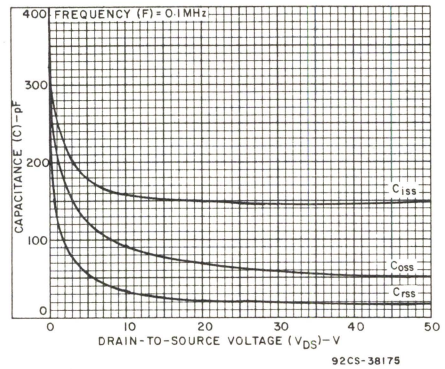


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

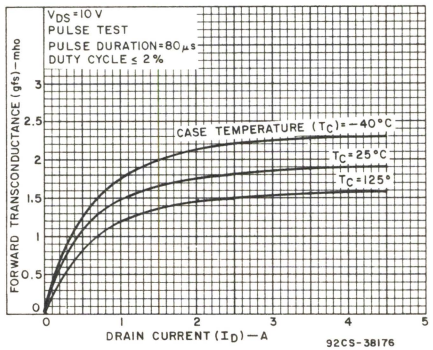


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

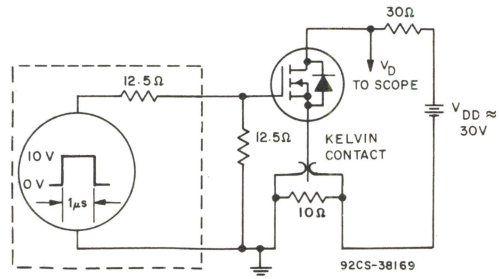


Fig. 11 - Switching Time Test Circuit.

HARRIS SEMICONDUCTOR

RFW2N06RLE

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors

May 1992

Features

- 2A, 60V
- $r_{DS}(on) = 0.160\Omega$
- UIS Rating Curve (Single Pulse)
- Design Optimized For 5 Volt Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Electrostatic Discharge Protected

Description

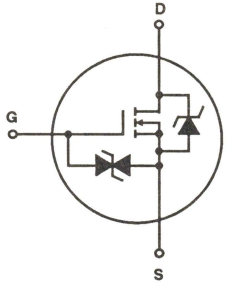
The RFW2N06RLE (TA9861) N-Channel logic level ESD protected power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFW2N06RLE was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor and relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFW2N06RLE is supplied in the 4-pin hexdip plastic package. (Similar to JEDEC outline TO-250)

Package

4-PIN HEXDIP
TOP VIEW

Terminal Diagram



6 LOGIC LEVEL POWER MOSFETs

Absolute Maximum Ratings ($T_C = +25^oC$)

			UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	+10, -5	V
Drain Current			
RMS Continuous	I_D	2	A
Pulsed Drain Current	I_{DM}	14	A
Single Pulse Avalance Rating	E_{AS}	Refer to UIS Curve	
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	KV
Power Dissipation			
$T_C = +25^oC$	P_D	1.09	W
Derate Above $+25^oC$	P_T	0.009	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2838.1**

Electrical Characteristics Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25mA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-1	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10V, V_{GS} = -5V		-	-	10	µA
				-	-	10	µA
On Resistance	$r_{DS(on)}$	I_D = 2A, V_{GS} = 5.0V, I_D = 2A, V_{GS} = 4.3V		-	-	160	mΩ
				-	-	200	mΩ
Turn-On Time	t_{on}	V_{DD} = 30V, I_D = 2A, R_L = 15, V_{GS} = 5V, R_{GS} = 25Ω		-	-	100	ns
Turn-On Delay Time	$t_{d(on)}$			-	13	-	ns
Rise Time	t_r			-	42	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	95	-	ns
Fall Time	t_f			-	45	-	ns
Turn-Off Time	t_{off}			-	-	200	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0 to 10V	V_{DD} = 48V, I_D = 2A, RL = 24Ω	-	20	30	nC
Gate Charge at 5V	Qg(5)	V_{GS} = 0 to 5V		-	11	16	nC
Threshold Gate Charge	Qg(th)	V_{GS} = 0 to 1V		-	0.6	1.0	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 2A, V_{DS} = 15V		-	-	4.3	V
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	535	-	pF
Output Capacitance	C_{oss}			-	175	-	pF
Reverse Transfer Capacitance	C_{rss}			-	32	-	pF
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30V, I_D = 2A, L = 0.21µH, R_L = 15Ω, V_{GS} = 5V, R_{GS} = 25Ω		-	-	10	µJ
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	115	°C/W

Source-Drain Diode Ratings And Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 2A	-	-	1.2	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/µs	-	-	200	ns

Performance Curves

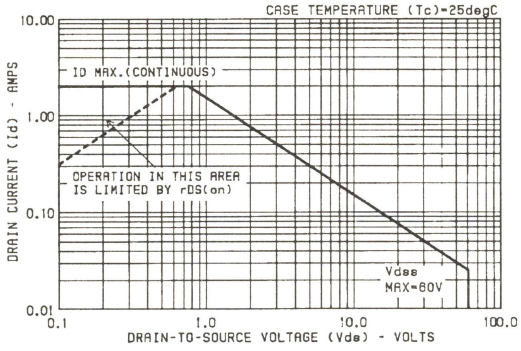


FIGURE 1. SAFE-OPERATING AREA CURVE

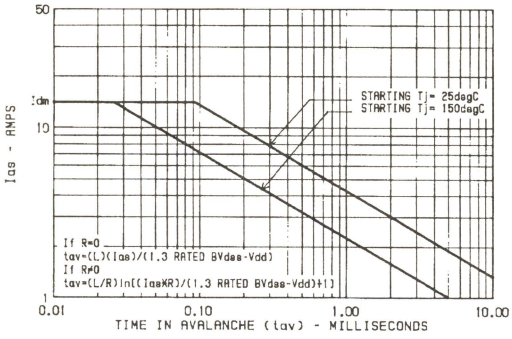


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

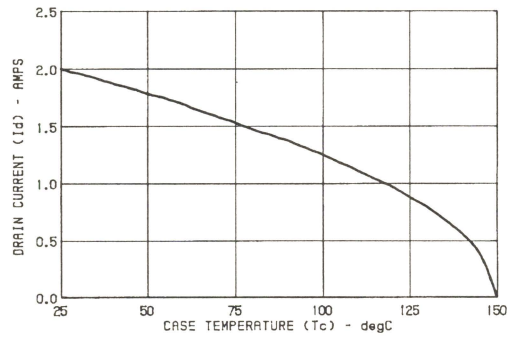


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

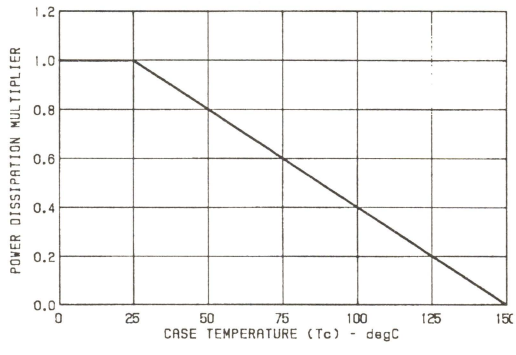


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

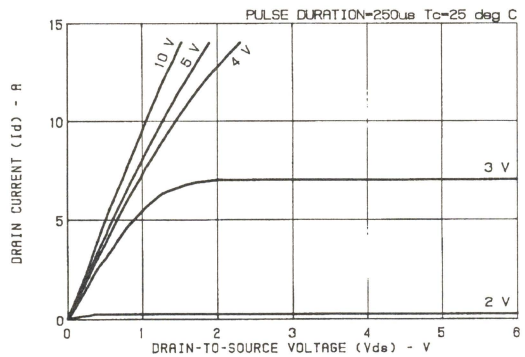


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

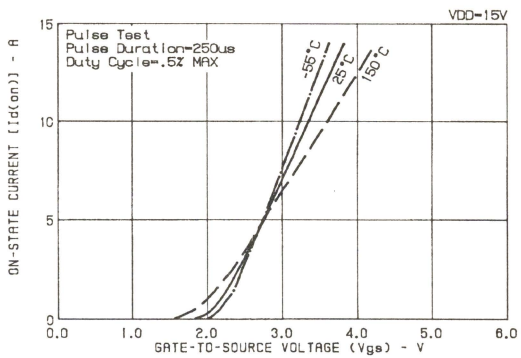


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Performance Curves (Continued)

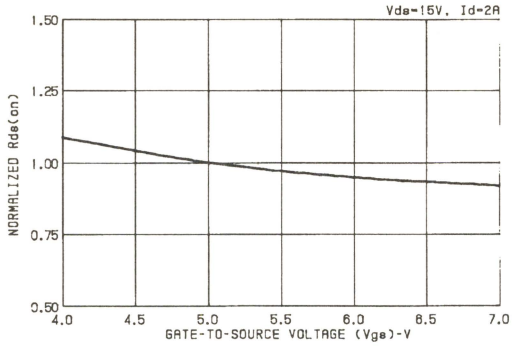


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs V_{gs}

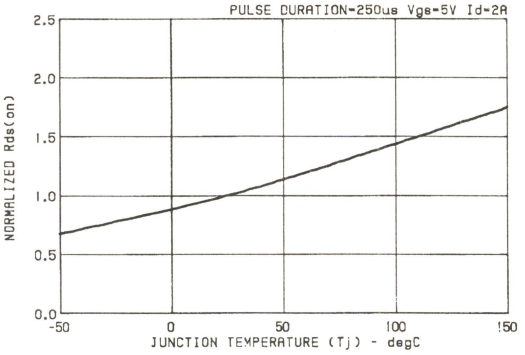


FIGURE 8. NORMALIZED $r_{DS(on)}$ vs JUNCTION TEMPERATURE

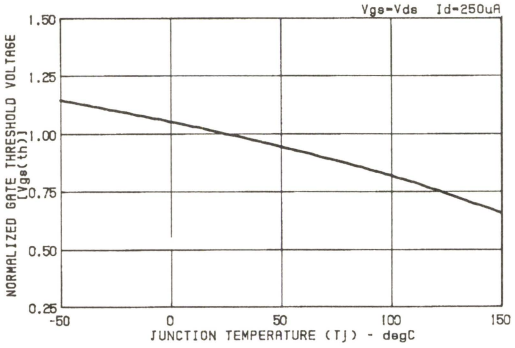


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

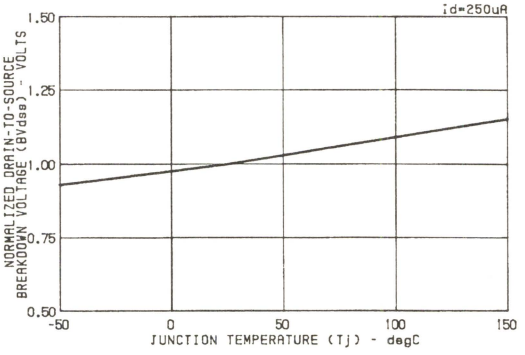


FIGURE 10. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

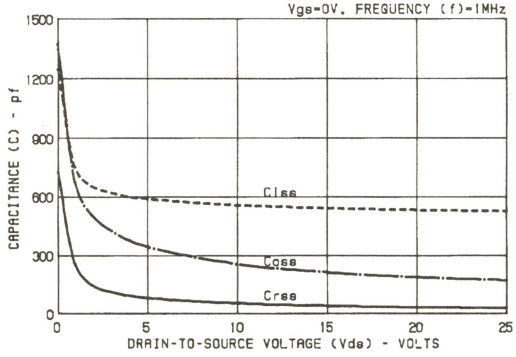


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

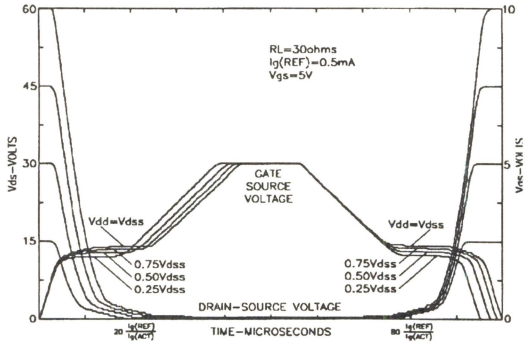


FIGURE 12. TYPICAL SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTES AN7254 AND AN7260

Performance Curves (Continued)

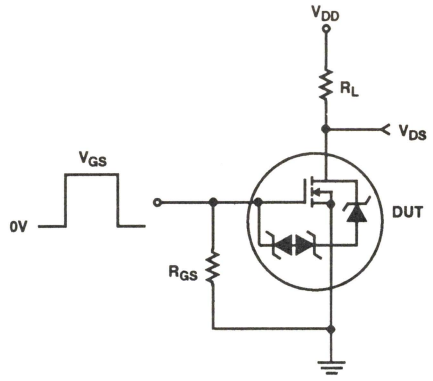


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUITS

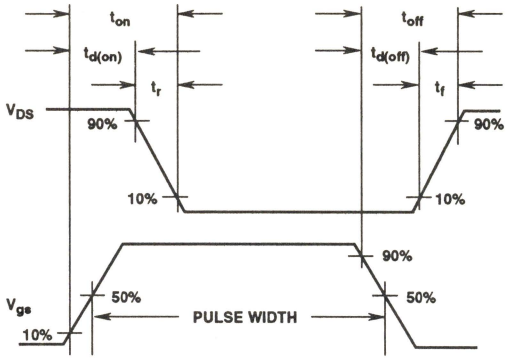


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

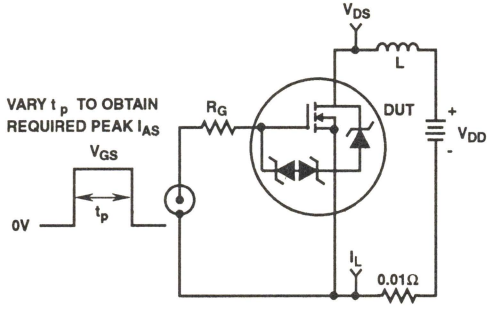


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

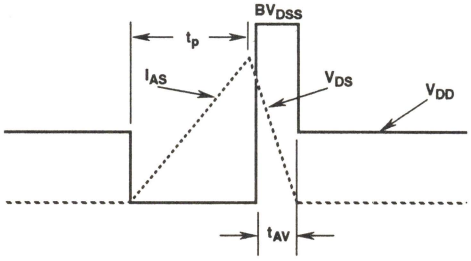


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

HARRIS

RFP2N08L
RFP2N10L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 80V and 100V
- $r_{DS(ON)} = 1.05\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

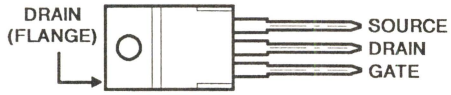
Description

The RFP2N08L and RFP2N10L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

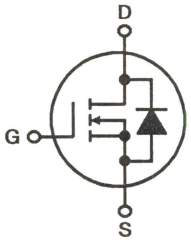
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFP2N08L	RFP2N10L	UNITS
Drain-Source Voltage	V_{DS}	80	100	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	80	100	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	25	25	W
Above $T_C = +25^oC$, Derate Linearly		0.2	0.2	W/^{o}C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2872**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N08L		RFP2N10L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	μA
		V_{DS} = 80V	–	–	–	1	μA
		T_C = +125°C V_{DS} = 65V	–	50	–	–	μA
		V_{DS} = 80V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.05	–	1.05	V
		I_D = 2A, V_{GS} = 5V	–	2.5	–	2.5	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.05	–	1.05	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		15 (typ)	45	15 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	45	25 (typ)	45	ns
Fall Time	t_f		20 (typ)	25	20 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N08L		RFP2N10L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = –1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

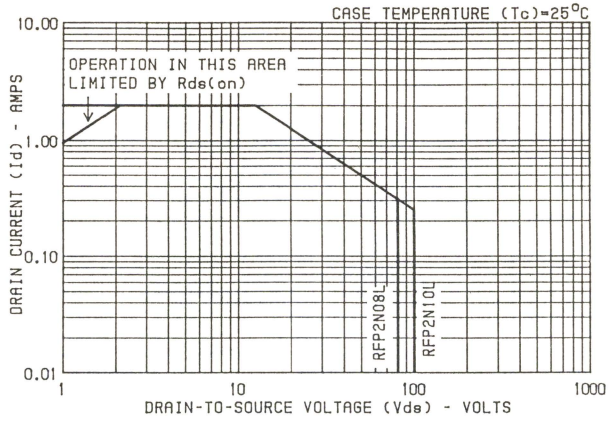


Fig. 1 — Maximum operating areas for all types.

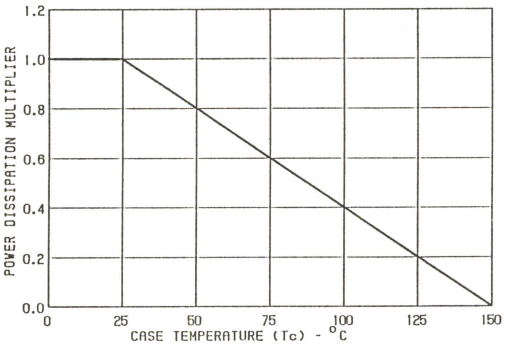


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

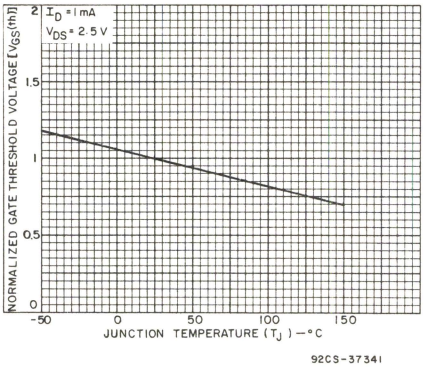


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

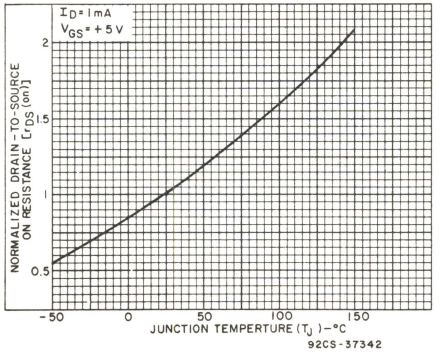


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

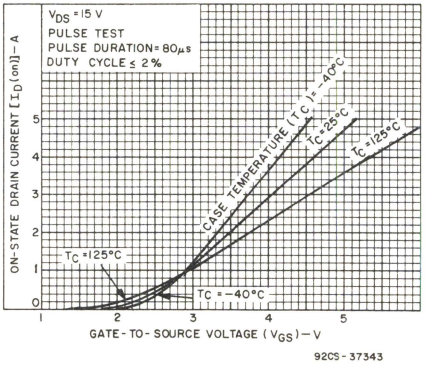


Fig. 5 — Typical transfer characteristics for all types.

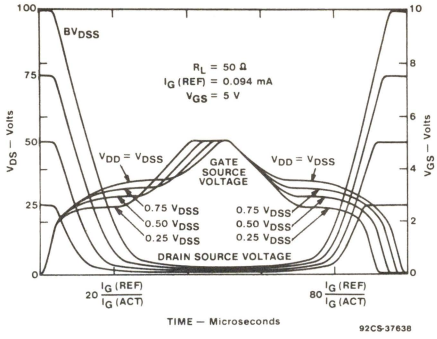


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

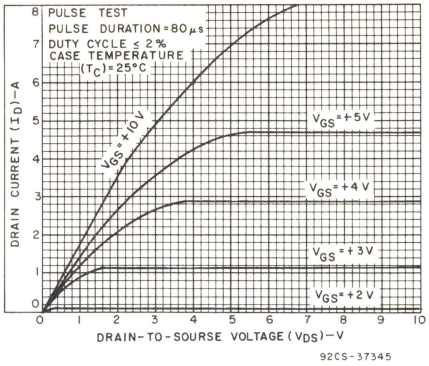


Fig. 7 — Typical saturation characteristics for all types.

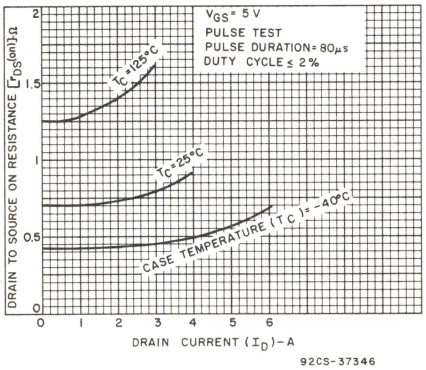


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

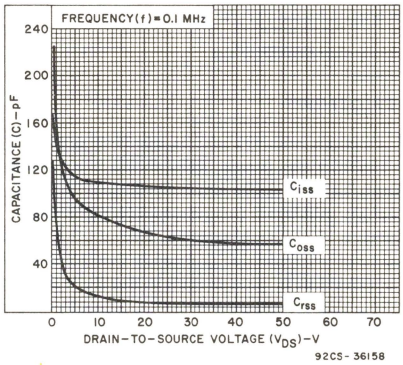


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

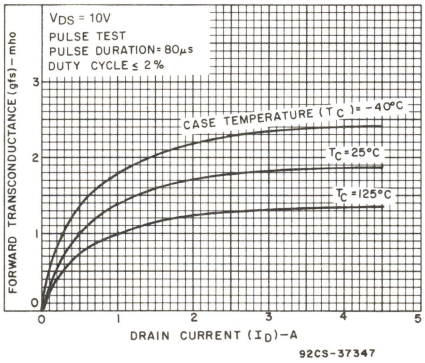


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

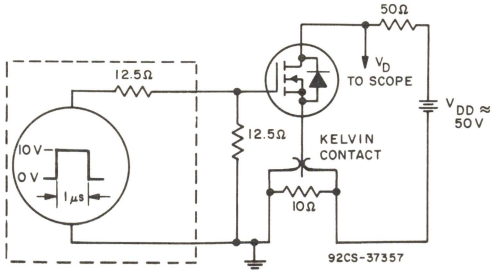


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP2N12L
RFP2N15L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 120V and 150V
- $r_{DS(ON)} = 1.75\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

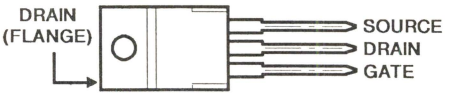
Description

The RFP2N12L and RFP2N15L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

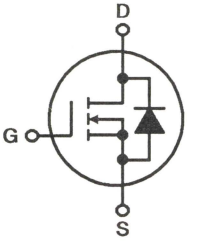
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFP2N12L	RFP2N15L	UNITS
Drain-Source Voltage	V_{DS}	120	120	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	120	150	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	5	5	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	25	25	W
Above $T_C = +25^oC$, Derate Linearly		0.2	0.2	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2874

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N12L		RFP2N15L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	120	–	150	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V	–	1	–	–	μA
		V_{DS} = 120V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 100V	–	50	–	–	μA
		V_{DS} = 120V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.75	–	1.75	V
		I_D = 2A, V_{GS} = 5V	–	4.2	–	4.2	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	1.75	–	1.75	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse Transfer Capacitance	C_{RSS}		–	35	–	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 75V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	45	10 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		24 (typ)	45	24 (typ)	45	ns
Fall Time	t_f		20 (typ)	25	20 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N12L		RFP2N15L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

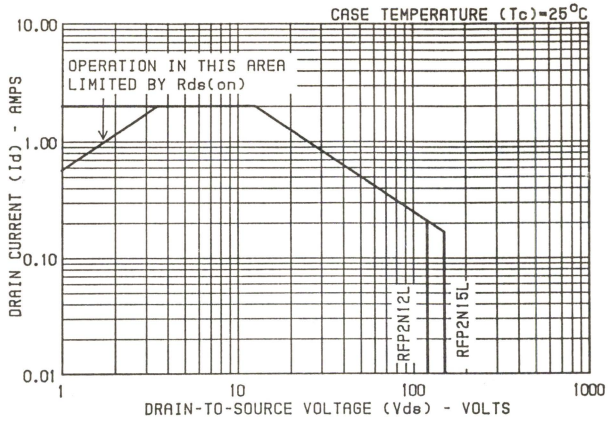


Fig. 1 — Maximum operating areas for all types.

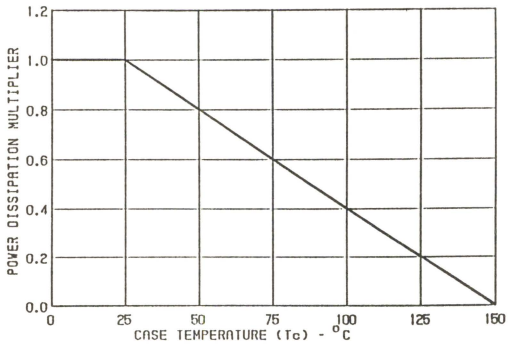


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

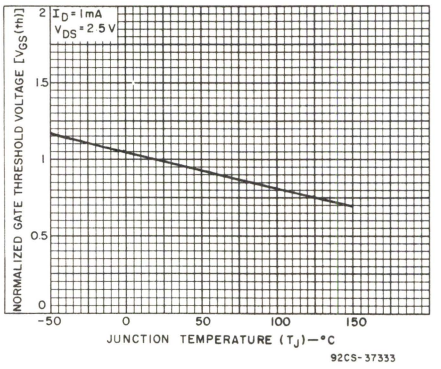


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

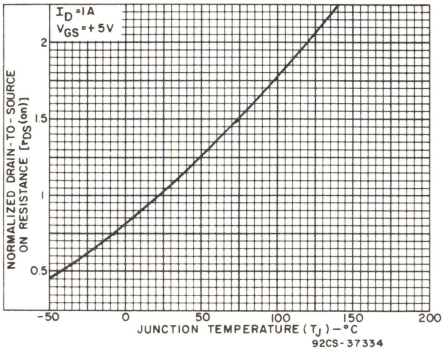


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

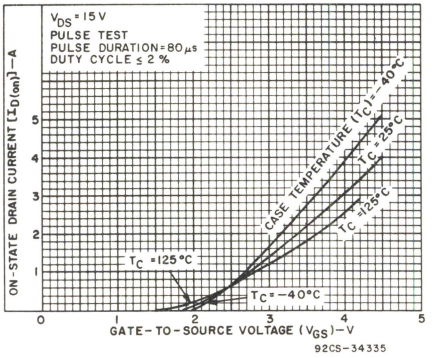


Fig. 5 — Typical transfer characteristics for all types.

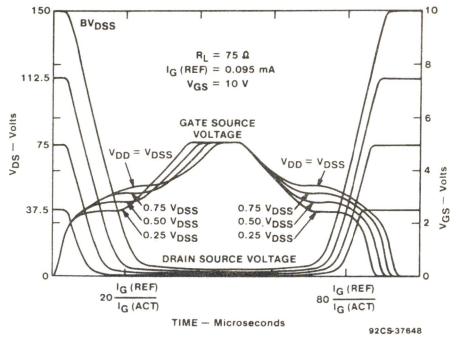


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

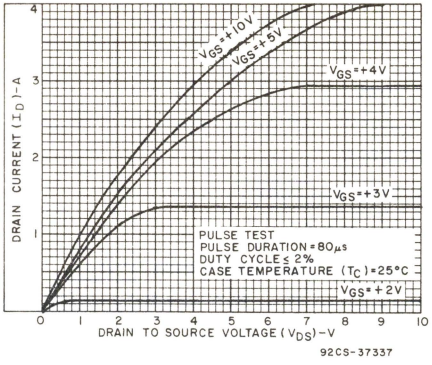


Fig. 7 — Typical saturation characteristics for all types.

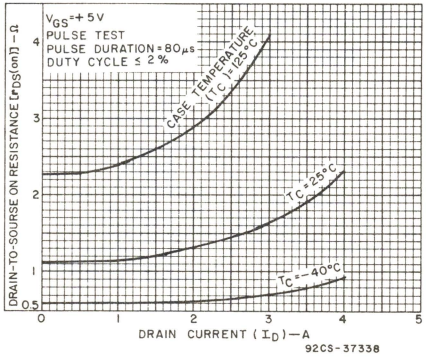


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

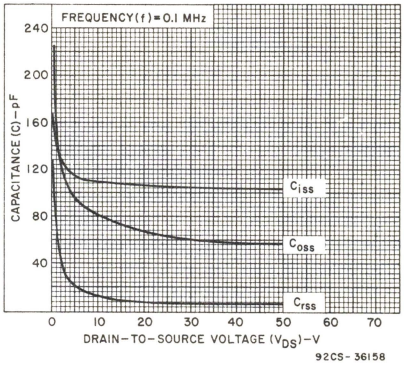


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

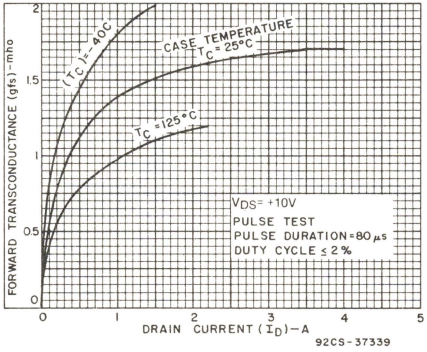


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

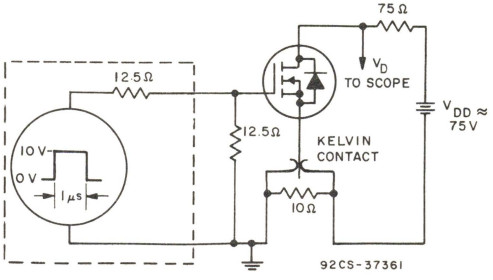


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP2N18L
RFP2N20L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 2A, 180V and 200V
- $r_{DS(ON)} = 3.5\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

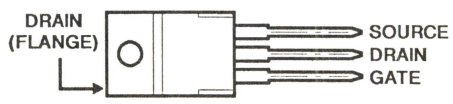
Description

The RFP2N18L and RFP2N20L are N-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

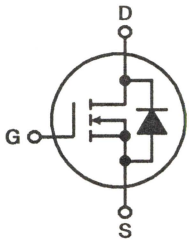
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFP2N18L	RFP2N20L	UNITS
Drain-Source Voltage	V_{DS}	180	200	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	180	200	V
Continuous Drain Current				
RMS Continuous	I_D	2	2	A
Pulsed Drain Current	I_{DM}	4	4	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	25	25	W
Above $T_C = +25^oC$, Derate Linearly		0.2	0.2	W/^{o}C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2875**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N18L		RFP2N20L		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	180	-	200	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145V	-	1	-	-	μA
		V_{DS} = 160V	-	-	-	1	μA
		T_C = +125°C V_{DS} = 145V	-	50	-	-	μA
		V_{DS} = 160V	-	-	-	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	-	100	-	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	-	3.5	-	3.5	V
		I_D = 2A, V_{GS} = 5V	-	9	-	9	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	-	3.5	-	3.5	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	-	800	-	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V f = 1MHz	-	200	-	200	pF
Output Capacitance	C_{OSS}		-	60	-	60	pF
Reverse Transfer Capacitance	C_{RSS}		-	35	-	35	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 100V R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	25	10 (typ)	25	ns
Rise Time	t_r		10 (typ)	30	10 (typ)	30	ns
Turn-Off Delay Time	$t_{d(off)}$		25 (typ)	40	25 (typ)	40	ns
Fall Time	t_f		20 (typ)	25	20 (typ)	25	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	5	-	5	°C/W

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFP2N18L		RFP2N20L		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = -1A	-	1.4	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A dI_F/dt = 50A/μs	200 (typ)	200 (typ)	200 (typ)	200 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

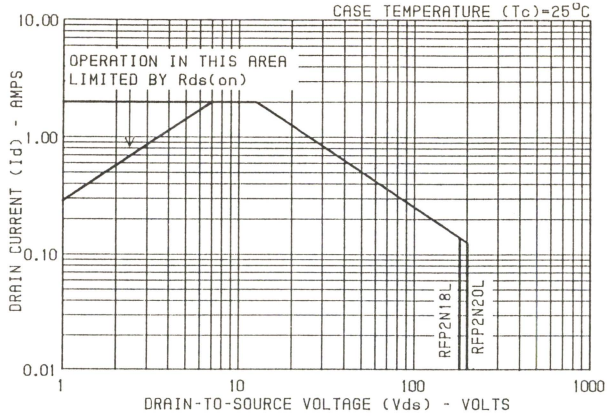


Fig. 1 — Maximum operating areas for all types.

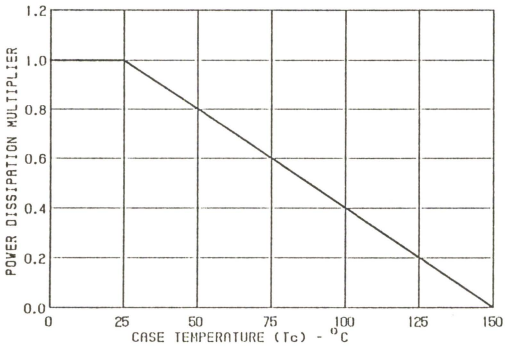


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

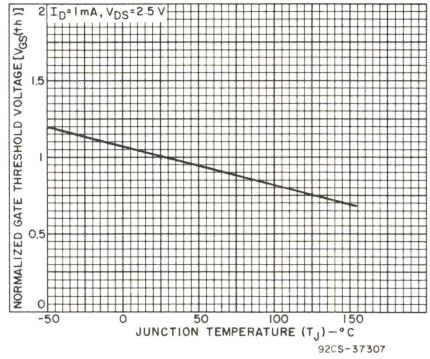


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

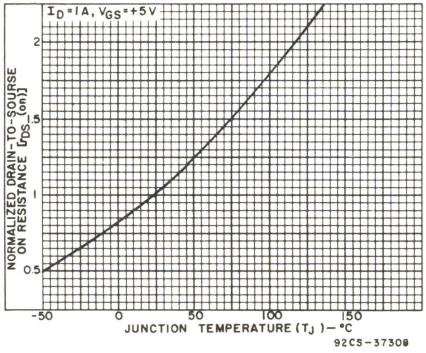


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

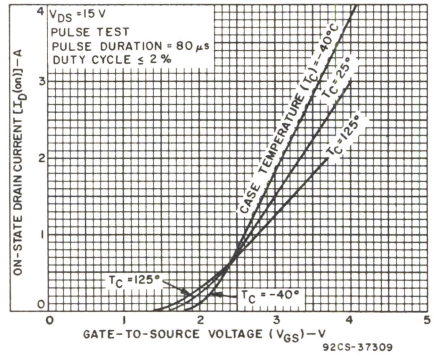


Fig. 5 — Typical transfer characteristics for all types.

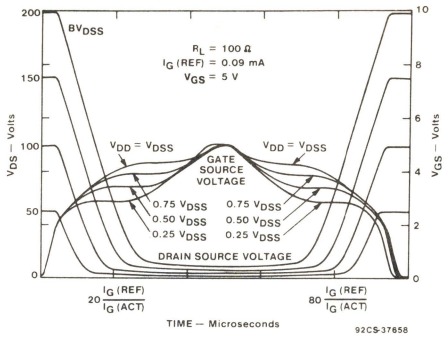


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

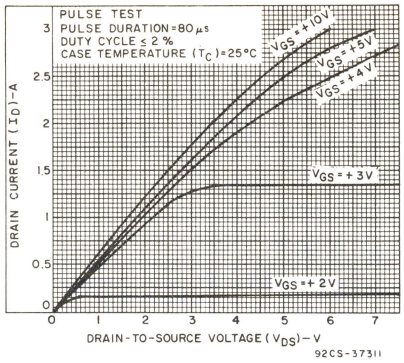


Fig. 7 — Typical saturation characteristics for all types.

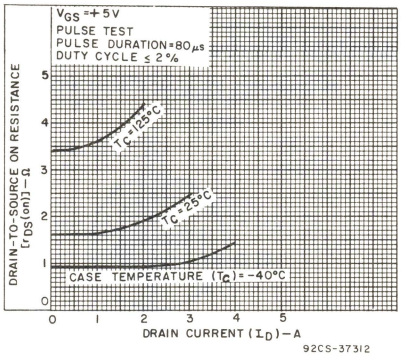


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

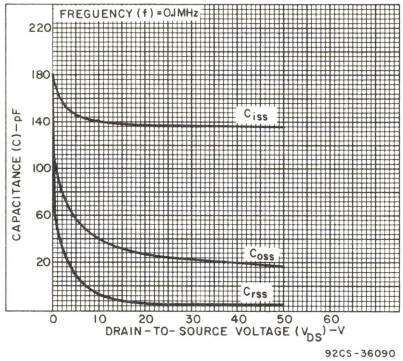


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

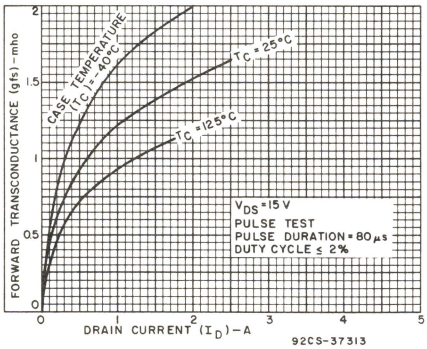


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

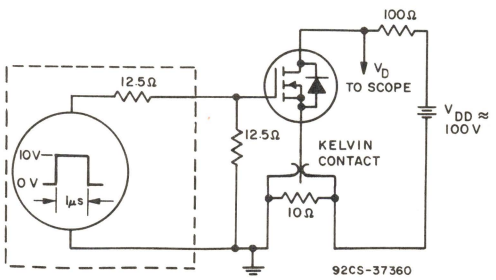


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFP4N05L
RFP4N06L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 4A, 50V and 60V
- $r_{DS(ON)} = 0.8\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

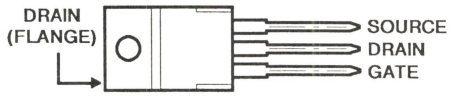
Description

The RFP4N05L and RFP4N06L are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP series types are supplied in the JEDEC TO-220AB plastic package.

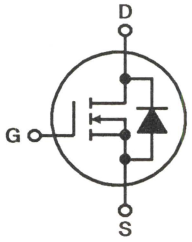
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

		RFP4N05L	RFP4N06L	UNITS
Drain-Source Voltage	V_{DS}	50	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	50	60	V
Continuous Drain Current				
RMS Continuous	I_D	4	4	A
Pulsed Drain Current	I_{DM}	10	10	A
Gate-Source Voltage	V_{GS}	±10	±10	V
Maximum Power Dissipation				
$T_C = +25^oC$	P_D	25	25	W
Above $T_C = +25^oC$, Derate Linearly		0.2	0.2	W/^{o}C
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2876

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05L MIN	LIMITS RFP4N05L MAX	LIMITS RFP4N06L MIN	LIMITS RFP4N06L MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	50	–	60	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V	–	1	–	–	μA
		V_{DS} = 50V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 40V	–	50	–	–	μA
		V_{DS} = 50V	–	–	–	50	mA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.8	–	0.8	V
		I_D = 2A, V_{GS} = 5V	–	2.0	–	2.0	V
		I_D = 4A, V_{GS} = 7.5V	–	4.8	–	4.8	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 5V	–	0.8	–	0.8	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	800	–	800	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	225	–	225	pF
Output Capacitance	C_{OSS}		–	100	–	100	pF
Reverse Transfer Capacitance	C_{RSS}		–	40	–	40	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 30V, R_{GEN} = ∞, R_{GS} = 6.25V, V_{GS} = 5V	10 (typ)	20	10 (typ)	20	ns
Rise Time	t_r		65 (typ)	130	65 (typ)	130	ns
Turn-Off Delay Time	$t_{d(off)}$		20 (typ)	40	20 (typ)	40	ns
Fall Time	t_f		30 (typ)	60	30 (typ)	60	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	5	–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS RFP4N05L MIN	LIMITS RFP4N05L MAX	LIMITS RFP4N06L MIN	LIMITS RFP4N06L MAX	UNITS
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 100A/μs	150 (typ)	150 (typ)	150 (typ)	150 (typ)	ns

* Pulse Test: Width ≤ 300μs, Duty Cycle ≤ 2%.

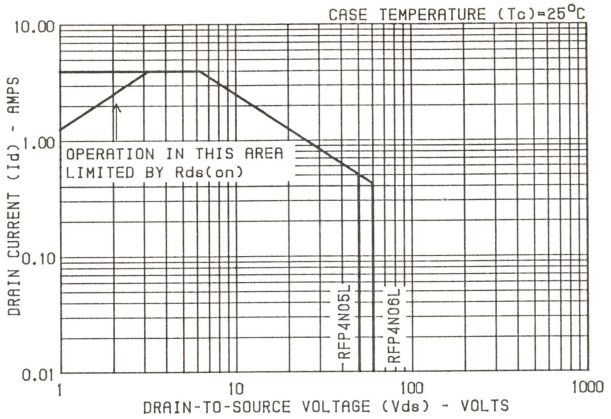


Fig. 1 - Maximum operating areas for all types.

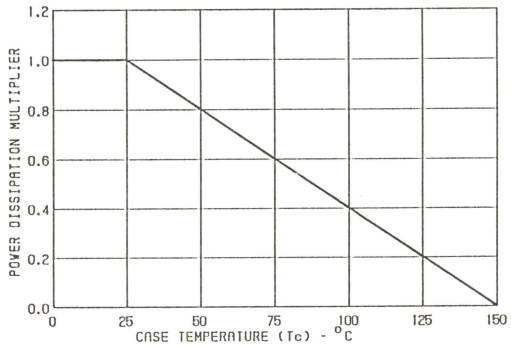


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

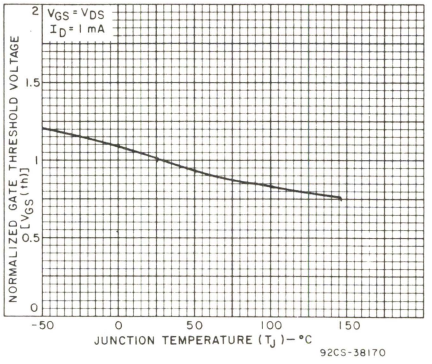
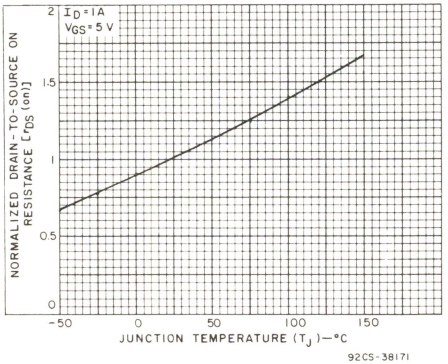


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.



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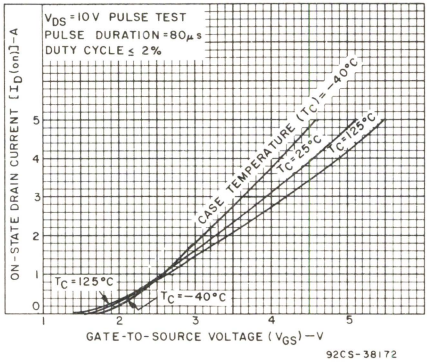


Fig. 5 - Typical transfer characteristics for all types.

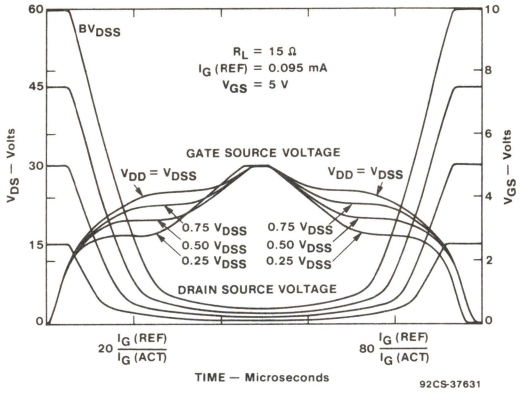


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

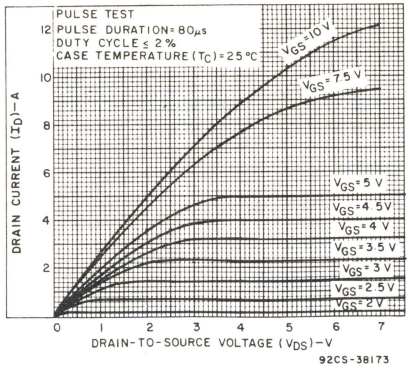


Fig. 7 - Typical saturation characteristics for all types.

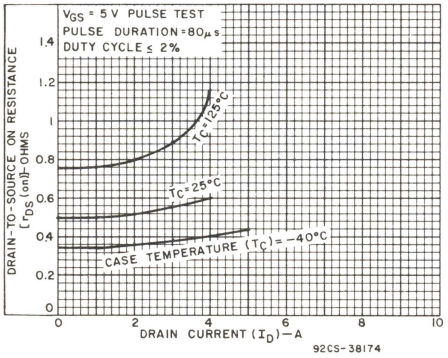


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

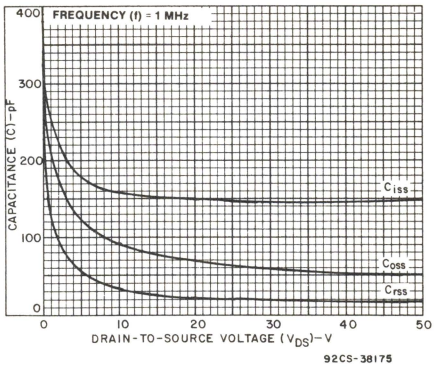


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

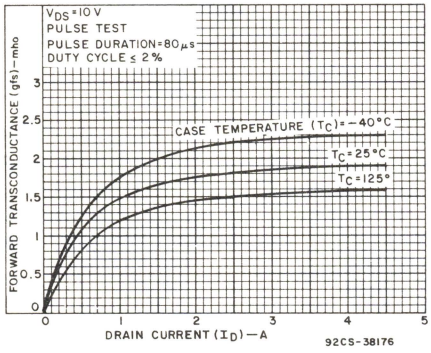


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

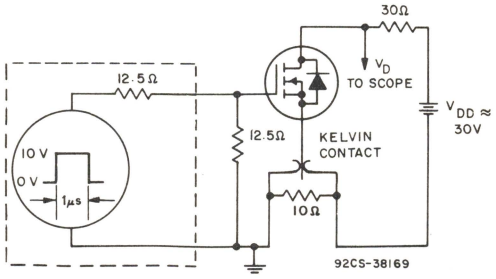


Fig. 11 - Switching Time Test Circuit.

HARRIS SEMICONDUCTOR

RFD7N10LE, RFD7N10LESM RFP7N10LE

7A, 100V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

February 1994

Features

- 7A, 100V
- $r_{DS(ON)} = 0.300\Omega$
- 2KV ESD Protected
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD7N10LE, RFD7N10LESM and RFP7N10LE N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V to 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

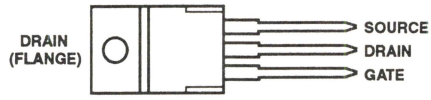
The RFD7N10LE is supplied in the JEDEC TO-251AA plastic package, the RFD7N10LESM is supplied in the JEDEC TO-252AA plastic package and the RFP7N10LE is supplied in the JEDEC TO-220AB plastic package. Due to space limitations the RFD7N10LE and RFD7N10LESM are branded 7N10LE; the RFP7N10LE is branded FP7N10LE.

When ordering use the entire part number; e.g. RFD7N10-LESM.

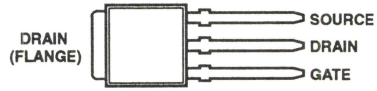
Formerly developmental type TA49046.

Packaging

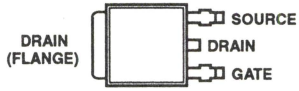
JEDEC TO-220AB
TOP VIEW



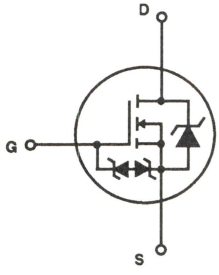
JEDEC TO-251AA
TOP VIEW



JEDEC TO-252AA
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RFD7N10LE, RFD7N10LESM, RFP7N10LE	UNITS
Drain Source Voltage	V_{DSS}	100	V
Drain Gate Voltage	V_{DGR}	100	V
Gate Source Voltage	V_{GS}	+10, -8	V
Drain Current			
RMS Continuous	I_D	7	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
(T_C = +25°C)	P_D	47	W
Derate above +25°C	P_T	0.318	W/°C
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	KV
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

Copyright © Harris Corporation 1994

File Number **3598**

Electrical Specifications $T_C = +25^oC$, **Unless Otherwise Specified**

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 0.25mA$, $V_{GS} = 0V$		100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 0.25mA$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = +10, -8V$		-	-	10	µA
On Resistance	$r_{DS(ON)}$	$I_D = 7A$, $V_{GS} = 5V$		-	-	0.300	W
Turn-On Time	t_{ON}	$V_{DD} = 50V$, $I_D = 7A$, $R_L = 7.1\Omega$, $V_{GS} = 5V$, $R_{GS} = 2.5\Omega$		-	-	110	ns
Turn-On Delay Time	$t_{D(ON)}$			-	10	-	ns
Rise Time	t_R			-	65	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	23	-	ns
Fall Time	t_F			-	18	-	ns
Turn-Off Time	t_{OFF}			-	-	60	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $10V$	$V_{DD} = 80V$, $I_D = 7A$, $R_L = 11.4\Omega$	-	125	150	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0$ to $5V$		-	67	80	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $1V$		-	3.7	4.5	nC
Plateau Voltage	$V_{(PLATEAU)}$	$I_D = 7A$, $V_{DS} = 15V$		-	-	4.0	V
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$		-	360	-	pF
Output Capacitance	C_{OSS}			-	70	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	20	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.15	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251 and TO-252 Package		-	-	100	°C/W
		TO-220 Package				80	

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 7A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 7A$, $dI_{SD}/dt = 100A/\mu s$	-	-	130	ns

Typical Performance Curves

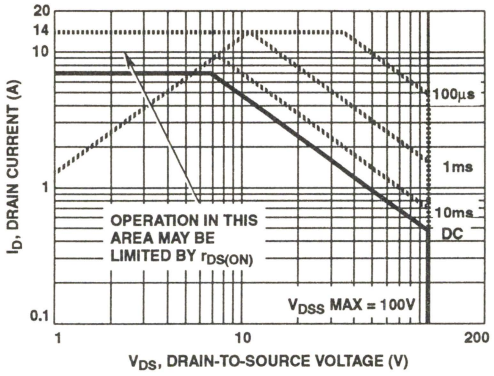


FIGURE 1. SAFE OPERATING AREA CURVE

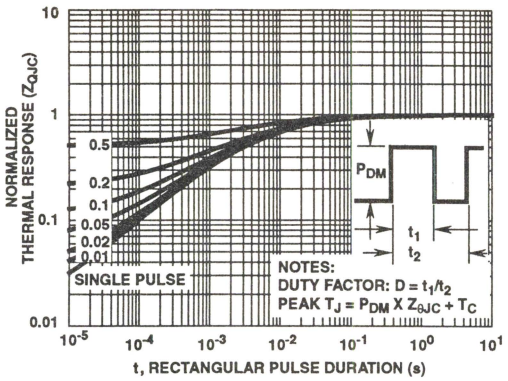


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

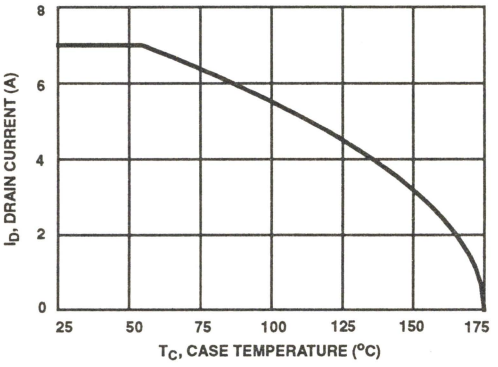


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

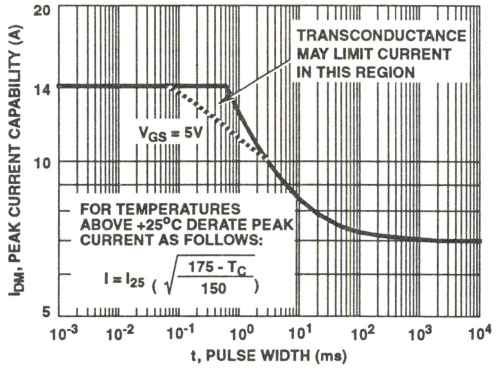


FIGURE 4. PEAK CURRENT CAPABILITY

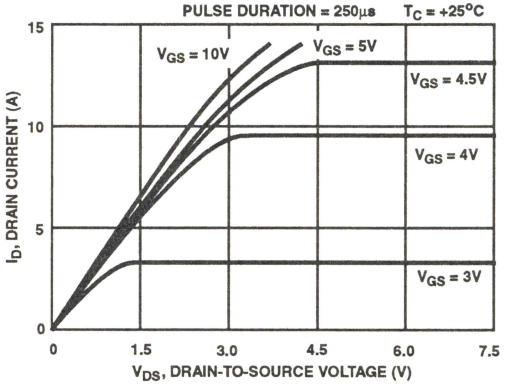


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

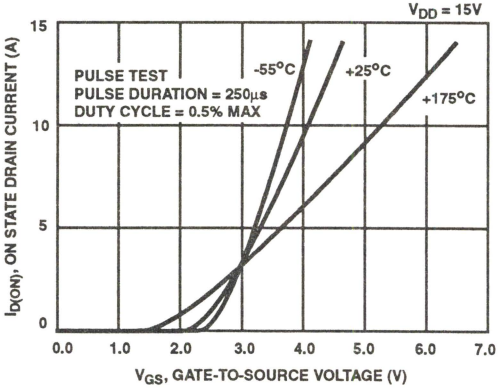


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

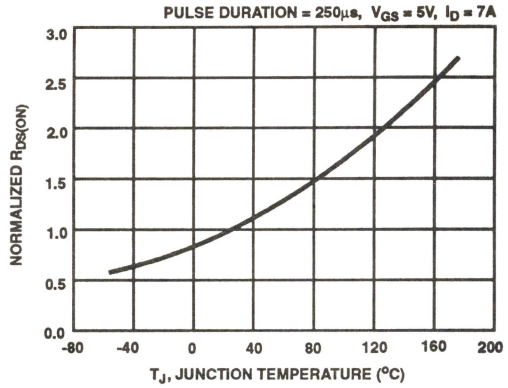


FIGURE 7. NORMALIZED $R_{DS(ON)}$ vs JUNCTION TEMPERATURE

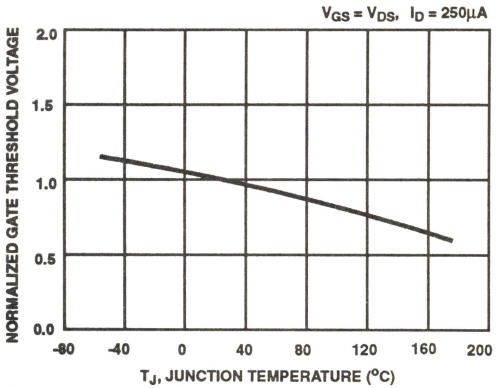


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

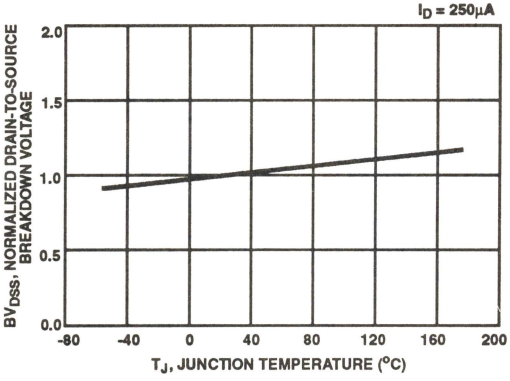


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

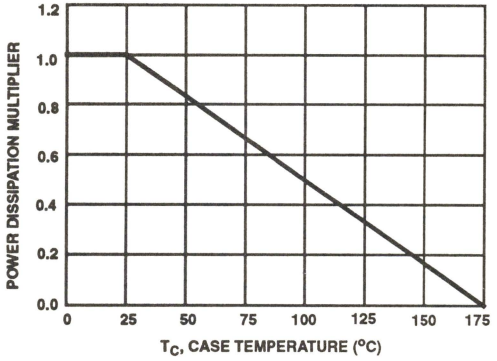


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

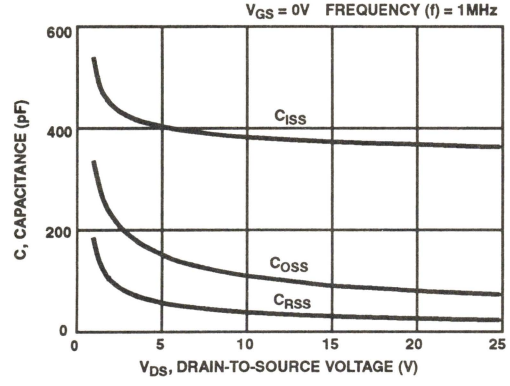


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN -TO-SOURCE VOLTAGE

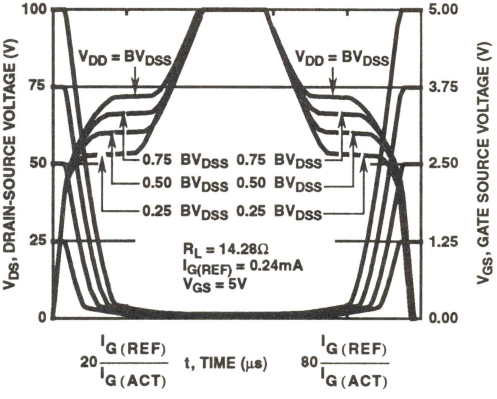


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

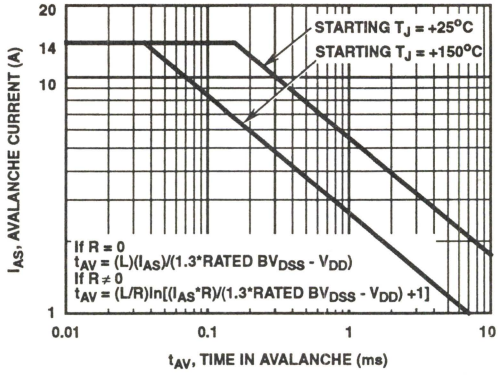


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

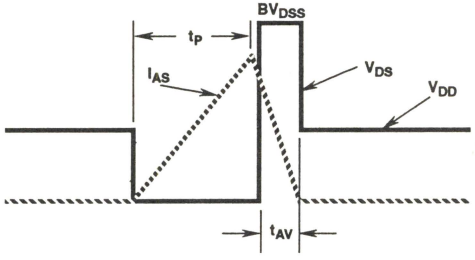


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

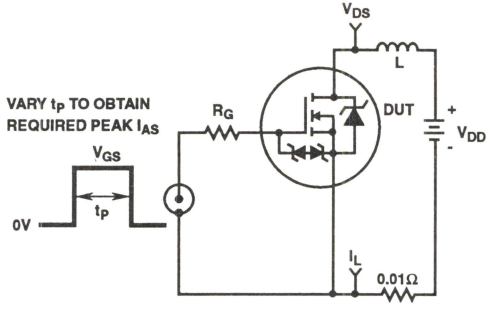


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

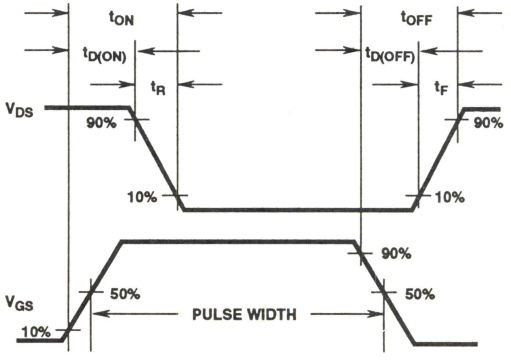


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

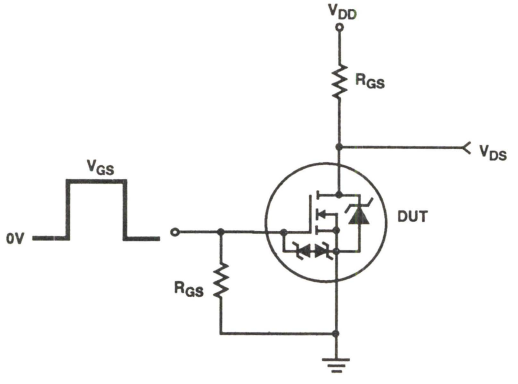


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

PSpice Model Listing

Temperature Compensated PSPICE for the RFD7N10LE, RFD7N10LESM, RFP7N10LE

SUBCKT RFD7N10LE 2 1 3; rev 6/2/93

CA 12 8 1.102e-9
CB 15 14 1.157e-9
CIN 6 8 0.370e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 115.8
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

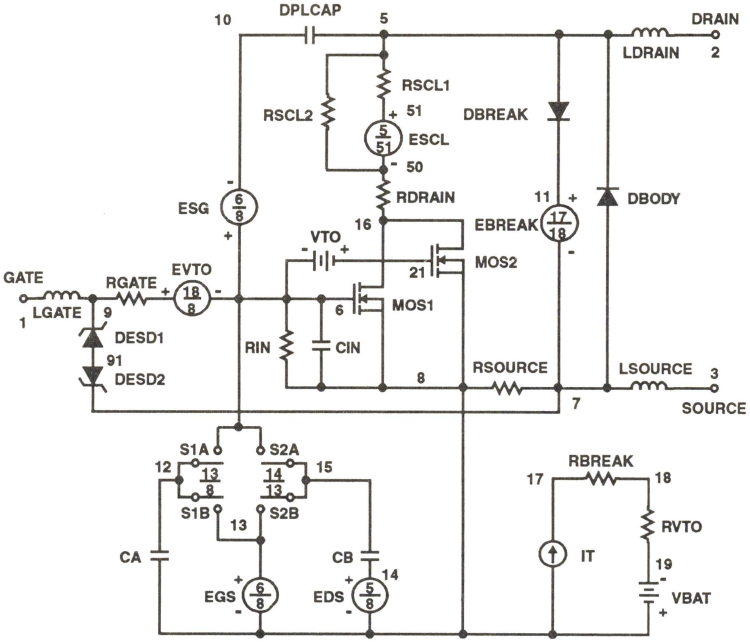
LDRAIN 2 5 1e-9
LGATE 1 9 3.58e-9
LSOURCE 3 7 3.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 136.9e-3
RGATE 9 20 7.61
RIN 6 8 1e9
RSCL1 5 51 RSLVCMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 84.4e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.444



ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/(15.5),7.25))}

.MODEL DBDMOD D (IS=5.07e-14 RS=1.37e-2 TRS1=1.72e-3 TRS2=-1.59e-6 CJO=2.57e-10 TT=3.84e-8)
.MODEL DBKMOD D (RS=2.32e-1 TRS1=6.50e-4 TRS2=1.72e-6)
.MODEL DESD1MOD D (BV=13.0 TBV1=2.2e-4 TBV2=0 RS=49 TRS1=0 TRS2=0)
.MODEL DESD2MOD D (BV=11.7 TBV1=-5.5e-4 TBV2=-8.5e-7 RS=0 TRS1=0 TRS2=0)
.MODEL DPLCAPMOD D (CJO=0.184e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=2.045 KP=14.07 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.13e-3 TC2=4.74e-8)
.MODEL RDSMOD RES (TC1=7.45e-3 TC2=2.68e-5)
.MODEL RSLVCMOD RES (TC1=1.75e-3 TC2=0)
.MODEL RVTOMOD RES (TC1=-2.73e-3 TC2=-5.46e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.35 VOFF=-1.75)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.75 VOFF=-4.35)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.75 VOFF=3.50)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.50 VOFF=-1.75)

.ENDS

NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records 1991.

HARRIS

RFM8N18L/20L
RFP8N18L/20L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 8A, 180V and 200V
- $r_{DS(ON)} = 0.5\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

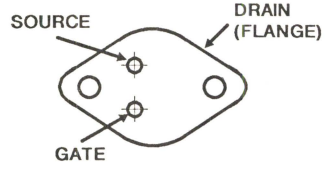
Description

The RFM8N18L and RFM8N20L and the RFP8N18L and RFP8N20L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

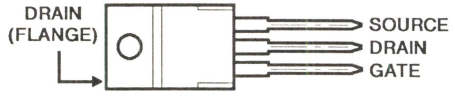
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Package

TO-204AA
BOTTOM VIEW

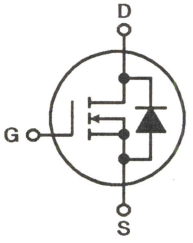


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

	RFM8N18L	RFM8N20L	RFP8N18L	RFP8N20L	UNITS
Drain-Source Voltage ..... V_{DS}	180	200	180	200	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$) ..... V_{DGR}	180	200	180	200	V
Continuous Drain Current					
RMS Continuous ..... I_D	8	8	8	8	A
Pulsed Drain Current ..... I_{DM}	20	20	20	20	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1514.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	2.0	—	2.0	V
		I_D=8 A V_{GS}=5 V	—	4.6	—	4.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	0.5	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=4 A	3.0	—	3.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	250	—	250	pF
Reverse-Transfer Capacitance	C_{rss}		—	120	—	120	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=4A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r		45(typ)	150	45(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	135	100(typ)	135	ns
Fall Time	t_f		60(typ)	105	60(typ)	105	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8N18L, RFM8N20L	—	1.67	—	1.67	°C/W
		RFP8N18L, RFP8N20L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=4 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	250(typ)		250(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

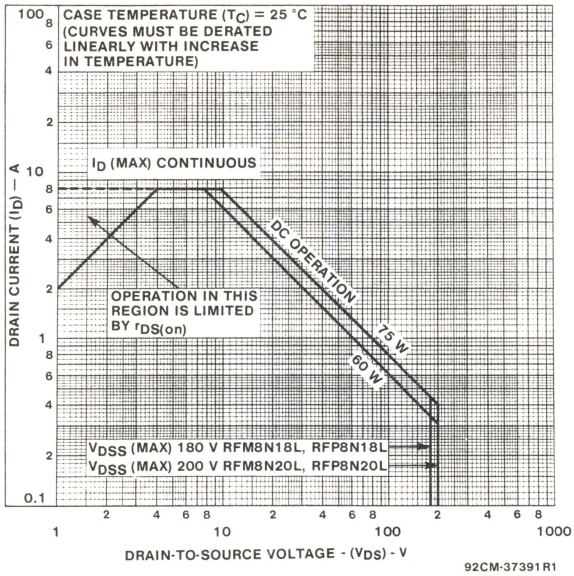


Fig. 1 — Maximum safe operating areas for all types.

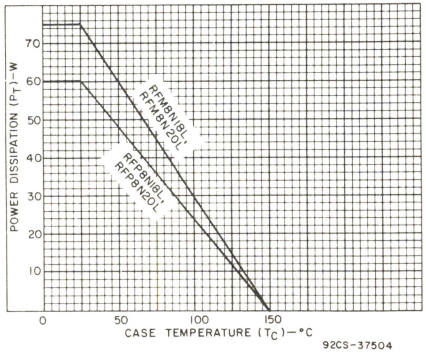


Fig. 2 — Power vs. temperature derating curve for all types.

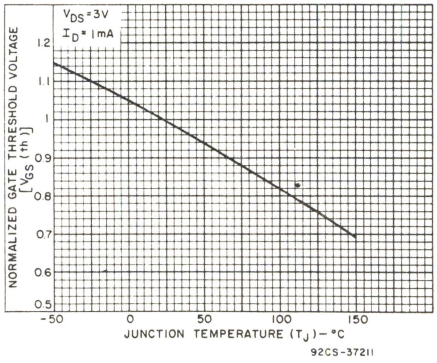


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

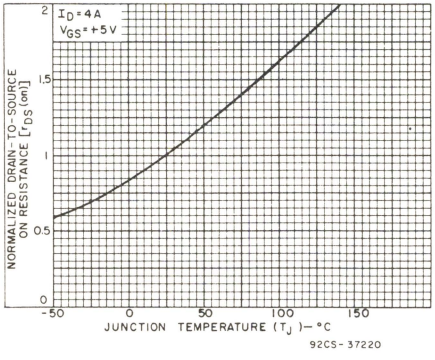


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

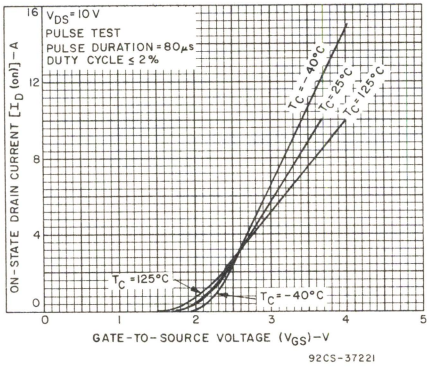


Fig. 5 — Typical transfer characteristics for all types.

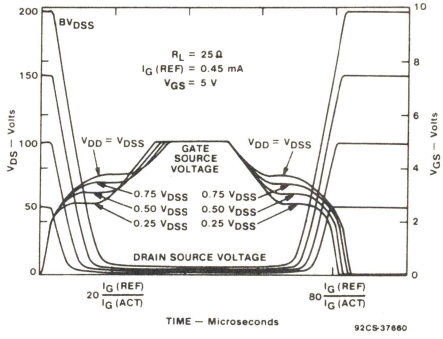


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

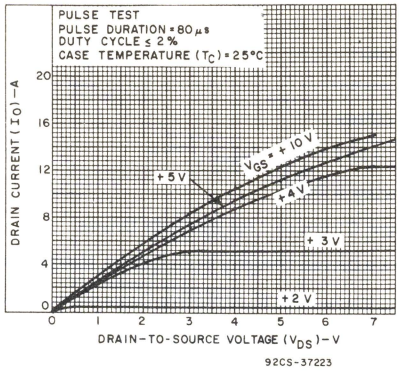


Fig. 7 — Typical saturation characteristics for all types.

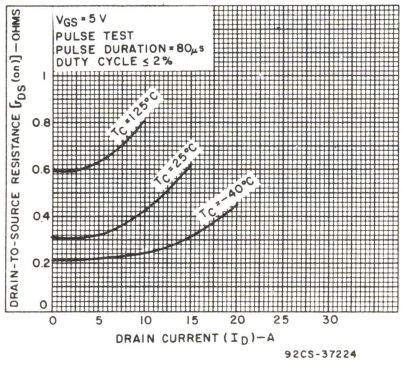


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

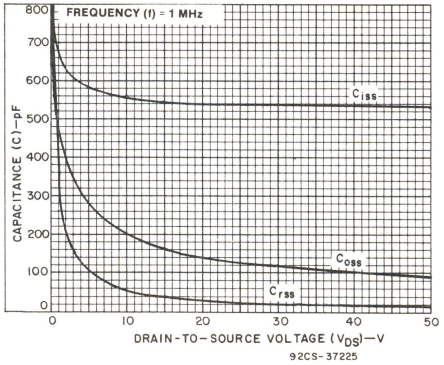


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

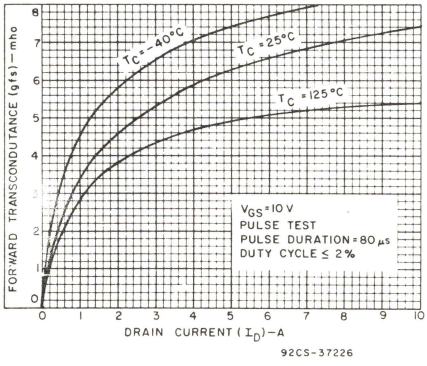


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

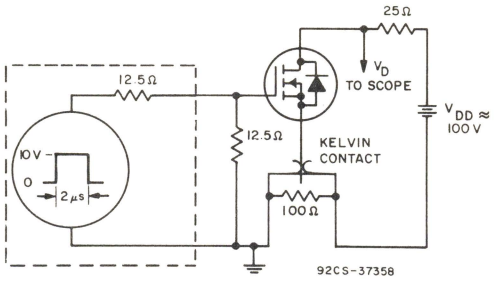


Fig. 11 — Switching Time Test Circuit.

HARRIS

RFM10N12L/15L
RFP10N12L/15L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 10A, 120V and 150V
- $r_{DS(ON)} = 0.3\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

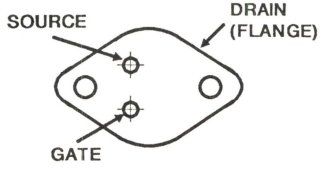
Description

The RFM10N12L and RFM10N15L and the RFP10N12L and RFP10N15L are N-channel enhancmement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

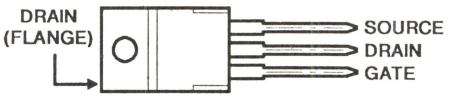
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Package

TO-204AA
BOTTOM VIEW

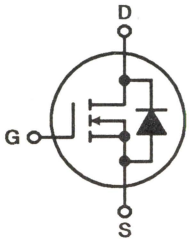


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

	RFM10N12L	RFM10N15L	RFP10N12L	RFP10N15L	UNITS
Drain-Source Voltage ..... V_{DS}	120	150	120	150	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$) ..... V_{DGR}	120	150	120	150	V
Continuous Drain Current					
RMS Continuous ..... I_D	10	10	10	10	A
Pulsed Drain Current ..... I_{DM}	25	25	25	25	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
$T_C = +25^oC$ ..... P_D	75	75	60	60	W
Above $T_C = +25^oC$, Derate Linearly	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1559.1**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 2 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V V_{DS} = 120 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 100 V V_{DS} = 120 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	1.5	—	1.5	V
		I_D = 10 A V_{GS} = 5 V	—	4	—	4	V
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	1200	—	1200	pF
Output Capacitance	C_{oss}		—	250	—	250	pF
Reverse-Transfer Capacitance	C_{rss}		—	120	—	120	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 75 V I_D = 5 A R_{gen} = ∞ R_{gs} = 6.25 Ω V_{GS} = 5 V	15(typ)	60	15(typ)	60	ns
Rise Time	t_r		50(typ)	135	50(typ)	135	ns
Turn-Off Delay Time	$t_{d(off)}$		90(typ)	135	90(typ)	135	ns
Fall Time	t_f		90(typ)	135	90(typ)	135	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N12L, RFM10N15L	—	1.67	—	1.67	°C/W
		RFP10N12L, RFP10N15L	—	2.083	—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%

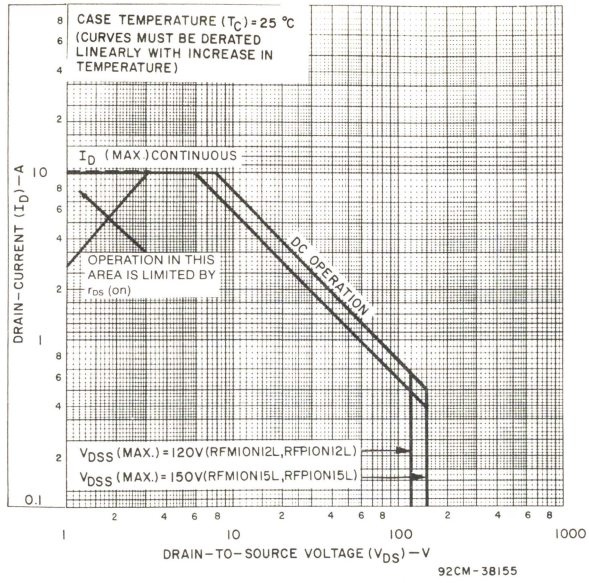


Fig. 1 - Maximum safe operating areas for all types.

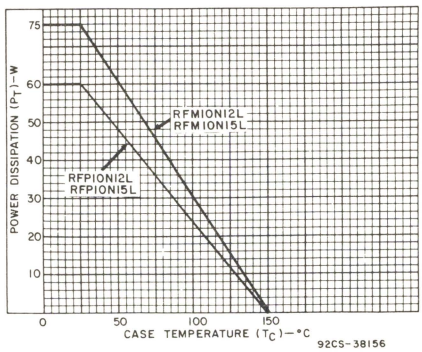


Fig. 2 - Power vs. temperature derating curve for all types.

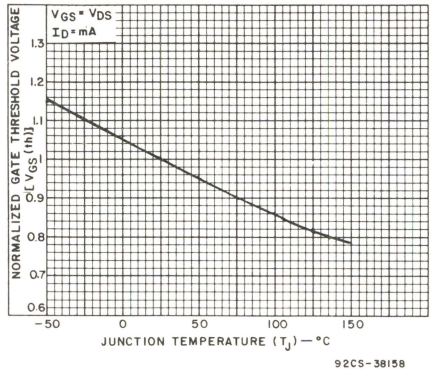


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

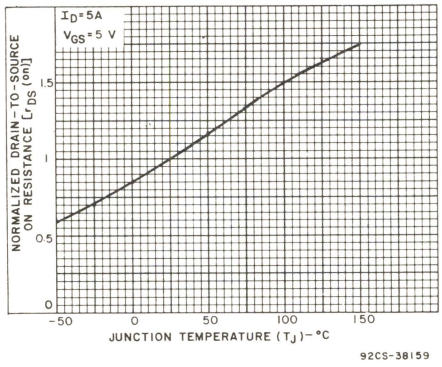


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

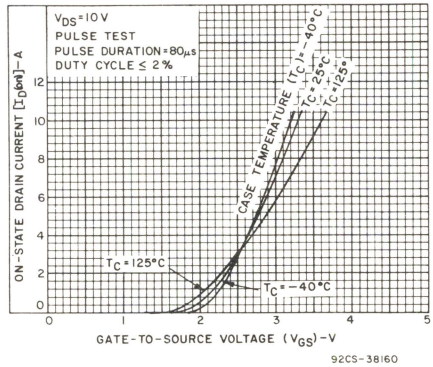


Fig. 5 - Typical transfer characteristics for all types.

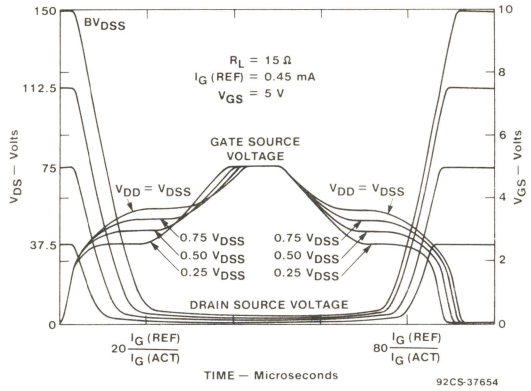


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

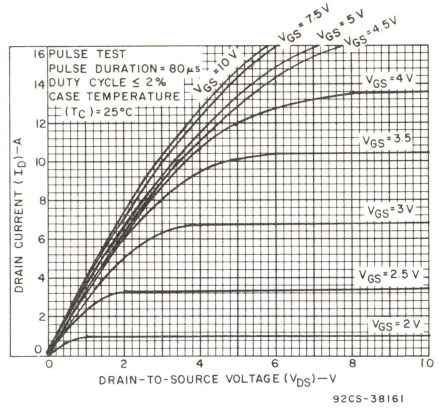


Fig. 7 - Typical saturation characteristics for all types.

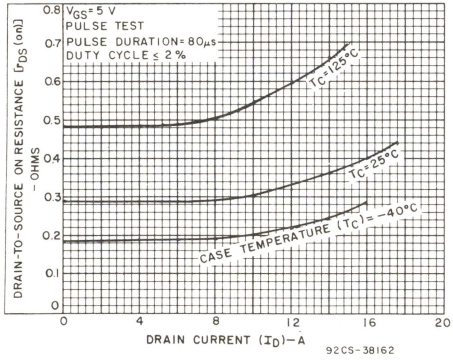


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

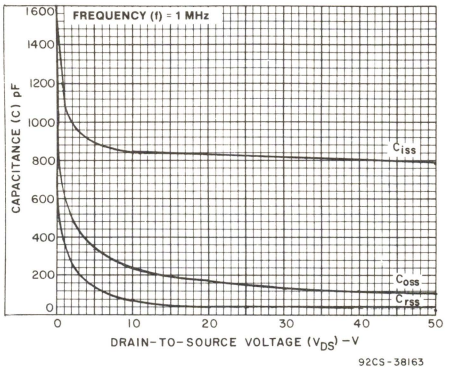


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

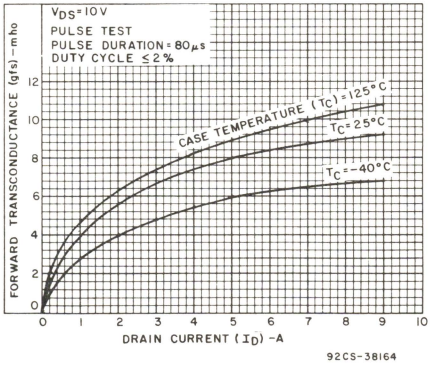


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

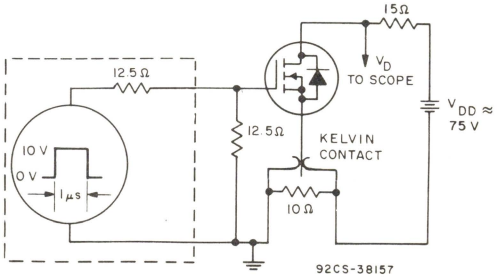


Fig. 11 - Switching Time Test Circuit.

HARRIS SEMICONDUCTOR

RFD12N06RLE, RFD12N06RLESM RFP12N06RLE

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

January 1994

Features

- 12A, 60V
- $r_{DS(on)} = 0.135\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

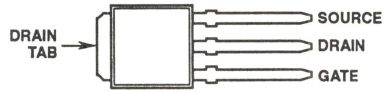
Description

These N-channel logic-level ESD protected power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

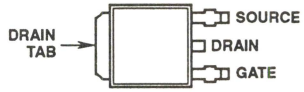
The RFD12N06RLE is supplied in the JEDEC TO-251, RFD12N06RLESM in the JEDEC T0-252, and RFP12N06-RLE in the JEDEC TO-220AB plastic package.

Packages

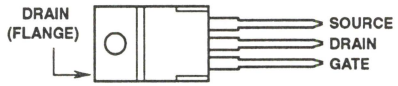
RFD12N06RLE (TO-251)
TOP VIEW



RFD12N06RLESM (TO-252)
TOP VIEW

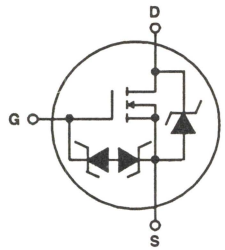


RFP12N06RLE (TO-220AB)
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	12	A
Pulsed Drain Current	I_{DM}	26	A
Gate-Source Voltage	V_{GS}	+10	-5V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Above T_C = +25°C, Derate Linearly		0.32	W/°C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve Electrostatic Discharge Rating,		2	KV
ESD, MIL-STD-883, Category B(2)			
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

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File Number **2407.2**

ELECTRICAL CHARACTERISTICS, *Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS		LIMITS RFD12N06RLE RFD12N06RLESM RFP12N06RLE		UNITS
				Min	Max	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA V_{GS} = 0 V		60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 0.25 mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V T_C = 150° C		— —	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10 V V_{GS} = -5 V		— —	10 10	μA
On Resistance	$r_{DS(on)}$	V_{GS} = 5.0 V, I_D = 12 A V_{GS} = 4.0 V, I_D = 12 A		— —	0.135 0.160	Ω
Turn-On Time	$t_{(on)}$	See Fig. 13		—	60	ns
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 6 A		12 (typ)	—	ns
Rise Time	t_r	R_L = 5.0 Ω		20 (typ)	—	ns
Turn-Off Delay Time	$t_{d(off)}$	Ig1 = Ig2 = 0.4 A		24 (typ)	—	ns
Fall Time	t_f	$V_{GS(clamp)}$ = +5 V, -0.6 V		12 (typ)	—	ns
Turn-Off Time	$t_{(off)}$			—	60	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-10 V	V_{DD} = 48 V I_D = 12 A R_L = 4.0 Ω	—	40	nC
Gate Charge at 5 Volts	$Q_{g(5)}$	V_{GS} = 0-5 V		—	20	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0-1 V		—	1.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 12 A, V_{DS} = 15 V		—	4.0	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30 V, I_D = 6 A L = 0.2 uH, Ig1 = Ig2 = 0.4 A $V_{GS(clamp)}$ = +5.0 V, -0.6 V R_L = 5.0 Ω		—	10	μJ
Thermal Resistance Junction to Case	RθJC			—	3.125	°C/W
Thermal Resistance Junction to Ambient	RθJA	TO-251 & TO-252 packages TO-220 package		— —	100 80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Forward Voltage	V_{SD}	I_{SD} = 12A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 12 A dI_F/dt = 100 A/μs	—	200	ns

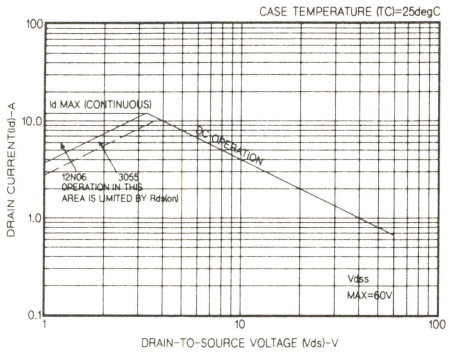


Fig. 1 - Safe-operating area curve. (Curves must be derated linearly with increase in case temperature.)

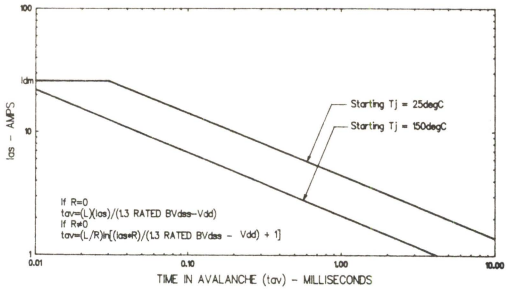


Fig. 2 - Unclamped-inductive-switching. Safe-operating-area. (Single pulse UIS SOA.)

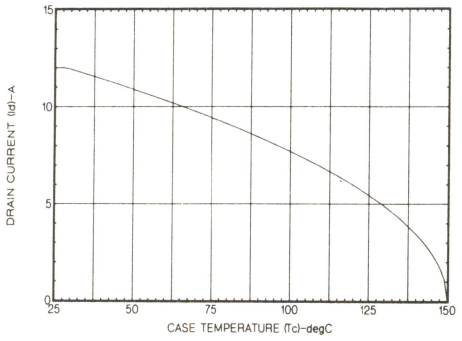


Fig. 3 - Maximum continuous drain current vs. temperature.

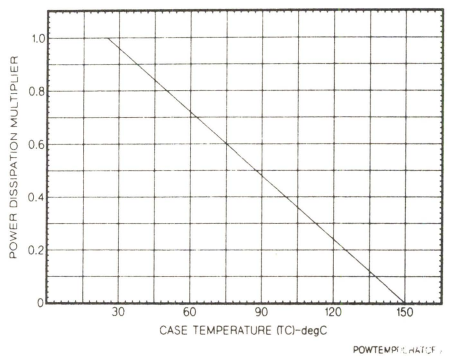


Fig. 4 - Normalized power dissipation vs. temperature derating curve.

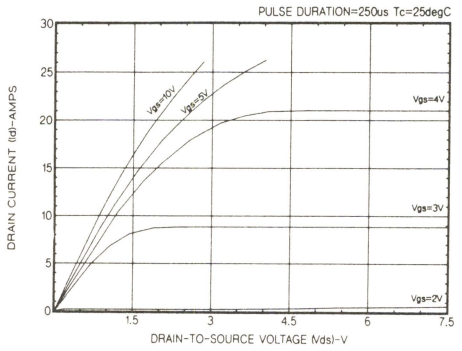


Fig. 5 - Typical saturation characteristics.

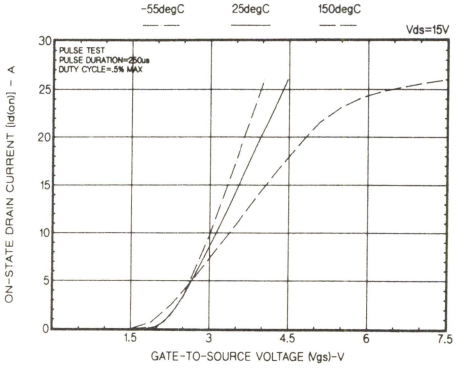


Fig. 6 - Typical transfer characteristics.

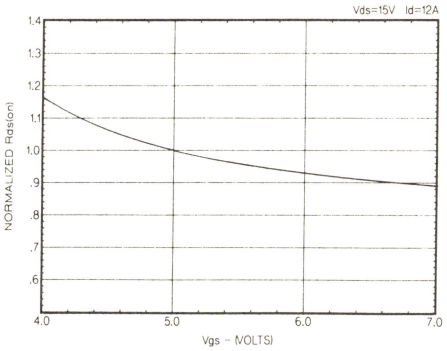


Fig. 7 - Normalized $r_{DS}(on)$ vs. V_{gs}.

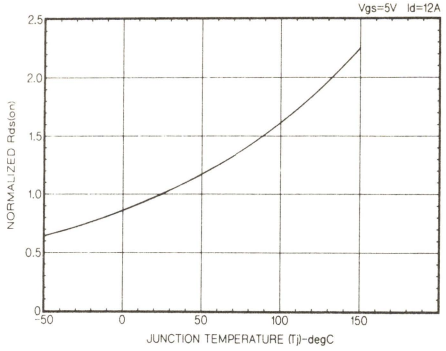


Fig. 8 - Normalized $r_{DS(on)}$ vs. junction temperature.

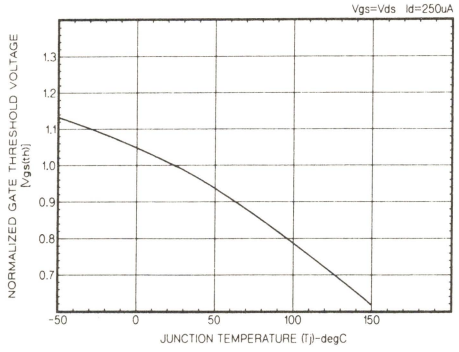


Fig. 9 - Normalized gate threshold voltage vs. temperature.

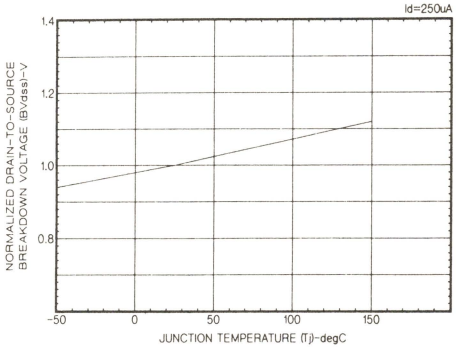


Fig. 10 - Normalized drain source breakdown voltage vs. temperature.

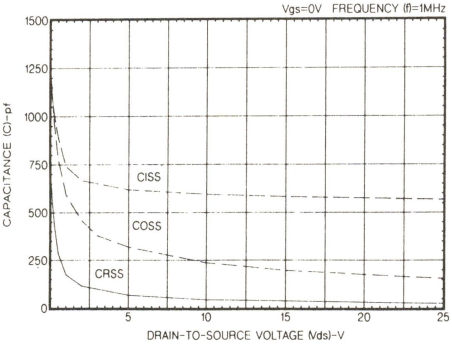


Fig. 11 - Typical capacitance vs. voltage.

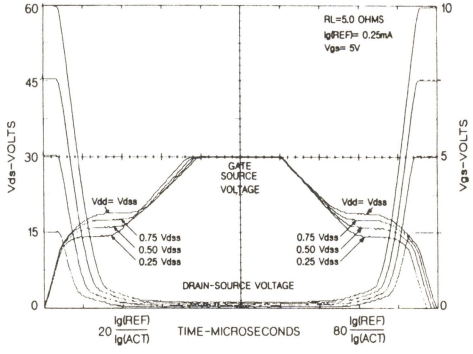


Fig. 12 – Typical switching waveforms for constant gate current. Refer to Harris application notes AN7254 and AN-7260.

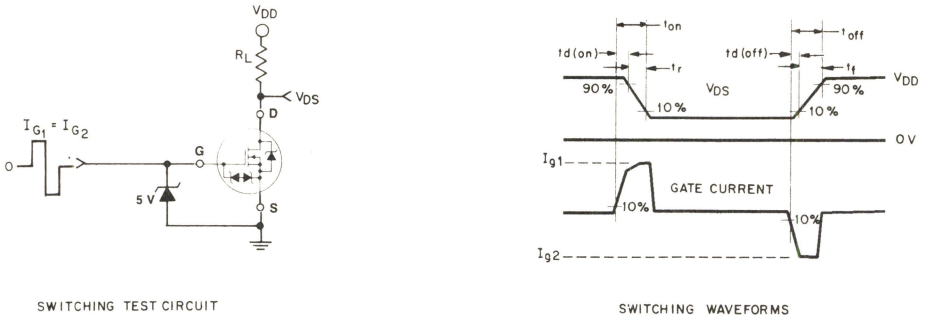


Fig. 13 - Resistive switching.

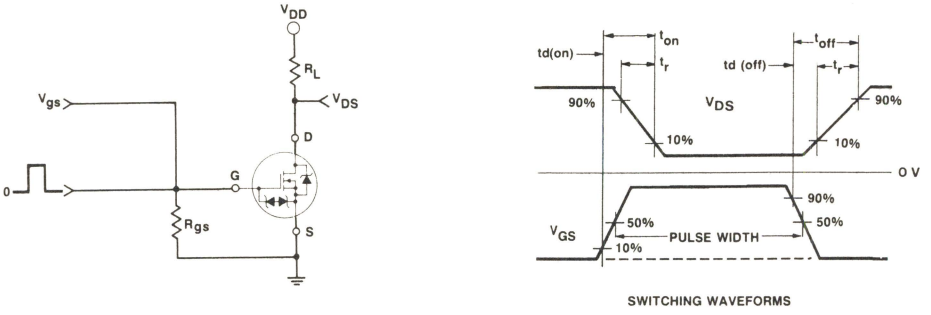


Fig. 14 - Resistive switching.

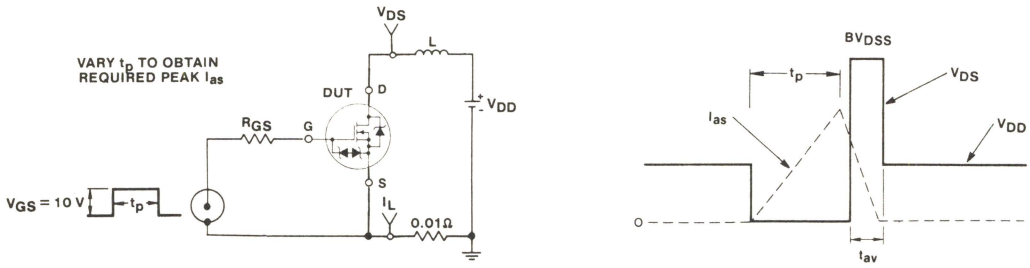


Fig. 15 - Unclamped inductive switching test.

HARRIS

RFM12N08L/10L
RFP12N08L/10L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 12A, 80V and 100V
- $r_{DS(ON)} = 0.2\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

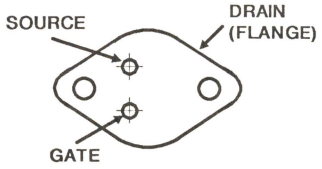
The RFM12N08L and RFM12N10L and the RFP12N08L and RFP12N10L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

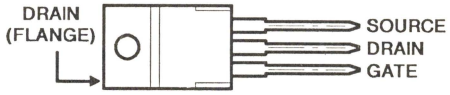
Because of space limitations branding (marking) on type RFP12N08L is F12N08L and on type RFP12N10L is F12N10L.

Package

TO-204AA
BOTTOM VIEW

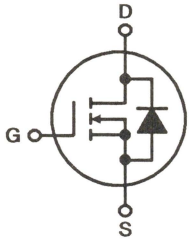


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	RFM12N08L	RFM12N10L	RFP12N08L	RFP12N10L	UNITS
Drain-Source Voltage ..... V_{DS}	80	100	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ) ..... V_{DGR}	80	100	80	100	V
Continuous Drain Current					
RMS Continuous ..... I_D	12	12	12	12	A
Pulsed Drain Current ..... I_{DM}	30	30	30	30	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	60	60	W
Above T_C = +25°C, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 1512.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=5 V	—	3.3	—	3.3	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	325	—	325	pF
Reverse-Transfer Capacitance	C_{rss}		—	170	—	170	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=6 A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	50	15(typ)	50	ns
Rise Time	t_r		70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	130	100(typ)	130	ns
Fall Time	t_f		80(typ)	150	80(typ)	150	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12N08L, RFM12N10L	—	1.67	—	1.67	°C/W
		RFP12N08L, RFP12N10L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

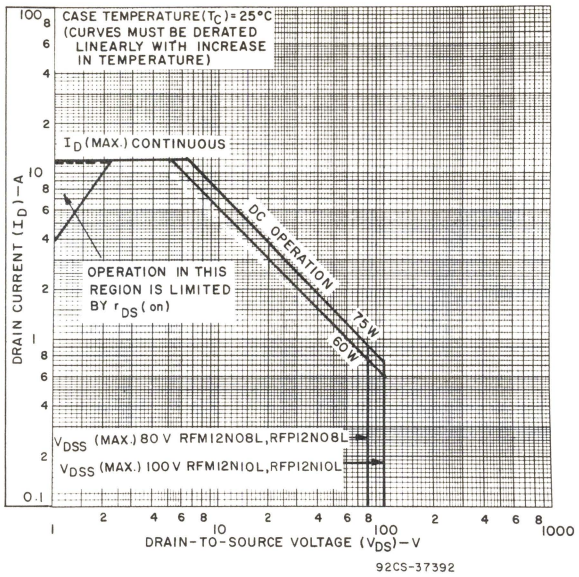


Fig. 1 — Maximum operating areas for all types.

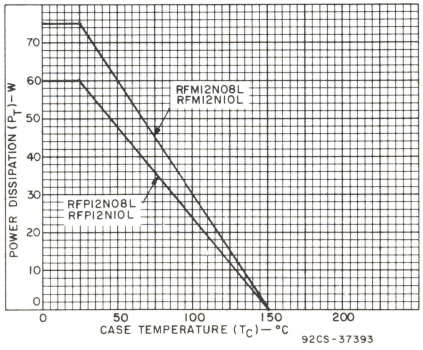


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

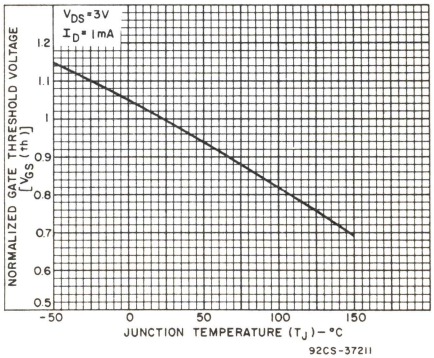


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

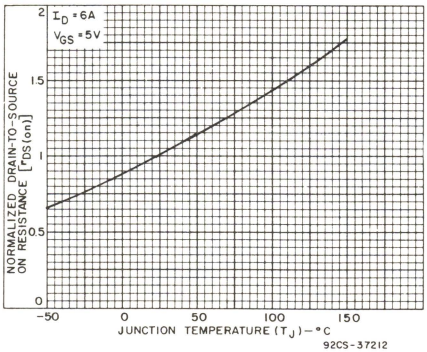


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

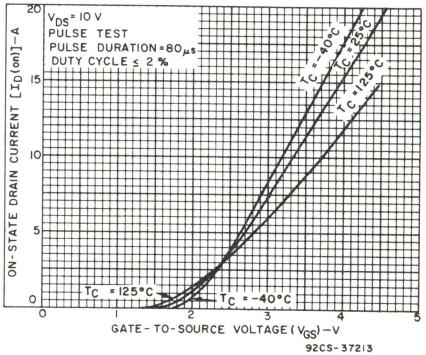


Fig. 5 — Typical transfer characteristics for all types.

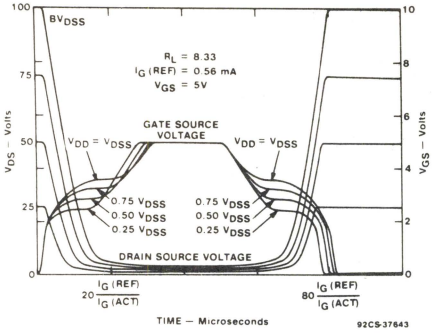


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

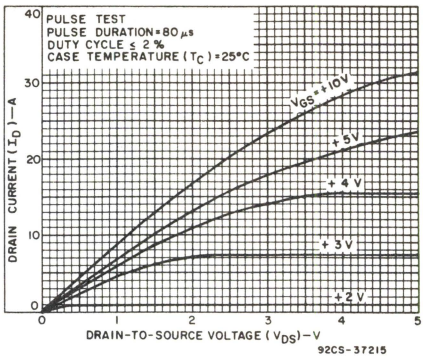


Fig. 7 — Typical saturation characteristics for all types.

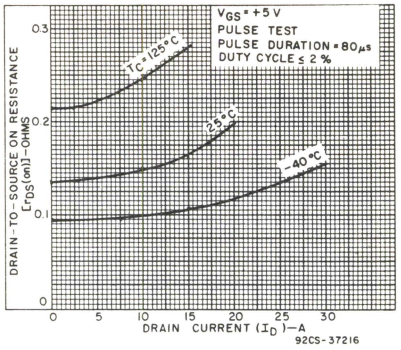


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

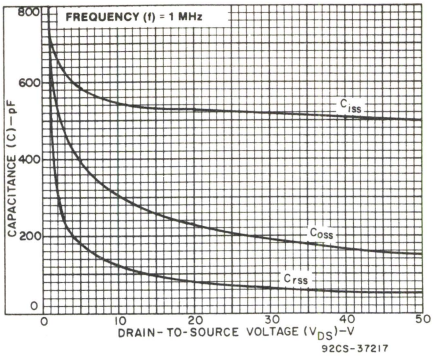


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

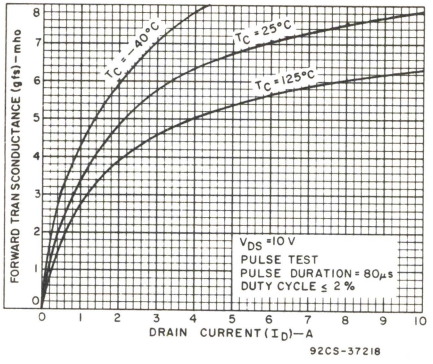


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

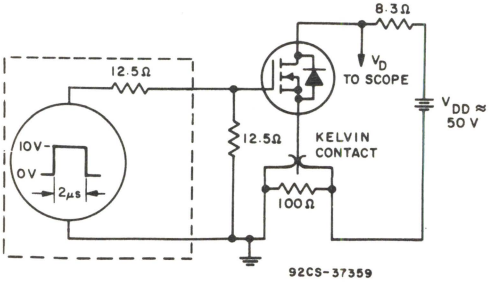


Fig. 11 — Switching Time Test Circuit.

RFD14N05L/05LSM
RFP14N05L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

June 1992

Features

- 14A, 50V
- $r_{DS(on)} = 0.100\Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Operating Temperature ..... +150°C

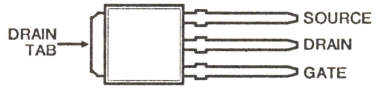
Description

The RFD14N05L, RFD14N05LSM and RFP14N05L N-Channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers, and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

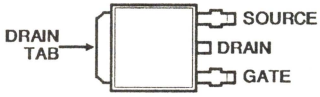
The RFD14N05L is supplied in the JEDEC TO-251 plastic package, the RFD14N05LSM in the JEDEC TO-252 plastic package and the RFP14N05L in the JEDEC TO-220AB plastic package.

Packages

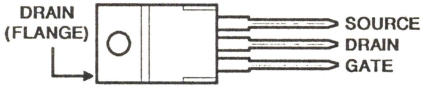
RFD14N05L
TO-251
TOP VIEW



RFD14N05LSM
TO-252
TOP VIEW

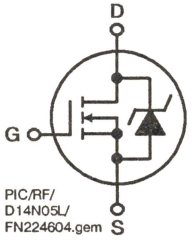


RFP14N05L
TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	14	A
Pulsed Drain Current	I_{DM}	35	A
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	40	W
Above T_C = +25°C, Derate Linearly		0.32	W/°C
Single Pulse Avalanche Rating		Refer to UIS SOA Curve	
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2246.1**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C) = 25° C Unless Otherwise Specified.

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V		—	1	μA
		T_C = 150° C		—	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On-Resistance	$r_{DS}(on)$	I_D = 14 A, V_{GS} = 5 V		—	0.1	Ω
		I_D = 14 A, V_{GS} = 4 V		—	0.12	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 7 A		—	60	ns
Turn-On Delay Time	$t_d(on)$	I_{g1} = I_{g2} = 0.4 A		—	13 (typ.)	ns
Rise Time	t_r	V_{GS}(clamp) +5 V, -0.6 V		—	24 (typ.)	ns
Turn-Off Delay Time	$t_d(off)$	R_L = 3.57 Ω		—	42 (typ.)	ns
Fall Time	t_f	(See Figs. 10 & 11)		—	16 (typ.)	ns
Turn-Off Time	t(off)			—	100	ns
Total Gate Charge	Q_g(total)	V_{DD} = 40 V	V_{GS} = 0-10 V	—	40	nC
Gate Charge at 5 V	$Q_g(5)$	I_D = 14 A	V_{GS} = 0-5 V	—	25	nC
Threshold Gate Charge	$Q_g(th)$	R_L = 2.86 Ω	V_{GS} = 0-1 V	—	1.5	nC
Plateau Voltage	V(plateau)	I_D = 14 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss Per Cycle	E_{off}	V_{DD} = 25 V, I_D = 7 A, L = 0.2 μH, R_L = 3.57 Ω, I_{g1} = I_{g2} = 0.2 A, V_{GS}(clamp) +5 V, -0.6 V		—	14	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	3.125	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	TO-251 & TO-252		—	100	°C/W
		TO-220		—	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/d_t = 100 A/μs	—	125	ns

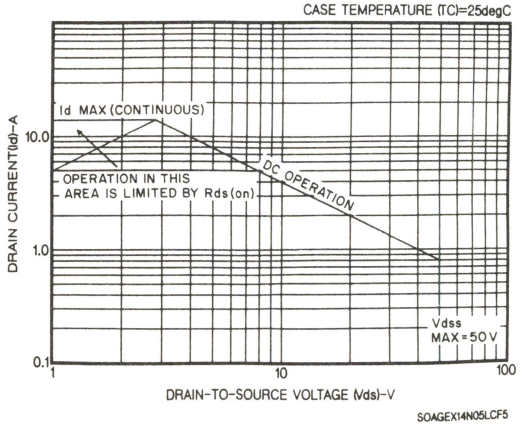


Fig. 1 - Safe-operating-area curve. (Curves must be derated linearly with increase in case temperature.)

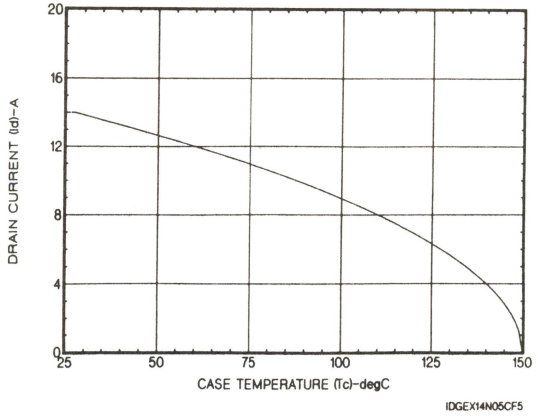


Fig. 2 - Maximum continuous drain current vs. temperature.

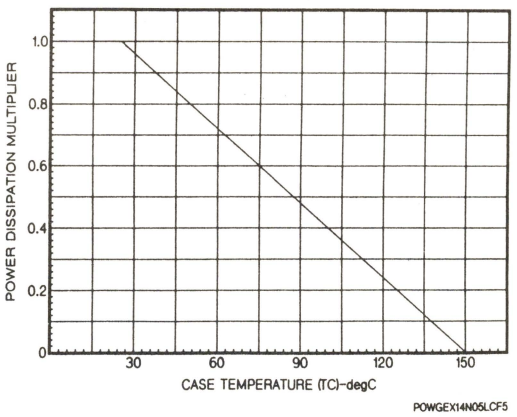


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

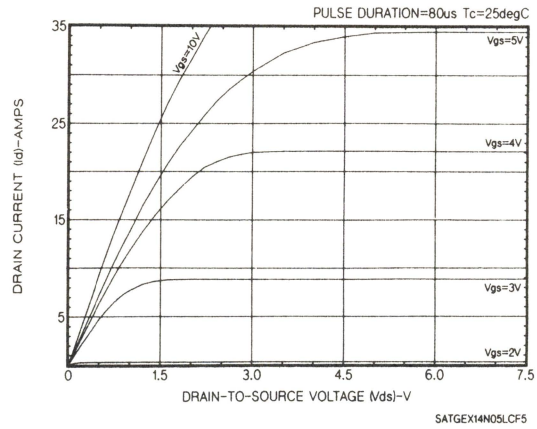


Fig. 4 - Typical saturation characteristics.

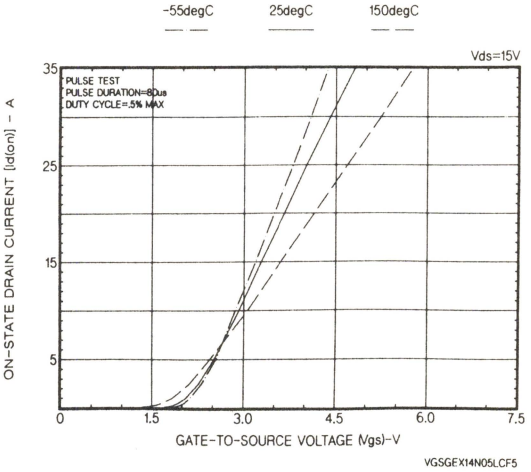


Fig. 5 - Typical transfer characteristics.

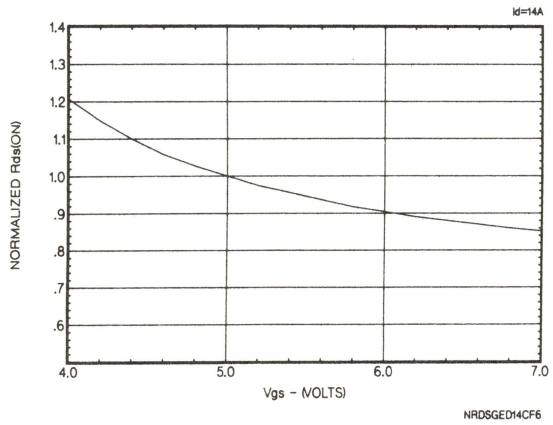


Fig. 6 - Normalized $r_{DS}(on)$ vs. V_{gs}.

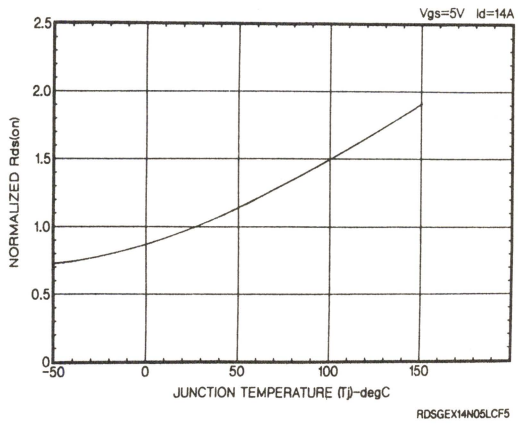


Fig. 7 - Normalized $r_{DS}(on)$ vs. junction temperature.

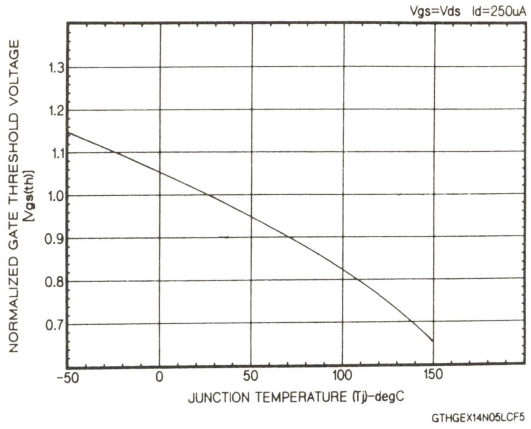


Fig. 8 - Gate threshold voltage vs. temperature.

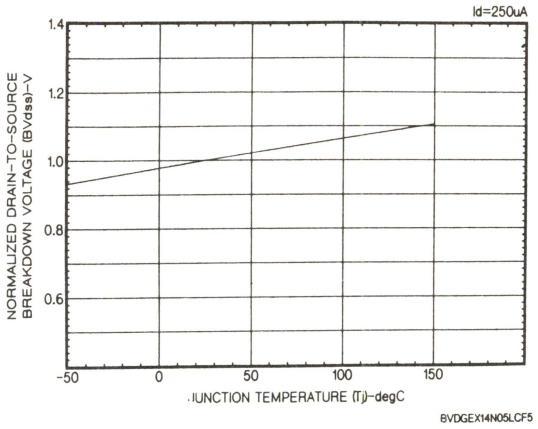


Fig. 9 - Drain source breakdown voltage vs. temperature.

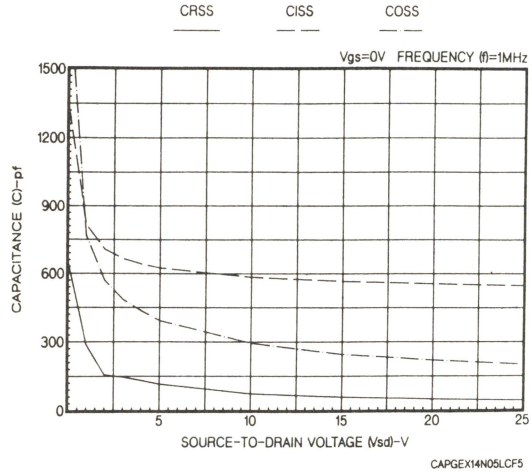


Fig. 10 - Typical capacitance vs. voltage.

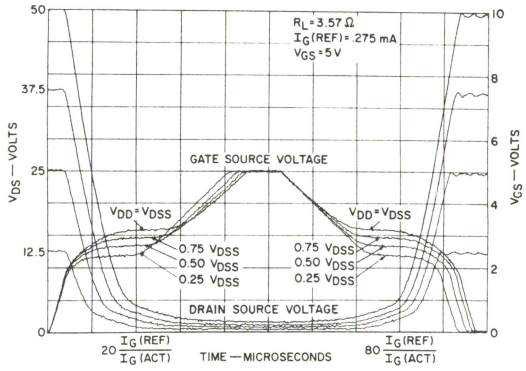


Fig. 11 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

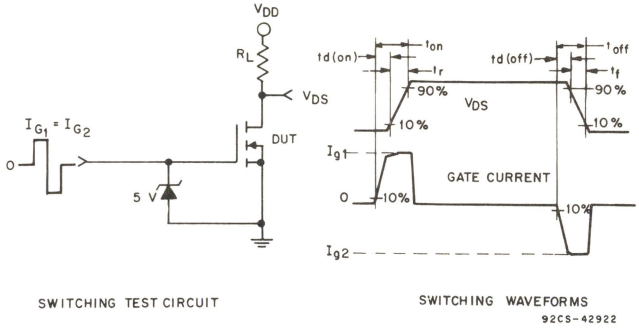


Fig. 12 - Resistive switching.

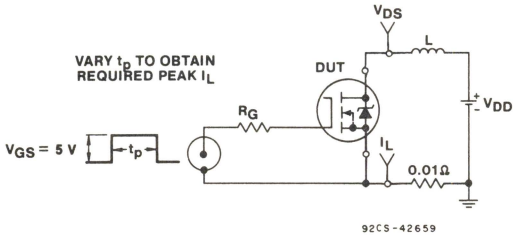


Fig. 13 - Unclamped energy test circuit.

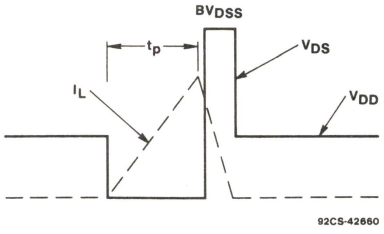


Fig. 14 - Unclamped energy waveforms.

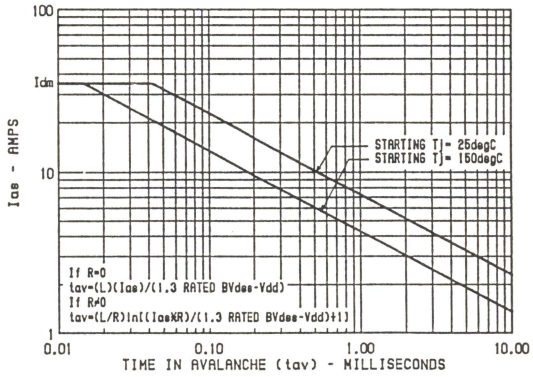


Fig. 15 - Unclamped inductive switching.

HARRIS

RFM15N05L/06L
RFP15N05L/06L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 15A, 50V and 60V
- $r_{DS(ON)} = 0.14\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

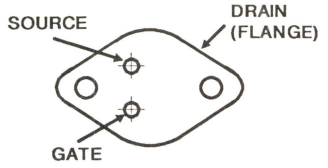
The RFM15N05L and RFM15N06L and the RFP15N05L and RFP15N06L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

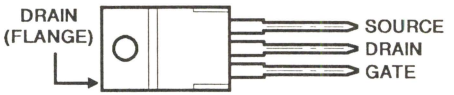
Because of space limitations branding (marking) on type RFP15N05L is F15N05L and on type RFP15N06L is F15N06L.

Package

TO-204AA
BOTTOM VIEW

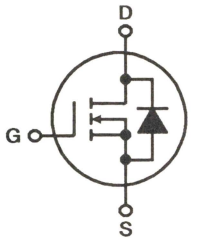


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	RFM15N05L	RFM15N06L	RFP15N05L	RFP15N06L	UNITS
Drain-Source Voltage ..... V_{DS}	50	60	50	60	V
Drain-Gate Voltage (R_{GS} = 1MΩ) ..... V_{DGR}	50	60	50	60	V
Continuous Drain Current					
RMS Continuous ..... I_D	15	15	15	15	A
Pulsed Drain Current ..... I_{DM}	40	40	40	40	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	60	60	W
Above T_C = +25°C, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **1558.1**

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125° C V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	1.05	—	1.05	V
		I_D = 15 A V_{GS} = 5 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 7.5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	900	—	900	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}	f = 1 MHz	—	200	—	200	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r	I_D = 7.5 A	250(typ)	325	250(typ)	325	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = ∞ R_{gs} = 6.25 Ω	200(typ)	325	200(typ)	325	
Fall Time	t_f	V_{GS} = 5 V	225(typ)	325	225(typ)	325	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM15N05L, RFM15N06L	—	1.67	—	1.67	°C/W
		RFP15N05L, RFP15N06L	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 7.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	225 (typ.)		225 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs, duty cycle = 2%.

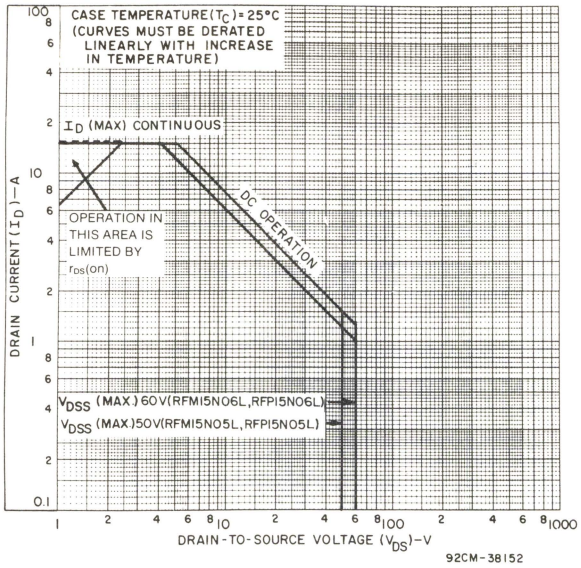


Fig. 1 - Maximum safe operating areas for all types.

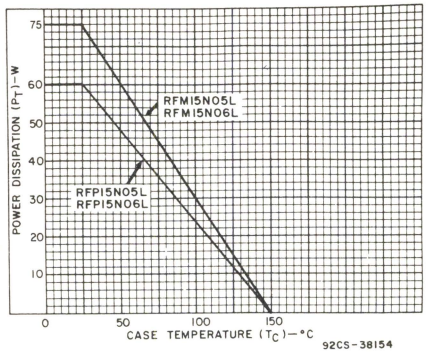


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

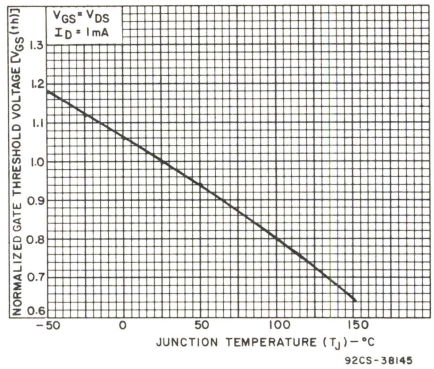


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

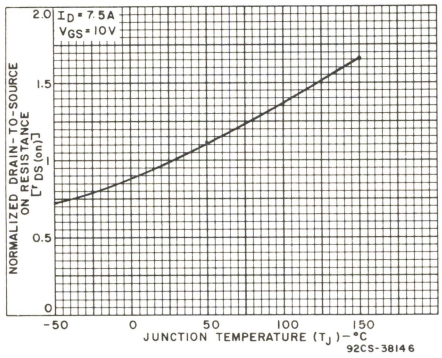


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

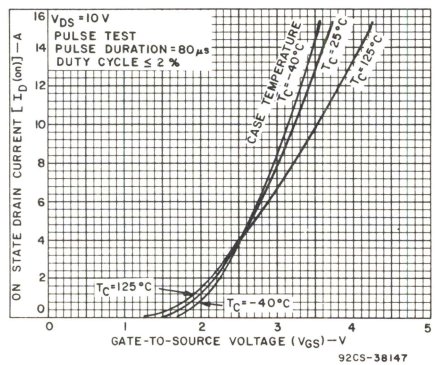


Fig. 5 - Typical transfer characteristics for all types.

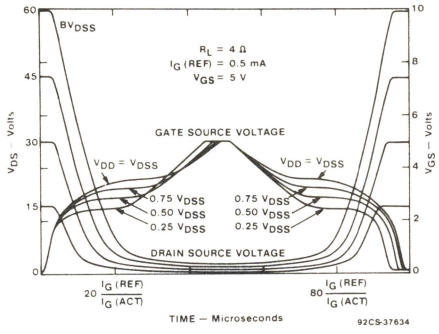


Fig. 6 – Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

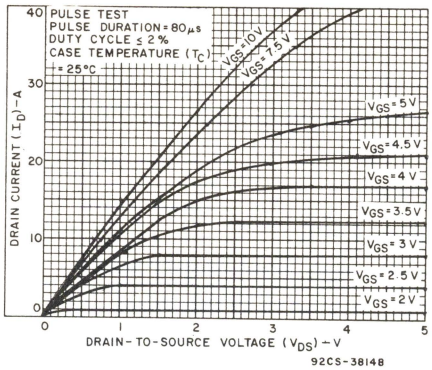


Fig. 7 - Typical saturation characteristics for all types.

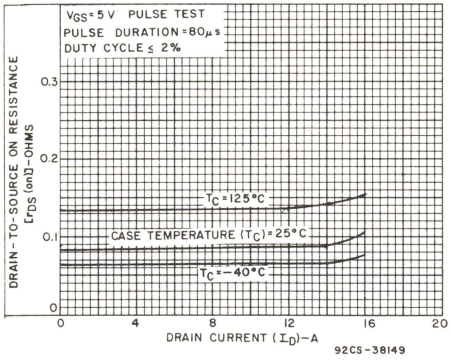


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

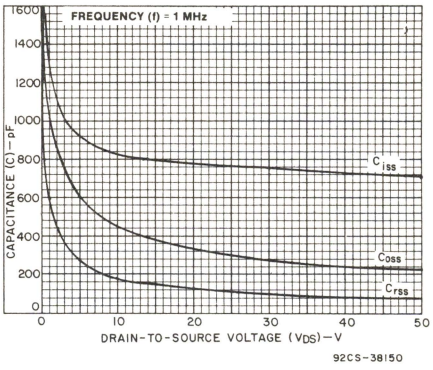


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

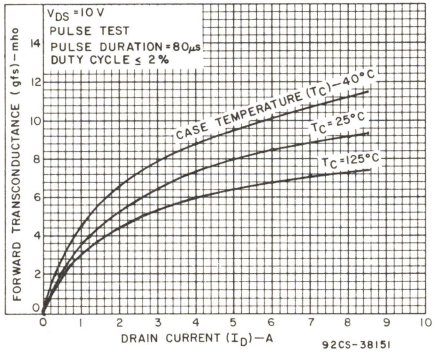


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

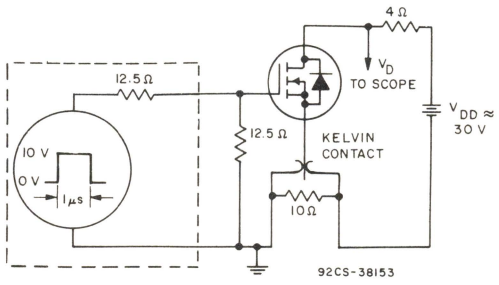


Fig. 11 - Switching Time Test Circuit.

HARRIS SEMICONDUCTOR

RFD16N05L
RFD16N05LSM

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

June 1992

Features

- 16A, 50V
- $r_{DS}(ON) = 0.047\Omega$
- UIS SOA Rating Curves (Single Pulse)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Operating Temperature +150°C

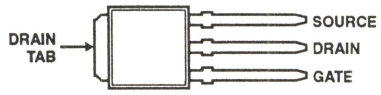
Description

The RFD16N05L and RFD16N05LSM N-channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFD16N05L and RFD16N05LSM were designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

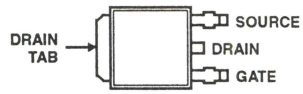
The RFD16N05L is supplied in the JEDEC TO-251 plastic package and the RFD16N05LSM in the JEDEC TO-252 plastic package.

Package

TO-251AA
TOP VIEW

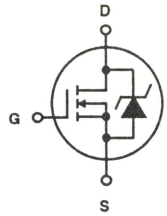


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	45	A
Single Pulse Avalance Rating		Refer to UIS SOA Curve	
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60	W
Above T_C = +25°C, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2269.1**

Electrical Characteristics At Case Temperature (Tc) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 2.05mA, V_{GS} = 0V		50	-	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 2.05mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V T_C = 150°C		-	1 50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GC} = ±10V, V_{DS} = 0V		-	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 16A, V_{GS} = 5V I_D = 16A, V_{GS} = 4V		- -	0.047 0.056	W
Turn-On Time	t(on)	V_{DD} = 25V, I_D = 8A, I_{G1} = I_{G2} = 0.4A, V_{GS} (clamp) + 5V, -0.6V, R_L = 3.125Ω		-	60	ns
Turn-On Delay Time	$t_d(on)$			-	14(typ)	ns
Rise Time	t_r			-	30 (typ)	ns
Turn-Off Delay Time	$t_d(off)$			-	42 (typ)	ns
Fall Time	t_f			-	14 (typ)	ns
Turn-Off Time	t(off)			-	100	ns
Total Gate Charge	Q_g(total)	V_{GS} = 0-10V	V_{DD} = 40V I_D = 16A R_L = 2.5Ω	-	80	nC
Gate Charge at 5V	Qg(5)	V_{GS} = 0-5V		-	45	nC
Threshold Gate Charge	Qg(th)	V_{GS} = 0-1V		-	3	nC
Plateau Voltage	V(plateau)	I_D = 16A, V_{DS} = 15V		-	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 8A, R_L = 3.125Ω, L = 0.2µH, I_{g1} = I_{g2} = 0.8A, V_{GS}(clamp) +5V, -0.6V		-	19	µJ
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$			-	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R\theta_{JA}$			-	100	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16A	-	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16A, dI_F/d_t = 100A/µs	-	125	ns

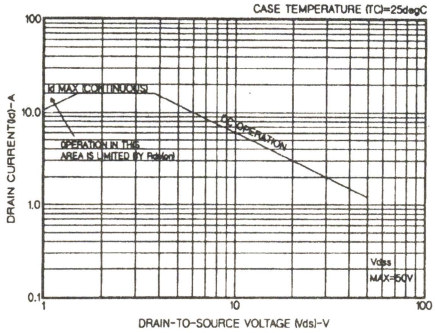


FIGURE 1. SAFE OPERATING AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN TEMP.)

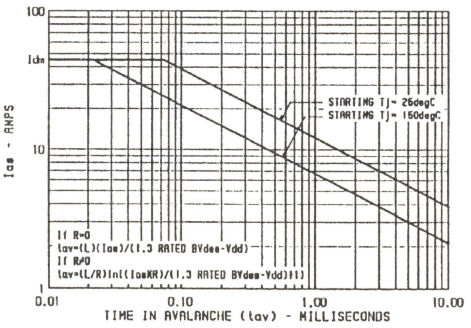


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING SOA. (SINGLE PULSE UIS SOA

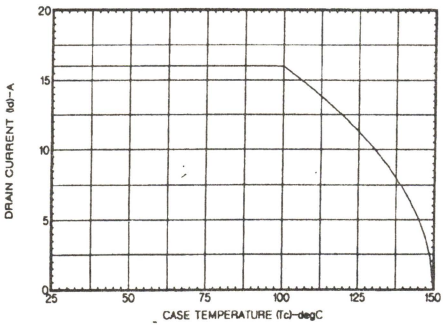


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

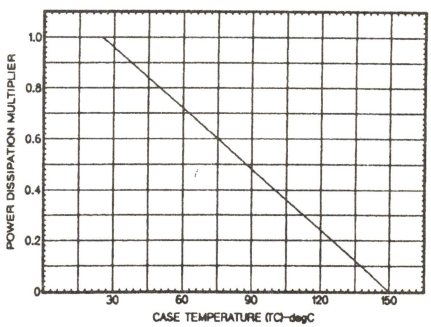


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

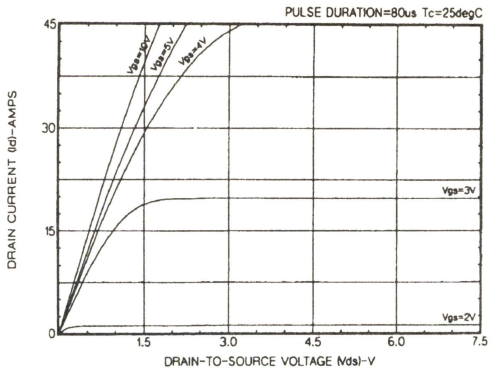


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

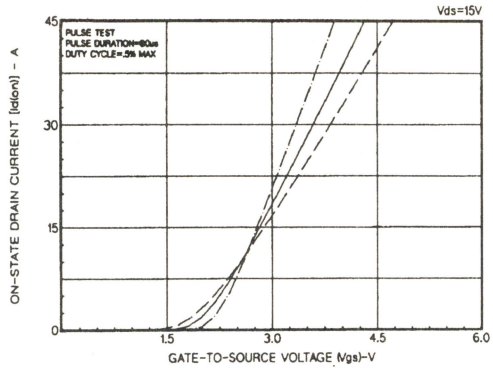


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

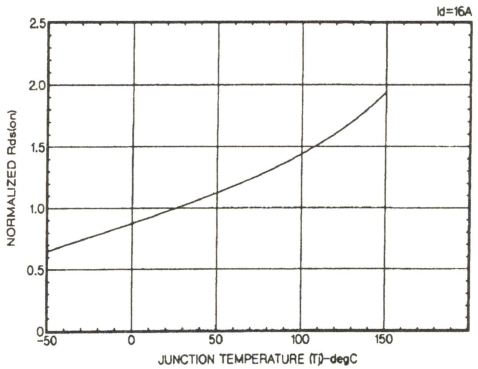


FIGURE 7. NORMALIZED $r_{DS}(on)$ vs JUNCTION TEMPERATURE

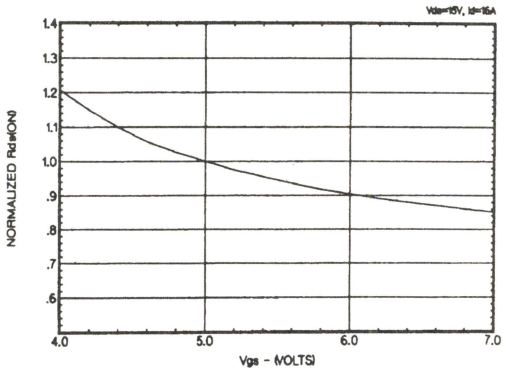


FIGURE 8. NORMALIZED $r_{DS}(on)$ vs V_{GS}

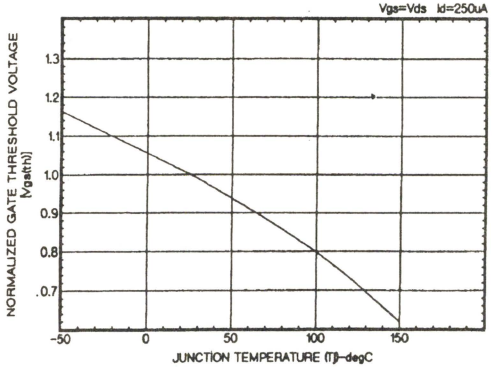


FIGURE 9. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE

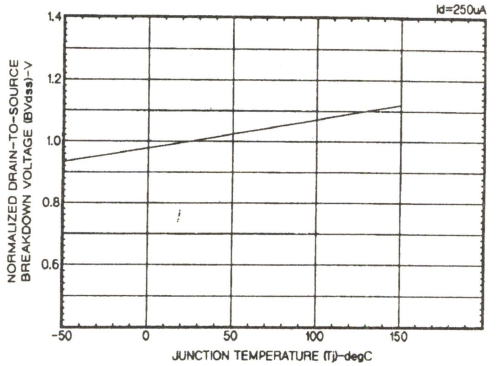


FIGURE 10. DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

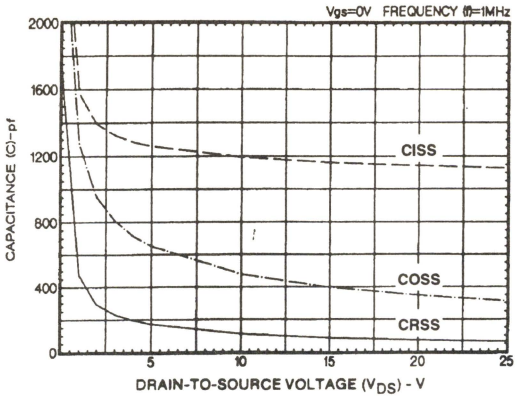


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

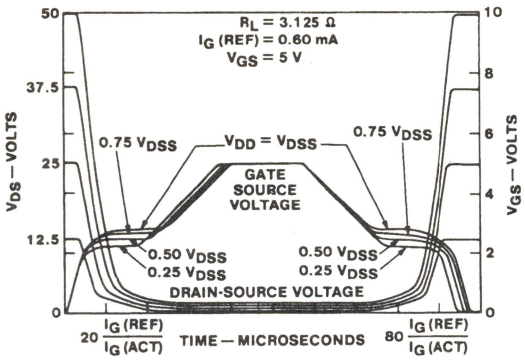


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260.

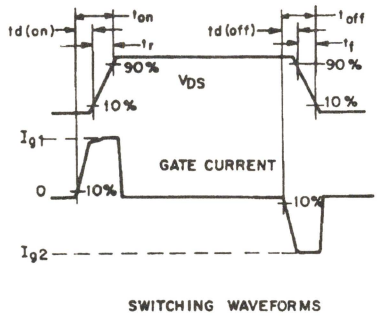


FIGURE 13. RESISTIVE SWITCHING

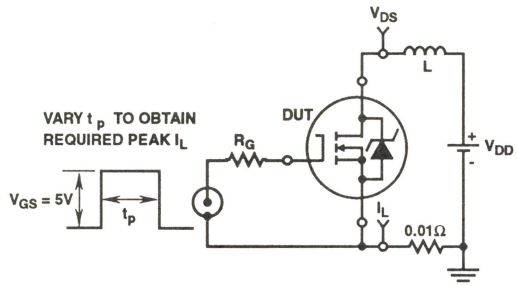


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

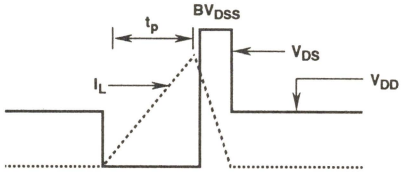


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

Spice Model (RFD16N05L)

```
.SUBCKT RFD16N05L  2  1  3;  rev 04/08/92
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=2.054  KP=24.73  IS=1e-30  N=10  TOX=1  L=1u  W=1u)
Vto  21  6  0.448
Rsource  8  7  RDSMOD  0.614E-3
Rdrain  5  16  RDSMOD  27.38E-3
.MODEL RDSMOD RES (TC1=3.66E-3  TC2=1.46E-5)
.MODEL RVTOMOD RES (TC1=-1.81E3  TC2=1.41E-6)
Ebreak 11  7  17  18  70.9
.MODEL RBKMOD RES (TC1=1.01E-3  TC2=5.21E-8)
.MODEL DBKMOD D (RS=8.82E-2  TRS1=-2.01E-3  TRS2=7.32E-10)
.MODEL DBDMOD D (IS=1.34E-13  RS=1.21E-2  TRS1=1.64E-3  TRS2=2.59E-6  +CJO=1.13E-9  TT=4.14E-8)
Cin  6  8  1.21E-9
Ca  12  8  3.33E-9
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-4.25  VOFF=-2.25)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=-4.25)
.MODEL DPLCAPMOD D (CJO=5.22E-10  IS=1e-30  N=10)
Cb  15  14  3.11E-9
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-0.65  VOFF=4.35)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=4.35  VOFF=-0.65)
Rgate  9  20  2.98
Lgate  1  9  1.38E-9
Ldrain  2  5  1.0E-12
Lsource  3  7  1.0E-9
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
MOS1  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS
```

HARRIS SEMICONDUCTOR

RFD16N06LE
RFD16N06LESM

16A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

March 1994

Features

- 16A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- 2KV ESD Protected
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFD16N06LE and RFD16N06LESM N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

The RFD16N06LE is supplied in the JEDEC TO-251AA plastic package and the RFD16N06LESM is supplied in the JEDEC TO-252AA plastic package. Due to space limitations the RFD16N06LE and the RFD16N06LESM are branded 16N06L.

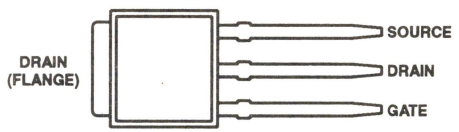
The RFD16N06LE and RFD16N06LESM incorporates ESD protection and is designed to withstand 2KV (Human Body Model) of ESD.

When ordering use the entire part number; eg. RFD16N06-LESM.

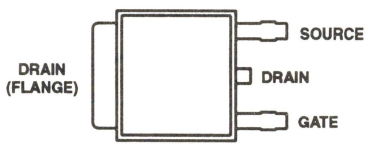
Formerly developmental type TA49027.

Packaging

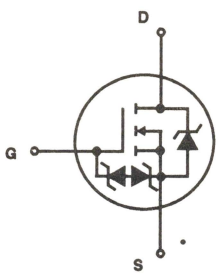
JEDEC TO-251AA
TOP VIEW



JEDEC TO-252AA
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RFD16N06LE, RFD16N06LESM	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	+10, -8	V
Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
(T_C = +25°C)	P_D	90	W
Derate above +25°C	P_T	0.606	W/°C
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	KV
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3628**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10, -8V		-	-	10	µA
On Resistance	$r_{DS(ON)}$	I_D = 16A, V_{GS} = 5V		-	-	0.047	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 16A, R_L = 1.88Ω, V_{GS} = 5V, R_{GS} = 5Ω		-	-	100	ns
Turn-On Delay Time	$t_{D(ON)}$			-	11	-	ns
Rise Time	t_R			-	60	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	48	-	ns
Fall Time	t_F			-	35	-	ns
Turn-Off Time	t_{OFF}			-	-	115	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 48V, I_D = 16A, R_L = 3Ω	-	51	62	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	29	35	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	1.8	2.6	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 16A, V_{DS} = 15V		-	-	3.5	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	1350	-	pF
Output Capacitance	C_{OSS}			-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	90	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.65	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 16A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} =16A, dI_{SD}/dt = 100A/µs	-	-	125	ns

Typical Performance Curves

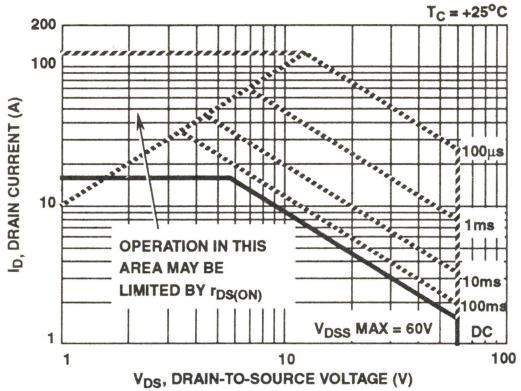


FIGURE 1. SAFE OPERATING AREA CURVE

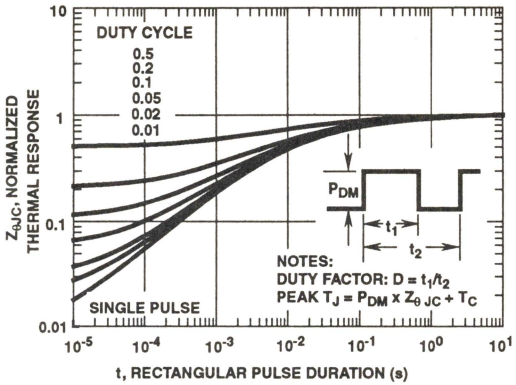


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

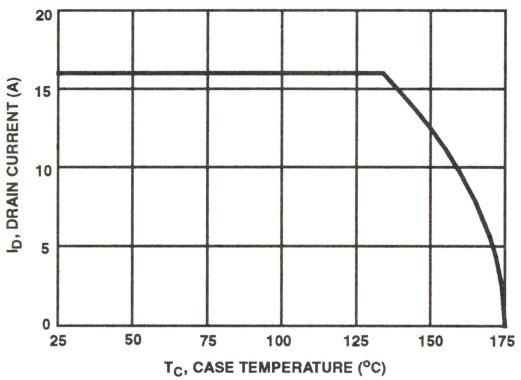


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

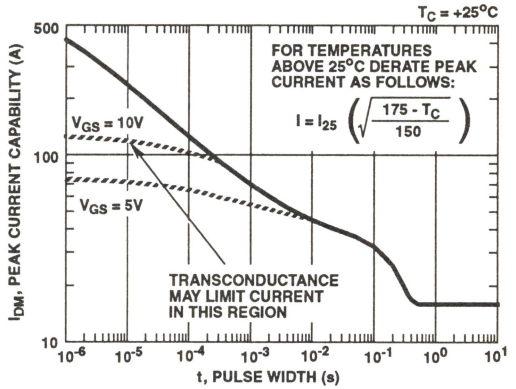


FIGURE 4. PEAK CURRENT CAPABILITY

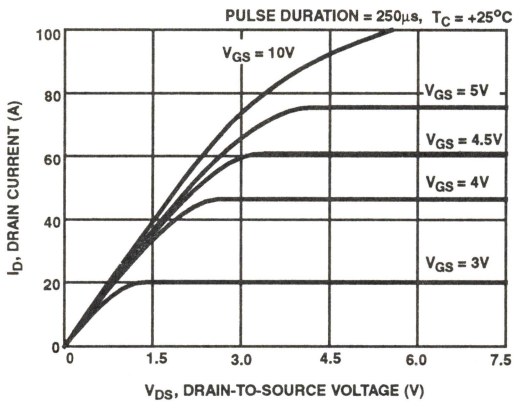


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

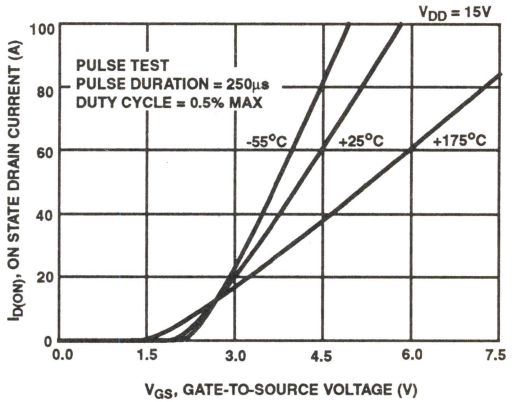


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

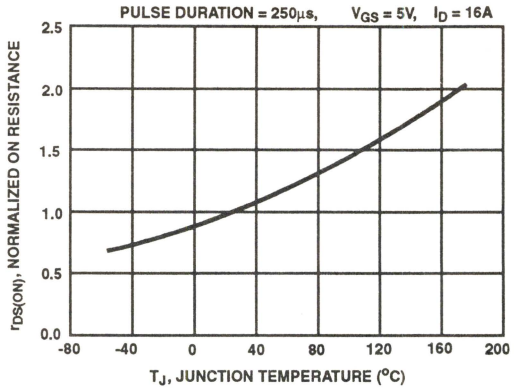


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

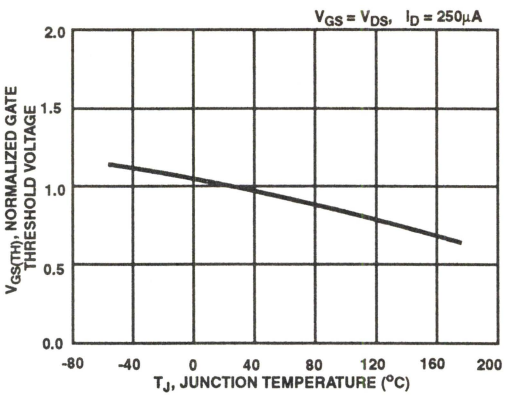


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

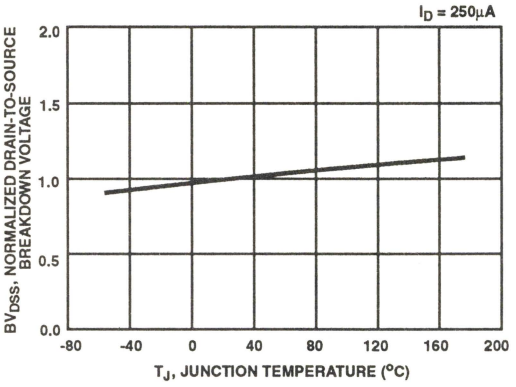


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

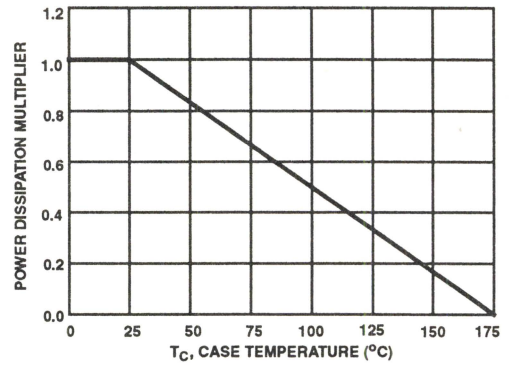


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

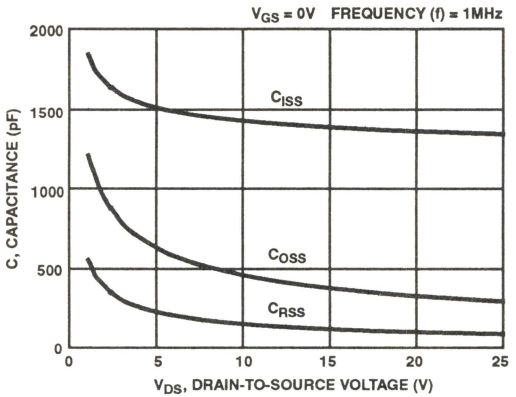


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

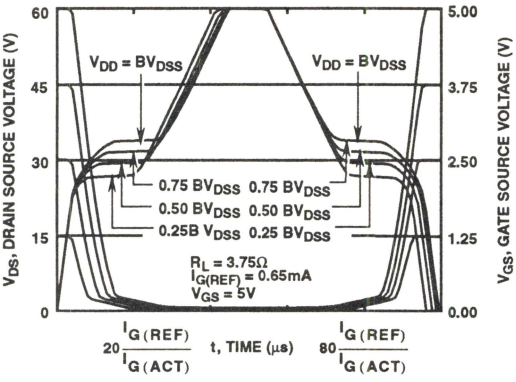


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

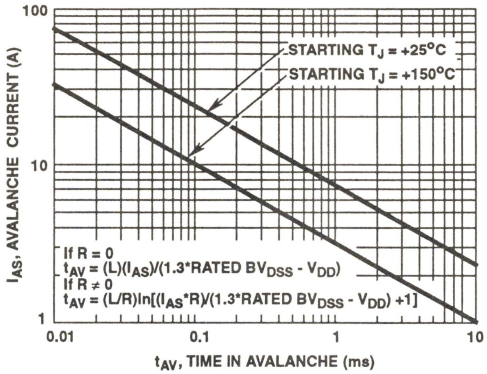


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

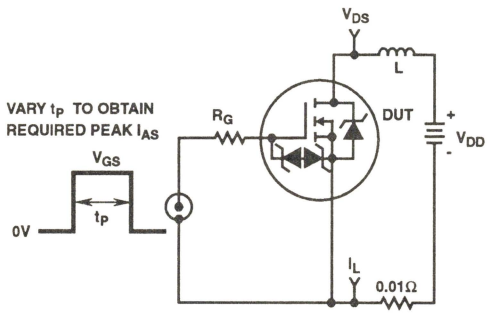


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

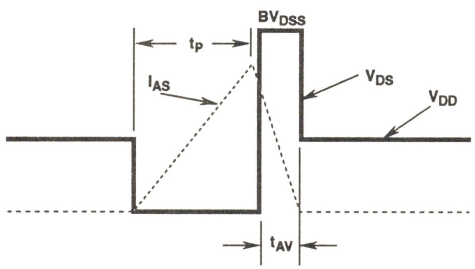


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

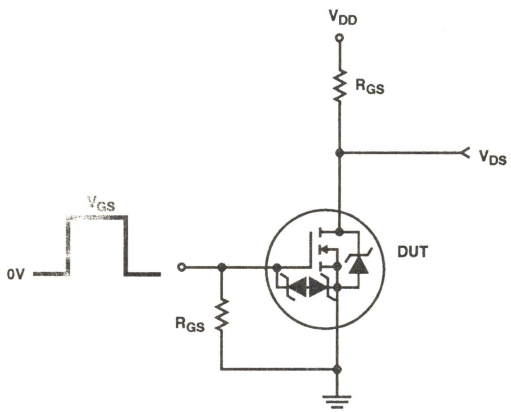


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

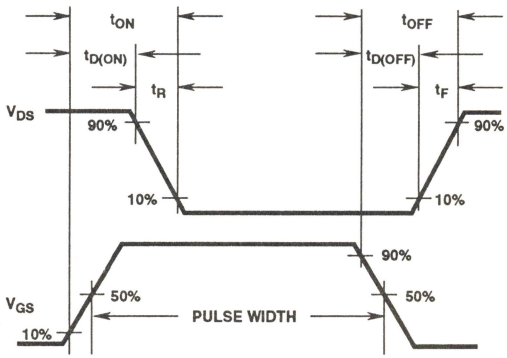


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD16N06LE, RFD16N06LESM

SUBCKT RFD16N06LE 2 1 3 ; rev 8/2/93

CA 12 8 3.364e-9
CB 15 14 3.41e-9
CIN 6 8 0 1.317e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 75.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

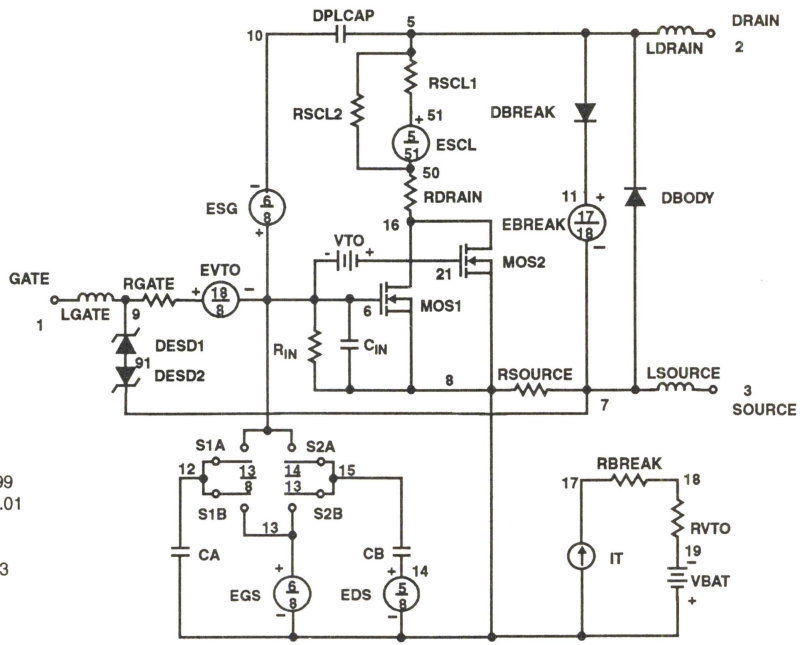
LDRAIN 2 5 1e-9
LGATE 1 9 4.9e-9
LSOURCE 3 7 4.9e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 11.86e-3
RGATE 9 20 2.52
RIN 6 8 1e9
RSCL1 5 51 RSLVCMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 26e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.49



.MODEL DBDMOD D (IS = 3.80e-13 RS = 1.12e-2 TRS1 = 1.61e-3 TRS2 = 6.08e-6 CJO = 1.05e-9 TT = 3.84e-8)
.MODEL DBKMOD D (RS = 1.44e-1 TRS1 = 6.59e-3 TRS2 = 9.71e-6)
.MODEL DESD1MOD D (BV = 13.5 TBV1 = 0 TBV2 = 0 RS = 48 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 10.24 TBV1 = -8.6756e-4 TBV2 = 7.425e-7 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 5.59e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.89 KP = 113 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.12e-3 TC2 = -9.59e-7)
.MODEL RDSMOD RES (TC1 = 4.98e-3 TC2 = 1.34e-5)
.MODEL RSLVCMOD RES (TC1 = 1.75e-3 TC2 = 3.75e-6)
.MODEL RVTOMOD RES (TC1 = -1.86e-3 TC2 = -3.63e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.85 VOFF= -1.85)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.85 VOFF= -3.85)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.34 VOFF= 2.76)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.76 VOFF= -2.34)

.ENDS

NOTE:

1. For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.

HARRIS

RFP17N06L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 17A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

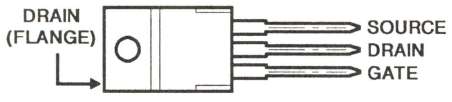
Description

The RFP17N06L is an N-Channel enhancement mode silicon-gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high power bipolar transistors requiring high speed and low gate drive power. This type can be operated directly from integrated circuits. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP17N06L is supplied in the JEDEC TO-220AB plastic package.

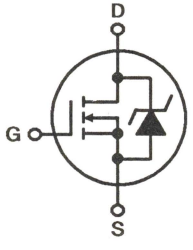
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	17	A
Pulsed Drain Current	I_{DM}	50	A
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
$T_C = +25^oC$	P_D	60	W
Above $T_C = +25^oC$, Derate Linearly		0.48	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	^{o}C

6 LOGIC LEVEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2272.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1.0 mA, V_{GS} = 0 V	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 1.0 mA	1	2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0 V	—	1	μA
		T_C = 150°C		50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V	—	100	nA
On Resistance	$R_{DS}(on)$	I_D = 8.5 A, V_{GS} = 4.0 V	—	0.150	Ω
		I_D = 8.5 A, V_{GS} = 5.0 V	—	0.100	
		I_D = 17.0 A, V_{GS} = 5.0 V	—	0.130	
Forward Transconductance	g_{FS}	I_D = 8.5 A, V_{DS} = 5.0 V	6.0	—	S
Turn-On Delay Time	$T_d(on)$	V_{DD} = 30 V, I_D = 8.5 A	—	40	ns
Rise Time	T_R	R_{GEN} = 12.5 ohms	—	150	
Turn-Off Delay Time	$T_d(off)$	R_{GS} = 12.5 ohms	—	240	
Fall Time	T_F	V_{GS} = +5 V	—	110	
Total Gate Charge	$Q_g(total)$	I_D = 8.5 A, V_{DD} = 30 V	—	45	nC
		V_{GS} = 10 V, R_L = 3.5 ohms			
Gate Charge at 5 volts	$Q_g(5)$	V_{GS} = 5 V	—	25	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 1 V	—	2.0	
Thermal Resistance Junction to Case	$R_{\theta JC}$		—	2.083	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Forward Voltage	V_{SD}	I_{SD} = 17 A	—	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 17 A, dI_F/d_t = 100 A/μs	115 (typ)		ns

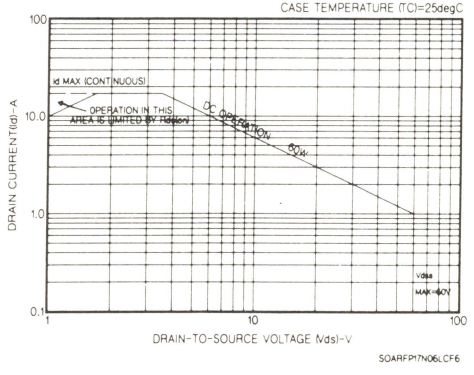


Fig. 1 - Maximum safe operating areas for all types.

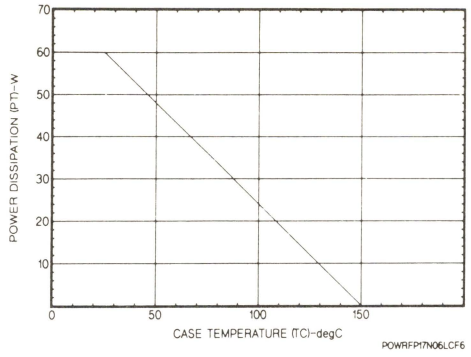


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

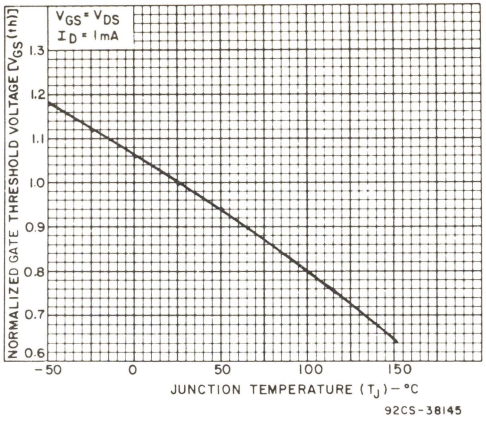


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

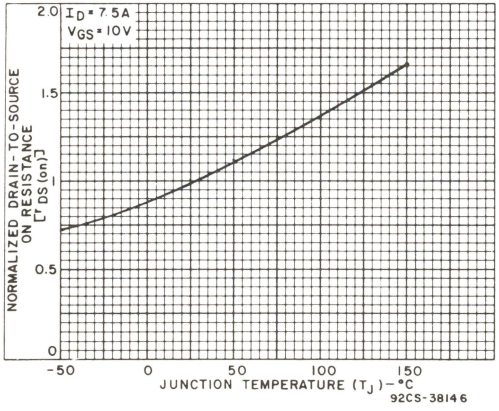


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

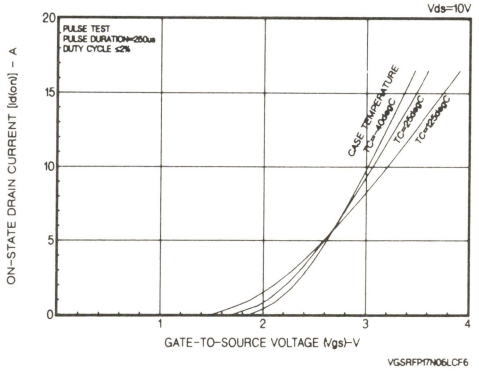


Fig. 5 - Typical transfer characteristics for all types.

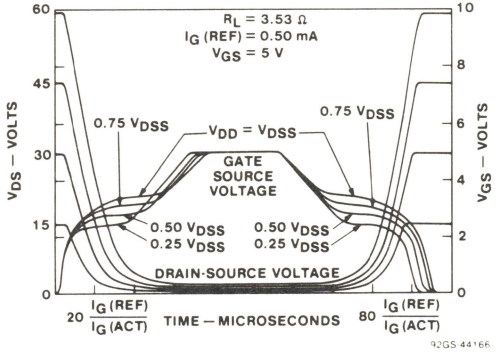


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

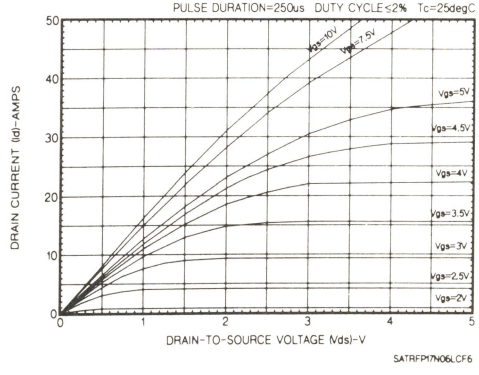


Fig. 7 - Typical saturation characteristics for all types.

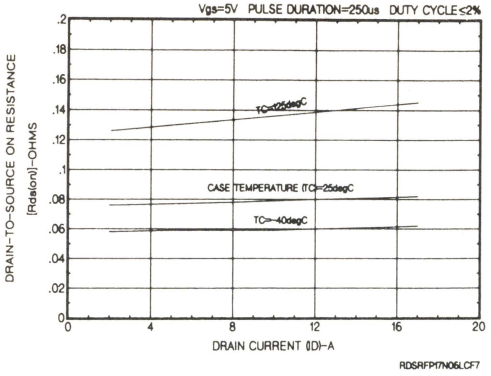


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

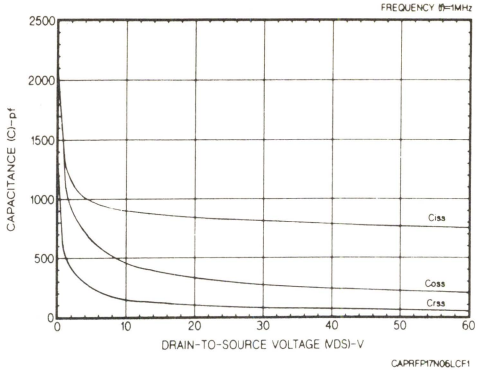


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

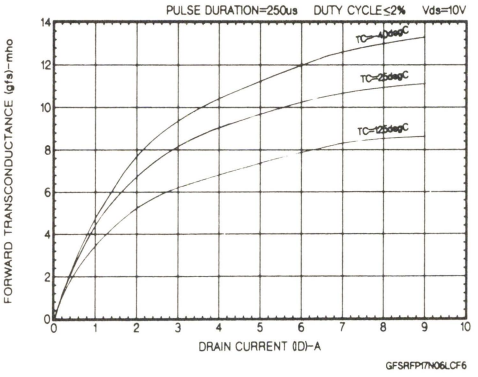


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

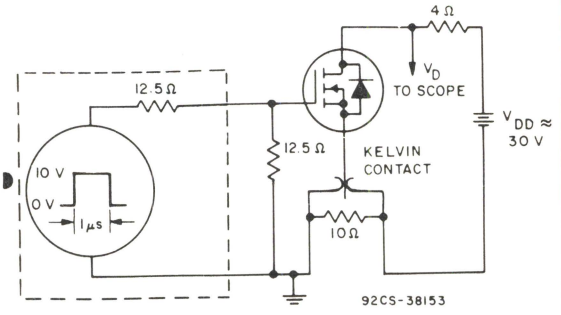


Fig. 11 - Switching Time Test Circuit.

HARRIS

RFP25N05L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor (MegaFETs)

June 1992

Features

- 25A, 50V
- $r_{DS(ON)} = 0.047\Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Operating Temperature ..... +150°C

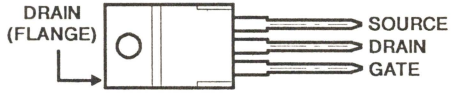
Description

The RFP25N05L is an N-Channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. The RFP25N05L was designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP25N05L is supplied in the JEDEC TO-220AB plastic package.

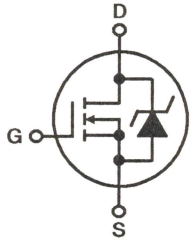
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	25	A
Pulsed Drain Current	I_{DM}	65	A
Single Pulse Avalanche Energy Rating		Refer to UIS SOA Curve*	
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	60	W
Above T_C = +25°C, Derate Linearly		0.48	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

* See Figures 13, 14 and 15

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2270.1

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150° C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 25 A, V_{GS} = 5 V I_D = 25 A, V_{GS} = 4 V		—	0.047 0.056	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 12.5 A I_{g1} = I_{g2} = 1 A V_{GS} (clamp) + 5 V, −0.6 V R_L = 2 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	15 (typ.)	
Rise Time	t_r			—	35 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	40 (typ.)	
Fall Time	t_f			—	14 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	Q_g(total)	V_{GS} = 0-10 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 5 V	$Q_g(5)$	V_{GS} = 0-5 V	I_D = 25 A	—	45	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-1 V	R_L = 1.6 Ω	—	3	
Plateau Voltage	V(plateau)	I_D = 25 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 12.5 A, R_L = 2 Ω L = 0.2 μH, I_{g1} = I_{g2} = 1 A V_{GS} (clamp) + 5 V, −0.6 V		—	30	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			—	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 25 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 25 A, dI_F/d_t = 100 A/μs	—	125	ns

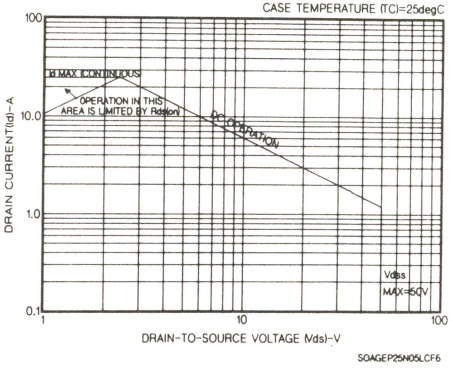


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

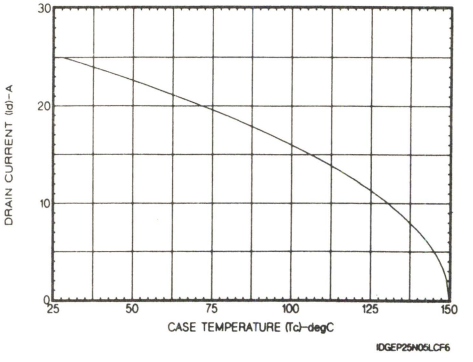


Fig. 2 - Maximum continuous drain current vs. temperature.

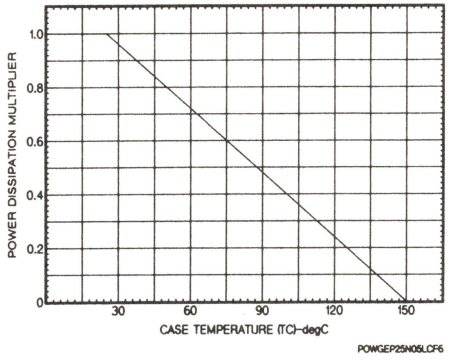


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

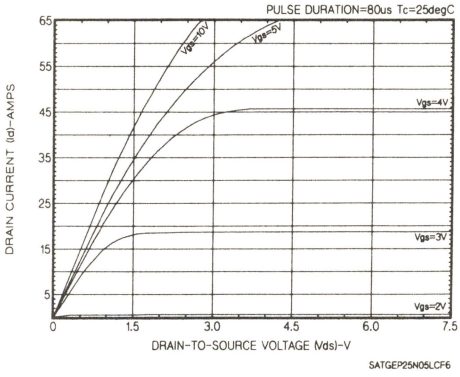


Fig. 4 - Typical saturation characteristics.

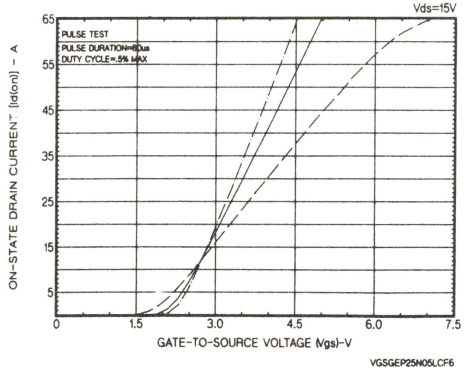


Fig. 5 - Typical transfer characteristics.

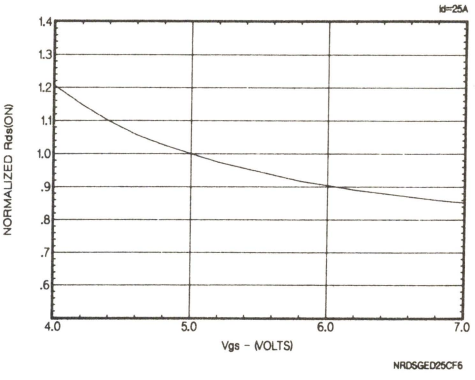


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

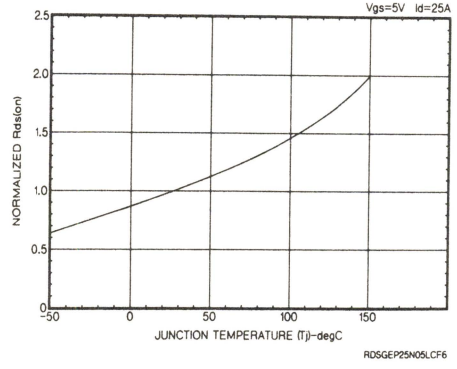


Fig. 7 - Normalized $r_{ds}(on)$ vs. junction temperature.

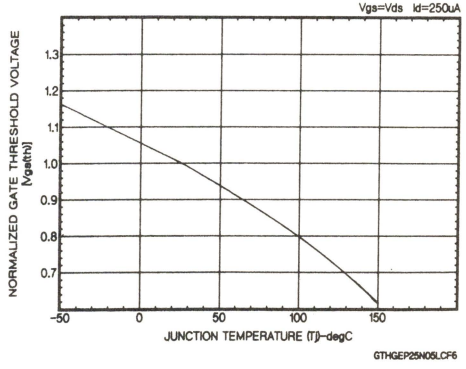


Fig. 8 - Typical normalized gate threshold voltage.

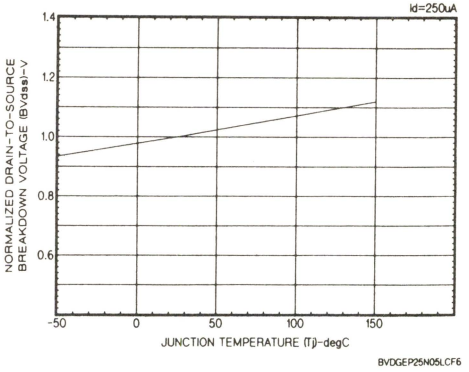


Fig. 9 - Drain source breakdown voltage vs. temperature.

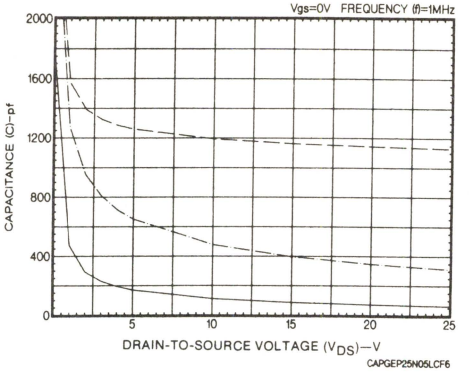


Fig. 10 - Typical capacitance vs. voltage

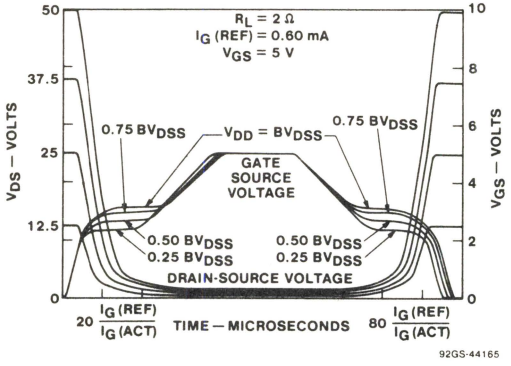


Fig. 11 - Normalized switching waveforms for constant gate-current (Refer to Harris application notes AN-7254 and AN-7260)

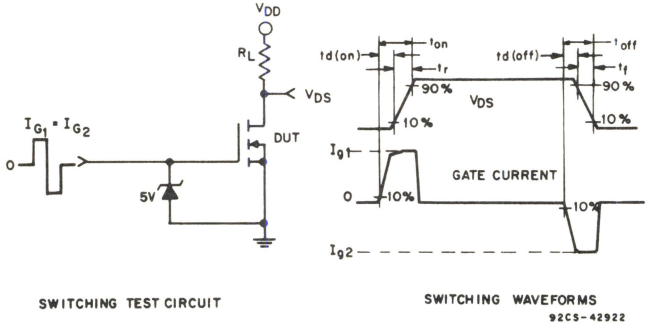


Fig. 12 - Resistive switching.

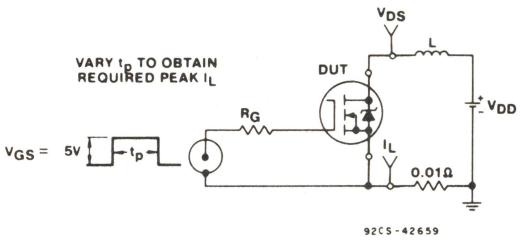


Fig. 13 - Unclamped energy test circuit.

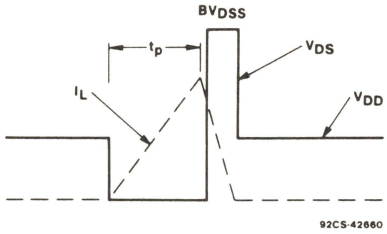


Fig. 14 - Unclamped energy waveforms.

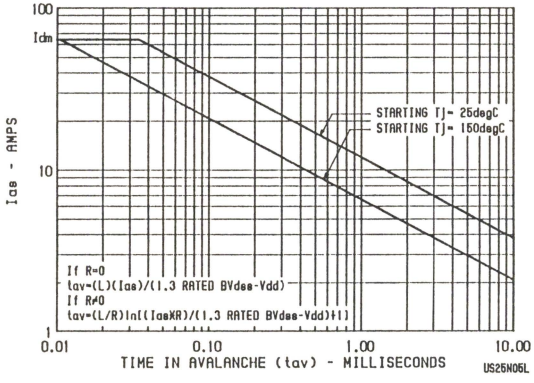


Fig. 15 – Unclamped-Inductive-Switching SOA
(Single Pulse UIS SOA)

HARRIS

RFP25N06L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistor (L^2FET)

August 1991

Features

- 25A, 60V
- $r_{DS(ON)} = 0.085\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

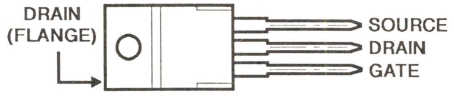
The RFP25N06L is an N-Channel enhancement-mode silicon-gate power field-effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFP25N06L is supplied in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP25N06L is F25N06L.

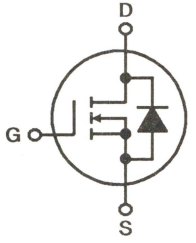
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$) Unless Otherwise Specified

			UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	60	V
Continuous Drain Current			
RMS Continuous	I_D	25	A
RMS Continuous @ $T_C = +85^oC$		18	A
Pulsed Drain Current	I_{DM}	60	A
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
$T_C = +25^oC$	P_D	75	W
Above $T_C = +25^oC$ Derate Linearly		0.6	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2044.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTICS		TEST CONDITIONS	LIMITS RFP25N06L MIN.	LIMITS RFP25N06L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$	60	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 1$ mA	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40$ V	—	—	μA
		$V_{DS} = 50$ V	—	1	
		$T_c = 125$ °C, $V_{DS} = 40$ V	—	—	
		$T_c = 125$ °C, $V_{DS} = 50$ V	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = 10$ V, $V_{DS} = 0$	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 5$ V	—	1.06	V
		$I_D = 25$ A, $V_{GS} = 5$ V	—	2.5	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 12.5$ A, $V_{GS} = 5$ V	—	0.085	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 5$ V, $I_D = 12.5$ A	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1 MHz	—	2000	pF
Output Capacitance	C_{oss}		—	900	
Reverse Transfer Capacitance	C_{rss}		—	400	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 30$ V, $I_D = 12.5$ A, $R_{gen} = \infty$, $R_{gs} = 6.25$ Ω, $V_{GS} = 5$ V	18 (typ.)	60	ns
Rise Time	t_r		120 (typ.)	225	
Turn-Off Delay Time	$t_{d(off)}$		123 (typ.)	225	
Fall Time	t_f		123 (typ.)	200	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFP25N06L	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

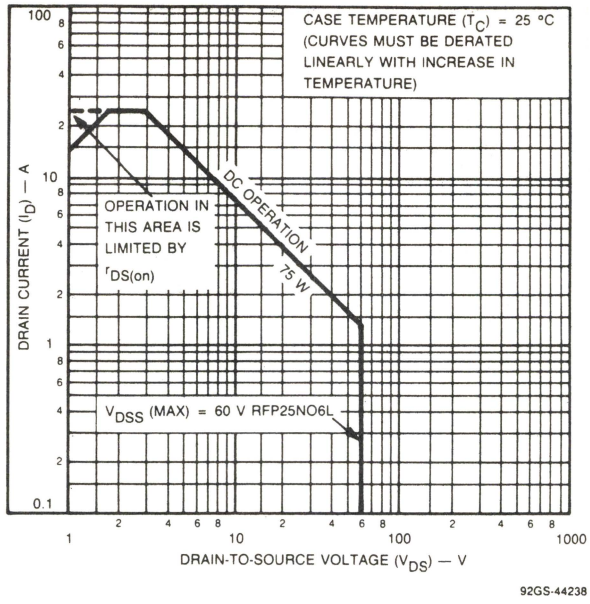


Fig. 1 - Maximum operating areas for all types.

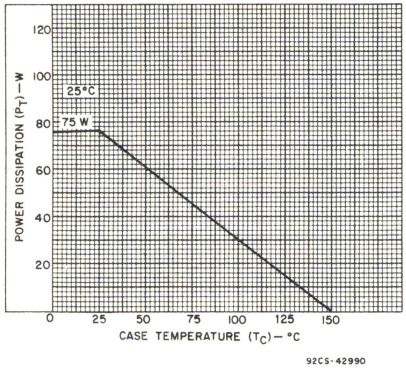


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

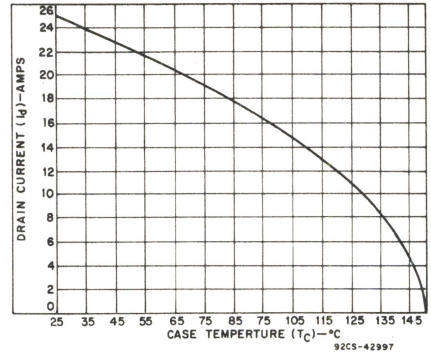


Fig. 3 - Maximum continuous drain current vs. case temperature.

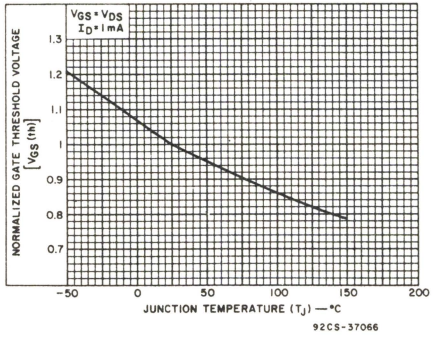


Fig. 4 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

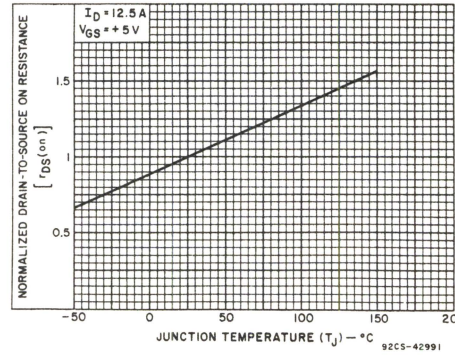


Fig. 5 - Normalized drain-to-source on resistance to junction temperature for all types.

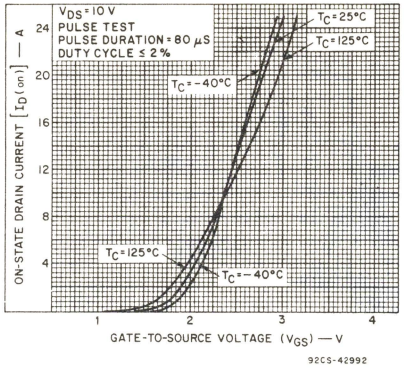


Fig. 6 - Typical transfer characteristics for all types.

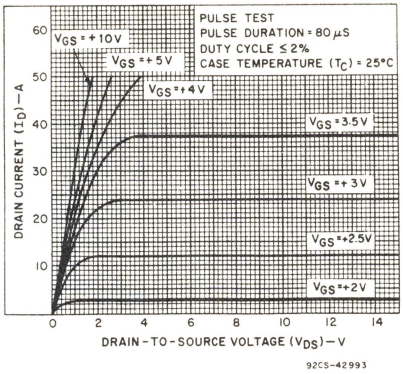


Fig. 7 - Typical output characteristics for all types.

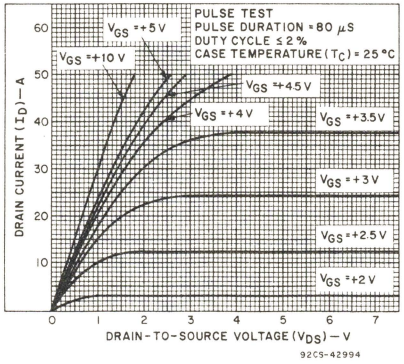


Fig. 8 - Typical saturation characteristics for all types.

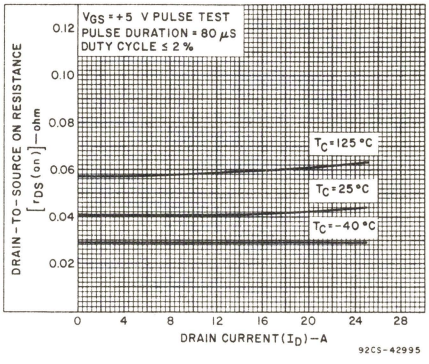


Fig. 9 - Typical drain-to-source on resistance as a function of drain current for all types.

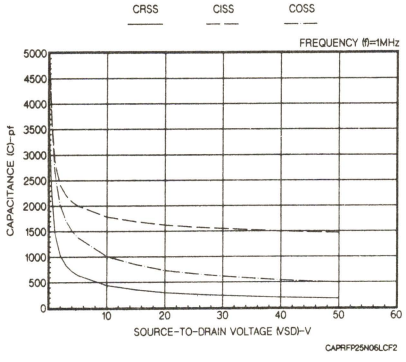


Fig. 10 - Typical capacitance vs. voltage.

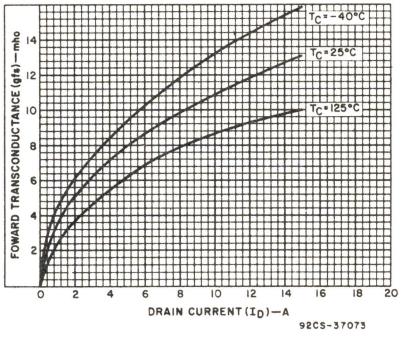


Fig. 11 - Typical forward transconductance as a function of drain current for all types.

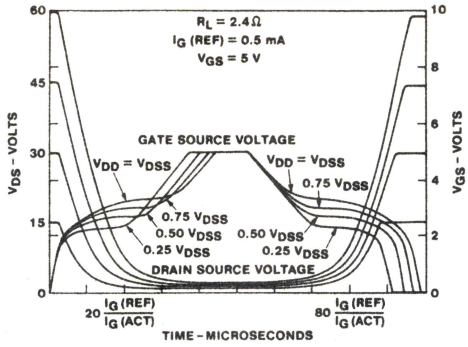


Fig. 12 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

HARRIS SEMICONDUCTOR

RFP30N06LE

30A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFET (MegaFET)

January 1994

Features

- 30A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- 2KV ESD Protected
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFP30N06LE N-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

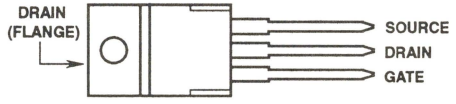
The RFP30N06LE incorporates ESD protection and is designed to withstand 2KV (Human Body Model) of ESD.

The RFP30N06LE is supplied in the JEDEC TO-220AB plastic package. Due to space limitations the RFP30N06LE is branded P30N06LE.

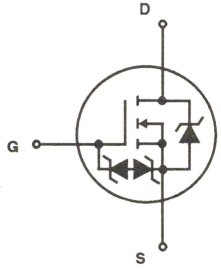
When ordering use the entire part number; RFP30N06LE. Formerly developmental type TA49027.

Package

TO-220AB
TOP VIEW



Symbol



6 LOGIC LEVEL POWER MOSFETs

Absolute Maximum Ratings (T_C = +25°C)

		RFP30N06LE	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	+10, -8	V
Drain Current			
RMS Continuous	I_D	30	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
(T_C = +25°C)	P_D	96	W
Derate above +25°C	P_T	0.645	W/°C
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	KV
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3629

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10, -8V		-	-	10	µA
On Resistance	$r_{DS(ON)}$	I_D = 30A, V_{GS} = 5V		-	-	0.047	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 30A, R_L = 1Ω, V_{GS} = 5V, R_{GS} = 2.5Ω		-	-	140	ns
Turn-On Delay Time	$t_{D(ON)}$			-	11	-	ns
Rise Time	t_R			-	88	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	30	-	ns
Fall Time	t_F			-	40	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 48V, I_D = 30A, R_L = 1.6Ω	-	51	62	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	28	34	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	1.8	2.6	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 30A, V_{DS} = 15V		-	-	4.0	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	1350	-	pF
Output Capacitance	C_{OSS}			-	290	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	85	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.55	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 30A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 30A, dI_{SD}/dt = 100A/µs	-	-	125	ns

Typical Performance Curves

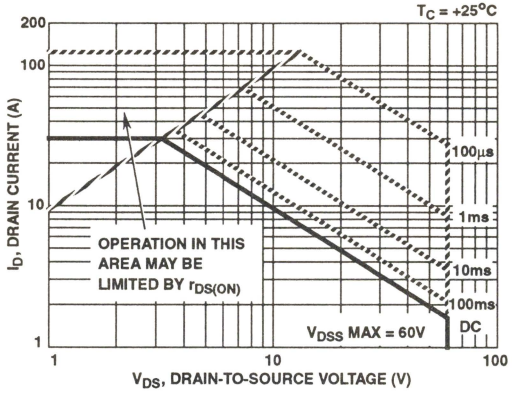


FIGURE 1. SAFE OPERATING AREA CURVE

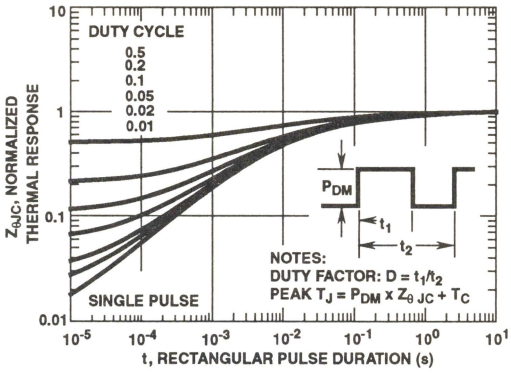


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

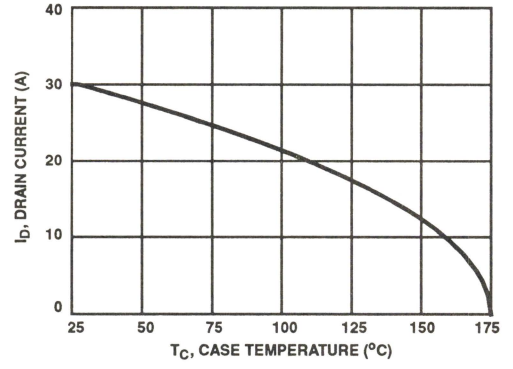


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

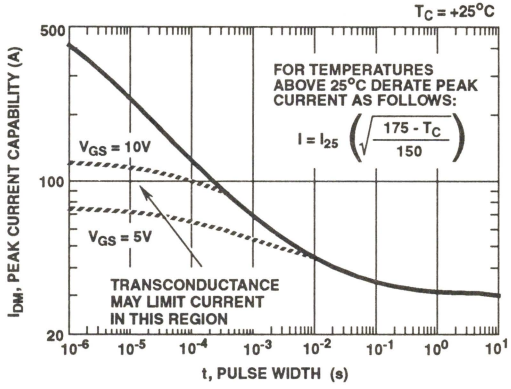


FIGURE 4. PEAK CURRENT CAPABILITY

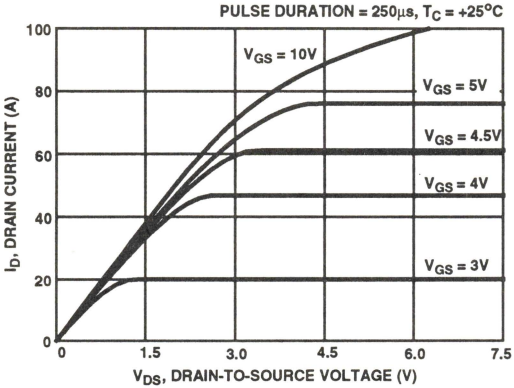


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

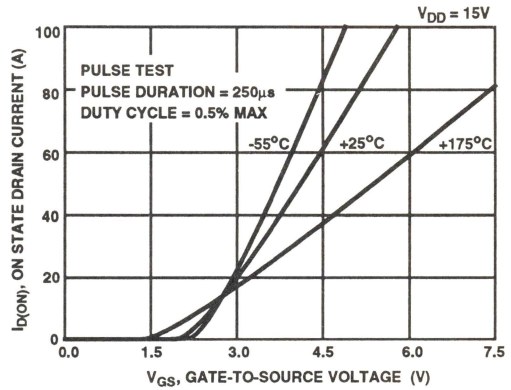


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

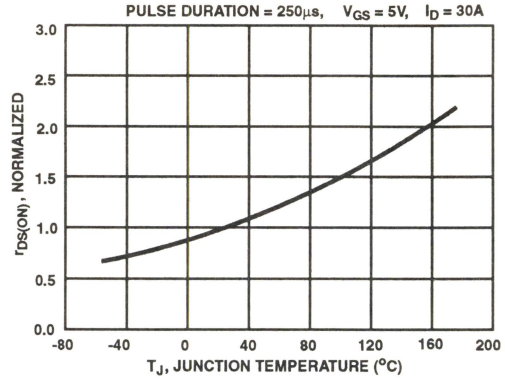


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE.

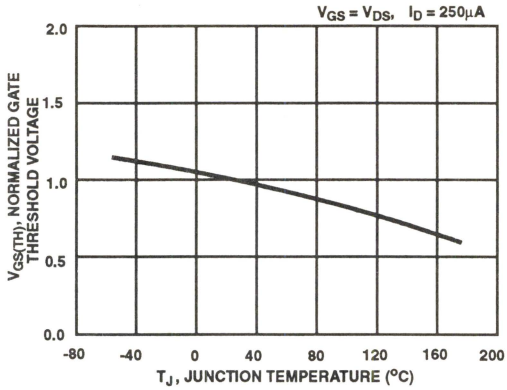


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE.

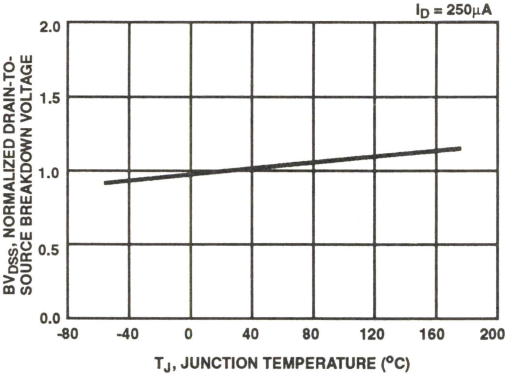


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

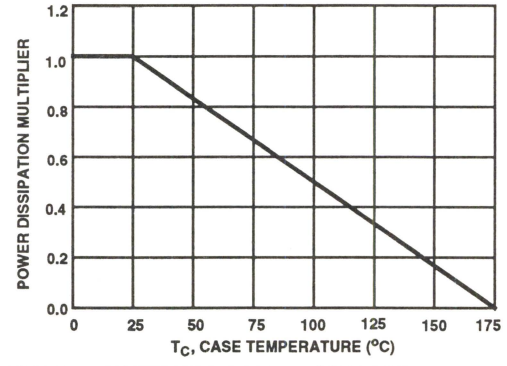


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

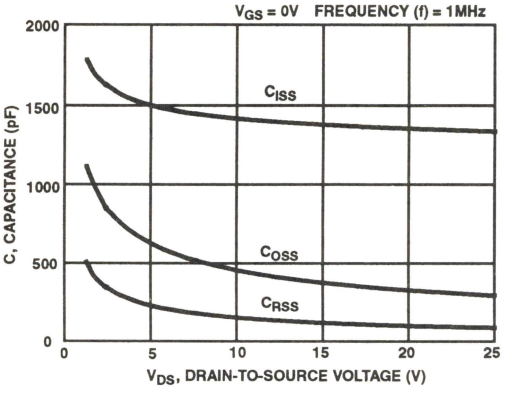


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

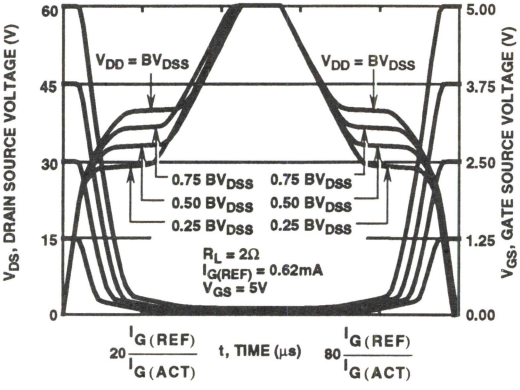


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

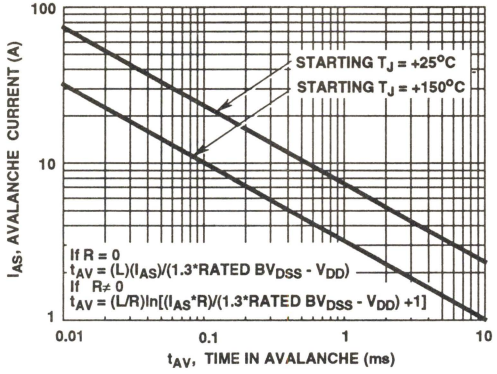


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

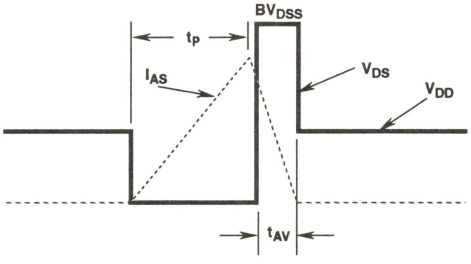


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

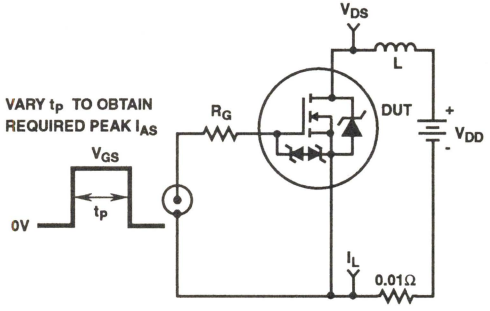


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

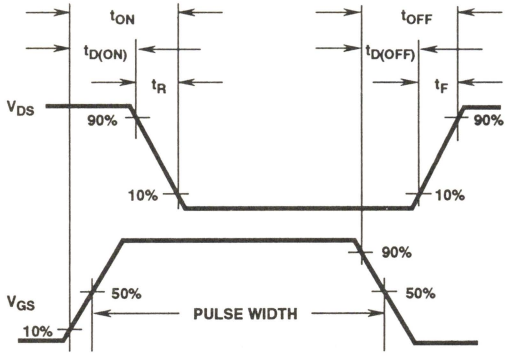


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

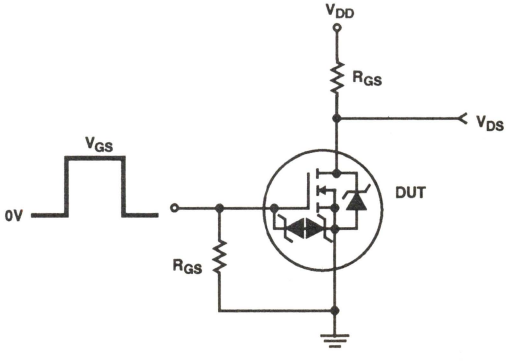


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

Temperature Compensated PSPICE Model for the RFP30N06LE

```
SUBCKT RFP30N06LE  2 1 3;      rev 6/2/93
CA 12 8 1 3.34e-9
CB 15 14 3.44e-9
CIN 6 8 0 1.343e-9

DBODY 7  5  DBDMOD
DBREAK 5 11  DBKMOD
DESD1 91 9  DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10  5  DPLCAPMOD

EBREAK 11 7  17 18  75.39
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN  2  5  1e-9
LGATE 1  9  7.22e-9
LSOURCE 3 7  6.31e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 11.86e-3
RGATE 9 20 2.52
RIN 6 8 1e9
RSCL1  5  51  RSLVCMOD 1e-6
RSCL2  5  50  1e3
RSOURCE 8 7 RDSMOD 26.6e-3
RVTO 18 19 RVTOMOD 1

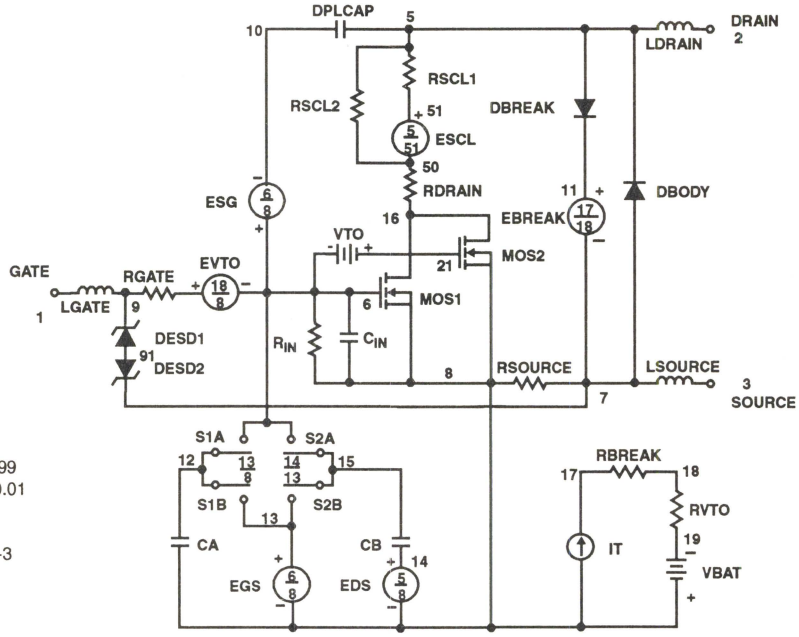
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6  0.5

ESCL  51 50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/89,7))

.MODEL DBDMOD D (IS = 3.80e-13  RS = 1.12e-2  TRS1 = 1.61e-3  TRS2 = 6.08e-6  CJO = 1.05e-9  TT = 3.84e-8)
.MODEL DBKMOD D (RS = 1.82e-1  TRS1 = 7.50e-3  TRS2 = -4.0e-5)
.MODEL DESD1MOD D (BV = 13.54  TBV1 = 0  TBV2 = 0  RS = 45.5  TRS1 = 0  TRS2 = 0)
.MODEL DESD2MOD D (BV = 11.46  TBV1 = -7.576e-4  TBV2 = -3.0e-6  RS = 0  TRS1 = 0  TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 0.591e-9  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 1.94  KP = 139.2  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3  TC2 = -3.03e-7)
.MODEL RDSMOD RES (TC1 = 5.38e-3  TC2 = 1.64e-5)
.MODEL RSLVCMOD RES (TC1 = 1.75e-3  TC2 = 3.90e-6)
.MODEL RVTOMOD RES (TC1 = -2.15e-3  TC2 = -5.43e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.05  VOFF = -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.5  VOFF = -4.05)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.2  VOFF = 2.8)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 2.8  VOFF = -2.2)

.ENDS
```



NOTE:

1. For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.

HARRIS

RFP50N05L
RFG50N05L

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

May 1992

Features

- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

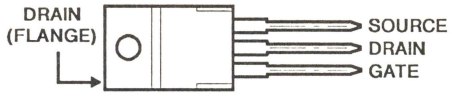
Description

The RFP50N05L and RFG50N05L N-channel logic-level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers, and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from integrated circuit supply voltages.

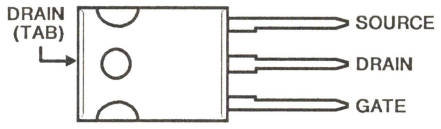
The RFP50N05L is supplied in the JEDEC TO-220AB plastic package and the RFG50N05L is supplied in the TO-247 plastic package.

Package

RFP50N05L
TO-220AB
TOP VIEW

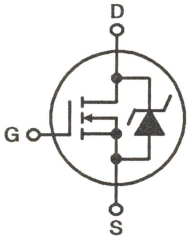


RFG50N05L
TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Maximum Ratings, Absolute-Maximum Values (T_C = +25°C)

			UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	50	V
Continuous Drain Current			
RMS Continuous	I_D	50	A
Pulsed Drain Current	I_{DM}	130	A
Single Pulse Avalance Rating, Refer to UIS SOA Curve			
Gate-Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation			
T_C = +25°C	P_D	110	W
Above T_C = +25°C, Derate Linearly		0.88	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2424.1**

ELECTRICAL CHARACTERISTICS *At Case Temperature (Tc) = 25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BVDSS	ID = 0.25 mA, VGS = 0 V		50	–	V
Gate Threshold Voltage	VGS(th)	VGS = VDS, ID = 0.25 mA		1	2	
Zero Gate Voltage Drain Current	IDSS	VDS = 40 V, VGS = 0 V Tc = 150°C		–	1 50	µA
Gate-Source Leakage Current	IGSS	VGS = ±10 V, VDS = 0 V		–	100	nA
Static Drain-Source on Resistance	rDS(on)	ID = 50 A, VGS = 5 V ID = 50 A, VGS = 4 V		– –	0.022 0.027	Ω
Turn-On Time	t(on)			–	100	ns
Turn-On Delay Time	td(on)	VDD = 25 V, ID = 25 A		15 (typ)	–	
Rise Time	tr	Ig1 = Ig2 = 2 A		50 (typ)	–	
Turn-Off Delay Time	td(off)	VGS (clamp): +5 V, -0.6 V		50 (typ)	–	
Fall Time	tr	RL = 1 Ω		15 (typ)	–	
Turn-Off Time	t(off)			–	100	
Total Gate Charge	Qg(total)	VGS = 0 to 10 V	VDD = 40 V	–	140	nC
Gate Charge at 5V	Qg(5)	VGS = 0 to 5 V	ID = 50 A	–	80	
Threshold Gate Charge	Qg(th)	VGS = 0 to 1 V	RL = 0.8 Ω	–	6	
Plateau Voltage	V(plateau)	ID = 50 A, VDS = 15 V		–	4	V
Turn-Off Energy Loss per Cycle	Eoff	VDD = 25 V, ID = 25 A, RL = 1 Ω L = 0.2 µH, Ig1 = Ig2 = 2 A VGS (clamp): +5 V, -0.6 V		–	150	µJ
Thermal Resistance, Junction to Case	RθJC			–	1.14	°C/W
Thermal Resistance, Junction to Ambient	RθJA			–	80	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Diode Forward Voltage	VSD	ISD = 50 A	–	1.5	V
Reverse Recovery Time	trr	ISD = 50 A, dISD/dt = 100 A/µs	–	1.25	ns

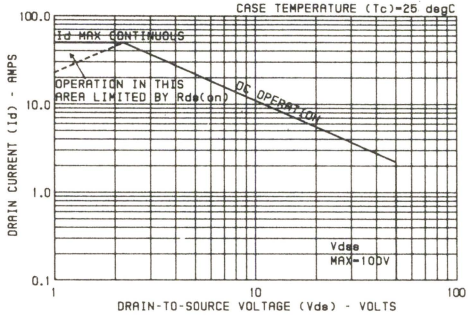


Figure 1 – Safe operating area curve.
(Curves must be derated linearly with increase in temperature.)

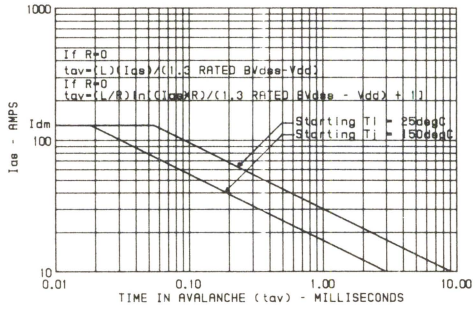


Figure 2 – Unclamped-inductive-switching safe-operating-area (single pulse UIS SOA). See Figure 14 for test circuit.

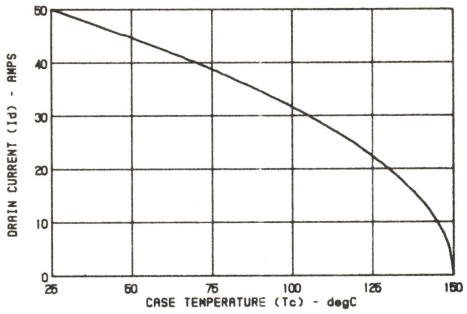


Figure 3 – Maximum continuous drain current vs. temperature.

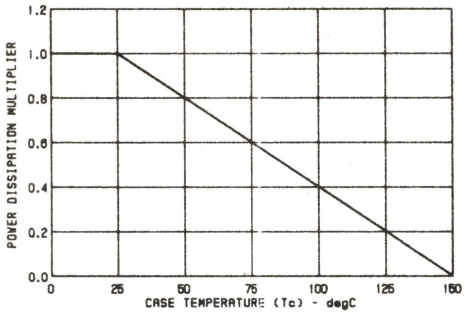


Figure 4 – Normalized power dissipation vs temperature derating curve.

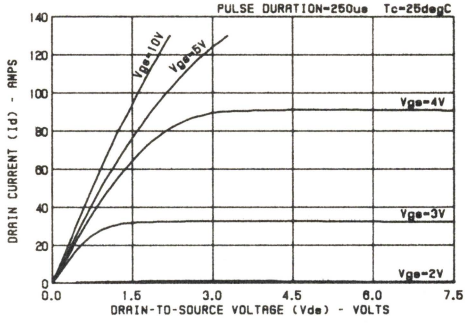


Figure 5 – Typical saturation characteristics.

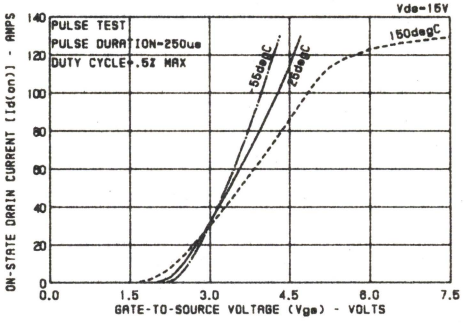


Figure 6 – Typical transfer characteristics.

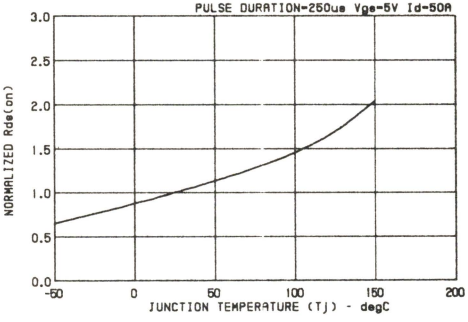


Figure 7 – Normalized Rds(on) vs junction temperature.

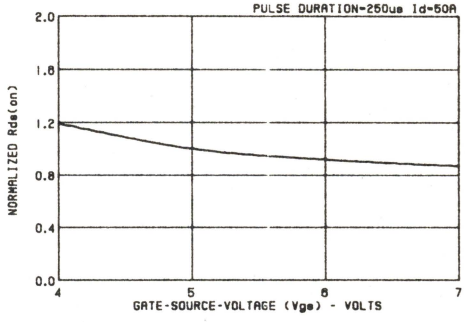


Figure 8 – Normalized Rds(on) vs Vgs.

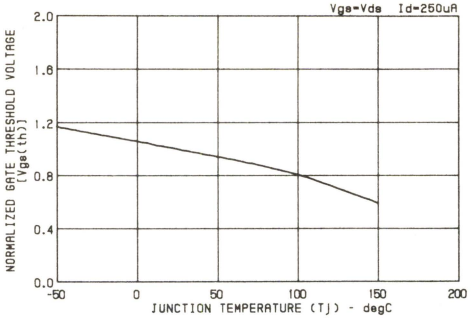


Figure 9 - Normalized gate threshold voltage.

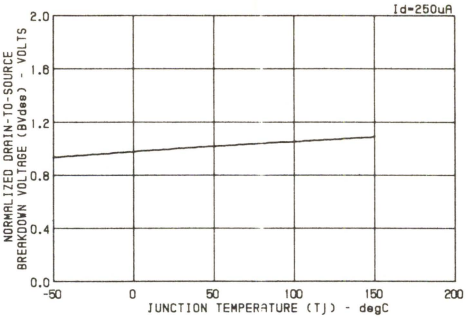


Figure 10 - Normalized drain source breakdown voltage vs temperature.

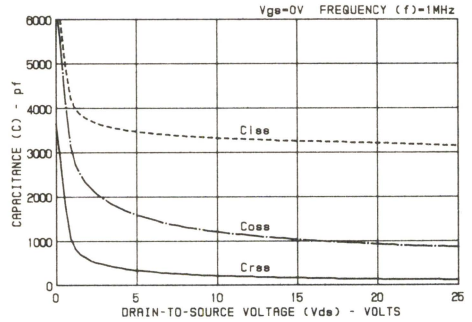


Figure 11 - Typical capacitance vs voltage.

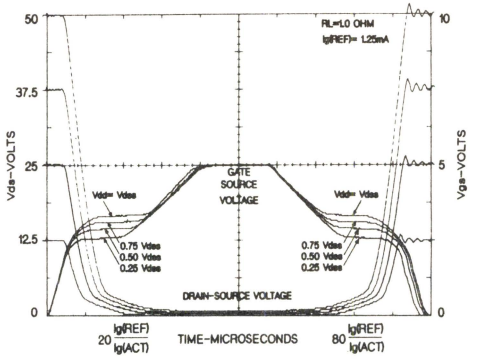
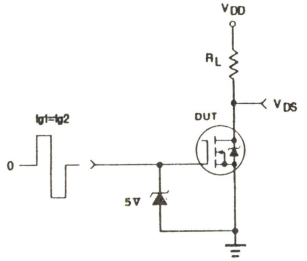
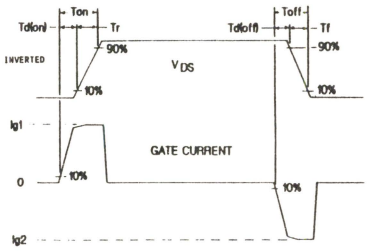


Fig. 12 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.



Switching Test Circuit



Switching Waveforms

Figure 13 - Resistive switching.

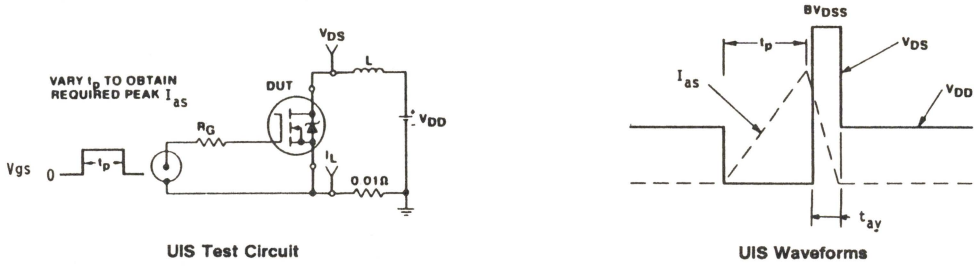


Figure 14 - Unclamped-inductive-switching test.

HARRIS SEMICONDUCTOR

RFD10P03L, RFD10P03LSM RFP10P03L

10A, -30V, Avalanche Rated, Logic Level P-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

March 1994

Features

- 10A, -30V
- $r_{DS(ON)}$ = 0.200Ω
- UIS Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- PSPICE Model

Description

The RFP10P03L P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

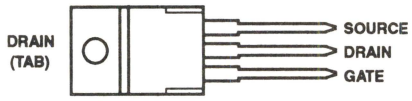
The RFD10P03L is supplied in the JEDEC TO-251AA plastic package, the RFD10P03LSM is supplied in the JEDEC TO-252AA plastic package and the RFP10P03L is supplied in the JEDEC TO-220AB plastic package. Due to space limitations the RFD10P03L and the RFD10P03LSM are branded 10P03L and the RFP10P03L is branded FP10P03L.

When ordering use the entire part number; e.g. RFD10-P03LSM.

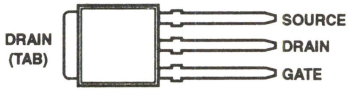
Formerly developmental type TA49012.

Package

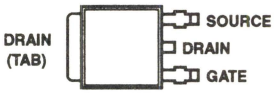
TO-220AB
TOP VIEW



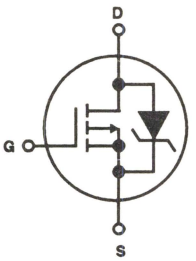
TO-251AA
TOP VIEW



TO-252AA
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RFD10P03L, RFD10P03LSM, RFP10P03L	UNITS
Drain Source Voltage	V_{DSS}	-30	V
Drain Gate Voltage	V_{DGR}	-30	V
Gate Source Voltage	V_{GS}	10	V
Drain Current			
RMS Continuous	I_D	10	A
Pulsed Drain Current	I_{DM}	25	A
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
(T_C = +25°C)	P_D	60	W
Derate above +25°C	P_T	0.4	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3515**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		-30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		-1	-	-2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V,	T_C = +25°C	-	-	-1	µA
		V_{GS} = 0V	T_C = +150°C	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 10A, V_{GS} = -5V		-	-	0.200	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 10A		-	-	110	ns
Turn-On Delay Time	$t_{D(ON)}$	R_L = 1.5Ω, V_{GS} = -5V		-	10	-	ns
Rise Time	t_R	R_{GS} = 5Ω		-	45	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	25	-	ns
Fall Time	t_F			-	35	-	ns
Turn-Off Time	t_{OFF}			-	-	120	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to -10V	V_{DD} = 24V,	-	25	30	nC
Gate Charge at 5V	$Q_{G(-5)}$	V_{GS} = 0 to -5V	I_D = 10A,	-	12	15	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to -1V	R_L = 2.4Ω	-	0.7	0.9	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 10A, V_{DS} = -15V		-	-	-4.4	V
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V		-	670	-	pF
Output Capacitance	C_{OSS}	f = 1MHz		-	225	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	58	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	2.5	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = -10A	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = -10A, dI_{SD}/dt = -100A/µs	-	-	125	ns

Typical Performance Characteristics

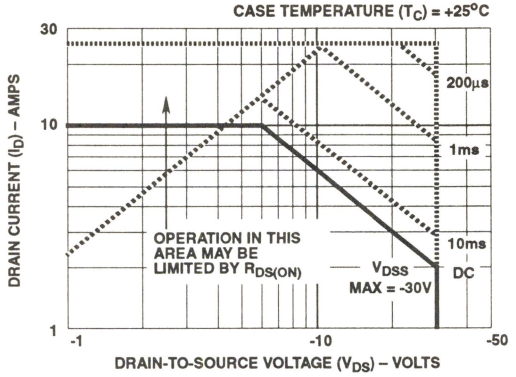


FIGURE 1. SAFE OPERATING AREA CURVE.

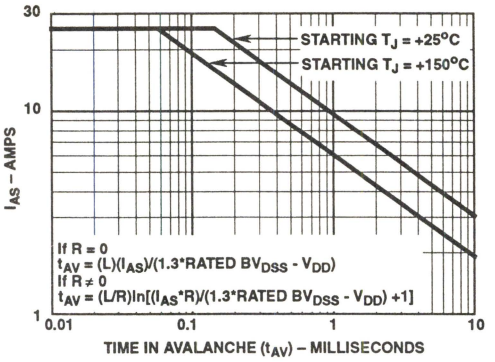


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING.

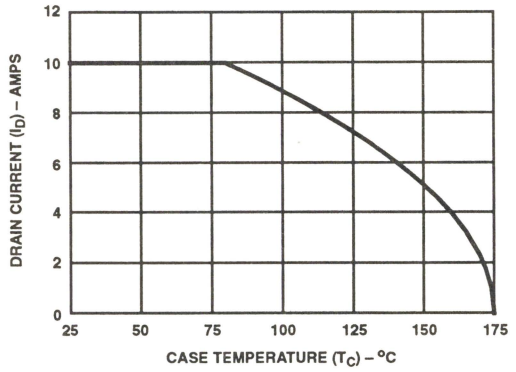


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE.

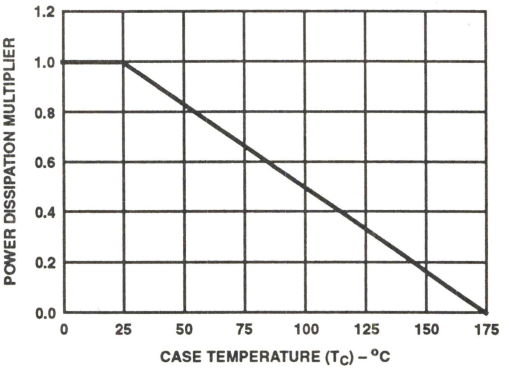


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE.

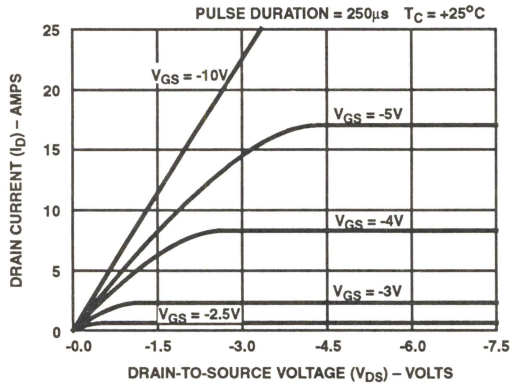


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS.

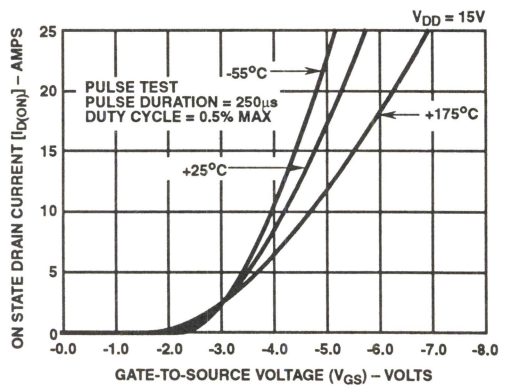


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS.

Typical Performance Characteristics (Continued)

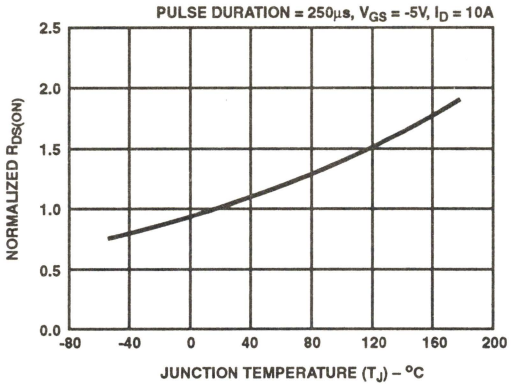


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE.

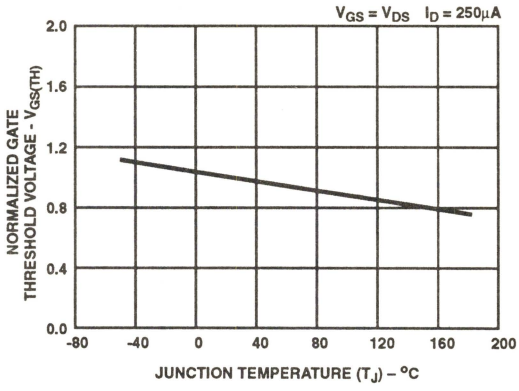


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE.

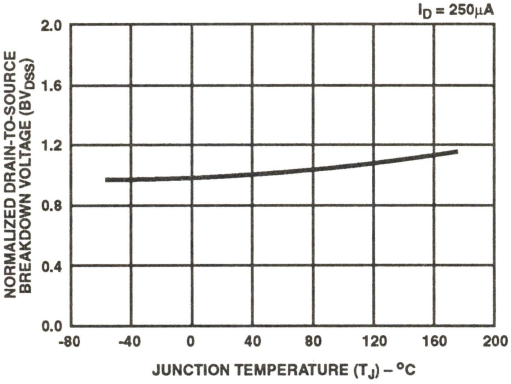


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE.

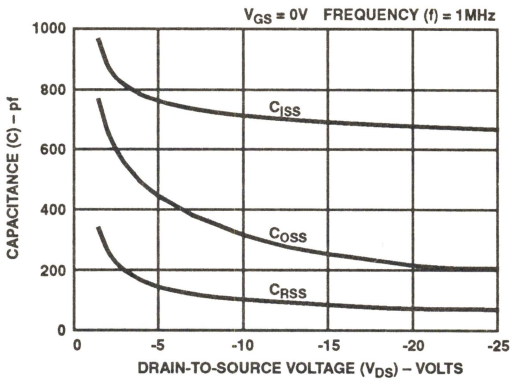


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE.

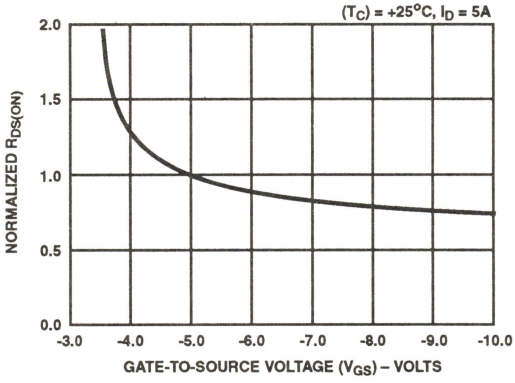


FIGURE 11. NORMALIZED $r_{DS(ON)}$ vs GATE VOLTAGE FOR CONSTANT DRAIN CURRENT.

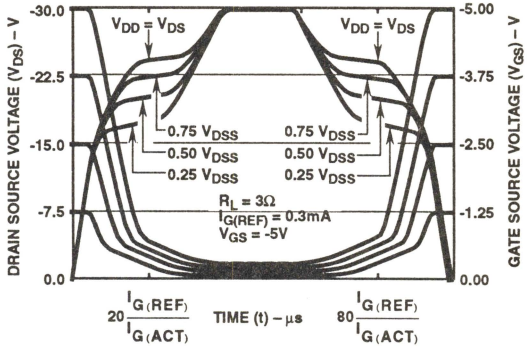


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260.

Typical Performance Characteristics (Continued)

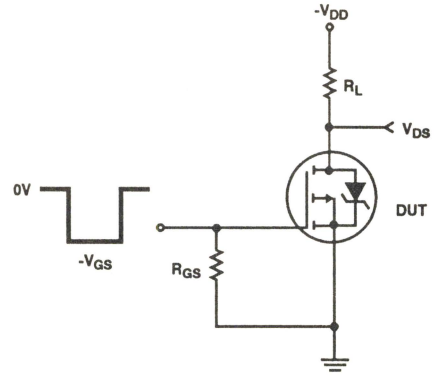


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT.

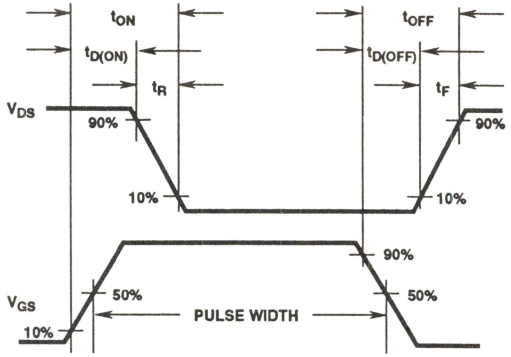


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS.

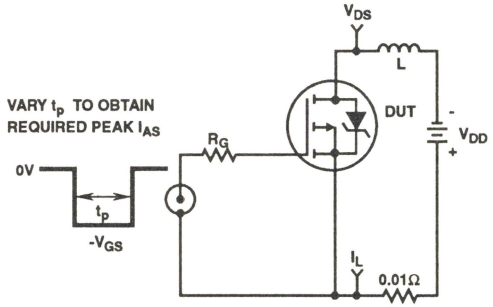


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT.

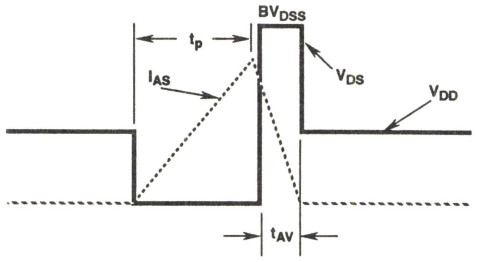


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS.

PSPICE Model for the RFD10P03L, RFD10P03LSM, RFD10P03L (Temperature Compensated)

```
CA 12 8 1.42e-9
CB 15 14 1.3e-9
CIN 6 8 0.67e-9

DBODY 5 7 DBDMOD
DBREAK 7 11  DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -51.9
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 8.7e-12
LSOURCE 3 7 7.6e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 79.08e-3
RGATE 9 20 12.25
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 27.49e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.50

.MODEL DBDMOD D (IS=1.14e-13 RS=2.86e-2 TRS1=6.29e-4 TRS2=-2.76e-6 CJO=8.55e-10 TT=3.84e-8)
.MODEL DBKMOD D (RS=3.32e-1 TRS1=5.50e-3 TRS2=-5.38e-5)
.MODEL DPLCAPMOD D (CJO=0.43e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-2.01 KP=5.3105 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=6.07e-4 TC2=3.30e-6)
.MODEL RDSMOD RES (TC1=3.48e-3 TC2=8.83e-6)
.MODEL RVTOMOD RES (TC1=-1.51e-3 TC2=8.74e-7)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.42 VOFF=2.42)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.42 VOFF=4.42)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.43 VOFF=-3.57)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.57 VOFF=1.43)

.ENDS
```

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

POWER MOSFETs 7

INTELLIGENT DISCRETES

PAGE

INTELLIGENT DISCRETE DATA SHEETS

RFB18N10CS	Current Sensing N-Channel Enhancement-Mode Power Field-Effect Transistor	7-3
RFV10N50BE	10A, 500V, Fast Switching N-Channel Enhancement-Mode Power MOSFETs	7-8
RLP1N06CLE	Voltage-Clamping Current-Limited ESD-Protected N-Channel Enhancement-Mode Power Field-Effect Transistor	7-13
RLP1N08LE	Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor.	7-20
RLP5N08LE	Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor.	7-27

HARRIS SEMICONDUCTOR

RFB18N10CS

Current Sensing N-Channel Enhancement-Mode Power Field-Effect Transistor

April 1993

Features

- 18A, 100V
- $r_{DS(ON)}$ 0.1Ω
- Built-In Current Sensing Ratio . . . . . 1350 to 1650
- UIS SOA Rating Curve (Single Pulse)
- -55°C to +175°C Operating and Storage Temperature

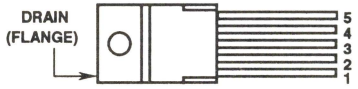
Description

The RFB18N10CS is an n-channel enhancement-mode silicon-gate power field-effect transistors which have a built-in current sensing function. The current sense lead provides an accurate fraction of the drain current that can be used as a feedback signal for control and/or protection. These devices can be repeatedly and economically produced on the standard PowerMOS production line.

Because of space limitations, branding (marking) on type RFB18N10CS is F18N10CS.

Package

TS-001AA
TOP VIEW

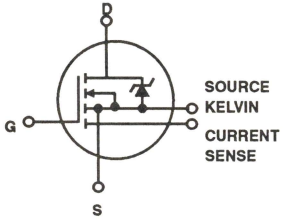


TERMINAL CONNECTIONS

1 - Gate
2 - Current Sense
3 - Drain
4 - Source Kelvin
5 - Source

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFB18N10CS	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage	V_{DGR}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current			
RMS Continuous	I_D	18	A
Pulsed Drain Current	I_{DM}	56	A
Single Pulse Avalance Rating, Refer to UIS SOA Curve (Figure 10)			
Power Dissipation			
T_C = +25°C	P_D	79	W
Above T_C = +25°C, Derate Linearly		0.53	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 2430.3

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V	100	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0			
		V_{DS} = 100V, T_C = 25°C	-	250	µA
		V_{DS} = 80V, T_C = 175°C	-	1000	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	±500	nA
Static Drain-Source On Resistance	$r_{DS(ON)}$	I_D = 9A, V_{GS} = 10V	-	0.10	Ω
Forward Transconductance	gfs	I_D = 9A, V_{DS} = 15V	4.7	-	S(℧)
Current Sensing Ratio	r	I_D = 14A, V_{GS} = 10V	1350	1650	
Turn-On Delay Time	$t_{D(ON)}$	V_{DS} = 50V	-	14	ns
Rise Time	t_R	I_D = 14A	-	63	ns
Turn-Off Delay Time	$t_{D(OFF)}$	V_{GS} = 10V	-	33	ns
Fall Time	t_F	R_{GS} = 12Ω	-	38	ns
Total Gate Charge	$Q_{G(TOTAL)}$	I_D = 14A, V_{DS} = 80V, V_{GS} = 10V	-	20	nC
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	1.9	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		-	75	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 14A	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 14A, dI_{SD}/dt = 100A/µs	-	310	ns

Typical Performance Curves

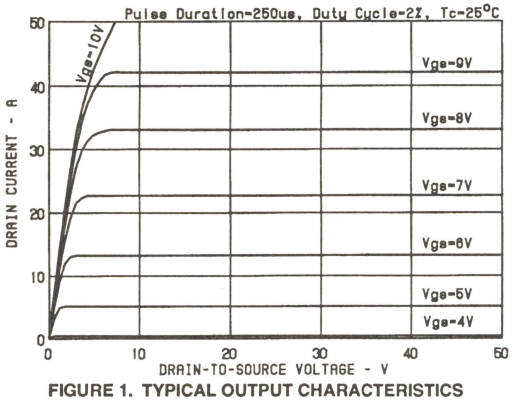


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

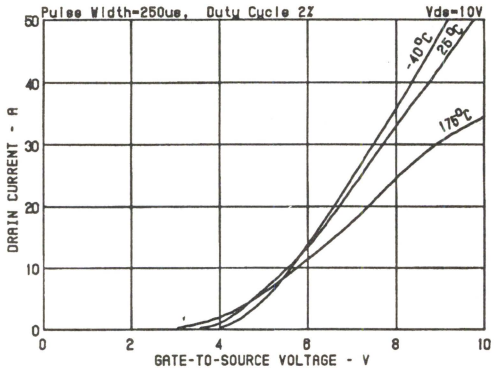


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

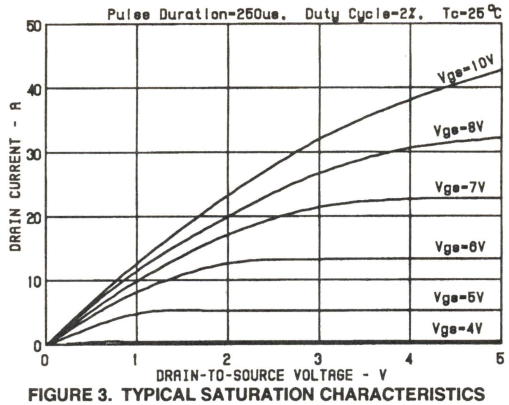


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

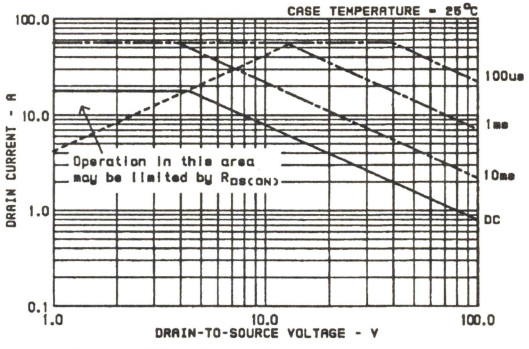


FIGURE 4. MAXIMUM SAFE OPERATING AREAS (CURVES MUST BE DERATED LINEARITY WITH INCREASE IN CASE TEMPERATURE)

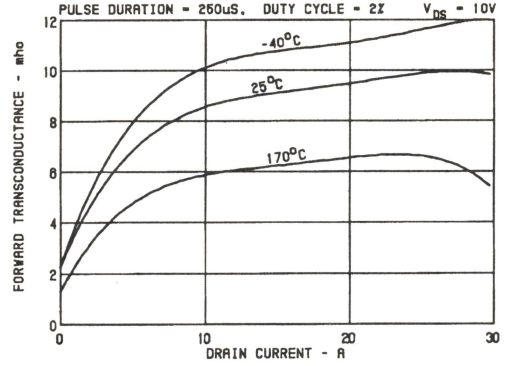


FIGURE 5. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

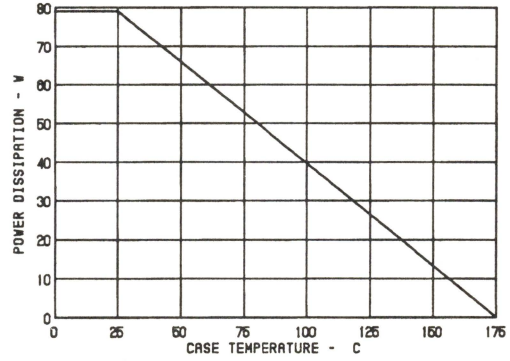


FIGURE 6. POWER DISSIPATION vs CASE TEMPERATURE DERATING CURVE

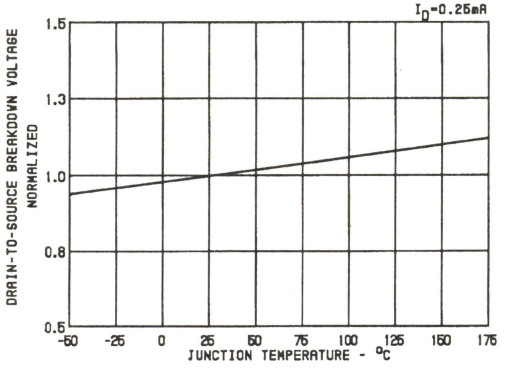


FIGURE 7. NORMALIZED BREAKDOWN VOLTAGE vs TEMPERATURE

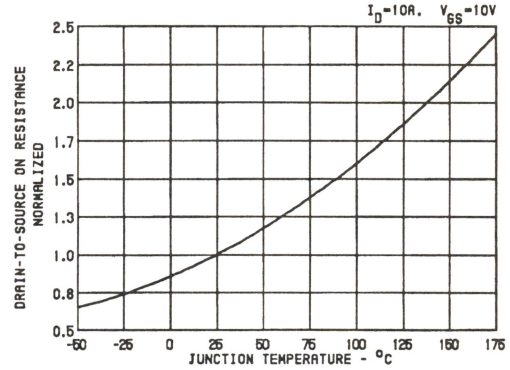


FIGURE 8. NORMALIZED ON-RESISTANCE vs TEMPERATURE

Typical Performance Curves (Continued)

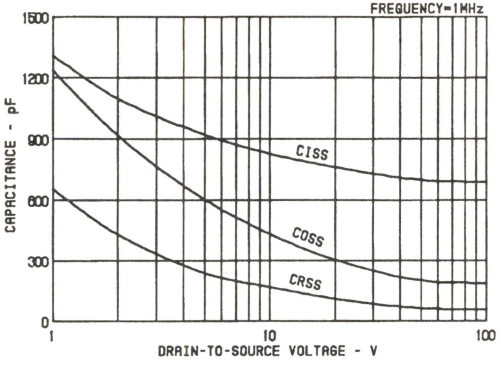


FIGURE 9. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

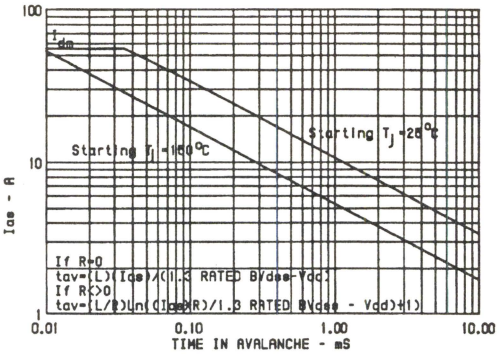


FIGURE 10. UNCLAMPED-INDUCTIVE SWITCHING SAFE OPERATING AREA

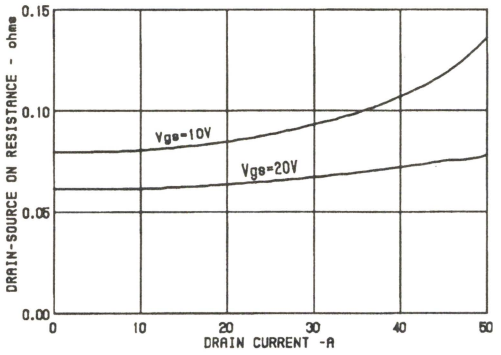


FIGURE 11. TYPICAL ON-RESISTANCE vs DRAIN CURRENT

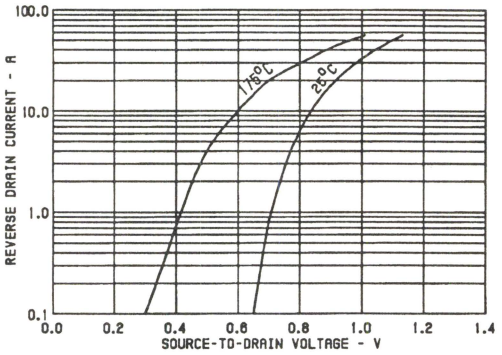


FIGURE 12. TYPICAL SOURCE-DRAIN-DIODE FORWARD VOLTAGE.

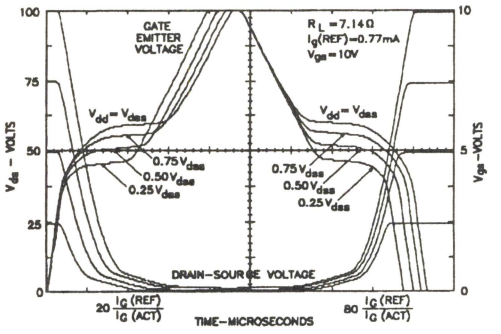


FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT (REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260)

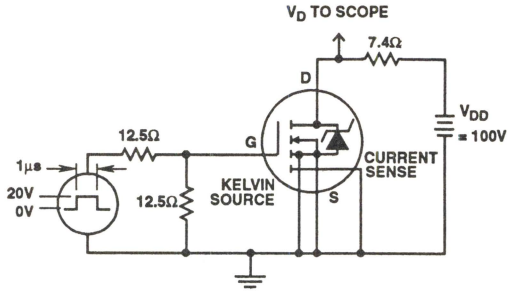


FIGURE 14. SWITCHING TIME TEST CIRCUIT

Typical Performance Curves (Continued)

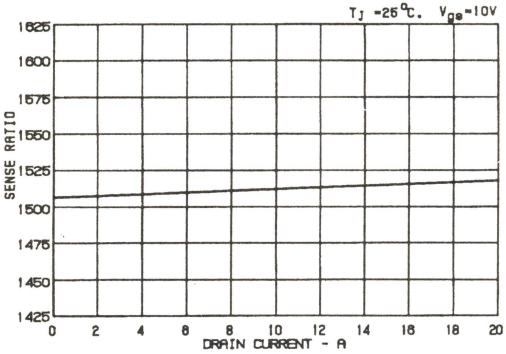


FIGURE 15. CURRENT SENSE RATIO vs DRAIN CURRENT

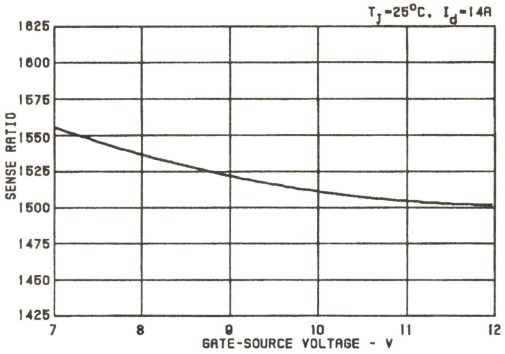


FIGURE 16. CURRENT SENSE RATIO vs GATE VOLTAGE

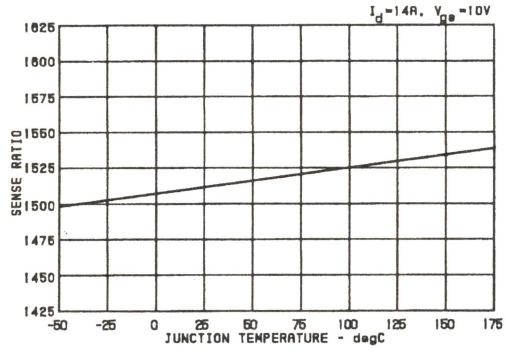


FIGURE 17. CURRENT SENSE RATIO vs JUNCTION TEMPERATURE

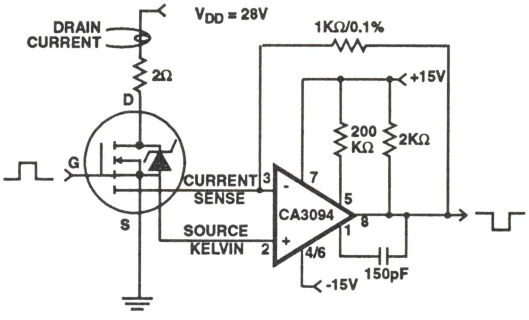


FIGURE 18. CURRENT SENSE RATIO TEST CIRCUIT

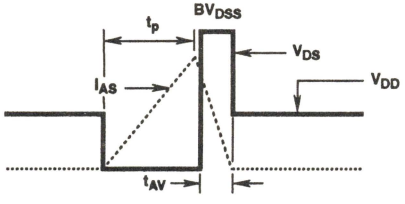


FIGURE 19. UIS WAVEFORMS

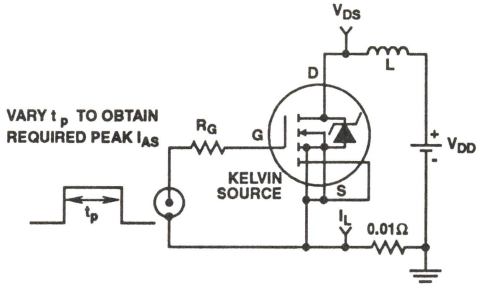


FIGURE 20. UIS TEST CIRCUIT

HARRIS SEMICONDUCTOR

RFV10N50BE

10A, 500V, Fast Switching N-Channel Enhancement-Mode Power MOSFETs

December 1992

Features

- 10A, 500V
- $r_{DS(on)} = 0.48\Omega$
- Very Fast Turn-Off Characteristics
- Nanosecond Switching Speeds
- Electrostatic Discharge Protected
- UIS Rating Curve (Single Pulse)
- SOA is Power Dissipation Limited
- High Input Impedance

Description

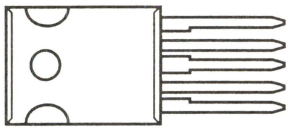
The RFV10N50BE is an N-Channel fast switching MOSFET transistor that is designed for switching regulators, inverters and motor drivers. The RFV10N50BE is a monolithic structure incorporating a high voltage, high current MOSFET, a control MOSFET and ESD protection diodes. As indicated in the symbol to the right, the turn-on of the main MOSFET is controlled by Gate 1 (G_1). The control MOSFET, controlled by Gate 2 (G_2), is distributed throughout the structure. Gate 2 provides a very low impedance and inductive path to rapidly discharge the gate of the main MOSFET. Gate 2 affords very fast turn-off (typically less than 25ns) when desired. A separate return connection, Source Kelvin (S_k), is supplied for the gate drive circuit to avoid voltage induced transients from the output circuit during switching. The RFV10N50BE can be operated directly from integrated circuits.

The RFV10N50BE is supplied in the 5 lead TO-247 style plastic package.

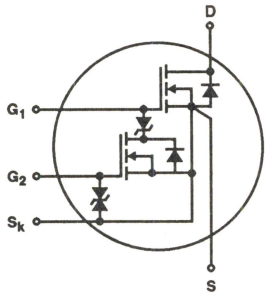
The RFV10N50BE was formally developmental type TA9881.

Package

5 LEAD TO-247 STYLE
TOP VIEW



Terminal Diagram



Absolute Maximum Ratings ($T_C = +25^oC$)

			UNITS
Drain Source Voltage	V_{DSS}	500	V
Gate Source Voltage	V_{GS}	+14, -0.3	V
Control FET Gate Source Voltage	V_{GS}	+14, -0.3	V
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	KV
Drain Current			
RMS Continuous	I_D	10	A
Pulsed Drain Current	I_{DM}	25	A
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Control FET Avalanche Current	I_{AS}	1.5	A
Control FET Single Pulse Avalanche Rating	E_{AS}	50	mJ
Power Dissipation			
$T_C = +25^oC$	P_D	156	W
Derate Above +25°C		1.25	W/°C
Control FET Power Dissipation			
$T_C = +25^oC$	P_D	21	W
Derate Above +25°C		0.17	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **3377**

Electrical Characteristics Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		500	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250µA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +125°C	-	-	250	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +12V, V_{GS} = -0.3V		-	-	±500	nA
On Resistance	$r_{DS(on)}$	I_D = 10A, V_{GS} = 10V		-	-	0.48	Ω
Turn-On Time	t_{on}	V_{DD} = 250V, I_D = 10A, R_L = 25Ω, V_{GS1} = V_{GS2} = +10V, R_{GS1} = 6.25Ω, R_{GS2} = 20Ω		-	-	75	ns
Turn-On Delay Time	$t_{d(on)}$			-	20	-	ns
Rise Time	t_r			-	30	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	21	-	ns
Fall Time	t_f			-	5	-	ns
Turn-Off Time	t_{off}			-	-	50	ns
Total Gate Charge	Q_{g10}	V_{GS} = 0V to 10V	V_{DD} = 400V, I_D = 10A, R_L = 40Ω	-	145	190	nC
Gate Source Charge	Q_{gs}			-	17	22	nC
Gate Drain ("Miller") Charge	Q_{gd}			-	57	74	nC
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3800	-	pF
Output Capacitance	C_{oss}			-	290	-	pF
Reverse Transfer Capacitance	C_{rss}			-	75	-	pF
Thermal Resistance	$R_{\theta JC}$	Junction to Case		-	-	0.8	°C/W
Thermal Resistance	$R_{\theta JA}$	Junction to Ambient		-	-	40	°C/W

Control FET Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Static Drain to Source	$r_{DS(on)}$	V_{GS} = 10V, I_D = 1.0A	-	1.6	-	Ω
Drain Source Breakdown Voltage	BV_{DSS}	I_D = 1.0mA, V_{GS} = 0V	14	15	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	2	-	4	V
Total Gate Charge	Q_{g10}	I_D = 1.0A, V_{GS} = 10V	-	-	5	nC

Source-Drain Diode Ratings And Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Continuous Source Current	I_S		-	-	10	A
Pulsed Source Current	I_{SM}		-	-	25	A
Forward Voltage	V_{SD}	I_{SD} = 10A, V_{GS} = 0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_{SD} = 10A, V_{GS} = 0V, dI_{SD}/dt = 100A/ms	-	-	750	ns

Performance Curves

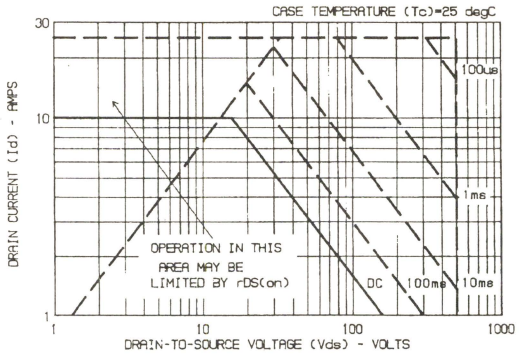


FIGURE 1. SAFE OPERATING AREA CURVE

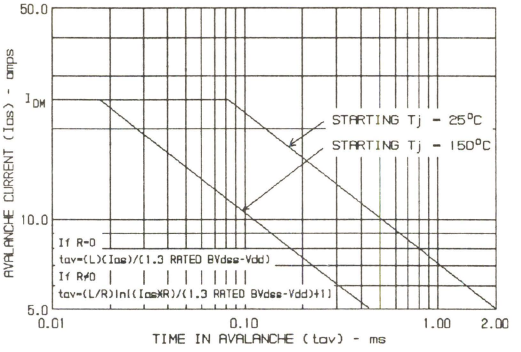


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

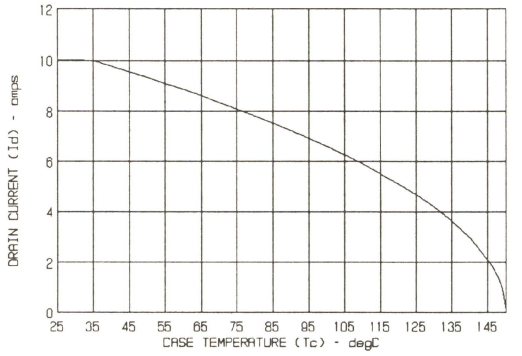


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

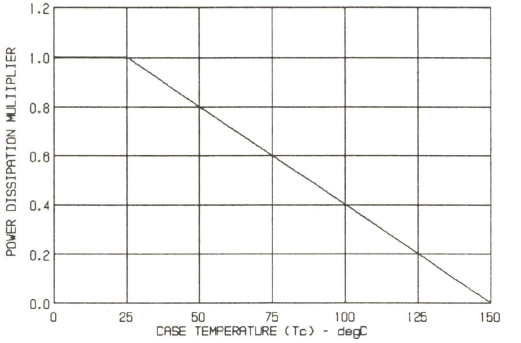


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

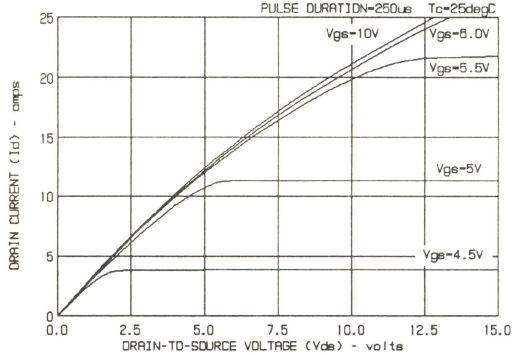


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

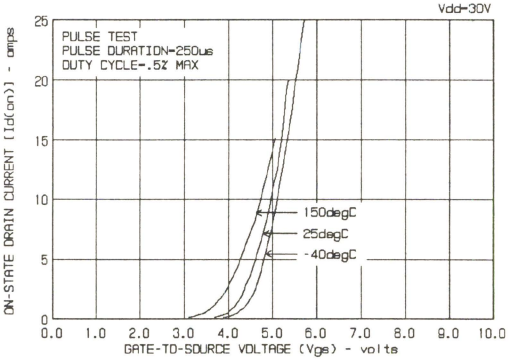


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Performance Curves (Continued)

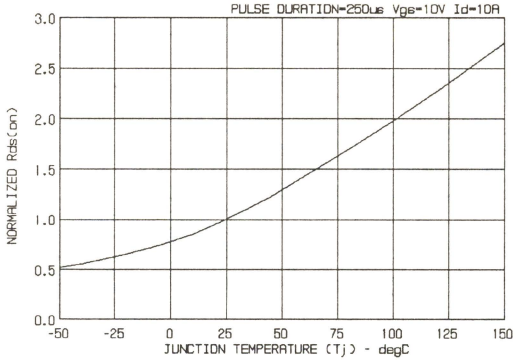


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs JUNCTION TEMPERATURE

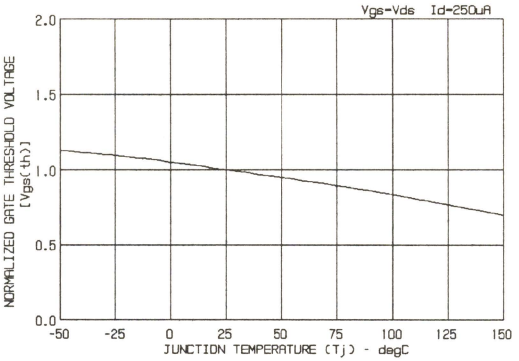


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

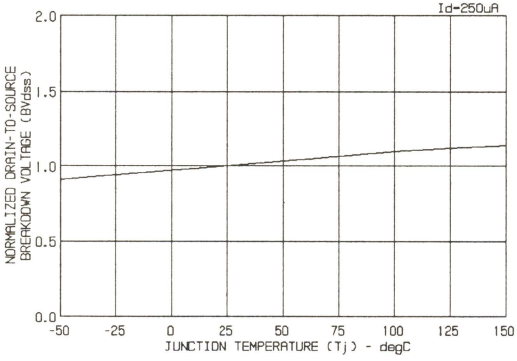


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

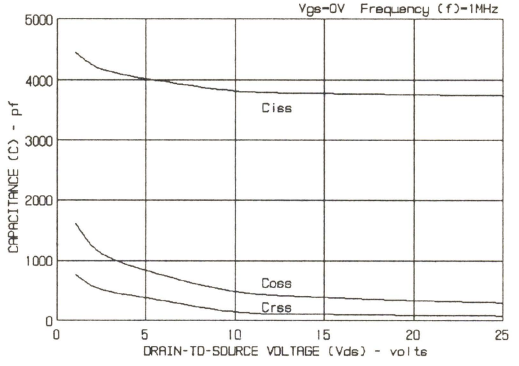


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

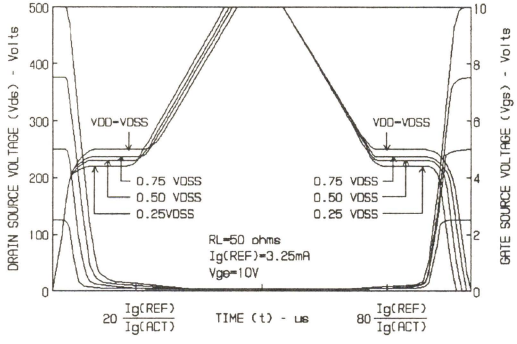


FIGURE 11. TYPICAL SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTES AN7254 AND AN7260

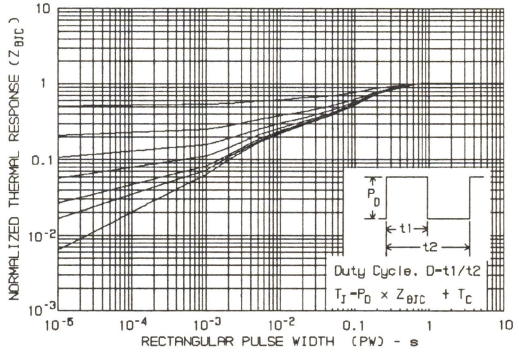


FIGURE 12. MAXIMUM NORMALIZED TRANSIENT THERMAL IMPEDANCE

Performance Curves (Continued)

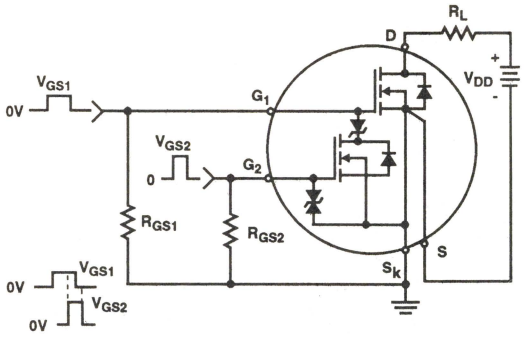


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUITS

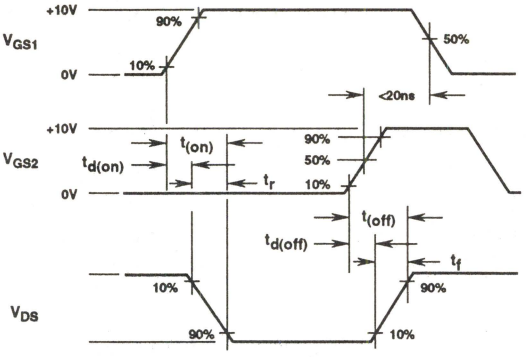


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

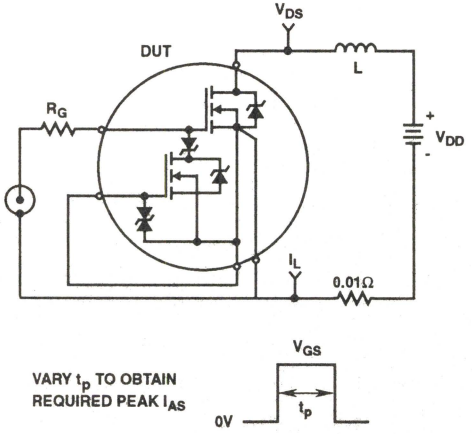


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

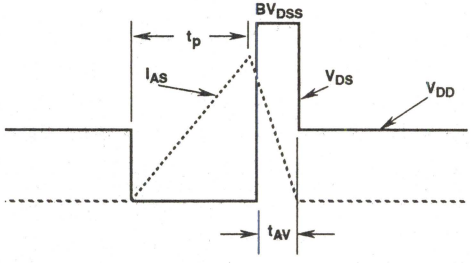


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

HARRIS

RLP1N06CLE

Voltage-Clamping Current-Limited ESD-Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

January 1994

Features

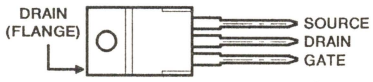
- 1A, 55V
- $R_{DS(ON)}$ 0.75Ω
- I_{Limit} ..... 1.1A to 1.5A Max @ +150°C
- Built In Voltage Clamp
- Built In Current Limiting
- ESD Protected .....2KV Min
- Controlled Switching Limits EMI and RFI
- +175°C Rated Junction Temperature
- Logic Level Gate

Description

The RLP1N06CLE is an intelligent monolithic power circuit which incorporates a lateral bipolar transistor, resistors, zener diodes, and a PowerMOS transistor. The current limiting of this device allows it to be used safely in circuits where it is anticipated that a shorted load condition may be encountered. The drain-source voltage clamping offers precision control of the circuit voltage when switching inductive loads. "Logic Level" gates allow this device to be fully biased on with only 5.0V from gate to source. Input protection is provided for ESD up to 2KV.

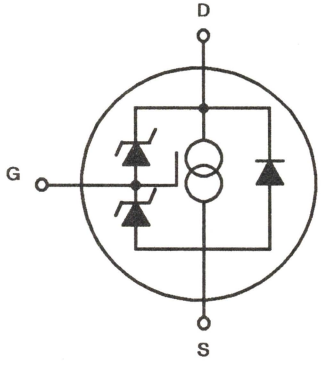
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RLP1N06CLE	UNITS
Drain-Source Voltage	V_{DSS}	55	V
Drain-Gate Voltage	V_{DGR}	55	V
Gate-Source Voltage*	V_{GS}	5.5	V
Reverse Voltage Gate Bias Not Allowed			
Electrostatic Voltage at T_C = +25°C	ESD	2	kV
Drain Current, Continuous	I_D	Self Limited	
Power Dissipation Total @ T_C = +25°C	P_D	36	W
Power Dissipation Derating T_C > +25°C		0.24	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

* May be exceeded if current is limited to 10mA.

7 INTELLIGENT DISCRETES

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number **2839.1**

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain Source Breakdown Voltage	BV_{DSS}	I_D = 20mA V_{GS} = 0V	55	70	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS} I_D = 0.25mA	1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 45V V_{GS} = 0V	-	5	µA
		at T_C = +150°C	-	20	µA
Gate Source Leakage Current	I_{GSS}	V_{GS} = 5V	-	5	µA
		at T_C = +150°C	-	20	µA
On Resistance	$R_{DS(ON)}$	I_D = 1A V_{GS} = 5.0V	-	0.75	Ω
		at T_C = +150°C	-	1.5	Ω
Limiting Current	$I_{DS(Limit)}$	V_{DS} = 15.0V V_{GS} = 5.0V	1.8	3	A
		@ T_C = 150°C	0.9	1.5	A
Turn-On Time	$t_{(ON)}$	V_{DD} = 30.0V	-	6.5	µs
Turn-On Delay Time	$t_{D(ON)}$	I_D = 1A	-	1.5	µs
Rise Time	t_R	V_{GS} = 5.0V	1.0	5.0	µs
Turn-Off Delay Time	$t_{D(OFF)}$	R_{GS} = 25Ω	-	7.5	µs
Fall Time	t_F	R_L = 30Ω	1.0	5.0	µs
Turn-Off Time	$t_{(OFF)}$		-	12.5	µs
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 1A V_{DS} = 15.0V	-	5.0	V
Thermal Resistance Junction to Case	$R\theta_{JC}$		-	4.17	°C/W
Thermal Resistance Junction to Ambient	$R\theta_{JA}$		-	80	°C/W
Electrostatic Voltage	ESD	Human Model (100pF, 1.5kΩ) MIL-STD-883B (Category B2)	2000	-	V

Source-Drain Diode Ratings and Characteristics

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 1A	-	1.5	V
Reverse Recovery Time	T_{RR}	I_F = 1A	-	1.0	ms

Performance Curves

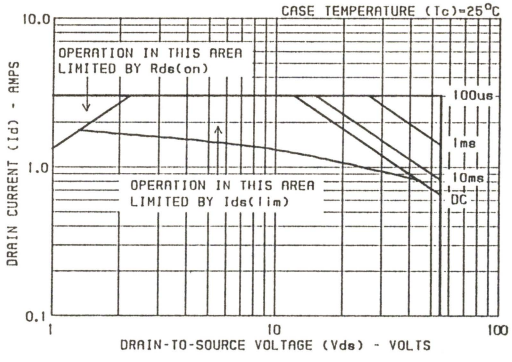


FIGURE 1. SAFE-OPERATING-AREA CURVE

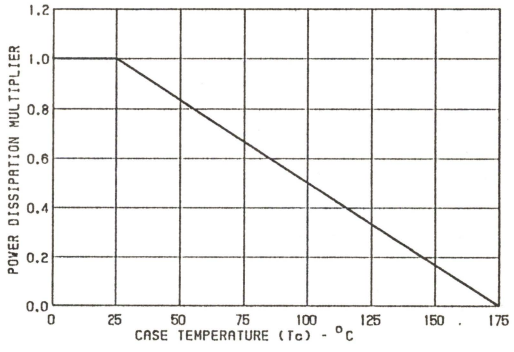


FIGURE 2. NORMALIZED POWER DISSIPATION vs. TEMPERATURE DERATING CURVE

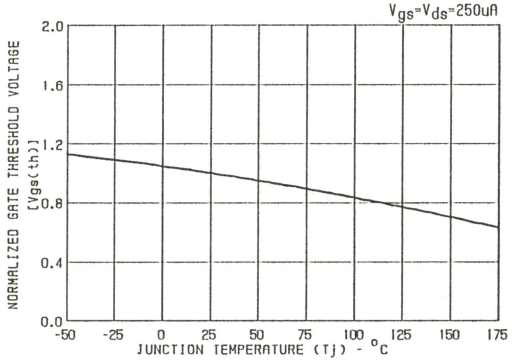


FIGURE 3. TYPICAL NORMALIZED GATE-THRESHOLD VOLTAGE

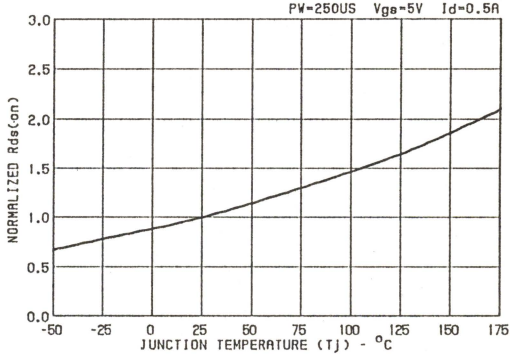


FIGURE 4. NORMALIZED $r_{DS(ON)}$ vs. JUNCTION TEMPERATURE

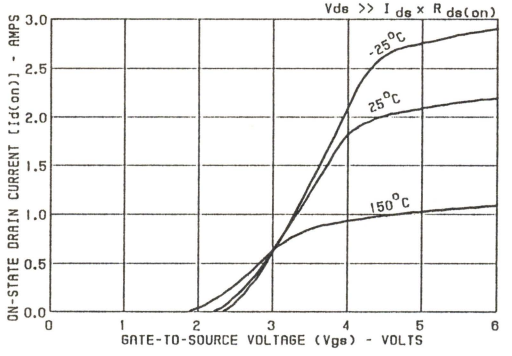


FIGURE 5. TYPICAL TRANSFER CHARACTERISTICS

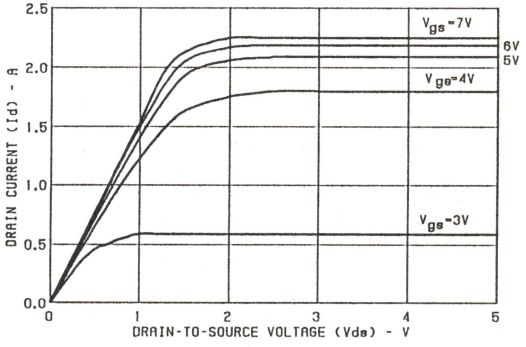


FIGURE 6. TYPICAL SATURATION CHARACTERISTICS

Performance Curves (Continued)

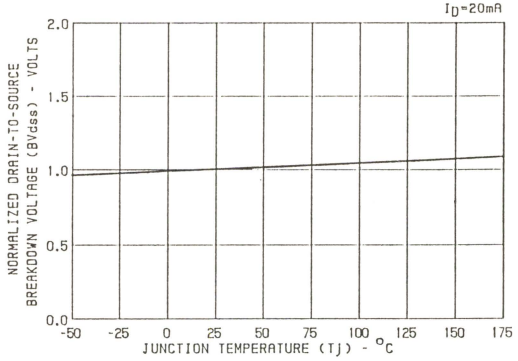


FIGURE 7. DRAIN-SOURCE BREAKDOWN VOLTAGE vs. TEMPERATURE

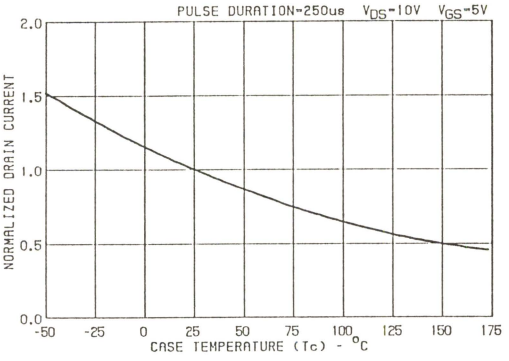


FIGURE 8. NORMALIZED CURRENT LIMIT vs. TEMPERATURE

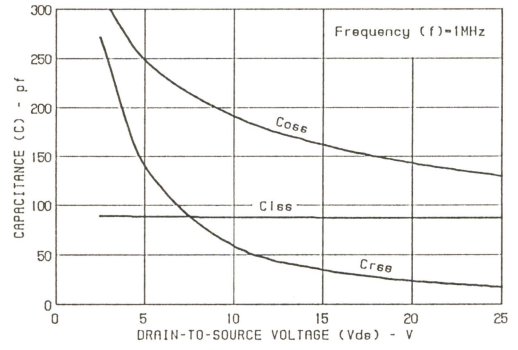


FIGURE 9. TYPICAL CAPACITANCE vs. VOLTAGE

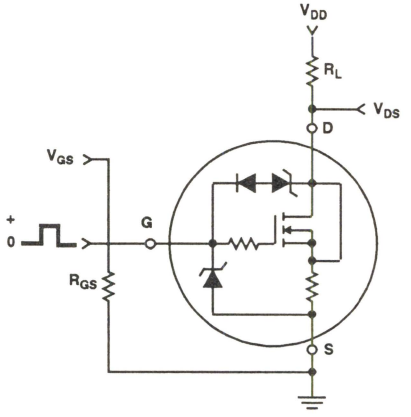


FIGURE 10. SWITCHING TEST CIRCUIT

Temperature Dependence of Current Limiting and Switching Speed

The RLP1N06CLE is a monolithic power device which incorporates a Logic Level PowerMOS transistor with a resistor in series with the source. The base and emitter of a lateral bipolar transistor is connected across this resistor, and the collector of the bipolar transistor is connected to the gate of the PowerMOS transistor. When the voltage across the resistor reaches the value required to forward bias the emitter base junction of the bipolar transistor, the bipolar transistor "turns on". A series resistor is incorporated in series with the gate of the PowerMOS transistor allowing the bipolar transistor ot drive the gate of the PowerMOS transistors to a voltage which just maintains a constant current in the PowerMOS transistor. Since both the resistance of the resistor in series with the PowerMOS transistor source and voltage required to forward bias the base emitter junction of the bipolar transistor vary with the temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 8.

The resistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

Performance Curves (Continued)

DC Operation of the RLP1N06CLE

The limit of the drain-to-source voltage for operation in current limiting on a steady state (DC) basis is shown as Figure A. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOSFET devices today, is limited to +150°C. The maximum voltage allowable can, therefore, be expressed as:

$$V_{DS} = \frac{(150°C - T_{AMBIENT})}{I_{LIM} \times (R_{\theta JC} + R_{\theta CA})}$$

Duty Cycle Operation of the RLP1N06CLE

In many applications either the drain-to-source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N06CLE is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_C = (V_{DS} \times I_D \times D \times R_{\theta CA}) + T_{AMBIENT}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to +150°C and using the T_C calculated above, the expression for maximum V_{DS} under duty cycle operation is:

$$V_{DS} = \frac{150 - T_C}{I_{LIM} \times D \times R_{\theta JC}}$$

These values are plotted as Figures B1 - B5 for various heatsink thermal resistances.

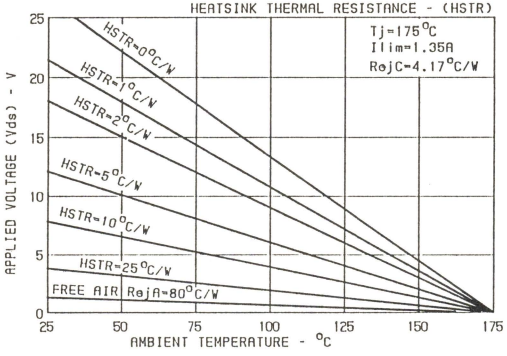


FIGURE A. DC OPERATION IN CURRENT LIMITING

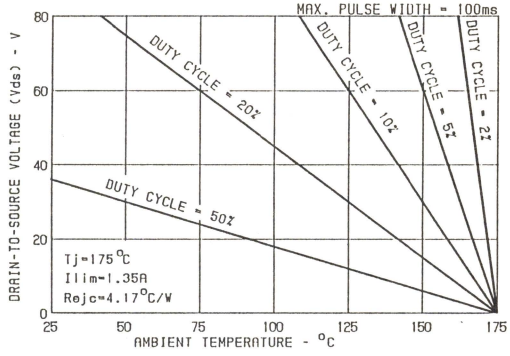


FIGURE B1. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 2°C/W)

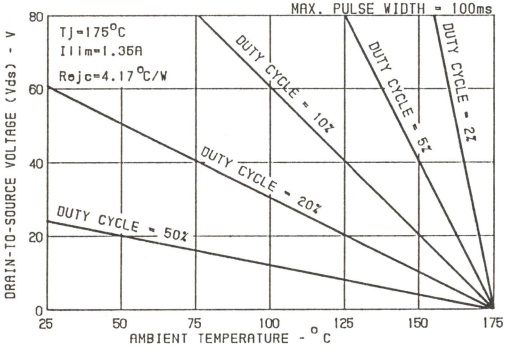


FIGURE B2. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 5°C/W)

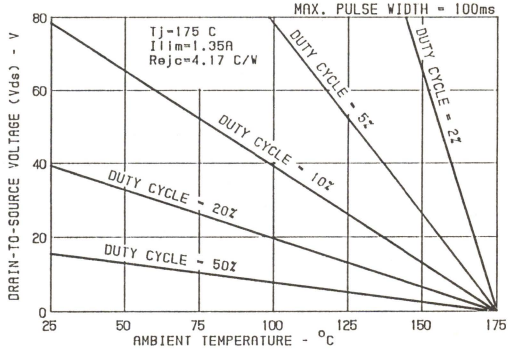


FIGURE B3. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 10°C/W)

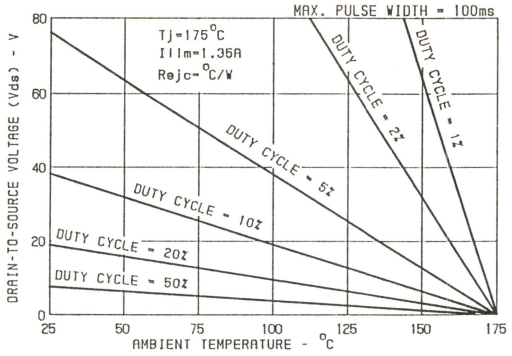


FIGURE B4. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 25°C/W)

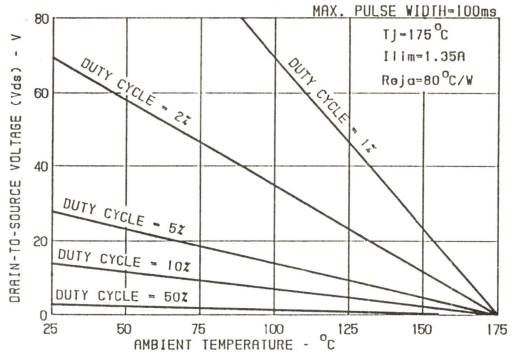


FIGURE B5. MAXIMUM V_{DS} vs. AMBIENT TEMPERATURE IN CURRENT LIMITING. (NO EXTERNAL HEATSINK)

Limited Time Operations of the RLP1N06CLE

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to a allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1-C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 175°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

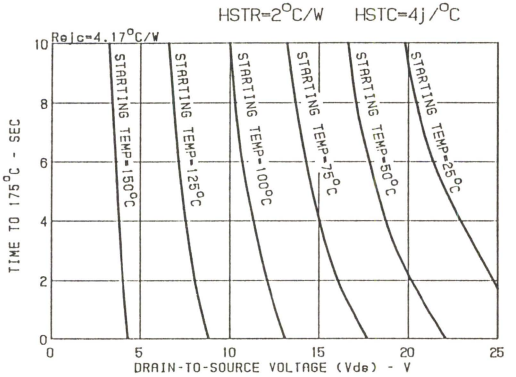


FIGURE C1. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W HEATSINK THERMAL CAPACITANCE = 4j/°C)

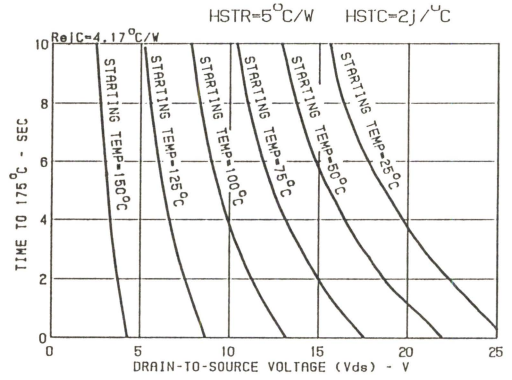


FIGURE C2. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W HEATSINK THERMAL CAPACITANCE = 2j/°C)

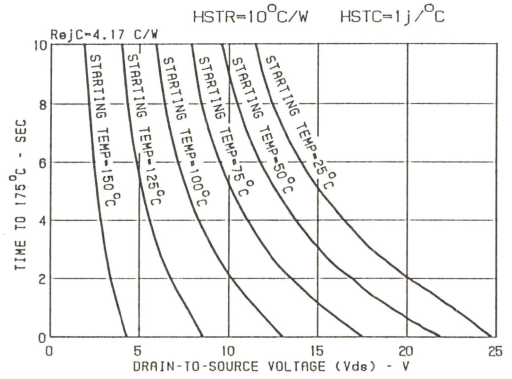


FIGURE C3. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W HEATSINK THERMAL CAPACITANCE = 1j/°C)

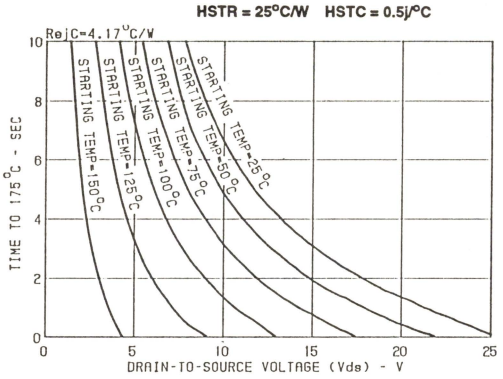


FIGURE C4. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W, HEATSINK THERMAL CAPACITANCE = 0.5j/°C)

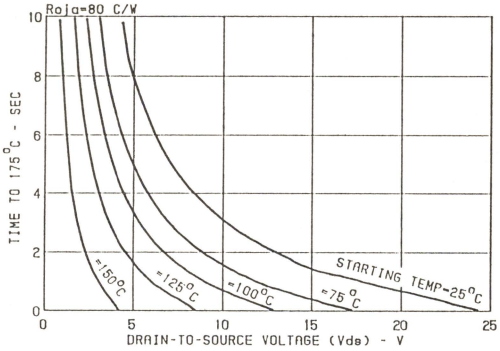


FIGURE C5. TIME TO 175°C IN CURRENT LIMITING (NO EXTERNAL HEATSINK)

HARRIS

RLP1N08LE

Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

January 1994

Features

- 1A, 80V
- $r_{DS(ON)} = 0.75\Omega$
- I_{LIMIT} at +150°C ..... 1.5A Max
- Built-In Current Limiting
- ESD Protected
- Controlled Switching Limits EMI and RFI
- Specified for +150°C Operation
- Temperature Compensated Spice Model Provided

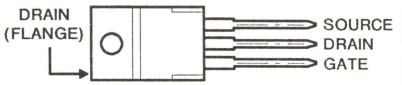
Description

The RLP1N08LE is a semi-smart monolithic power circuit which incorporates a lateral bipolar transistor, two resistors, a zener diode, and a PowerMOS transistor. Good control of the current-limiting levels allows use of these devices where a shorted load condition may be encountered. "Logic level" gates allow this device to be fully biased on with only 5 volts from gate to source. The zener diode provides ESD protection up to 2kV. These devices can be produced on the standard PowerMOS production line.

The RLP-series types are supplied in the JEDEC TO-220AB plastic packages.

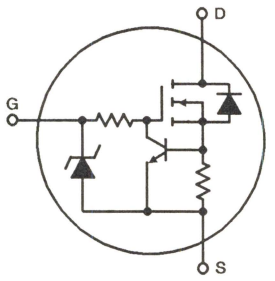
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RLP1N08LE	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage (1)	V_{GS}	5.5	V
Reverse Voltage Gate Bias Not Allowed			
Electrostatic Voltage at 100pF, 1500Ω	ESD	2	kV
Drain Current, Continuous	I_D	Self Limited	
Power Dissipation Total @ T_C = +25°C	P_D	30	W
Power Dissipation Derating T_C > +25°C		0.24	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +150	°C

(1) May be exceeded if current is limited to 10mA.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number **2252.2**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified.*

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V	80	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	1	2	
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V, V_{GS} = 0 V	—	1	μA
		T_C = 150° C	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 5 V, T_C = 150° C	—	50	
On Resistance	$r_{DS}(on)$	I_D = 1 A, V_{GS} = 5 V	—	0.75	Ω
		T_C = 150° C	—	1.5	
Limiting Current	$I_{DS}(Lim)$	V_{DS} = 15 V, V_{GS} = 5 V	1.8	3	A
		T_C = 150° C	1.1	1.5	
Turn-On Time	t(on)	V_{DD} = 30 V, I_D = 1 A V_{GS} = 5 V, R_{GS} = 25 Ω R1 = 30 Ω	—	6.5	μs
Turn-On Delay Time	$t_d(on)$		—	1.5	
Rise Time	t_r		1	5	
Turn-Off Delay Time	$t_d(off)$		—	7.5	
Fall Time	t_f		1	5	
Turn-Off Time	t(off)		—	12.5	
Plateau Voltage	V(plateau)	I_D = 1 A, V_{DS} = 15 V	—	5	V
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		—	4.17	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		—	80	
Electrostatic Voltage	ESD	Human Model (100 pF, 1.5 kΩ)	2000	—	V

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD} = 1 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 1 A	—	1	ms

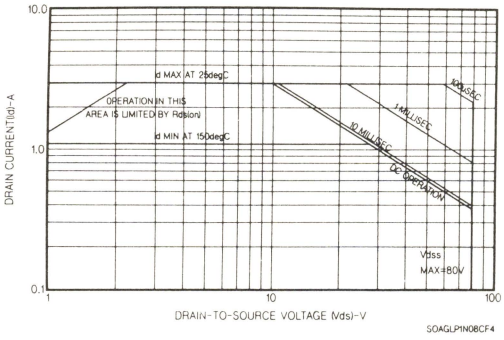


Fig. 1 - Safe-operating-area curve.

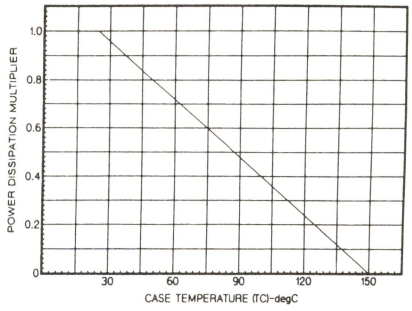


Fig. 2 - Normalized power dissipation vs. temperature derating curve.

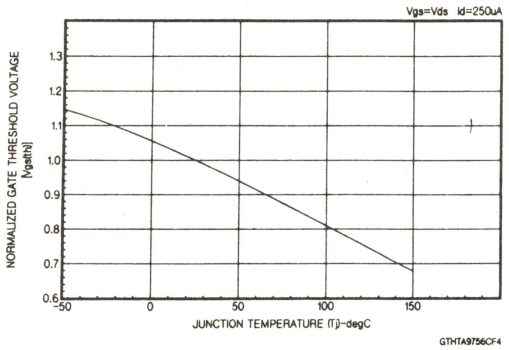


Fig. 3 - Typical normalized gate-threshold voltage.

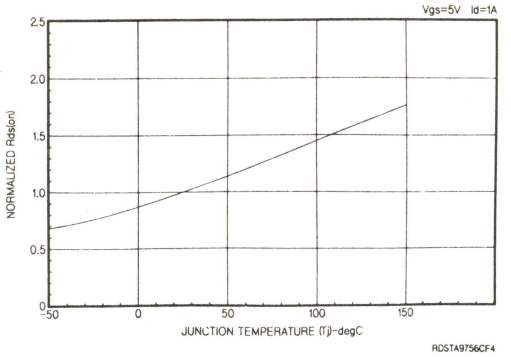


Fig. 4 - Normalized $r_{DS}(on)$ vs. junction temperature.

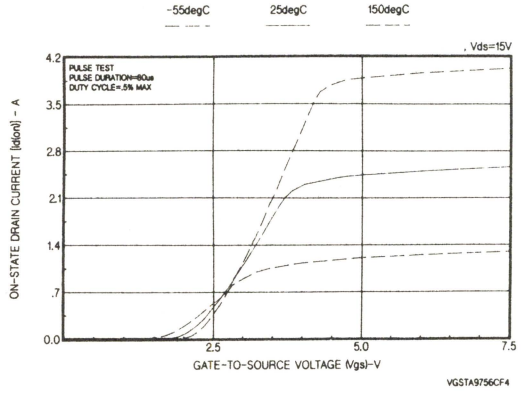


Fig. 5 - Typical transfer characteristics.

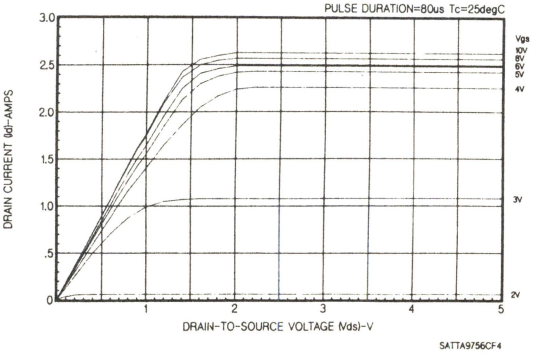


Fig. 6 - Typical saturation characteristics.

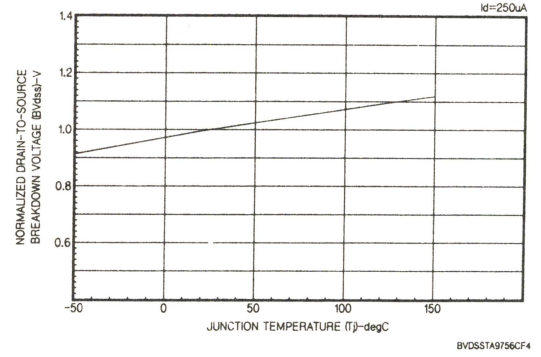


Fig. 7 - Drain-source breakdown voltage vs. temperature.

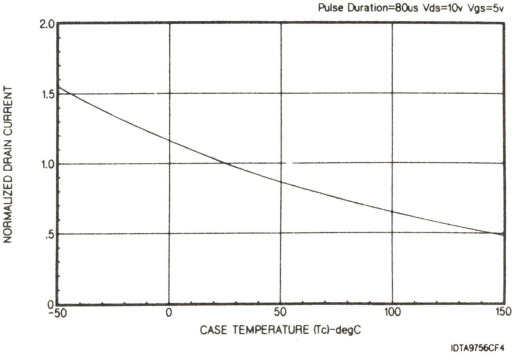


Fig. 8 - Normalized current limit vs. temperature.

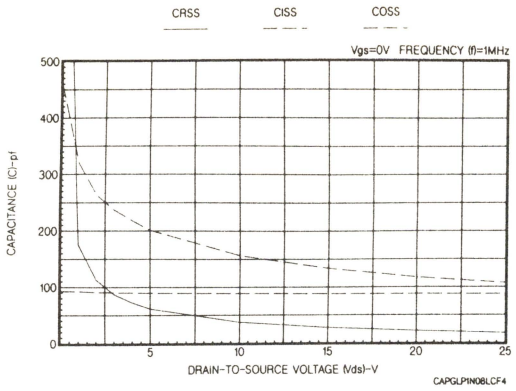
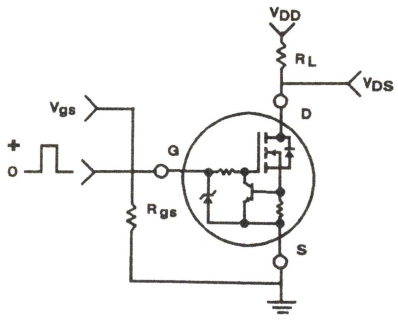


Fig. 9 - Typical capacitance vs. voltage.



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The resistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP1N08LE

The limit on drain-to-source voltage for operation in current limiting on a steady state (dc) basis is shown as Figure A. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOS devices today, is limited to 150°C. The maximum voltage allowable can, therefore, be expressed as:

$$V_{DS} = \frac{(150°C - T_{AMBIENT})}{I_{LIM} \times (R_{\theta JC} + R_{\theta CA})}$$

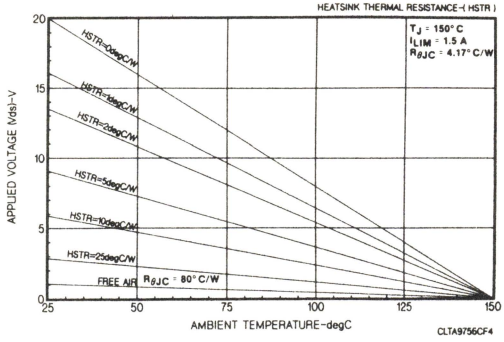


Fig. A - DC operation in current limiting.

Duty Cycle Operation of the RLP1N08LE

In many applications either the drain-to-source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N08LE is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_C = (V_{DS} \times I_D \times D \times R_{\theta CA}) + T_{AMBIENT}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 150°C and using the T_C calculated above, the expression for maximum V_{DS} under duty cycle operation is:

$$V_{DS} = \frac{150 - T_C}{I_{LIM} \times D \times R_{\theta JC}}$$

These values are plotted as Figures B1 - B5 for various heat sink thermal resistances.

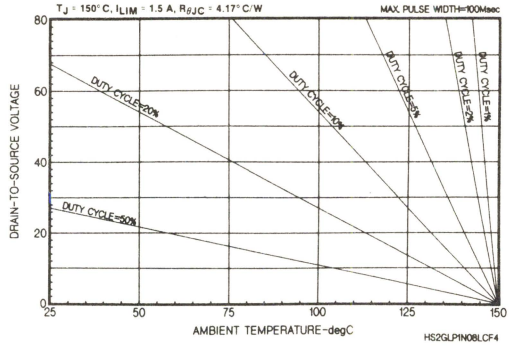


Fig. B1 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 2°C/W)

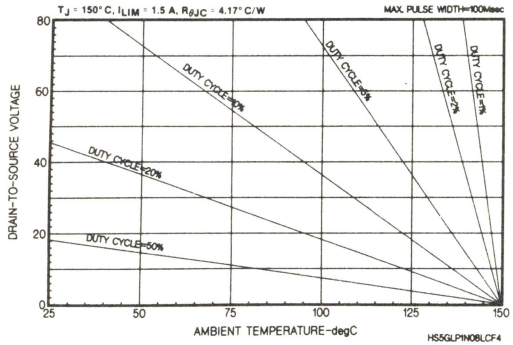


Fig. B2 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 5°C/W)

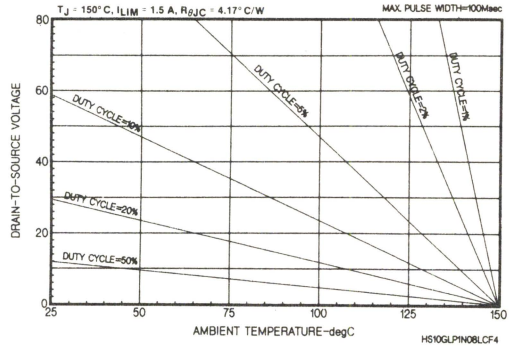


Fig. B3 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 10°C/W)

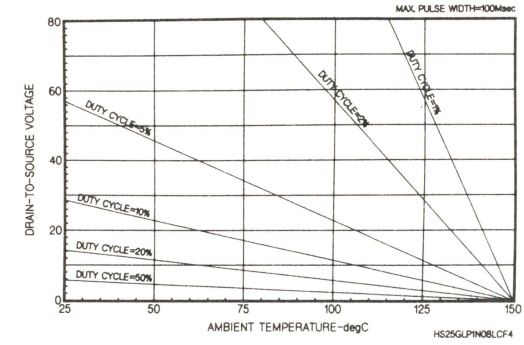


Fig. B4 - Maximum V_{DS} vs. ambient temperature in current limiting. (Heatsink thermal resistance = 25°C/W)

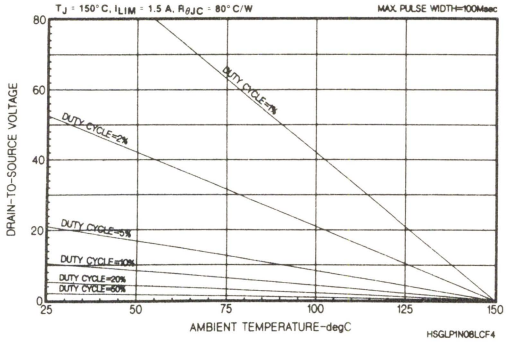


Fig. B5 - Maximum V_{DS} vs. ambient temperature in current limiting. (No external heatsink)

Limited Time Operations of the RLP1N08LE

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1 - C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 150°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

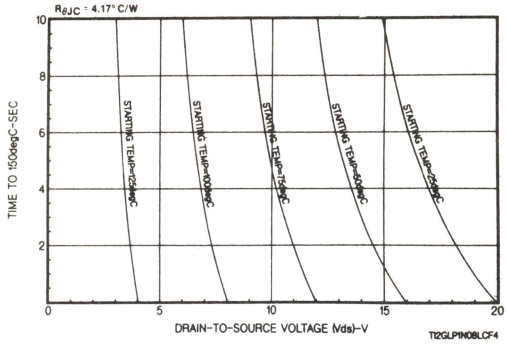


Fig. C1 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 2° C/W
Heatsink thermal capacitance = 4 j/° C)

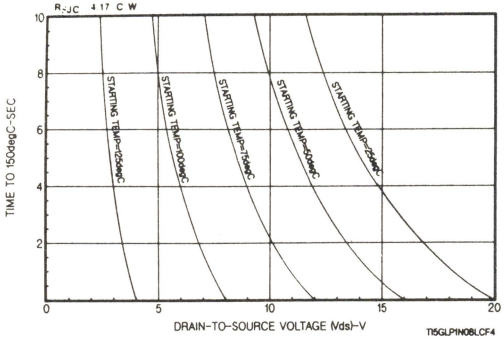


Fig. C2 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 5° C/W
Heatsink thermal capacitance = 2 j/° C)

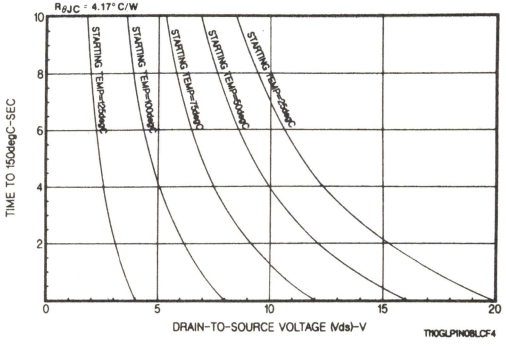


Fig. C3 - Time to 150° C in current limiting.
(Heatsink thermal resistance = 10° C/W
Heatsink thermal capacitance = 1 j/° C)

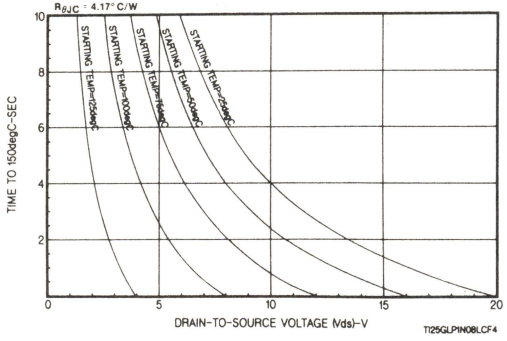


Figure C4. Time to 150°C in current limiting
(Heatsink thermal resistance = 25°C/W,
Heatsink thermal capacitance = 0.5j/°C)

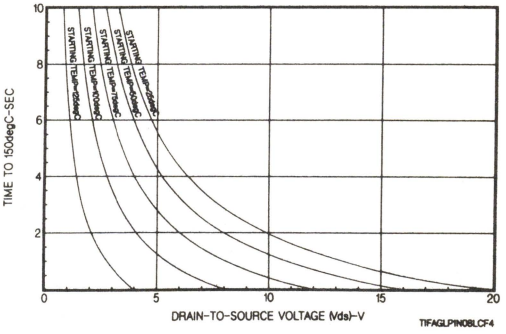


Fig. C5 - Time to 150° C in current limiting.
(No external heatsink)

Spice Model (RLP1N08LE)

```
.SUBCKT RLP1N08LE  2  1  3;  rev 09/16/91
*Nominal Temperature = 25°C
.MODEL MOSMOD NMOS (VTO=1.7  KP=2.1  IS=1e-30  N=10  TOS=1  L=1u  W=1u)
Vto  21  6  0.33
Rsource  8  7  RDSMOD  0.28
Rdrain  5  16  RDSMOD  0.2
.MODEL RDSMOD RES (TC1=7.54E-3  TC2=2.23E-5)
.MODEL RVTOMOD RES (TC1=-2.23E3  TC2=-5.29E-7)
.MODEL RVTOMOD2 RES (TC1=0  TC2=0)
Ebreak 11  7  17  18  107.3
.MODEL RBKMOD RES (TC1=1.11E-3  TC2=-6.83E-7)
.MODEL DBKMOD D (RS=2.78  TRS1=-8.88E-3  TRS2=2.55E-5)
.MODEL DBDMOD D (IS=9.91E-15  RS=3.01E-1  TRS1=3.79E-3  TRS2=1.11E-6  +CJO=4.32E-10  TT=2E-7
Cin  6  8  3.75E-10
Ca  12  8  6.5E-10
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-3  VOFF=-1)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1  VOFF=-3)
.MODEL DPLCAPMOD D (CJO=2E-10  IS=1e-30  N=10)
Cb  12  14  6.5E-10
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.65  VOFF=3.35)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.35  VOFF=-1.65)
Rgate  9  20  4.48E3
Lgate  1  9  9.5E-10
Ldrain  2  5  2.5E-9
Lsource  3  7  2.5E-9
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
MOS1  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
*Current Limiting Control Section
.MODEL RSMOD RES (TC1=3.2E-3)
Q Control 20  8  7  QMOD  10
.MODEL QMOD NPN (BF=5  VJE=0.5)
*ESD Protection
DESD  7  9  DESMOD
.MODEL DESMOD D(BV=7.185  TBV1=3.5E-4  TBV2=2.2E-6)
.ENDS
```

HARRIS

RLP5N08LE

Current Limited ESD Protected N-Channel Enhancement-Mode Power Field-Effect Transistor

May 1992

Features

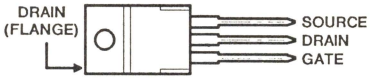
- 5.5A, 80V
- $R_{DS(ON)}$ 0.12Ω
- I_{Limit} ..... 5.5A to 8.5A at +150°C
- Built In Current Limiting
- E_{SD} Protected ..... 2KV Min
- Controlled Switching Limits EMI and RFI
- Specified For +150°C Operation
- +175°C Rated Junction Temperature
- Logic Level Gate

Description

The RLP5N08LE is an "Intelligent Discrete" monolithic power circuit which incorporates a small signal bipolar transistor, two resistors, a zener diode, and a PowerMOS transistor. Low $R_{DS(ON)}$ is achieved by the use of separate current sensing cells. Good control of the current limiting levels allows these devices to be used where it is anticipated that a shorted load condition may be encountered. "Logic Level" gates allow this device to be fully biased on with only 5.0V from gate to source. The zener diode provides E_{SD} protection of 2KV minimum.

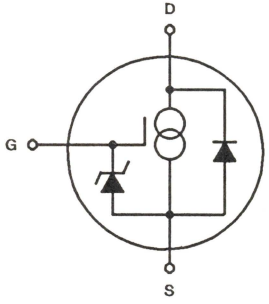
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RLP5N08LE	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage	V_{GS}	5.5	V
Reverse Voltage Gate Bias Not Allowed			
Electrostatic Voltage at 100pF, 1500Ω	ESD	2	kV
Drain Current, Continuous	I_D	Self Limited	
Power Dissipation Total @ T_C = +25°C	P_D	72	W
Power Dissipation Derating T_C > +25°C		0.48	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

7 INTELLIGENT DISCRETES

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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File Number 2493.1

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA V_{GS} = 0V	80	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS} I_D = 0.25mA	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V V_{GS} = 0V	-	1	µA
		at T_C = +150°C	-	50	µA
Gate Source Leakage Current	I_{GSS}	V_{GS} = 5V	-	1	µA
		at T_C = +150°C	-	50	µA
On Resistance	$R_{DS(ON)}$	I_D = 5.5A V_{GS} = 5.0V	-	0.12	Ω
		at T_C = +150°C	-	0.24	Ω
Limiting Current	$I_{DS(Limit)}$	V_{DS} = 15.0V V_{GS} = 5.0V	9.0	14	A
		@ T_C = 150°C	5.5	8.5	A
Turn-On Time	$t_{(ON)}$	V_{DD} = 30.0V	-	6.5	µs
Turn-On Delay Time	$t_{D(ON)}$	I_D = 5.5A	-	1.5	µs
Rise Time	t_R	V_{GS} = 5.0V	1.0	5.0	µs
Turn-Off Delay Time	$t_{D(OFF)}$	R_{GS} = 25Ω	-	10.0	µs
Fall Time	t_F	R_L = 5.45Ω	1.0	5.0	µs
Turn-Off Time	$t_{(OFF)}$		-	15.0	µs
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 7.5A V_{DS} = 15.0V	-	5.0	V
Thermal Resistance Junction to Case	$R\theta_{JC}$		-	2.083	°C/W
Thermal Resistance Junction to Ambient	$R\theta_{JC}$		-	75	°C/W
Electrostatic Voltage	E_{SD}	Human Model (100pF, 1.5kΩ) Mil-Std-883S (Category B2)	2000	-	V
SOURCE DRAIN DIODE RATINGS AND CHARACTERISTICS					
Forward Voltage	V_{SD}	I_{SD} = 5.5A	-	1.5	V
Reverse Recovery Time	T_{RR}	I_F = 5.5A	-	1.0	ms

Performance Curves

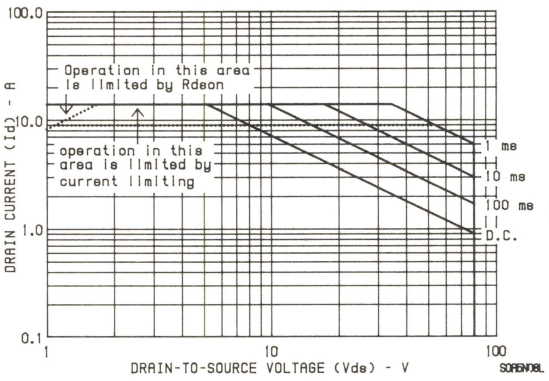

FIGURE 1. SAFE OPERATING AREA CURVE

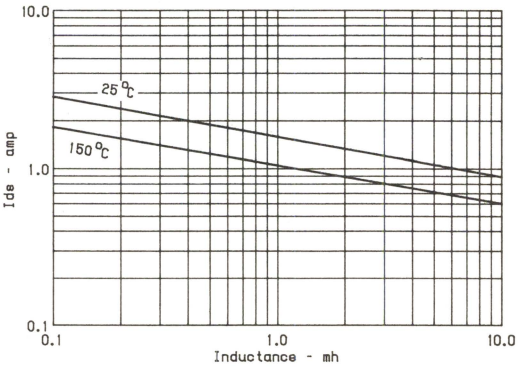

FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING SOA (SINGLE PULSE UIS SOA)

Performance Curves (Continued)

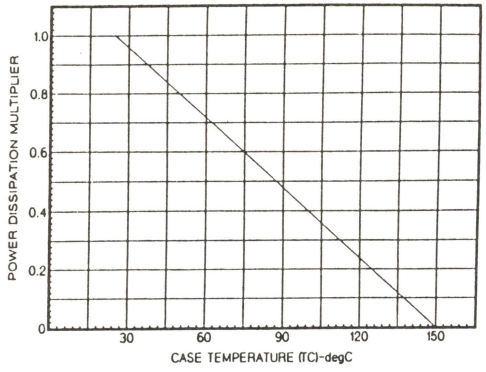

FIGURE 3. NORMALIZED POWER DISSIPATION vs. TEMPERATURE DERATING CURVE

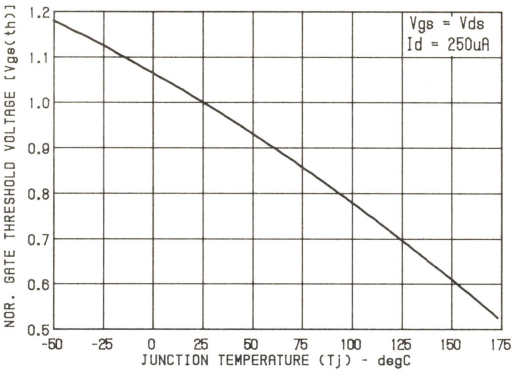

FIGURE 4. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE

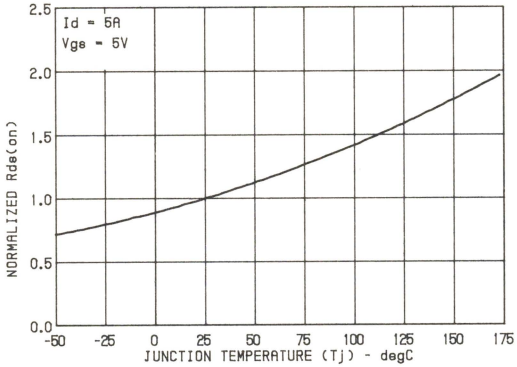

FIGURE 5. NORMALIZED $R_{DS(ON)}$ vs. JUNCTION TEMPERATURE

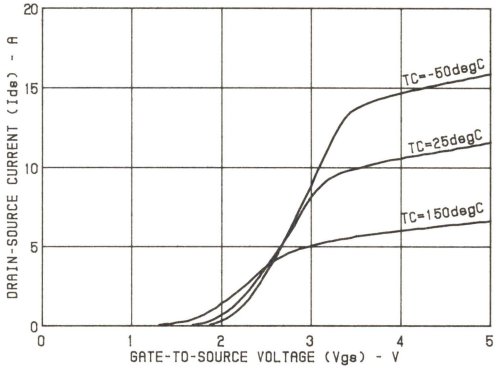

FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

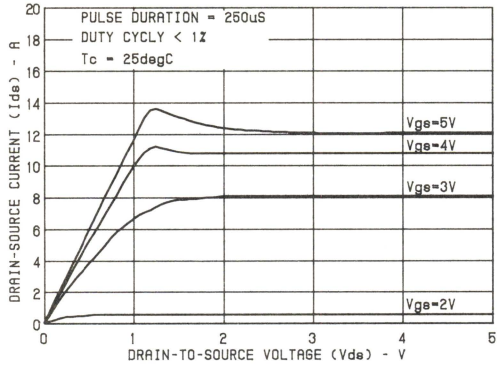

FIGURE 7. TYPICAL SATURATION CHARACTERISTICS

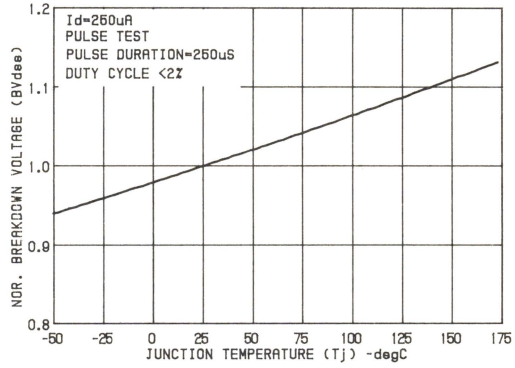

FIGURE 8. DRAIN SOURCE BREAKDOWN VOLTAGE vs. TEMPERATURE

Temperature Dependence of Current Limiting and Switching Speed Performance

The RLP5N08LE is a monolithic power device which incorporates a Logic Level PowerMOS transistor with a current sensing scheme and control circuitry to enable the device to self limit drain-source current flow. The current sensing scheme supplies current to a resistor that is connected across the base to emitter of a bipolar transistor in the control section. The collector of this bipolar transistor is connected to the gate of the PowerMOSFET. When the ratiometric current from the current sensing reaches the value required to forward bias the base-emitter

Performance Curves (Continued)

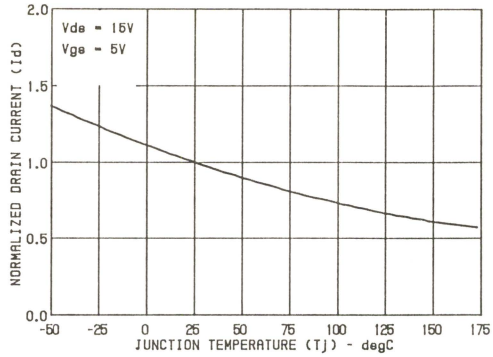

FIGURE 9. NORMALIZED CURRENT LIMIT vs. TEMPERATURE

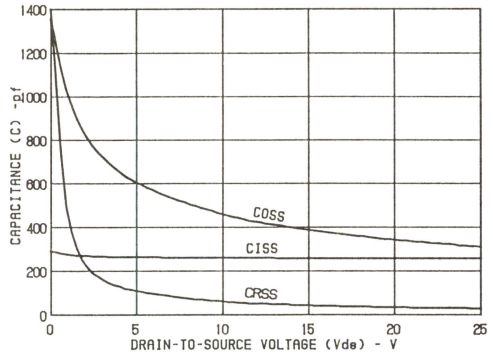

FIGURE 10. TYPICAL CAPACITANCE vs. VOLTAGE

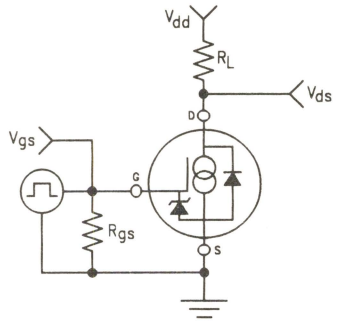

FIGURE 11. SWITCHING TEST CIRCUIT

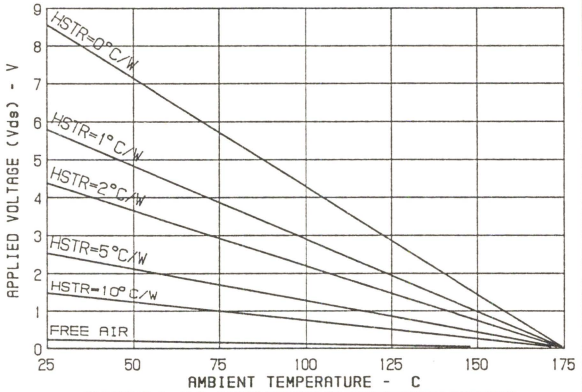

FIGURE A. DC OPERATION IN CURRENT LIMITING

junction of this bipolar transistor, the bipolar "turns-on". A resistor is incorporated in series with the gate of the PowerMOSFET allowing the bipolar transistor to adjust the drive on the gate of the PowerMOSFET to a voltage which then maintains a constant current in the PowerMOSFET. Since both the ratiometric current sensing scheme and the base-emitter junction voltage of the bipolar transistor vary with temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 9.

The resistor in series with the gate of the PowerMOSFET also results in much slower switching performance than in standard PowerMOSFETs. This is an advantage where fast switching can cause EMI or RFI. Switching speed is very predictable; a minimum as well as a maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP5N08LE

The limit of drain-to-source voltage for operation in current limiting on a steady state (DC) basis is shown in equation below. The dissipation in the device is simply the applied drain-to-source voltage multiplied by the limiting current. This device, like most PowerMOSFET devices, is limited to +175°C. The maximum voltage allowable can, therefore, be expressed as:

$$V_{DS} = \frac{+175^{o}C - T_{Ambient}}{I_{LIMIT} \times (R\theta_{JC} + HSTR)}$$

The results of this equation are plotted in Figure A for various heatsinks.

Duty Cycle Operation of the RLP5N08LE

In many applications either drain-to-source voltage or gate drive is not available 100% of the time. The copper header on which the RLP5N08LE is mounted has a very large thermal storage capability, so for pulse widths of less than 1ms header temperature can be considered a constant. Thereby, junction temperature can be calculated simply as:

$$T_J = (V_{DS} \times I_{DS} \times D \times R\theta_{J\text{-}Amb}) + T_{ambient}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to +175°C and using T_C calculated above, the expression for maximum V_{DS} under duty cycle operation is:

$$V_{DS} = \frac{+175^{o}C - T_{ambient}}{I_{LIMIT} \times D \times R\theta_{J\text{-}ambient}}$$

These values are plotted as Figures B1 - B6 for various heatsink thermal resistances.

Performance Curves (Continued)

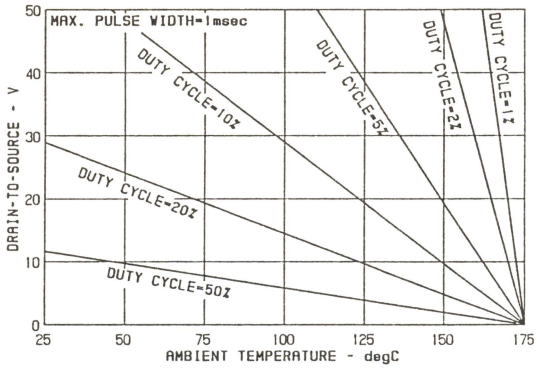

FIGURE B1. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 1°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

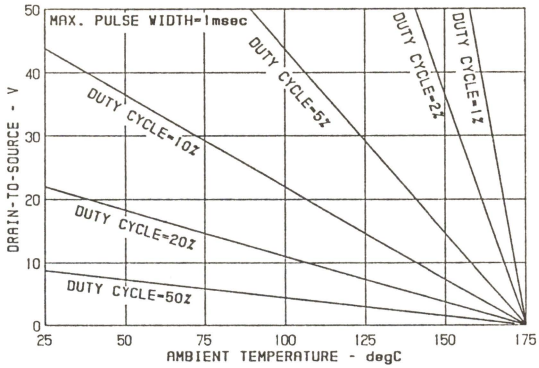

FIGURE B2. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING
(HEATSINK THERMAL RESISTANCE = 2°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

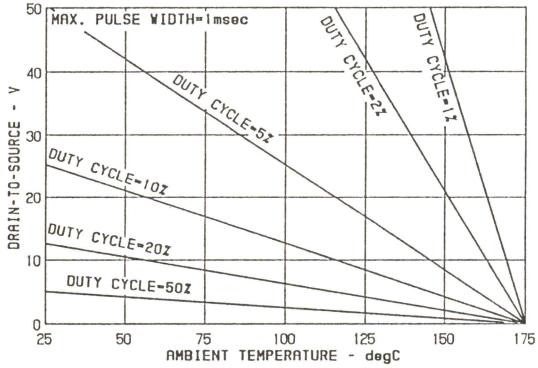

FIGURE B3. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 5°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

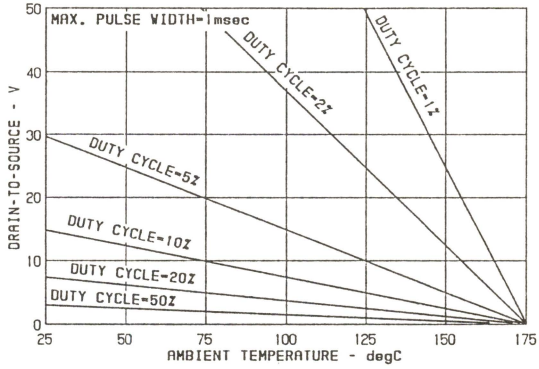

FIGURE B4. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 10°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

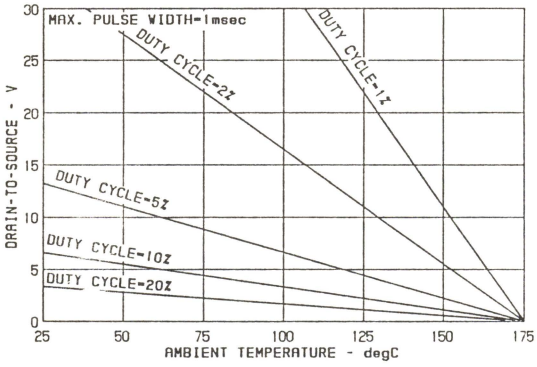

FIGURE B5. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(HEATSINK THERMAL RESISTANCE = 25°C/W)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

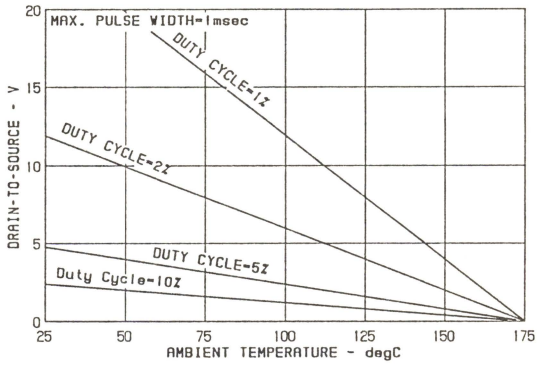

FIGURE B6. MAXIMUM V_{DS} vs. TEMPERATURE IN CURRENT LIMITING.
(NO EXTERNAL HEATSINK)
(T_J = +175°C, I_{LIMIT} = 5.5A, R_{JC} = 2.083°C/W)

Performance Curves (Continued)

Limited Time Operations of the RLP5N08LE

Protection for a limited period of time is sufficient for many applications. As previously stated, heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures C1 - C5 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified +175°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

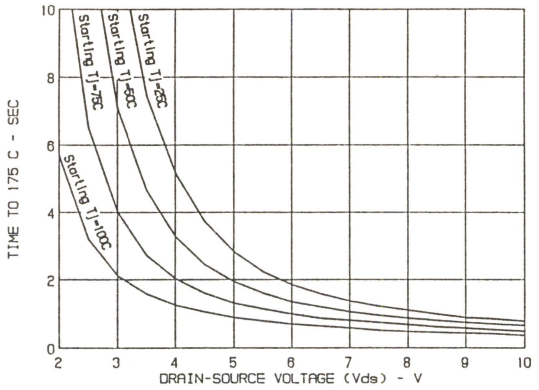

FIGURE C3. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W, HEATSINK THERMAL CAPACITANCE = 2J/°C)

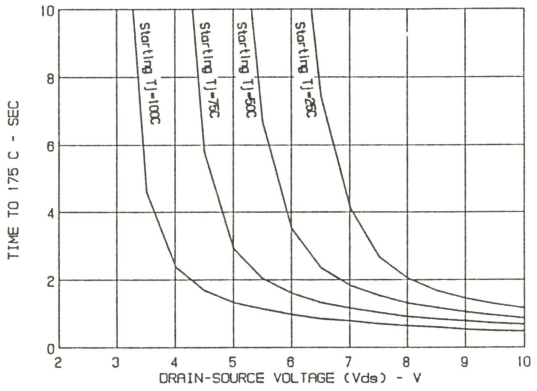

FIGURE C1. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 1°C/W, HEATSINK THERMAL CAPACITANCE = 8J/°C)

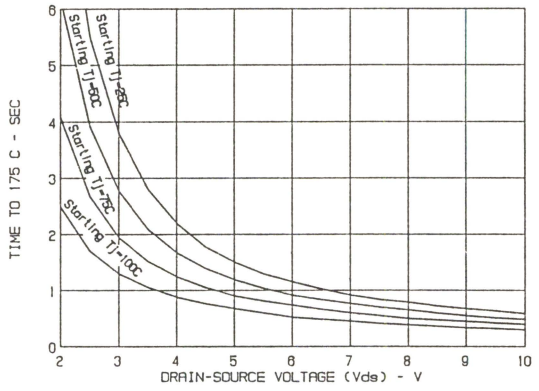

FIGURE C4. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W, HEATSINK THERMAL CAPACITANCE = 1J/°C)

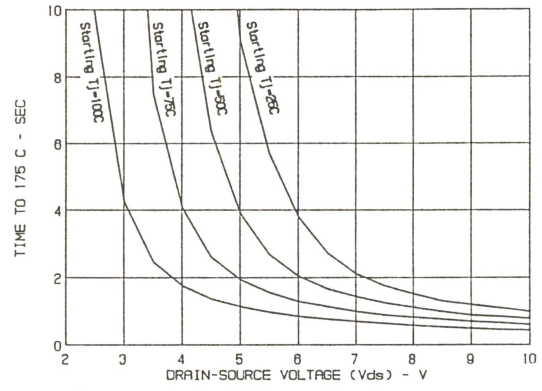

FIGURE C2. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W, HEATLINK THERMAL CAPACITANCE = 4J/°C)

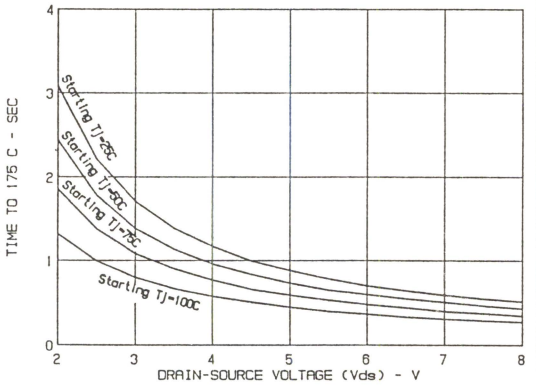

FIGURE C5. TIME TO +175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W, HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

POWER MOSFETs 8

MILITARY AND RAD-HARDENED POWER MOSFETs

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NOTE: Technical information on types listed in this section can be found in the Rad-Hard products databook DB235B or the individual datasheets

Radiation Hardened MOSFET Nomenclature System

FR X XXXX X X

HARRIS RADIATION HARDENED POWER MOSFET

PACKAGE DESIGNATION

M - TO-204AA (TO-3 with 40 mil diameter leads)
K - TO-204AE (TO-3 with 60 mil diameter leads)
L - TO-205AF (TO-39 with Low Profile Cap)
F - TO-254AA
S - TO-257AA
E - TO-258AA

DIE DESIGNATION

All Numeric Characters
N-Channel (Three Digits) - XXX
P-Channel (Four Digits) - 9XXX

RADIATION (TOTAL DOSE) ASSURANCE LEVEL

D - 10kRAD (Si)
R - 100kRAD (Si)
H - 1000kRAD (Si)

RELIABILITY SCREENING LEVEL

1 - Non-TX (Commerical)
2 - TX Equivalent of MIL-S-19500
3 - TXV Equivalent of MIL-S-19500
4 - Space Equivalent of MIL-S-19500

Features

- **Gamma**
  - **Meets Pre-Rad Specifications to 100KRAD(Si)**
  - **Defined End Point Specifications at 300KRAD(Si) and 1000KRAD(Si)**
  - **Performance Permits Limited Use to 3000KRAD(Si)**
- **Gamma Dot**
  - **Survives 3E9RAD(Si)/sec at 80% BV_{DSS} Typically**
  - **Survives 2E12 Typically if Current Limited to IDM**
- **Photo Current**
  - **3.0nA Per-RAD(Si)/sec Typically**
- **Neutron**
  - **Pre-RAD Specifications for 1E13 Neutrons/cm^2**
  - **Usable to 1E14 Neutrons/cm^2**
- **Single Event**
  - **Typically Survives 1E5 Ions/cm^2 Having an LET ≤ 35MeV/mg/cm^2 and a Range ≥ 30 m at 80% BV_{DSS}**

Description

The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000K RAD(Si) with neutron hardness ranging from 1E13n/cm^2 for 500V product to 1E14n/cm^2 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

These MOSFETs are enhancement-mode silicon-gate power field effect transistors of the vertical DMOS (VDMOS) structure. They are specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

These parts may be supplied as dies or in various packages other than shown. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the devices listed.

QPL Approved JANTX/TXV Power MOSFETs

PART NUMBER	MIL-S-19500/	LEVEL		PACKAGE	P_T (W)	I_D (A)	BV_{DSS} (V)	$R_{DS(ON)}$ (Ω)
		TX	TXV					
N-CHANNEL TYPES								
2N6756	542	X	X	TO-204AA	75	14	100	0.18
2N6758	542	X	X	TO-204AA	75	9	200	0.4
2N6760	542	X	X	TO-204AA	75	5.5	400	1.0
2N6762	542	X	X	TO-204AA	75	4.5	500	1.5
2N6764	543	X	X	TO-204AE	150	38	100	0.055
2N6766	543	X	X	TO-204AE	150	30	200	0.085
2N6768	543	X	X	TO-204AA	150	14	400	0.3
2N6770	543	X	X	TO-204AA	150	12	500	0.4
2N6782	556	X	X	TO-205AF	15	3.5	100	0.6
2N6784	556	X	X	TO-205AF	15	2.25	200	1.5
2N6786	556	X	X	TO-205AF	15	1.25	400	3.6
2N6788	555	X	X	TO-205AF	20	6	100	0.3
2N6790	555	X	X	TO-205AF	20	3.5	200	0.8
2N6792	555	X	X	TO-205AF	20	2	400	1.8
2N6794	555	X	X	TO-205AF	20	1.5	500	3.0
2N6796	557	X	X	TO-205AF	25	8	100	0.18
2N6798	557	X	X	TO-205AF	25	5.5	200	0.4
2N6800	557	X	X	TO-205AF	25	3	400	1.0
2N6802	557	X		TO-205AF	25	2.5	500	1.5
2N7224	592	X	X	TO-254AA	150	34	180	0.07
2N7225	592	X	X	TO-254AA	150	27.4	200	0.1
2N7227	592	X	X	TO-254AA	150	14	400	0.315
2N7228	592	X	X	TO-254AA	150	12	500	0.415
N-CHANNEL LOGIC LEVEL TYPES								
2N6901	570	X	X	TO-205AF	8.33	1.69	100	1.4
2N6902	566	X	X	TO-204AA	12	75	100	0.2
2N6903	570	X		TO-205AF	8.33	0.98	200	3.65
2N6904	566	X		TO-204AF	75	8	200	0.65
P-CHANNEL TYPES								
2N6895	565	X	X	TO-205AF	8.33	1.5	100	3.65
2N6896	565	X		TO-204AA	60	6	100	0.6
2N6897	565	X	X	TO-204AA	100	12	100	0.3
2N6898	565	X	X	TO-204AE	150	25	100	0.2
2N6849	564	X	X	TO-205AF	25	6.5	100	0.3
2N6851	564	X	X	TO-205AF	25	4	200	0.8

Tactical and Strategic Level Selections

Radiation Hardened MOSFETs (N-Channel)

DIE FAMILY	TO-3		TO-39		TO-254		TO-257		TO-258	
	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL
17631	FRM130D FRM130R FRM130H	2N7271	FRL130D FRL130R FRL130H	2N7272	- - -	-	FRS130D FRS130R FRS130H	2N7273	- - -	-
17632	FRM230D FRM230R FRM230H	2N7274	FRL230D FRL230R FRL230H	2N7275	- - -	-	FRS230D FRS230R FRS230H	2N7276	- - -	-
17633	FRM234D FRM234R FRM234H	2N7277	FRL234D FRL234R FRL234H	2N7278	- - -	-	FRS234D FRS234R FRS234H	2N7279	- - -	-
17635	FRM430D FRM430R FRM430H	2N7280	FRL430D FRL430R FRL430H	2N7281	- - -	-	FRS430D FRS430R FRS430H	2N7282	- - -	-
17641	FRM140D FRM140R FRM140H	2N7283	- - -	-	- - -	-	FRS140D FRS140R FRS140H	2N7284	- - -	-
17642	FRM240D FRM240R FRM240H	2N7285	- - -	-	- - -	-	FRS240D FRS240R FRS240H	2N7286	- - -	-
17643	FRM244D FRM244R FRM244H	2N7287	- - -	-	- - -	-	FRS244D FRS244R FRS244H	2N7288	- - -	-
17645	FRM440D FRM440R FRM440H	2N7289	- - -	-	- - -	-	FRS440D FRS440R FRS440H	2N7290	- - -	-
17651	FRK150D FRK150R FRK150H	2N7291	- - -	-	FRF150D FRF150R FRF150H	2N7292	- - -	-	- - -	-
17652	FRK250D FRK250R FRK250H	2N7293	- - -	-	FRF250D FRF250R FRF250H	2N7294	- - -	-	- - -	-
17653	FRK254D FRK254R FRK254H	2N7295	- - -	-	FRF254D FRF254R FRF254H	2N7296	- - -	-	- - -	-
17655	FRM450D FRM450R FRM450H	2N7297	- - -	-	FRF450D FRF450R FRF450H	2N7298	- - -	-	- - -	-
17661	FRK160D FRK160R FRK160H	2N7299	- - -	-	- - -	-	- - -	-	FRE160D FRE160R FRE160H	2N7300
17662	FRK260D FRK260R FRK260H	2N7301	- - -	-	- - -	-	- - -	-	FRE260D FRE260R FRE260H	2N7302
17663	FRK264D FRK264R FRK264H	2N7303	- - -	-	- - -	-	- - -	-	FRE264D FRE264R FRE264H	2N7304
17665	FRK460D FRK460R FRK460H	2N7305	- - -	-	- - -	-	- - -	-	FRE460D FRE460R FRE460H	2N7306

Radiation Hardened MOSFETs (P-Channel)

DIE FAMILY	TO-3		TO-39		TO-254		TO-257		TO-258	
	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL	INTERIM	FINAL
17731	FRM9130D FRM9130R FRM9130H	2N7307	FRL9130D FRL9130R FRL9130H	2N7308	- - -	-	FRS9130D FRS9130R FRS9130H	2N7309	- - -	-
17732	FRM9230D FRM9230R FRM9230H	2N7310	FRL9230D FRL9230R FRL9230H	2N7311	- - -	-	FRS9230D FRS9230R FRS9230H	2N7312	- - -	-
17741	FRM9140D FRM9140R FRM9140H	2N7316	- - -	-	- - -	-	FRS9140D FRS9140R FRS9140H	2N7317	- - -	-
17742	FRM9240D FRM9240R FRM9240H	2N7318	- - -	-	- - -	-	FRS9240D FRS9240R FRS9240H	2N7319	- - -	-
17751	FRK9150D FRK9150R FRK9150H	2N7322	- - -	-	FRF9150D FRF9150R FRF9150H	2N7323	- - -	-	- - -	-
17752	FRM9250D FRM9250R FRM9250H	2N7324	- - -	-	FRF9250D FRF9250R FRF9250H	2N7325	- - -	-	- - -	-
17761	FRK9160D FRK9160R FRK9160H	2N7328	- - -	-	-	-	- - -	-	FRE9160D FRE9160R FRE9160H	2N7329
17762	FRK9260D FRK9260R FRK9260H	2N7330	- - -	-	-	-	- - -	-	FRE9260D FRE9260R FRE9260H	2N7331

Pre-Post Radiation Characteristics

N-Channel

RATED BV_{DSS}	PART NUMBER	PACKAGE OUTLINE (TO-)	PRE-RADIATION RATINGS			POST 10K RAD OR POST 100K RAD (Si) RATINGS			POST 1M RAD (Si) RATINGS		
			I_D (A)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)	BV_{DSS} (V)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)	BV_{DSS} (V)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)
100	2N7271	204AA	14	0.180	2 - 4	100	0.180	2 - 4	95	0.270	1.5 - 4.5
	2N7272	205AF	8	0.180	2 - 4	100	0.180	2 - 4	95	0.270	1.5 - 4.5
	2N7273	257AA	12	0.195	2 - 4	100	0.195	2 - 4	95	0.293	1.5 - 4.5
	2N7283	204AA	23	0.130	2 - 4	100	0.130	2 - 4	95	0.200	1.5 - 4.5
	2N7284	257AA	17	0.145	2 - 4	100	0.145	2 - 4	95	0.218	1.5 - 4.5
	2N7291	204AE	40	0.055	2 - 4	100	0.055	2 - 4	95	0.083	1.5 - 4.5
	2N7292	254AA	25	0.070	2 - 4	100	0.070	2 - 4	95	0.105	1.5 - 4.5
	2N7299	204AE	50	0.040	2 - 4	100	0.040	2 - 4	95	0.060	1.5 - 4.5
	2N7300	258AA	41	0.050	2 - 4	100	0.050	2 - 4	95	0.075	1.5 - 4.5
200	2N7274	204AA	8	0.500	2 - 4	200	0.500	2 - 4	190	0.750	1.5 - 4.5
	2N7275	205AF	5	0.500	2 - 4	200	0.500	2 - 4	190	0.750	1.5 - 4.5
	2N7276	257AA	7	0.515	2 - 4	200	0.515	2 - 4	190	0.773	1.5 - 4.5
	2N7285	204AA	16	0.240	2 - 4	200	0.240	2 - 4	190	0.360	1.5 - 4.5
	2N7286	257AA	12	0.255	2 - 4	200	0.255	2 - 4	190	0.383	1.5 - 4.5
	2N7293	204AE	27	0.100	2 - 4	200	0.100	2 - 4	190	0.140	1.5 - 4.5
	2N7294	254AA	23	0.115	2 - 4	200	0.115	2 - 4	190	0.161	1.5 - 4.5
	2N7301	204AE	46	0.070	2 - 4	200	0.070	2 - 4	190	0.105	1.5 - 4.5
	2N7302	258AA	31	0.080	2 - 4	200	0.080	2 - 4	190	0.120	1.5 - 4.5
250	2N7277	204AA	7	0.700	2 - 4	250	0.700	2 - 4	238	1.000	1.5 - 4.5
	2N7278	205AF	4	0.700	2 - 4	250	0.700	2 - 4	238	1.000	1.5 - 4.5
	2N7279	257AA	5	0.715	2 - 4	250	0.715	2 - 4	238	1.070	1.5 - 4.5
	2N7287	204AA	12	0.400	2 - 4	250	0.400	2 - 4	238	0.600	1.5 - 4.5
	2N7288	257AA	9	0.415	2 - 4	250	0.415	2 - 4	238	0.623	1.5 - 4.5
	2N7295	204AE	20	0.170	2 - 4	250	0.170	2 - 4	238	0.215	1.5 - 4.5
	2N7296	254AA	17	0.185	2 - 4	250	0.185	2 - 4	238	0.234	1.5 - 4.5
	2N7303	204AE	34	0.120	2 - 4	250	0.120	2 - 4	238	0.180	1.5 - 4.5
	2N7304	258AA	23	0.130	2 - 4	250	0.130	2 - 4	238	0.195	1.5 - 4.5
500	2N7280	204AA	3	2.500	2 - 4	500	2.500	2 - 4	475	3.750	1.5 - 4.5
	2N7281	205AF	2	2.500	2 - 4	500	2.500	2 - 4	475	3.750	1.5 - 4.5
	2N7282	257AA	3	2.520	2 - 4	500	2.520	2 - 4	475	3.780	1.5 - 4.5
	2N7289	204AA	6	1.400	2 - 4	500	1.400	2 - 4	475	2.100	1.5 - 4.5
	2N7290	257AA	5	1.420	2 - 4	500	1.420	2 - 4	475	2.130	1.5 - 4.5
	2N7297	204AA	10	0.600	2 - 4	500	0.600	2 - 4	475	0.860	1.5 - 4.5
	2N7298	254AA	9	0.615	2 - 4	500	0.615	2 - 4	475	0.879	1.5 - 4.5
	2N7305	204AE	17	0.400	2 - 4	500	0.400	2 - 4	475	0.600	1.5 - 4.5
	2N7306	258AA	12	0.410	2 - 4	500	0.410	2 - 4	475	0.615	1.5 - 4.5

Pre-Post Radiation Characteristics (Continued)

P-Channel

RATED BV_{DSS}	PART NUMBER	PACKAGE OUTLINE (TO-)	PRE RADIATION RATINGS			POST 10K RAD OR POST 100K RAD (Si) RATINGS			POST 1M RAD (Si) RATINGS		
			I_D (A)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)	BV_{DSS} (V)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)	BV_{DSS} (V)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (V)
100	2N7307	204AA	6	0.550	2 - 4	100	0.550	2 - 4	95	0.830	2 - 6
	2N7308	205AF	5	0.550	2 - 4	100	0.550	2 - 4	95	0.830	2 - 6
	2N7309	257AA	6	0.565	2 - 4	100	0.565	2 - 4	95	0.848	2 - 6
	2N7316	204AA	11	0.300	2 - 4	100	0.300	2 - 4	95	0.450	2 - 6
	2N7317	257AA	11	0.315	2 - 4	100	0.315	2 - 4	95	0.473	2 - 6
	2N7322	204AE	26	0.125	2 - 4	100	0.125	2 - 4	95	0.188	2 - 6
	2N7323	254AA	23	0.140	2 - 4	100	0.140	2 - 4	95	0.210	2 - 6
	2N7328	204AE	40	0.085	2 - 4	100	0.085	2 - 4	95	0.128	2 - 6
	2N7329	258AA	30	0.095	2 - 4	100	0.095	2 - 4	95	0.143	2 - 6
200	2N7310	204AA	4	1.300	2 - 4	200	1.300	2 - 4	190	1.950	2 - 6
	2N7311	205AF	3	1.300	2 - 4	200	1.300	2 - 4	190	1.950	2 - 6
	2N7312	257AA	4	1.320	2 - 4	200	1.320	2 - 4	190	1.980	2 - 6
	2N7318	204AA	7	0.720	2 - 4	200	0.720	2 - 4	190	1.080	2 - 6
	2N7319	257AA	7	0.735	2 - 4	200	0.735	2 - 4	190	1.100	2 - 6
	2N7324	204AA	16	0.300	2 - 4	200	0.300	2 - 4	190	0.450	2 - 6
	2N7325	254AA	14	0.315	2 - 4	200	0.315	2 - 4	190	0.473	2 - 6
	2N7330	204AE	26	0.200	2 - 4	200	0.200	2 - 4	190	0.300	2 - 6
	2N7331	258AA	19	0.210	2 - 4	200	0.210	2 - 4	190	0.315	2 - 6

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PREVIEW PRODUCTS

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HARRIS

RFD3N08L
RFD3N08LSM

N-Channel Logic Level Power Field Effect Transistors

August 1991

Features

- 3A, 80V
- $R_{DS(on)} = 0.80\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly From Q-MOS, N-MOS, or TTL Circuits
- SOA is Power-Dissipation Limited
- 175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

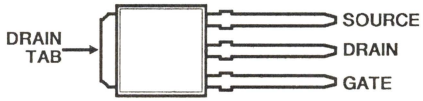
Description

The RFD3N08L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

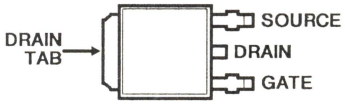
The RFD3N08L is supplied in the JEDEC TO-251 plastic package and the RFD3N08LSM is supplied in the JEDEC TO-252 plastic package.

Packages

TO-251AA
TOP VIEW

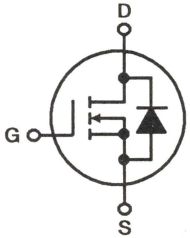


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 80V
Drain-Gate Voltage, ($R_{GS} = 1m\Omega$), V_{DGR} 80V
Gate-Source Voltage, V_{GS} ..... ±10V
Drain Current:
  RMS Continuous, I_D 3A
  Pulsed, I_{DM} 7A
Power Dissipation, P_D:
  $T_C = +25^oC$ 30W
  Derate Above $T_C = +25^oC$ ..... 0.20W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG} ..... -55 to +175°C

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PREVIEW PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.
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File Number 2836

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V		80	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA		1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 70V		–	1	μA
		V_{DS} = 70V @ T_C = 125°C		–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 10V, V_{DS} = 0V		–	100	nA
Drain-Source on Voltage	$V_{DS(on)}$	I_D = 1.5A, V_{GS} = 5V		–	1.2	Ω
		I_D = 3A, V_{GS} = 5V		–	2.5	V
On Resistance	$R_{DS(on)}$	I_D = 1.5A, V_{GS} = 5V		–	0.8	Ω
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to 10V	V_{DD} = 48V	–	8	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0 to 5V	I_D = 2A	–	5	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to 1V	R_L = 24Ω	–	1	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 3A, V_{DS} = 15V		–	4.5	V
Turn-On Delay Time	$t_{D(on)}$	V_{DD} = 40V, I_D = 1A		–	20	ns
Rise Time	t_R	R_G = 6.25V, V_{GS} = 5V		–	130	ns
Turn-Off Delay Time	$t_{D(off)}$			–	40	ns
Fall Time	t_F			–	160	ns
Thermal Resistance, Junction to Case	$R_{\theta JC}$			–	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 1A	–	1.4	V
Reverse Recovery Time	t_{rr}	I_f = 2A, di_f/dt = 100A/μs	–	150(typ.)	ns

HARRIS

RFD4N06L
RFD4N06LSM

N-Channel Logic Level Power Field Effect Transistors

August 1991

Features

- 4A, 60V
- $R_{DS(on)} = 0.60\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly From Q-MOS, N-MOS, or TTL Circuits
- SOA is Power-Dissipation Limited
- 175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

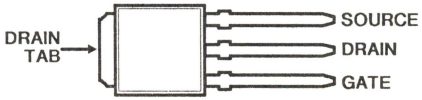
Description

The RFD4N06L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

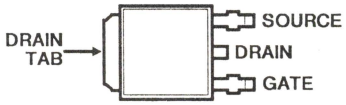
The RFD4N06L is supplied in the JEDEC TO-251 plastic package and the RFD4N06LSM is supplied in the JEDEC TO-252 plastic package.

Packages

TO-251AA
TOP VIEW

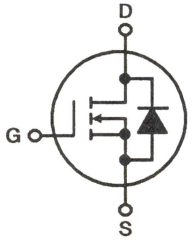


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^oC$), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS} 60V
Drain-Gate Voltage, V_{DSS} 60V
Gate-Source Voltage, V_{GS} ..... ±10V
Drain Current:
  RMS Continuous, I_D 4A
  Pulsed, I_{DM} 10A
Power Dissipation, P_D:
  $T_C = +25^oC$ 30W
  Derate Above $T_C = +25^oC$ ..... 0.20W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG} ..... -55 to +175°C

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PREVIEW PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.
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File Number 2837

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS MIN	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V		60	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA		1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50V		-	1	μA
		V_{DS} = 50V @ T_C = 125°C		-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 10V, V_{DS} = 0V		-	100	nA
Drain-Source on Voltage	$V_{DS(on)}$	I_D = 1A, V_{GS} = 5V		-	0.8	V
		I_D = 2A, V_{GS} = 5V		-	2.0	V
		I_D = 4A, V_{GS} = 7.5V		-	4.0	V
On Resistance	$R_{DS(on)}$	I_D = 1A, V_{GS} = 5V		-	0.6	Ω
Total Gate Charge	$Q_{g(total)}$	V_{GS} = 0 to 10V	V_{DD} = 48V	-	8	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0 to 5V	I_D = 2A	-	5	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to 1V	R_L = 24Ω	-	1	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 4A, V_{DS} = 15V		-	4.5	V
Turn-On Delay Time	$t_{D(on)}$	V_{DD} = 30V, I_D = 1A		-	20	ns
Rise Time	t_R	R_G = 6.25V, V_{GS} = 5V		-	130	ns
Turn-Off Delay Time	$t_{D(off)}$			-	40	ns
Fall Time	t_F			-	160	ns
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	5	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS MAX.	UNITS
Forward Voltage	V_{SD}	I_{SD} = 1A	-	1.4	V
Reverse Recovery Time	t_{rr}	I_f = 2A, di_f/dt = 100A/μs	-	150(typ.)	ns

HARRIS

RFP15N08L

N-Channel Logic Level Power Field-Effect Transistor

August 1991

Features

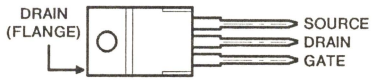
- 15A, 80V
- $R_{DS(ON)}$: 0.14Ω
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly from Q-MOS, N-MOS, TTL Circuits
- SOA is Power-Dissipation Limited
- +175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

Description

The RFP15N08L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

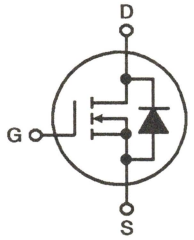
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP15N08L	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current, RMS Continuous	I_D	15	A
Pulsed	I_{DM}	40	A
Power Dissipation Total @ T_C = +25°C	P_D	72	W
Power Dissipation Derating T_C = +25°C		0.48	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

9 PREVIEW PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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File Number 2840

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA	V_{GS} = 0V	80	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}	I_D = 1mA	1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V		-	1	μA
		V_{DS} = 65V	at T_C = +125°C	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V	V_{DS} = 0V	-	100	nA
Drain-Source On Voltage	$V_{DS(ON)}$	I_D = 7.5A	V_{GS} = 5V	-	1.05	V
		I_D = 15A	V_{GS} = 5V	-	3.0	V
On Resistance	$R_{DS(ON)}$	I_D = 7.5A	V_{GS} = 5V	-	0.14	Ω
Total Gate Charge	$Q_{G(TOTAL)}$	V_{GS} = 0-10V	V_{DD} = 64V	-	80	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0-5V	I_D = 15A	-	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0-1V	R_L = 4.27Ω	-	3	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D =15A	V_{DS} =15V	-	4.5	V
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 40V	I_D = 7.5A	-	40	ns
Rise Time	t_r	R_G = 6.25Ω	V_{GS} = 5V	-	325	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	325	ns
Fall Time	t_f			-	325	ns
Thermal Resistance Junction to Case	$R\theta_{JC}$	-		-	2.083	°C/W

Source-Drain Diode Ratings and Characteristics

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 7.5A	-	1.4	V
Reverse Recovery Time	T_{RR}	I_F = 4A, di_f/dt = 100a/μs	-	225(typ)	ns

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SPICE MODELS

SPICE MODELS		PAGE
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AN9209	A Spice-2 Subcircuit Representation For Power MOSFETs, Using Empirical Methods	10-11
AN9210	A New PSpice Subcircuit For The Power MOSFET Featuring Global Temperature Options	10-15
SPICE MODEL CKT FILE		10-27

APPNOTE

No. AN8610.1 February 1994

SPICING-UP SPICE II SOFTWARE FOR POWER MOSFET MODELING

Author: C.F. Wheatley, Jr., H.R. Ronan, Jr., G.M. Dolny

The SPICE II simulation software package is familiar to most designers working in computer-aided design of integrated circuits. Developed by L. W. Nagel in 1973, SPICE II has become a widely available, well-understood design tool for IC modeling and analysis. But, SPICE II has a shortcoming: its standard simulation programs were developed when all MOSFETs were low-power devices. Power MOS devices are growing in use today, both as discrete components and, potentially, as output stages of power integrated circuits. SPICE II in its current form doesn't recognize these new developments. Its built-in FET models aren't able to simulate all the modes of new power MOS device operation. For example, SPICE II doesn't recognize the way a power MOSFET's internal capacitances change with bias conditions, the presence of a cascode JFET that complicates both static and dynamic operation, or the presence of a parasitic body diode that affects operation in the third quadrant. Without this information, SPICE II will predict power MOSFET performance that is incorrect.

Since SPICE II's internal device models can't be easily changed for all existing copies, we looked for another approach to update the capabilities of this widely used simulation package in its standard form. Adding a "subcircuit" of external components that complement the devices within the SPICE II software, so as to form a true, equivalent circuit of a power MOSFET, is the answer.

The subcircuit works nicely with the standard SPICE II software, providing a model with all the terminal characteristics of a power MOSFET. Parameters of the subcircuit model can be determined from simple terminal measurements or from standard data sheets, using the algorithmic and empirical approach described below. Once these parameters are in place, SPICE II can be used to accurately simulate either p-channel or n-channel power MOSFET devices over a wide range of currents and voltages. The subcircuit functions as an embedded subroutine, so it can be used repetitively for any number of power MOSFETs in a design. This technique can be used to model power MOSFETs with any version of the SPICE II program presently available, without any modifications to its internal source code. The technique can also be used with other commercially available or in-house-developed circuit simulators.

Modeling The Power MOSFET

A cross-sectional view of a cell of a Harris IRF130 power MOSFET is shown in Figure 1. The easiest way to understand its electrical characteristics is to think of it as a vertical JFET, driven in cascode from a low-voltage lateral MOSFET.[1, 2] When the gate is positively biased with respect to the n-bulk, an accumulation layer forms in the n-region beneath the gate. This layer acts as the drain of the lateral MOSFET, as well as the source of the vertical JFET. The JFET channel is then-region between the two p-type body diffusions, which act as the gate of the JFET. The JFET drain is the n+ bulk, usually thought of as the power MOSFET drain.

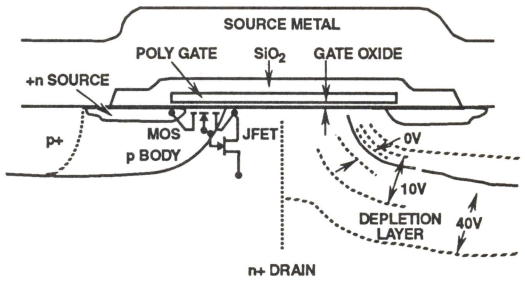

FIGURE 1. A CROSS-SECTIONAL VIEW SHOWS THE PHYSICAL MAKEUP OF THE LATERAL LOW-VOLTAGE MOSFET AND VERTICAL JFET THAT OPERATE IN CASCODE AS THE POWER MOSFET.

When you look at the power MOSFET this way, it becomes possible to use the standard SPICE II built-in device models, because SPICE II can simulate both the vertical JFET and the lateral MOSFET. When we use the subcircuit to add the rest of the Harris IRF130 power MOSFET to these SPICE II-simulated devices, we get a satisfactory equivalent circuit, shown in Figure 2.

The gate-to-source capacitance of the Harris IRF130 power MOSFET is represented by C_{21}. It is really a composite of two capacitances. The first is formed between the polysilicon gate and source metal (with the thick oxide as a dielectric). The second is formed between the gate and the n+ source (with the thin oxide acting as the dielectric). The value of C_{21} is essentially unchanged by voltage or current.

Capacitor C_{24} is formed between the power MOSFET gate and the accumulation layer, with the thin gate oxide as a dielectric. So long as the gate is positive with respect to the n-neck region, the accumulation layer exists and C_{24} doesn't

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change. But, if the external drain voltage (less their voltage drop across then-drift region) approaches the gate voltage, the accumulation layer starts to disappear. When that happens, C_{24} abruptly drops in value. This sudden change has to be taken into consideration.

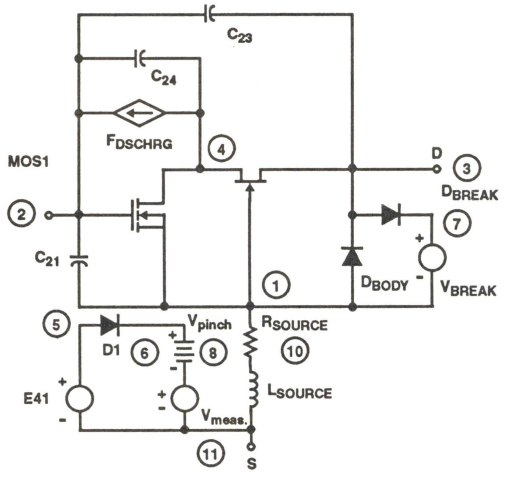

FIGURE 2. THE EQUIVALENT CIRCUIT OF THE POWER MOSFET IS MADE BY COMBINING SPICE II MODEL ELEMENTS WITH SOFTWARE SPECIFIED COMPONENTS ON A "SUBCIRCUIT."

Capacitor C_{23} represents the gate-to-drain capacitance of the Harris IRF130 power MOSFET. Because the accumulation layer normally acts as an electrostatic shield, C_{23} has no significance until the layer ceases to exist under the conditions just described. When it does disappear, the effect upon C_{23} is abrupt, and also has to be taken into consideration. The sudden changes in C_{24} and C_{23} cannot be easily modeled with the standard SPICE II software.

Figure 2 illustrates what happens: If the JFET source voltage (node 4) is very low compared to its pinch-off voltage, the JFET will be highly conductive, tightly coupling C_{24} to the JFET drain (which is also the drain of the Harris IRF130 power MOSFET). However, as the node 4 voltage approaches the pinch-off voltage (V_{PINCH}) of the JFET, it operates in a constant-current mode. This action decouples C_{24} from the JFET drain, making possible a much faster slew-rate, determined by C_{23}. If the node 4 voltage is allowed to exceed V_{PINCH} of the JFET, errors will exist in the output waveforms predicted by the standard SPICE II model.

To correct the situation, the added subcircuit includes a current-controlled current source, F_{DSCHRG}, and a current-sense network containing D1. If node 4 voltage begins to exceed V_{PINCH} of the JFET, D1 conducts, and its current is sensed at V_{MEAS}. The high-gain current source F_{DSCHRG} is turned-on rapidly and partially discharges C_{24}, pinning node 4 voltage at the pinch-off voltage of the JFET. In setting up the parameters of the subcircuit, the ideality factor of D1 is set at 0.03 to assure that node 4 voltage will never exceed V_{PINCH} of the JFET by more than a few millivolts. This condition results in waveform predictions from the SPICE II model that represent the true characteristics of the power MOSFET.

The body diode (D_{BODY} in Figure 2) is formed by the drain-to-body diffusion pn junction of the Harris IRF130 power MOSFET. D_{BODY} is added as an external component in the subcircuit because the built-in gate-to-drain diode of the SPICE II JFET model is inconvenient when it comes to modeling third-quadrant conduction of a power MOSFET. We want most of the third-quadrant current to flow in D_{BODY}. So, we effectively delete the SPICE II model's built-in diode by setting its saturation current parameter to an artificially low value, such as 10^{-20} ampere.

To round-out the subcircuit, a resistor value is chosen for the JFET drain of the SPICE II model to represent the series resistance of the n-drain region of the Harris IRF130 power MOSFET.[3] We also add resistor R_{SOURCE} to represent the series source resistance of the Harris IRF130 power MOSFET: a composite of resistances in the n+ source region, contact resistance, and source-metal series resistance. Finally, we add inductor L_{SOURCE} to represent the source inductance of the power MOSFET contributed by the source metallization and bond wires.

Choosing Parameters to Simulate A Power MOSFET

To accurately simulate the terminal characteristics of the physical power MOSFET you are working with, you will need to adjust the SPICE II model parameters and select subcircuit component values. Look first at adjustment of the SPICE II model. The static current-voltage characteristics of the power MOSFET are determined by the low-voltage lateral MOSFET included in the SPICE II model; Figure 2. In saturation (large values of V_{DS}), the lateral MOSFET device is modeled according to the following equation:

$$I_{DS} = \frac{(K_P)W\,(V_{GS} - V_{TO})^2}{2L}$$

where

K_P = Process Transconductance Parameter

V_{TO} = Threshold Voltage

W = L = 1μm (Fixed In This Note For Convenience)

I_{DS} = MOSFET Drain Current

V_{GS} = MOSFET Gate-To-Source Voltage

Continuing with the example device, the Harris IRF130 power MOSFET, a plot of the square root of I_{DS} versus gate voltage (V_{GS}) provides the curves shown in Figure 3 for V_{DS} = 10 volts. These curves provide the process transconductance parameter, $(K_P/2)^{0.5}$, and threshold voltage, V_{TO}, directly. This data can then be used to find the value of source resistance, R_{SOURCE}. This series resistance is important because it causes the curve produced by plotting the square root of I_{DS} versus V_{GS} to depart from linearity at high current levels. Departure at very low current levels is caused by subthreshold conduction, which we ignore in this model.

To find the JFET drain resistance, we use the value of source resistance, R_{SOURCE}, and plots of I_{DS} versus V_{DS} for operation in the linear region, as shown in Figure 4.

To find the current, resistance and capacitance parameters of the body diode (D_{BODY} in Figure 2), first plot log I_{DS} versus V_{DS}, as shown in Figure 5, holding the gate voltage, V_{GS}, negative for third-quadrant operation; i.e., where V_{DS} is less than 0. This plot gives the saturation current and resistance of D_{BODY}. The minority-carrier transit-time parameter (TT) of the SPICE II program is chosen to provide the best fit to measured transient reverse-recovery data. The junction capacitance value of D_{BODY} is equal to the power MOSFET device output capacitance, C_{OSS}, at zero volts. This value can be obtained from the device data sheet, or by bridge measurement. It is usually specified at 25 volts, and may be converted to zero volts by multiplying by 6.

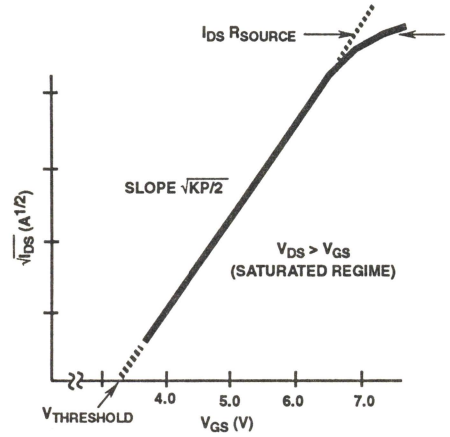

FIGURE 3. THIS PLOT OF THE SQUARE ROOT OF DRAIN CURRENT vs. GATE VOLTAGE DEFINES THE THRESHOLD VOLTAGE, V_{TO}, $(K_P/2)^{0.5}$, AND R_{source}, FOR THE POWER MOSFET.

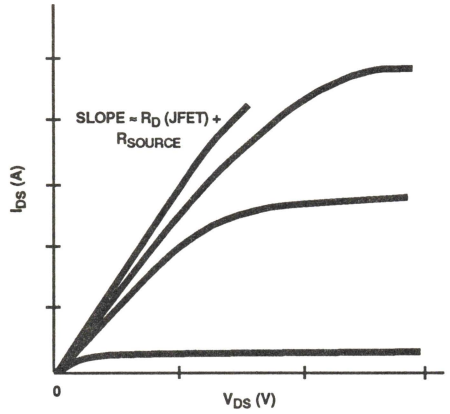

FIGURE 4. DRAIN CURRENT vs. DRAIN VOLTAGE OF THE POWER MOSFET PLOTTED USING CONSTANT GATE VOLTAGES. THIS CURVE DEFINES THE ON RESISTANCE OF THE DEVICE.

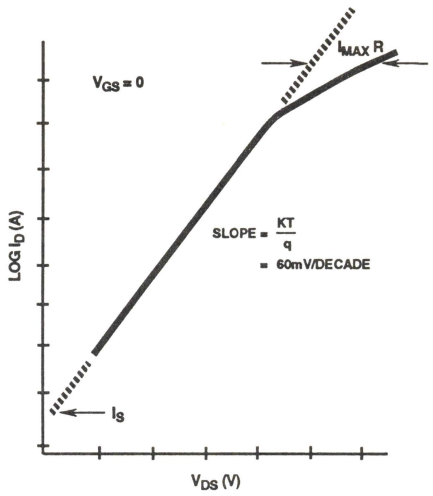

FIGURE 5. THIS PLOT OF LOG I_D VS V_{DS} IN THIRD-QUADRANT OPERATION OF THE POWER MOSFET DEFINES I_S AND R_S, OF THE PARASITIC BODY DIODE, D_{BODY}.

To properly simulate avalanche breakdown voltage with the added clamp circuit (diode D_{BREAK} and voltage source V_{break} in Figure 2), first set the voltage level of V_{BREAK} equal to the measured value of drain breakdown voltage. Then, adjust the SPICE II model parameters I_S, N, and R_S for D_{break} to obtain the best fit to the measured breakdown voltage curve.

Selection of capacitors C_{21}, C_{23}, and C_{24}, and the parameters of the JFET (all shown in Figure 2), can be made using the curves of Figure 6. This is a plot of drain and gate voltage versus time for a power MOSFET driven with constant

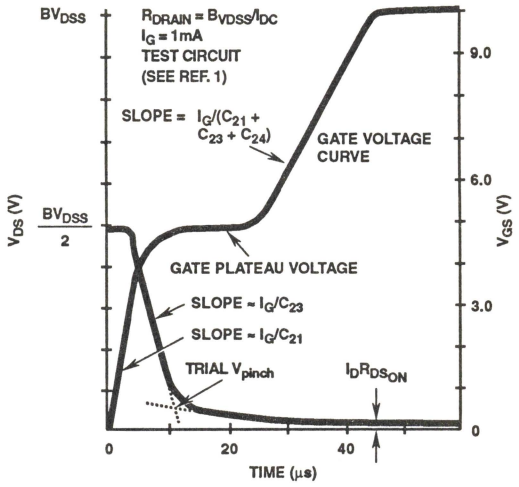

FIGURE 6. PLOTTING DRAIN AND GATE VOLTAGES OF THE POWER MOSFT VS TIME DETERMINES THE VALUES OF C_{21}, C_{23}, C_{24}, AND V_{pinch}.

gate current (I_G).[1] The initial slope of the V_{GS} curve defines C_{21} (since for any value of gate voltage, V_{GS}, less than threshold voltage, V_{TO}, the power MOSFET is in its off-state, so that the gate-to-source capacitance, C_{21}, charges linearly under constant-current conditions). As V_{TO} is reached, the low-voltage lateral MOSFET (Figure 2) turns on, and its drain voltage drops toward its minimum value.

At the outset, the JFET is operating beyond pinch-off, and the slope of the V_{DS}-versus-time curve is controlled by C_{23}. However, when the drain voltage falls below V_{PINCH}, the JFET conducts, strongly coupling C_{24} to the JFET drain and greatly reducing the drain voltage slew rate. Thus, the value of C_{23} can be approximated from the steep slope of the VDS curve in Figure 6, while the value of $C_{21}+C_{23}+C_{24}$ corresponds to the labelled V_{GS} slope. These values can be adjusted slightly to give the best slope fit. A trial value of V_{PINCH} (and V_{TO}) is given by the labelled intercept of the V_{DS} curve. Adjustments of this value will control the length of the gate plateau voltage needed to complete the curve fit.

Table I lists the preferred algorithm for parameter extraction; Table II summarizes the required empirical inputs. Together, these tables will aid in setting up the parameters for evaluation of a power MOSFET with SPICE II and the subcircuit. As an example, Table 3 summarizes the input parameters for the SPICE II model and subcircuit, determined for the Harris IRF130 power MOSFET, using the approach just described. The IRF130 is rated at 14 amperes and has a 100-volt blocking capability.

TABLE 1. PREFERRED ALGORITHM FOR PARAMETER EXTRACTION

1.	Determine K_P of lateral MOS
2.	Determine V_{TO} of lateral MOS
3.	Determine C_{21}
4.	Determine $C_{21} + C_{23} + C_{24}$
5.	Determine Rsource and JFET drain resistance
6.	Assign beta of JFET = 100 x K_P of lateral MOS
7.	Use trial V_{PINCH}
8.	Use trial C_{23} and calculate C_{24}
9.	Curve fit for slope by repeating step 8 with different values of C_{23}.
10.	Adjust V_{PINCH} and V_{TO} of JFET to fix gate-voltage plateau

TABLE 2. EMPIRICAL INPUTS

MOSFET	Enhancement mode:W = L = 1μm; K_P (Figure 3); V_{TO} (Figure 3); C's = 0; T_{OX} = 1E6μm
JFET	Depletion mode; area factor = 1; Beta = 100K_P (Figure 3); V_{TO} = -V_{pinch} (Figure 6); C's = diode lifetime = 0; diode ideality factor = 1.0; Is = 1E - 20; R_D (Figure 4)
D_{BODY}	I_S from Figure 5; Ideality Factor = 1.0; R_S from Figure 5 (must be very much smaller than R_D); C (from C_{OSS}); lifetime = best fit to T_{RR}

TABLE 2. EMPIRICAL INPUTS (Continued)

D_{BREAK}	I_S = arbitrary; C = lifetime = 0; ideality factor = best low-current fit; R = best high-current fit
D1	I_S = 1E - 13; C = lifetime = 0; ideality factor = 0.03; R_S = 1
R_{SOURCE}	Figure 3
L_{SOURCE}	Approx. (5L)ln(4L/d) nH; L and d are source wire inches
V_{PINCH}	Figure 6
V_{BREAK}	Avalanche voltage
C_{21}	Figure 6
C_{23}	Figure 6
C_{24}	Figure 6

TABLE 3 - INPUT PARAMETERS OF IRF130 TO SPICE MODEL

SPICE PARAMETER	HARRIS IRF130 VALUE
LATERAL MOS	
Model Level	1
T_{OX}	1E06μ
V_{TO}	3.4V
K_P	6.4A/V^2
W, L	1.0μ
VERTICAL JFET	
JMOD Area	1
V_{TO}	-6.4V
Beta	640
I_S	10^{-20}
R_D	42.15 x $10^{-3}\Omega$
D_{BODY}	
CJO	1650pF
IT	70 x 10^{-9}
I_S	3 x 10^{-12}
R_S	2.5 x $10^{-3}\Omega$
PASSIVE ELEMENTS	
C_{21}	900pF
C_{23}	40pF
C_{24}	1360pF
R_{SOURCE}	17.5 x $10^{-3}\Omega$
L_{SOURCE}	7.5 x 10^{-9}H
V_{BREAK}	117V

Implementing The Subcircuit in SPICE II

Table IV is the input listing for the implementation of the power MOSFET subcircuit in SPICE II software. Nodes are identified for drain, gate, and source of the power MOSFET. The subcircuit then "hooks" to these nodes wherever specified in the SPICE II simulation. Any number of power MOSFETs can be specified. The parameters listed are for an IRF130 power MOSFET.

The Results

The real test of the enhanced SPICE II model is how closely its predicted performance compares with actual measurements. Using the input parameters for the Harris IRF130 device example given in Table III, we calculated transfer and output curves for the model. These curves were then compared against measured static data. Figures 7 and 8 show the precise fit between predicted and measured static data, even at low values of drain voltage.

To see how the model performs in dynamic prediction, we simulated first-quadrant operation (including avalanche mode) and third-quadrant operation for the Harris IRF130 power MOSFET. Once again, the predicted performance of the enhanced SPICE II model fits actual measurements satisfactorily over the entire operating range of the Harris IRFI30, as shown in Figures 9 and 10.

To compare calculated switching performance versus actual measurement on the Harris IRF130, we used the enhanced SPICE II model to generate switching curves. Figure11 shows drain and gate voltages versus time with a constant gate-current drive. Figure 12 shows drain and gate voltages versus time for a step gate-voltage input. Actual measured data was then taken and overlaid on the points predicted by the enhanced SPICE II model. Again, the fit was accurate in each case.

TABLE 4 - INPUT LISTING OF SUBCIRCUIT MODEL
Listed Parameters Valid for a Harris IRFI30 Power MOSFET

```
* THIS IS THE POWER MOS SUBCIRCUIT
* NODE 3 IS THE POWERMOS DRAIN
* NODE 2 IS THE POWERMOS GATE
* NODE 11 IS THE POWERMOS SOURCE
*
*
.OPTIONS NOMOD NOLIST NOACCT NONODE LIMPTS=250 GMIN=1.0E-20
.SUBCKT POWMOS 3 2 11
C21 2 1 900P
C23 2 3 40P
C24 2 4 1360P
FDSCHRG 4 2 VMEAS 1.0
MOS1 4 2 11 MOSMOD L=1U W=1U
JFET 3 1 4 JMOD AREA=1
DBODY 1 3 DMOD2
RSOURCE 1 10 17.5E-03
LSOURCE 10 11 7.5N
E41 5 11 4 1 1.0
D1 5 6 DMOD
VPINCH 6 8 DC 6.4
VMEAS 8 11 DC 0.0
DBREAK 3 7 DMOD3
VBREAK 7 1 DC 117
.MODEL MOSMOD NMOS VTO=3.4 KP=6.40 TOX=1.0E+06U
.MODEL JMOD NJF VTO=-6.4 BETA=640 IS=1.0E-20 RD=42.5E-03
.MODEL DMOD D IS=1.0E-13 N=0.03 RS=1.0
.MODEL DMOD2 D CJO=1650P TT=70N IS=3.0E-12 RS=2.5E-03
.MODEL DMOD3 D IS=1E-13 RS=2.0 N=1.0
.ENDS
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*
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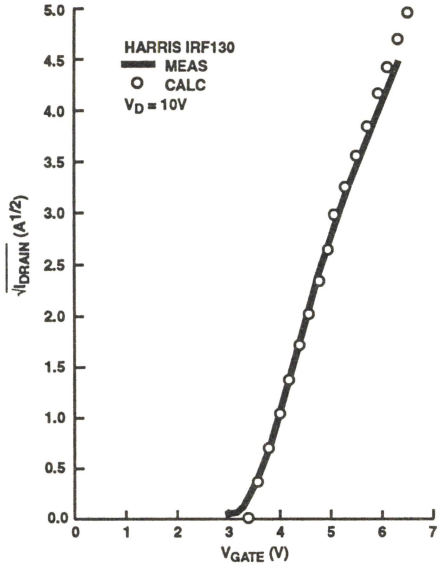

FIGURE 7. MEASURED SQUARE ROOT OF DRAIN CURRENT (DRAIN VOLTS = 10) vs. GATE VOLTAGE FOR THE HARRIS IRF130 POWER MOSFET IS PLOTTED ALONG WITH THE CALCULATED VALUES FOR THE ENHANCED SPICE II MODEL. AN EXCELLENT FIT IS OBTAINED.

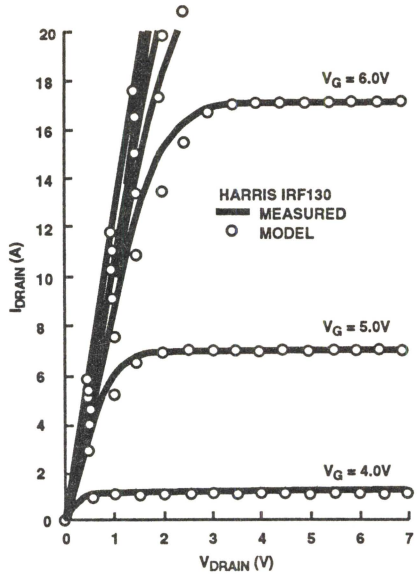

FIGURE 8. PLOTS OF DRAIN CURRENTvs. DRAIN VOLTAGE FOR THE HARRIS IRF130 POWER MOSFET SHOW AN EXCELLENT FIT BETWEEN MEASURED VALUES AND THOSE CALCULATED BY THE ENHANCED SPICE II MODEL FOR VARIOUS VALUES OF CONSTANT GATE VOLTAGE.

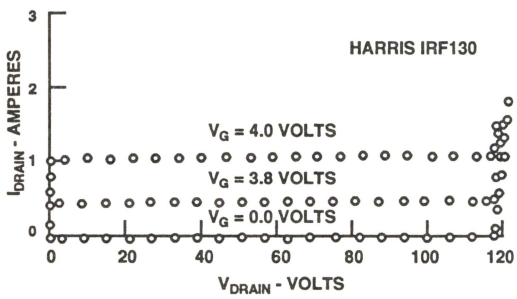

FIGURE 9. FIRST QUADRANT DRAIN CURRENT vs. DRAIN VOLTAGE WITH V_{GS} HELD CONSTANT IS CALCULATED BY THE ENHANCED SPICE II MODEL OF THE HARRIS IRF130 POWER MOSFET. NOTE THAT THE MODEL PREDICTS AVALANCHE BREAKDOWN.

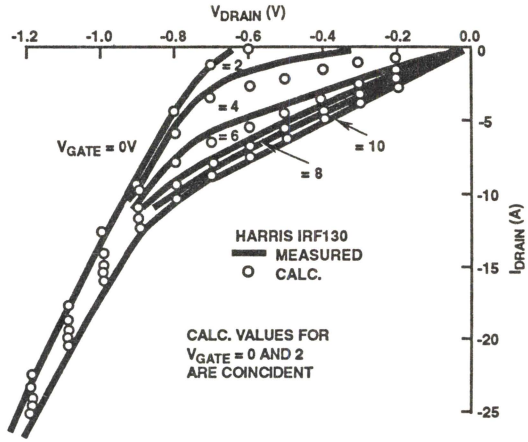

FIGURE 10. THIRD-QUADRANT OPERATION OF THE HARRIS IRF130 SHOWS AGREEMENT BETWEEN THE PREDICTED VALUES OF THE ENHANCED SPICE II MODEL AND ACTUAL MEASURED VALUED OF DRAIN CURRENT vs DRAIN VOLTAGE AT DIFFERENT VALUED OF CONSTANT GATE VOLTAGE.

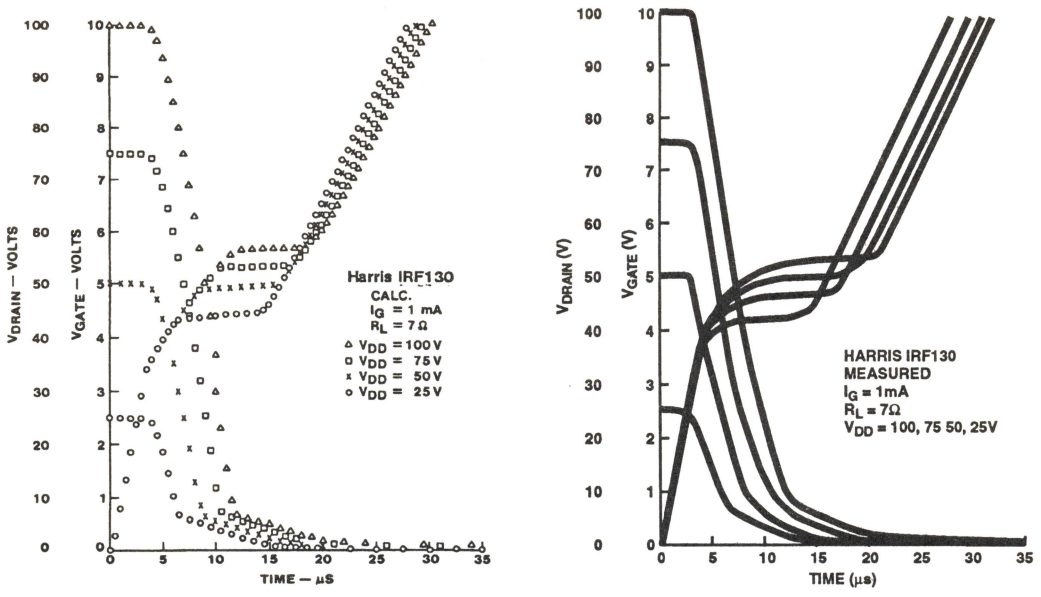

FIGURE 11. THESE PLOTS OF DRAIN AND GATE VOLTAGES vs. TIME FOR CONSTANT GATE CURRENT SHOW AGREEMENT BETWEEN THE PREDICTIONS OF THE ENHANCED SPICE II MODEL (a) AND MEASURED PERFORMANCE OF THE HARRIS IRF130 POWER MOSFET (b).

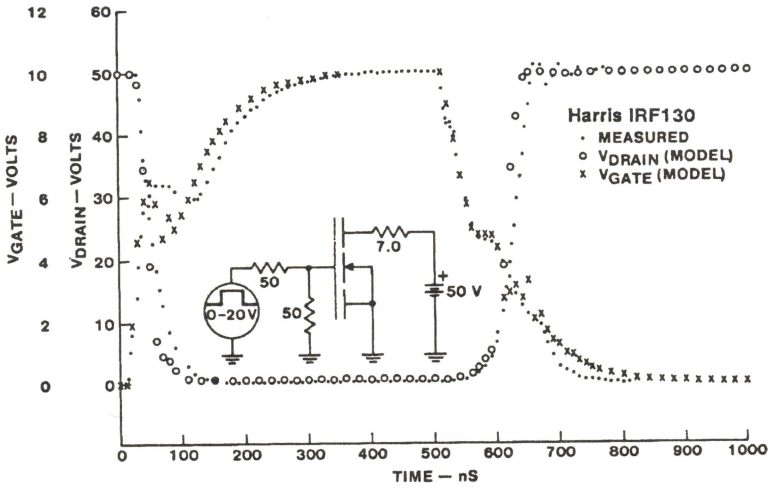

FIGURE 12. SWITCHING PERFORMANCE OF THE HARRIS IRF130 POWER MOSFET IS CLOSELY PREDICTED BY THE ENHANCED SPICE II MODEL IN THIS PLOT OF MEASURED AND CALCULATED VALUES OF DRAIN AND GATE VOLTAGES vs. TIME IN A STANDARD SWITCHING CIRCUIT.

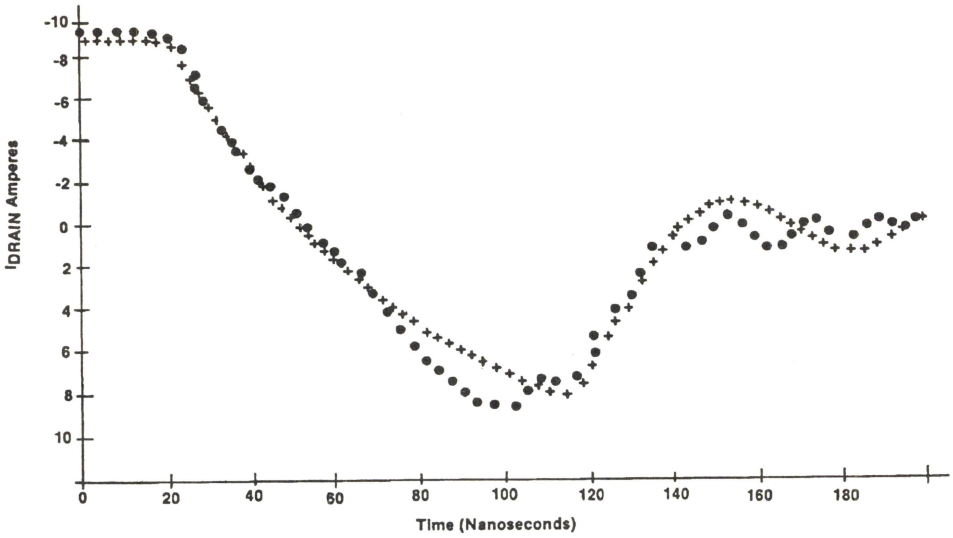

FIGURE 13. THE CALCULATED THIRD-QUADRANT DIODE RECOVERY WAVEFORM OF THE ENHANCE SPICE II MODEL SHOWS GOOD AGREEMENT WITH THAT ACTUALLY MEASURED FOR THE HARRIS IRF130 POWER MOSFET

Finally, the enhanced model was used to compare calculated and measured body diode (D_{BODY} in Figure 2) recovery time curves in third-quadrant operation of the Harris power MOSFET. Figure 13 shows the good agreement between predicted and actual results.

This approach provides excellent results when there is a need to model the performance of a power MOSFET. Not only will the approach update SPICE II (or other circuit simulation CAD program) so that it will simulate the latest state-of-the-art in MOS power, but it will allow quick analysis of every static and dynamic characteristic for suitability in a proposed design.

References

1. Wheatley, Jr., C.F. and Ronan Jr., H.R., "Switching Waveforms of the L^2FET: A 5-Volt Gate Drive Power MOSFET," Power Electronic Specialist Conference Record, June 1984, p. 238.
2. Ronan Jr., H.R. and Wheatley Jr., C.F., "Power MOSFET Switching Waveforms: A New Insight," Proceedings of Powercon 11, April 1984, p. C3.
3. Niehaus, H.A., Bowers, J.C. and Herren Jr., P.C., "A High Power MOSFET Computer Model," Power Conversion International, January 1982, p. 65.

A SPICE-2 SUBCIRCUIT REPRESENTATION FOR POWER MOSFETs, USING EMPIRICAL METHODS

Author: C. Frank Wheatley Jr., and Harold R. Ronan, Jr., RCA Solid State Division**

Abstract

An accurate power-MOSFET model is not widely available for CAD circuit simulation. This work provides a subcircuit model which is compatible with SPICE-2 software and MOSFET terminal measurements. SPICE-2 is the circuit simulation package of choice for this work because of its universal availability, despite its inherent limitations. These limitations are circumvented through circuit means.

This effort models power-MOSFET terminal behavior consistent with SPICE-2 limitations; hence it will differ from the physical model as suggested by Wheatley, et al[1], Ronan et al[2] and others. We feel we have advanced prior efforts[3] particularly in areas of third-quadrant operations, avalanche-mode simulation, switching waveforms and diode recovery waveforms.

Discussion

The subcircuit shown in Figure 1 is described in Table 1. All passive circuit elements are constants. The very-high-gain JFET is used to simulate the dual-slope drain voltage vs time switching curve common to the power MOSFET.[1,2]

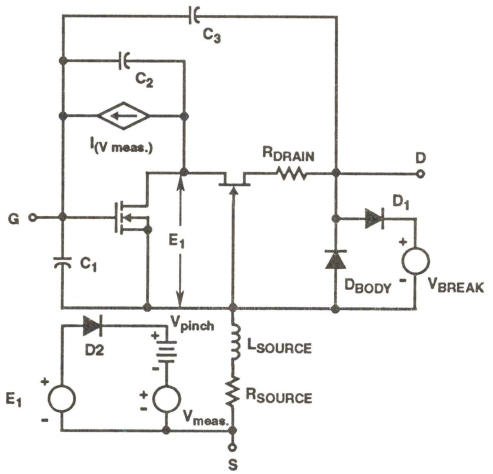

FIGURE 1. SPICE-2 SUBCIRCUIT FOR POWER MOSFET SIMULATION.

NOTE: If the JFET source voltage, E_1, is very low relative to its V_{PINCH} voltage, the JFET is in a highly conductive state, tightly coupling C_2 to the JFET drain. However, as the voltage E_1 approaches V_{PINCH}, the JFET operates in a constant-current mode, thereby permitting a much faster drain slew rate, which is determined primarily by C_3.

If E_1 exceeds V_{PINCH}, errors will exist in the turn-on waveforms. The C_2 discharge current-controlled current source remedies this situation in conjunction with the subcircuit containing D_2. The D_2 ideality factor was set at 0.03 to assure that E_1 minus V_{PINCH} does not exceed several millivolts.

The body diode cannot be properly modeled by the JFET gate-drain diode, hence D_{BODY}. Conditions of Table 1 assure that most third-quadrant current flow is via D_{BODY}. Avalanche breakdown is more accurately modeled by the clamp circuit containing D_1.

Table 1 in combination with Figures 2, 3, 4 and 5 provides the required empirical inputs. Table 2 lists the preferred algorithm for parameter extraction.

TABLE 1. EMPIRICAL INPUTS

MOSFET	Enhancement mode; W = L = 1μm; K_P (Figure 2); V_{TO} (Figure 2); C's = 0; I_{DSO} = IE -12
JFET	Depletion mode; areas factor = 1; B = 100K_P (Figure 2); $V_{TO} = V_{PINCH}$ (Figure 5); C's = diode lifetime = R_{SERIES} = 0; diode ideality factor = 1.0, I_{DSO} = IE -20
BODY DIODE	I_S from Figure 4; Ideality Factor = 1.0; R from Figure 4 (must be very much greater than R_D); C (from C_{OSS}); lifetime = best fit to T_{RR}
D_1	I_S = arbitrary; C = lifetime = 0; ideality factor = best low-current fit; R = best high-current fit
D_2	I_S = 1E -8; C = lifetime = R = 0; ideality factor = 0.03
R_S	Figure 2.
R_{DRAIN}	Figure 3.
L_S	Approximately (5L) ln (4 L/d) nH; L and d are source wire inches.
V_{PINCH}	V_{TO} of JFET.
V_{BRK}	Avalanche voltage.
C_1	From Figure 5.
C_2	Maximum from Figure 5.
C_3	Minimum from Figure 5.

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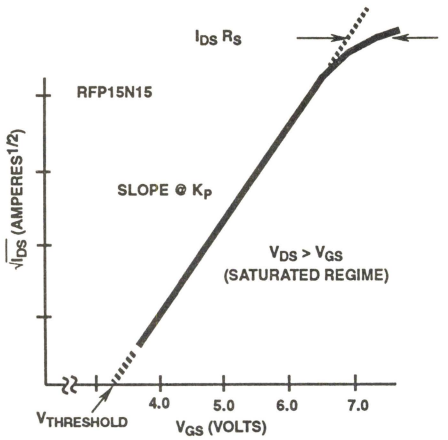

FIGURE 2. SQUARE ROOT OF DRAIN CURRENT vs GATE VOLTAGE DEFINES $V_{THRESHOLD}$, K_P, AND R_S.

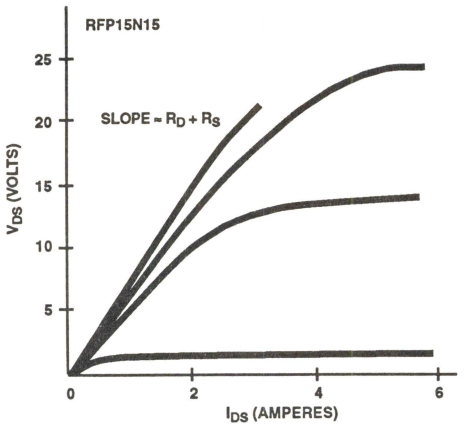

FIGURE 3. DRAIN CURRENT vs DRAIN VOLTAGE WITH CONSTANT GATE VOLTAGE DEFINES "ON" RESISTANCE.

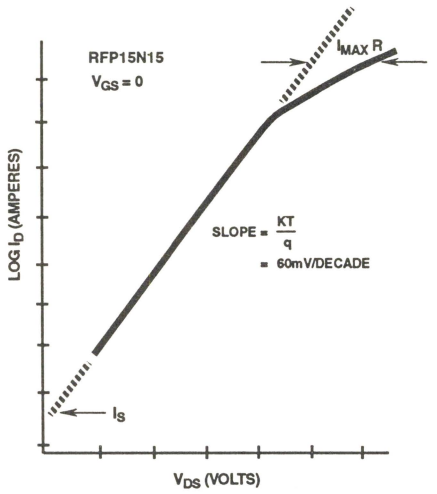

FIGURE 4. THIRD-QUADRANT OPERATION DEFINES I_S AND R OF DIODE D_{BODY}.

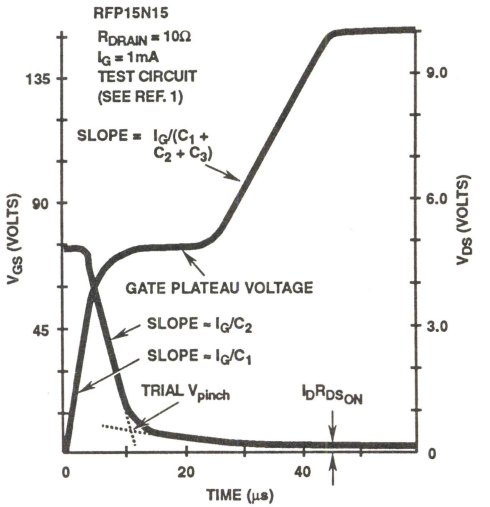

FIGURE 5. DRAIN AND GATE VOLTAGE vs TIME DETERMINE C_1, C_2, C_3 AND V_{PINCH}.

TABLE 2. PREFERRED ALGORITHM FOR PARAMETER EXTRACTION

1. Determine K_P of lateral MOS
2. Determine V_{TH} of lateral MOS
3. Determine C_1
4. Determine $C_1 + C_2 + C_3$
5. Determine R_{DS}
6. Assign B of JFET = 100 x K_P of lateral MOS
7. Use trial V_{PINCH}
8. Use C_2 (Maximum), C_3 (Minumum) are curve-fit C's
9. Adjust V_{PINCH} to fix gate voltage plateau

Results

Figure 6 and Figure 7 compare measured static data to calculated transfer curves and output curves. Calculated static-output curves are shown in Figure 8 and Figure 9 for third-quadrant range, including avalanche.

Calculated switching data is compared to measured switching curves[1,2] in Figure 10 and Figure 11. Calculated body-diode recovery curves are shown in Figure 12.

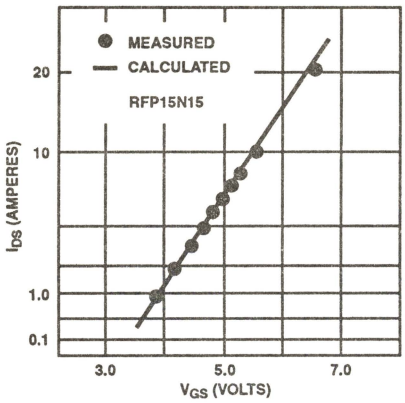

FIGURE 6. DRAIN CURRENT vs GATE VOLTAGE (NOTE SQUARE ROOT SCALE) - MEASURED CURVE vs CALCULATED POINTS.

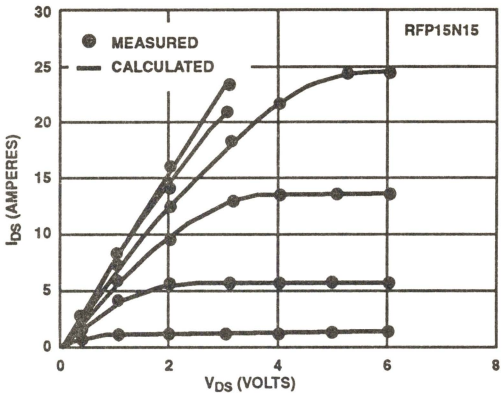

FIGURE 7. DRAIN CURRENT vs DRAIN VOLTAGE FOR CONSTANT VALUES OF GATE VOLTAGE - MEASURED CURVES vs CALCULATED POINTS.

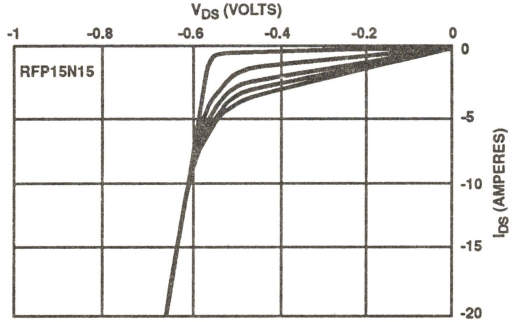

FIGURE 8. THIRD-QUADRANT DRAIN CURRENT vs DRAIN VOLTAGE WITH CONSTANT POSITIVE GATE VOLTAGE (CALCULATED).

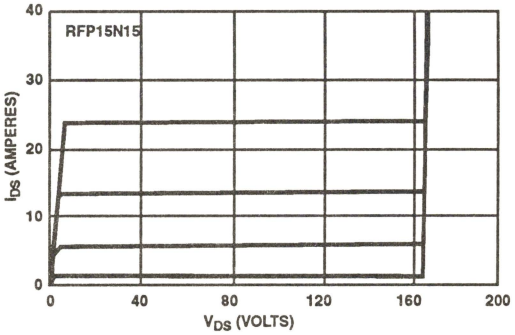

FIGURE 9. FIRST-QUADRANT DRAIN CURRENT vs DRAIN VOLTAGE, V_{GS} = CONSTANT. NOTE AVALANCHE BREAKDOWN (CALCULATED).

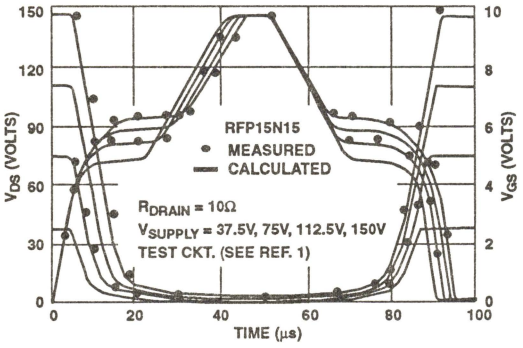

FIGURE 10. DRAIN AND GATE VOLTAGE vsTIME FOR CONSTANT GATE CIRCUIT - MEASURED CURVES vs CALCULATED POINTS.

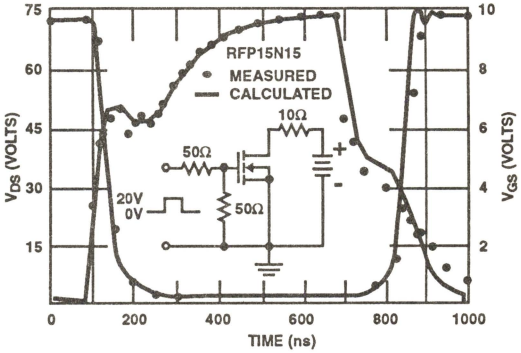

FIGURE 11. DRAIN AND GATE VOLTAGE vs TIME FOR STANDARD SWITCHING CIRCUIT - MEASURED CURVES vs CALCULATED POINTS.

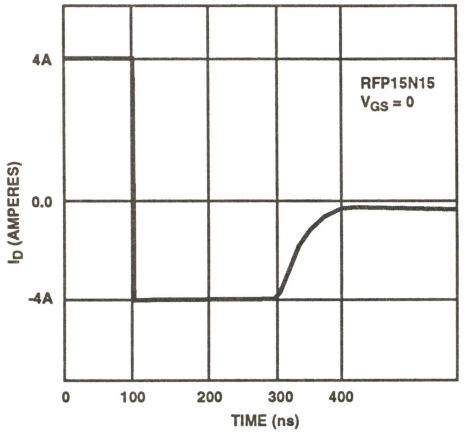

FIGURE 12. THIRD-QUADRANT DIODE-RECOVERY-TIM CURVE (CALCULATED).

Conclusion

An equivalent-circuit model for power-MOSFETs, that is suitable for use with the SPICE CAD program, has been demonstrated. The model is compatible with all versions of SPICE presently available without modification to the program's internal code. The model addresses static and dynamic behavior of first and third-quadrant operation, including avalanche breakdown, and is empirical in nature; all necessary input parameters may be inferred from data sheets or simple terminal measurements.

Excellent agreement has been obtained between measured and simulated results.

References

1. Wheatley Jr., C. F. and Ronan Jr., H. R., "Switching Waveforms of the L2FET: A 5-Volt Gate-Drive Power MOSFET," Power Electronic Specialists Conference Record, June 1984, p. 238
2. Ronan Jr., H. R. and Wheatley Jr., C. F., "Power MOSFET Switching Waveforms: A New Insight," Proceedings of Powercon II, April 1984, p. C-3
3. Nienhaus, H. A., Bowers, J. C., and Herren Jr., P. C., "A High Power MOSFET Computer Model," Power Conversion International, January 1982, p 65

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Harris Semiconductor

APPNOTE

No. AN9210 February 1994

Harris Power MOSFETs

A NEW PSPICE SUBCIRCUIT FOR THE POWER MOSFET FEATURING GLOBAL TEMPERATURE OPTIONS

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C. Frank Wheatley Jr. - (SM, IEEE) - Consultant

Abstract

An empirical sub-circuit was implemented in PSpice® and is presented. It accurately portrays the vertical DMOS power MOSFET electrical and for the first time, thermal responses. Excellent agreement is demonstrated between measured and modeled responses including first and third quadrant MOSFET and gate charge behavior, body diode effects, breakdown voltage at high and low currents, gate equivalent series resistance, and package inductances for temperatures between -55°C and 175°C. Parameter extraction is relatively straight forward as described.

Introduction

Circuit simulation commonly uses one of the SPICE [1] programs. However, power circuits require proper models for unique devices which are not included in the supplied libraries. Efforts have been published to model the power MOSFET [2-10] with varying degrees of success. The more successful papers have used sub-circuit representation. To-date, a thermal model has not been offered.

Objective

It is the goal of this effort to provide for the first time a thermal sub-circuit model capable of providing accurate simulation throughout all of the power MOSFET regimes. In addition the sub-circuit should be readily understood and accepted by users, and the ease of parameter extraction should be demonstrated.

Method

A sub-circuit approach is employed which is empirical. It is developed to provide black box conformity to the power MOSFET throughout the operating regime normally traversed by the dictates of most power circuit applications including junction temperature. Although device thermal behavior is the driving force, respect is maintained toward the physics and the SPICE algorithms.

The developed sub-circuit schematic is shown in Figure 1.

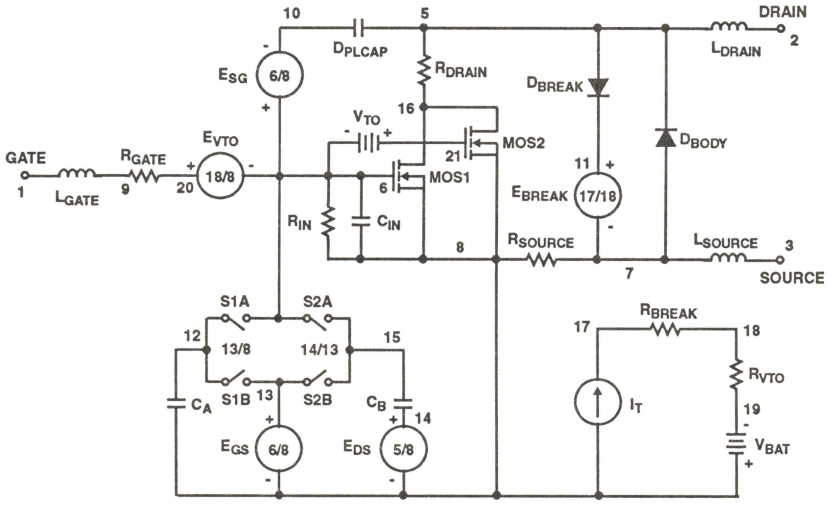

FIGURE 1. PSPICE MODEL SUBCIRCUIT

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There are many forms of SPICE, each with its own strengths and weaknesses. PSpice® was chosen for the following reasons.

1. An evaluation copy capable of considerable circuit analysis for power circuits is available.
2. The PROBE feature provides excellent displays.
3. Programmed time slice defaults and DC convergence routines make it very friendly.
4. The switch algorithm of PSpice® provides a very smooth transition from off to on.

Other forms of SPICE were not investigated, but they should be amenable to the development of a similar sub-circuit by paralleling the teachings of this work.

Driving constraints for this work were:

1. The SPICE device equations should not be modified.
2. Global temperature should be included.
3. All modes and levels of power MOSFET operation should be modeled.
4. The sub-circuit should be empirically developed to complement the device physics and the source code algorithms.
5. The sub-circuit should be acceptable to a circuit design user.
6. Parameter extraction should require little or no iteration.

Temperature Modeling

Use is made of voltage controlled voltage sources and model statements in order to form master/slave circuit relationships. In this manner, resistors can often be used to establish a first and second order temperature correction where direct PSpice algorithms will not permit thermal modeling.

An Overview (Figure 1)

The primary device for gate controlled positive or negative current flow is provided by Mos1 which is defined by the level 1 model MOSMOD. The second order effect of threshold voltage is set by Mos2 combined with the voltage V_{TO}. Model MOSMOD also defines Mos2 but with a 1 percent scaling.

It is necessary that R_{SOURCE} and R_{DRAIN} be provided as separate resistors, rather than being included with the mosfets. In this manner, 1st and 2nd order temperature effects may be added as described by model RDSMOD.

The thermal variation of KP as provided by the source code is a satisfactory representation. However, the threshold voltage of Mos1 must be modified by the voltage dependent voltage source E_{VTO}. E_{VTO} provides an additive or subtractive voltage in series with the gate as a function of temperature. It is equal to the sum of V_{BAT} and the product of It and R_{VTO}. Temperature variation is provided by model RVTOMOD.

Avalanche breakdown of the MOSFET is provided by the clamp circuit of D_{BREAK} in series with E_{BREAK}. The value of E_{BREAK} is provided by the multiplier of E_{BREAK} and the product of It times R_{BREAK}. Temperature variation is provided by model RBKMOD. High current voltage drops are provided by RS of the model DBKMOD including thermal sensitivity.

The power MOSFET being modelled contains a third quadrant diode as a fabrication consequence, and it is represented by D_{BODY}. Model DBDMOD provides the leakage current IS, the transit time for stored charge effects TT, the body diode series resistance RS, temperature dependence of this resistor TRS1 and TRS2, and the MOSFET output capacitance CJO.

The inductances associated with the device terminals are represented by L_{SOURCE}, L_{GATE}, and L_{DRAIN}.

The effective series resistance associated with the gate is modelled by the resistor R_{GATE}.

A gate to source input capacitance is represented by C_{IN}. MOSFET output capacitance is provided by model DBDMOD as described above. Feedback capacitance is provided by D_{PLCAP} as defined by model DPLCAPMOD. A diode was used for this function to provide a square root dependency with drain to source voltage. The voltage dependent voltage generator E_{SG} is added to assure that the drain to source voltage is imposed across the feedback capacitor while forcing the feedback current flow into the gate node. It is further necessary that the ideality factor N of model DPLCAPMOD be made large to exclude forward diode conduction during third quadrant operation of the MOSFET.

A capacitor C_A is switched in parallel with C_{IN} when the gate to source voltage becomes sufficiently negative. This switching is implemented by the switch S1A. Model S1AMOD defines the switch closed resistance, open resistance, and the gate to source voltages through which the fully on to fully off transition occurs. During this transition, switch S1B also transitions from fully off to fully on. Switch S1B is defined by model S1BMOD. Voltage controlled voltage generator E_{GS} provides the proper charge state for C_A when switch S1A is open.

In a similar manner, the capacitor C_B is switched in parallel with C_{IN} when the drain to gate voltage becomes negative. Switch S2A is defined by model S2AMOD for the on resistance, off resistance, and drain to gate voltage transition range. During this transition switch S2B also transitions as defined by model S2BMOD. Voltage controlled voltage generators E_{DS} and E_{GS} provide the proper charge state for C_B when switch S2A is open.

In order to facilitate DC convergence, PSpice® provides a minimum conductance between all nodes as defined by the PSpice® analysis options. In order to assure that a floating gate initial condition will not exist should a modeler drive from a current source, a very large gate to source resistor R_{IN} is added. Inclusion of R_{IN} is recommended but not required.

All sub-circuit elements are treated as being independent of temperature if they are not otherwise defined.

Gate propagation effects [15], radiation effects, and inherent VDMOS design deficiencies are not modelled. This is discussed later.

All discussions apply equally to P channel although N channel is discussed exclusively.

Applications

The sub-circuit combined with external circuitry may be analyzed for many responses. Three circuits are modelled to demonstrate the capability of the PSpice® sub-circuit model. A synchronous rectifier producing 100 watts at 5 volts DC from a 100KHz square wave demonstrates the ability to handle the first and third quadrant regimes of two MOSFETs, including conversion efficiency versus temperature. Calculated waveforms are presented, but they are unsupported by measured data. The diode recovery waveform is modelled and compared to the measured response. Switching waveforms of the power MOSFET are also modelled and compared to the measured results.

SYNCHRONOUS RECTIFIER

The schematic of a synchronous rectifier circuit is shown in Figure 2. The rectifier power MOSFETs are a pair of cross coupled RFH75N05 megafet devices. Conduction is offered by a forward gate bias with negative drain current (third quadrant mosfet operation) and voltage blocking is assured by a slightly negative gate bias for first quadrant MOSFET operation.

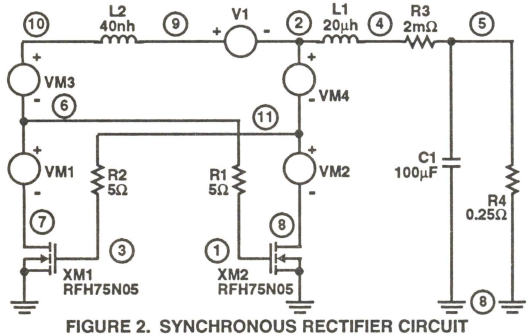

FIGURE 2. SYNCHRONOUS RECTIFIER CIRCUIT

VM1 to VM4 are voltage sources of zero potential and are used to permit a recording of branch currents. The transformer secondary normally used in a supply of this sort is represented by voltage source V1 and leakage inductance L2. Filter inductor L1 and capacitor C1 provide energy storage and smoothing for the 100KHz square wave of V1. Rise and fall times of the square wave are not critical, but were set at 40ns. Gate coupling resistors R1 and R2 are somewhat critical, in that too high a value will restrict the conduction transition time of the MOSFET. Alternatively, a value too low will permit a high voltage drain spike to appear on the gate of the MOSFET.

The calculated output voltage turn on transient is shown in Figure 3. Of course this represents a feed forward circuit response only. In practice, the unmodelled drive circuit with pulse width modulation and feedback would provide a much faster response which would be slew rate limited. The ripple voltage is 5mV RMS.

The efficiency for this portion of the synchronous rectifier circuit is plotted in Figure 4 as a function of temperature from -25°C to 150°C. As a convenience, the equation used by PROBE® (PSpice's® waveform plotter routine) is included. This equation yields a solution rapidly.

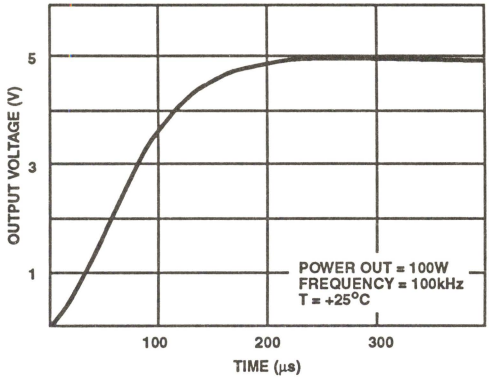

FIGURE 3. RECTIFIER OUTPUT VOLTAGE

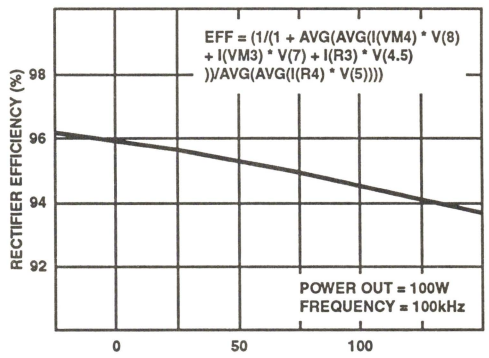

FIGURE 4. RECTIFIER EFFICIENCY

Transition voltage waveforms of the input voltage, one drain voltage, and one gate voltage are plotted in Figure 5. The value of drain voltage during third quadrant conduction is approximately -0.2 volts. Other waveforms are readily available by use of the PSpice® system.

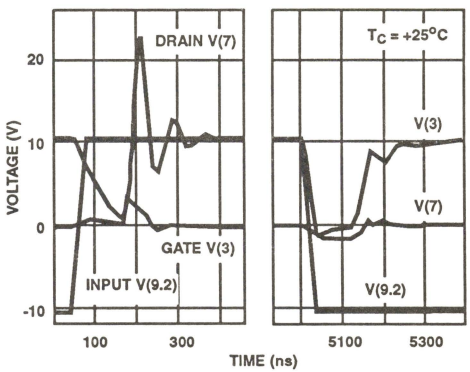

FIGURE 5. TRANSITION VOLTAGE WAVEFORMS

RECOVERY WAVEFORMS

Figure 6 shows the MOSFET current of the parasitic 3rd quadrant diode vs time as modelled with the sub-circuit and as measured using the Berman SM30 equipment. Measurements show very little temperature sensitivity. Therefore it is not modelled.

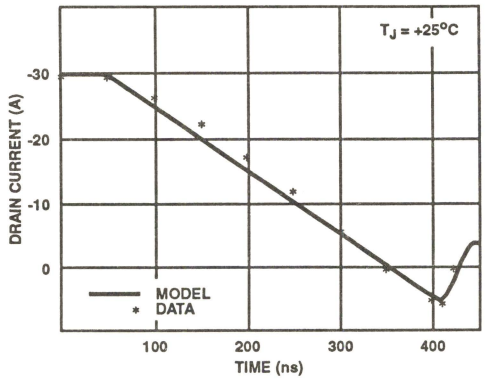

FIGURE 6. DIODE RECOVERY WAVEFORMS

SWITCHING WAVEFORMS

Switching time measurements of the power MOSFET are usually taken in a circuit similar to that of Figure 7. Although parasitic wiring inductance is not normally shown, it exists and is modelled as shown. The waveforms of gate and drain voltages are presented as measured and modelled in Figure 8. Switching times of Figure 8 are listed in Table 1.

TABLE 1. SWITCHING TIME DATA

PARAMETER	DATA	MODEL	UNITS
Turn on Delay Time	72	67	ns
Rise time	238	208	ns
Turn Off Delay Time	440	460	ns
Fall Time	259	240	ns

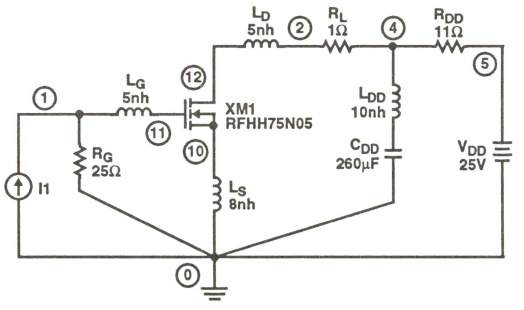

FIGURE 7. SWITCHING TIME CIRCUIT

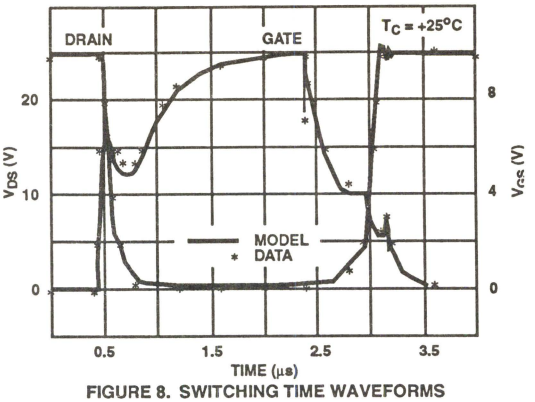

FIGURE 8. SWITCHING TIME WAVEFORMS

Measured vs Modelled Characteristics

The device characteristics have been measured (data points) and modelled (solid line) as plotted in Figures 9 to 19. Thermal responses were omitted from some figures to improve the clarity of presentation.

Discussion Of Results

Excellent correlation generally exists between measured and modelled information over the current range from zero to three times the device rated current. As the drain voltage is increased from zero volts with a constant gate voltage, the MOSFET transitions from the linear mode to the saturated mode. Conformance of modelled to actual data is very good in the constant current regime (saturated mode). A forcing of conformance exists for the very high gate voltages in the linear mode, with departure existing for the linear mode with lesser values of constant gate voltages.

The actual drain voltage in the linear mode is seen to be as much as 20 percent below the modelled value in worst cases. This represents a conservative error for circuit calculations in that the conduction loss is somewhat less than modelled. In addition, the gate drive is usually high under MOSFET conduction, thereby avoiding operation in the regions of discussion.

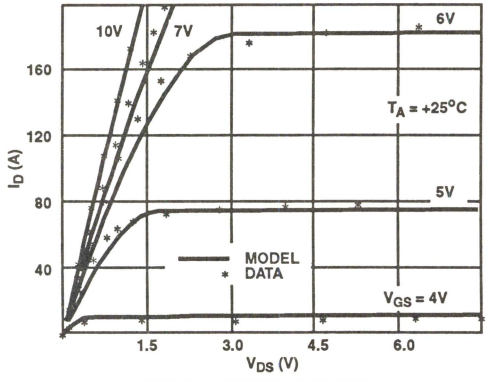

FIGURE 9. OUTPUT CURVES

The discrepancy results because the PSpice® algorithm for a mosfet assumes the channel surface concentration to be constant. In the power MOSFET, the surface concentration is gaussian along the channel length. Hence, the observed behavior is as would be expected.

The modelled response can be improved by changing the PSpice® algorithm, however changes of this type were ruled out for this work.

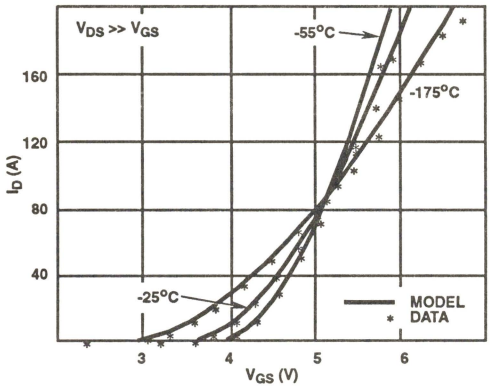

FIGURE 10. TRANSFER CURVES

Excellent agreement exists.

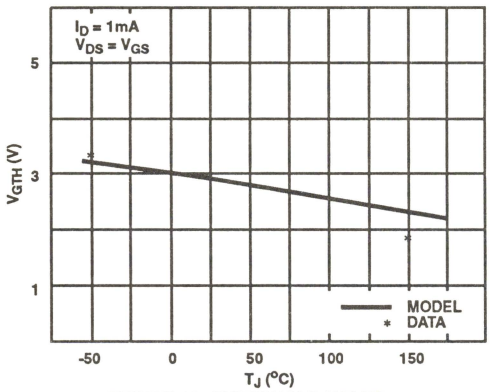

FIGURE 11. THRESHOLD VOLTS

Excellent agreement exists. This would not be so without the inclusion of Mos2 to represent the sharp corners of the many hexagonal cells of the structure. The flat part of the hex cells results in a two dimensional diffusion during processing and the establishment of a source to body junction cross-over concentration at the surface, resulting in Mos1 as modelled. However, the corners of the hex cells introduce a three dimensional diffusion resulting in a lower source to body junction cross-over concentration at the surface. The unpublished work of Klodzinski, et al [11] processed test and control devices upon a common wafer where the corners of the hex source implant were excluded versus included, revealing threshold voltages approximately 0.4 volts higher for the test.

Omission of Mos2 would not impact circuit performance, however a reverence of attached importance to the MOSFET threshold voltage mandates modelled to measured agreement.

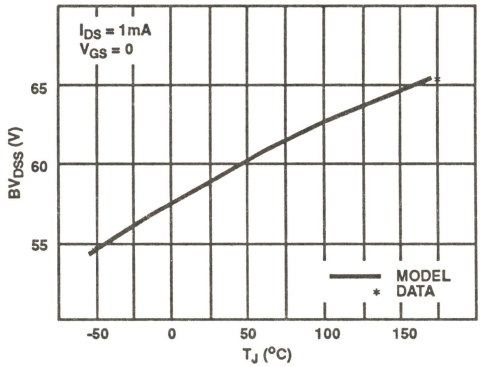

FIGURE 12. BREAKDOWN VOLTAGE, LOW CURRENT BV_{DSS}

Excellent agreement exists.

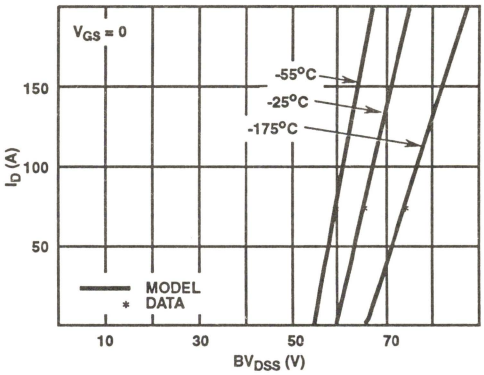

FIGURE 13. BREAKDOWN VOLTAGE,, HIGH CURRENT BV_{DSS}

Excellent agreement exists.

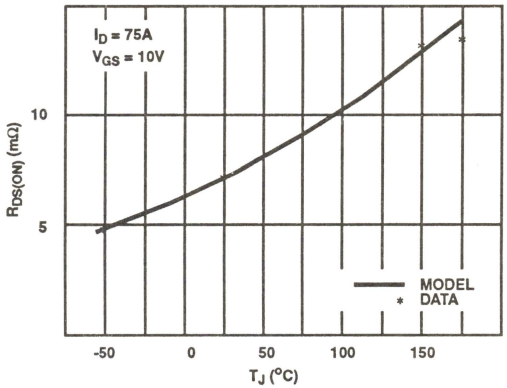

FIGURE 14. ON RESISTANCE vs TEMPERATURE

Excellent agreement exists.

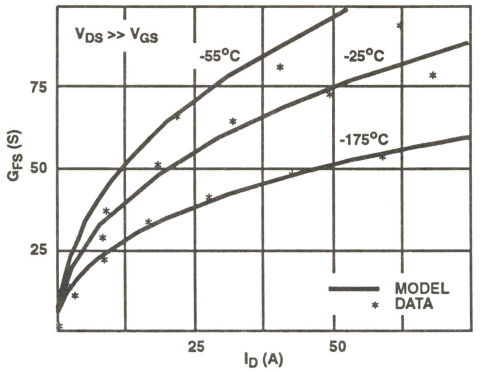

FIGURE 15. TRANSCONDUCTANCE CURVES

Excellent agreement exists.

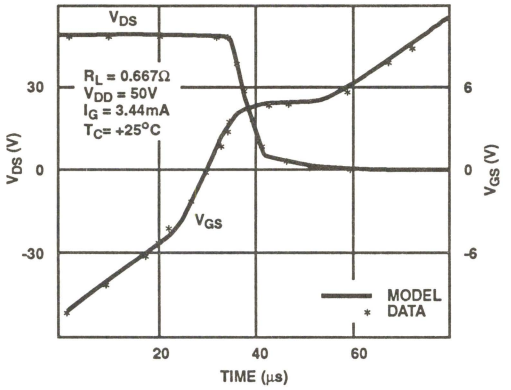

FIGURE 16. GATE CHARGE CURVES

Excellent agreement exists. The non linear behavior of gate charge for negative gate bias is seldom shown. A significant increase in turn on delay results by operating from a negative gate voltage.

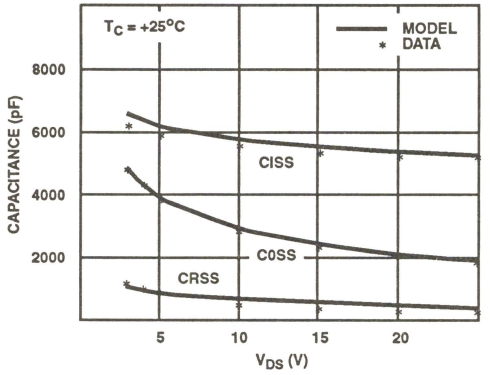

FIGURE 17. CAPACITANCE CURVES

Excellent agreement exists.

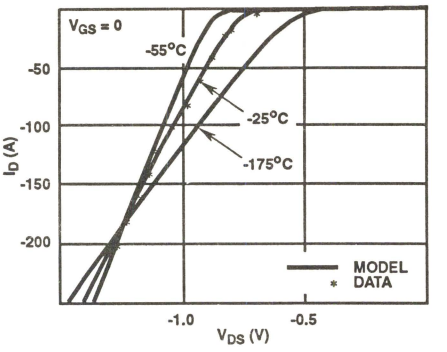

FIGURE 18. BODY DIODE CURVES

All three measured data curves were noted to cross at a drain current of 180amps. Excellent agreement exists.

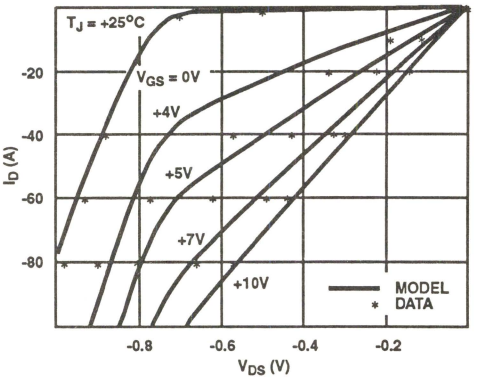

FIGURE 19. 3RD QUADRANT MOSFET CURVES

Good agreement exists. The departure seen between modelled and measured exists for the same reason as the departure of the output curves in the linear regime. This would also be improved by changing the PSpice algorithm as suggested relative to Figure 9.

Parameter Extraction

The sub-circuit is chosen to minimize interdependencies between parameters. A listing of the sub-circuit is presented in Table 2 as a template which routes the Modeler through extraction with guiding comments. Although the template is a complete and workable PSpice® sub-circuit listing, all parameter values except KP and VTO are chosen to be transparent to the results of the analysis. As the transparent values are replaced with extracted values, the model is developed. The listing in Table 2 is structured so that parameters being extracted have very little dependency upon those values which are not yet determined. If desired after completing the extraction, an iteration may be made for the comfort of the Modeler.

EXTRACTION OF MODEL PARAMETERS FROM PHYSICAL MEASUREMENTS

TABEL 2. TEMPLATE		TABLE 3. FINAL MODEL
.SUBCKT TEMPLATE 2 1 3 ; rev 12/17/90 *Nom Temp=25 deg C		.SUBCKT RFH75N05 2 1 3 ; rev 3/20/91 *Nom Temp=25 deg C
Mos1 16 6 8 8 MOSMOD M=0.99 ; .MODEL MOSMOD NMOS (VTO=3 KP=10 +IS=1e-30 N=10 TOX=1 L=1u W=1u)	Step 1	Mos1 16 6 8 8 MOSMOD M=0.99 .MODEL MOSMOD NMOS (VTO=3.48 KP=78.5 +IS=1e-30 N=10 TOX=1 L=1u W=1u)
Mos2 16 21 8 8 MOSMOD M=0.01 ; Vto 21 6 0	Step 2	Mos2 16 21 8 8 MOSMOD M=0.01 Vto 21 6 0.6
Rsource 8 7 RDSMOD 1e-12 ;	Step 3	Rsource 8 7 RDSMOD 2e-3
Rdrain 5 16 RDSMOD 1e-12 ;	Step 4	Rdrain 5 16 RDSMOD 3.07e-3
.MODEL RDSMOD RES (TC1=0 TC2=0)	Step 5	.MODEL RDSMOD RES (TC1=5.2e-3 TC2=1.37e-5)
Evto 20 6 18 8 1 ; Rvto 18 19 RVTOMOD 1 It 8 17 1 Vbat 8 19 DC 1 .MODEL RVTOMOD RES (TC1=0 TC2=0)	Step 6	Evto 20 6 18 8 1 Rvto 18 19 RVTOMOD 1 It 8 17 1 Vbat 8 19 DC 1 .MODEL RVTOMOD RES (TC1=-3.78e-3 TC2=-7.51e-7)
Ebreak 11 7 17 18 1000 ; Dbreak 5 11 DBKMOD Rbreak 17 18 RBKMOD 1	Step 7	Ebreak 11 7 17 18 58.4 Dbreak 5 11 DBKMOD Rbreak 17 18 RBKMOD 1
.MODEL RBKMOD RES (TC1=0 TC2=0) ;	Step 8	.MODEL RBKMOD RES (TC1=9.5e-4 TC2=-1.17e-6)
.MODEL DBKMOD D (RS=0 TRS1=0 TRS2=0) ;	Step 9	.MODEL DBKMOD D (RS=8e-2 TRS1=2.5e-3 TRS2=0)
Dbody 7 5 DBDMOD ; .MODEL DBDMOD D (IS=1e-30 RS=0 TRS1=0 +TRS2=0 CJO=0 TT=0)	Step 10	Dbody 7 5 DBDMOD .MODEL DBDMOD D (IS=2.23e-12 RS=2.28e-3 TRS1=2.98e-3 +TRS2=2.22E-12 CJO=7.55e-9 TT=4e-8)
Lgate 1 9 1e-12 ; Ldrain 2 5 1e-12 Lsource 3 7 1e-12 Rgate 9 20 1	Step 11	Lgate 1 9 5e-9 Ldrain 2 5 1e-9 Lsource 3 7 3e-9 Rgate 9 20 1.2
Cin 6 8 1e-15 ;	Step 12	Cin 6 8 4.48e-9
Dplcap 10 5 DPLCAPMOD ; .MODEL DPLCAPMOD D (CJO=0 IS=1e-30 N=10) Esg 6 10 6 8 1	Step 13	Dplcap 10 5 DPLCAPMOD .MODEL DPLCAPMOD D (CJO=2.14e-9 IS=1e-30 N=10) Esg 6 10 6 8 1
Ca 12 8 1e-15 ; S1a 6 12 13 8 S1AMOD S1b 13 12 13 8 S1BMOD .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-3 VOFF=-1) .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-1 VOFF=-3) Egs 13 8 6 8 1	Step 14	Ca 12 8 8.98e-9 S1a 6 12 13 8 S1AMOD S1b 13 12 13 8 S1BMOD .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-2.48 VOFF=-0.48) .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-0.48 VOFF=-2.48) Egs 13 8 6 8 1
Cb 15 14 1e-15 ; S2a 6 15 14 13 S2AMOD S2b 13 15 14 13 S2BMOD .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-2.5 VOFF=2.5) .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=2.5 VOFF=-2.5) Eds 14 8 5 8 1	Step 15	Cb 15 14 8.81e-9 S2a 6 15 14 13 S2AMOD S2b 13 15 14 13 S2BMOD .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-2.25 VOFF=2.75) .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=2.75 VOFF=-2.25) Eds 14 8 5 8 1
Rin 6 8 1e9 ;	Step 16	Rin 6 8 1e9
.ENDS		.ENDS

OBTAINING EXPERIMENTAL DATA

When the authors experienced difficulty in parameter extraction the problems were traceable to erroneous data in all cases. The following caveats are offered:

1. Obtain all data from a single device.
2. Read gate voltage data to the nearest 0.01 volt.
3. Employ Kelvin sensing to the package leads.
4. Avoid self heating (a difficult assignment)
5. Inconsistencies lurk in data sheet curves and specifications.

FINAL MODEL

The final model for the RFH75N05 is shown in Table 3 and serves as an aid to understanding as it is developed from the template.

STEP 1 - MODEL MOSMOD (VTO AND KP)

The square root of drain current is plotted versus the gate to source voltage for the MOSFET in the saturated regime; a straight line results. The zero current intercept defines VTO and the slope defines the square root of (KP/2). Vary VTO and KP to obtain the best fit to data for the low to medium current experimental data at 25°C.

VTO is not the threshold voltage as measured. In order to use the algorithm of the PSpice® Level 1 model, W(the channel width) and L(the channel length) are defined as one micron. Therefore KP times W divided by L reduces to the model value called KP. Likewise IS, N, and TOX are set to values chosen to avoid other algorithm problems. Figure 20 shows the PSpice® generated curve after the correct values of KP and VTO of model MOSMOD are chosen.

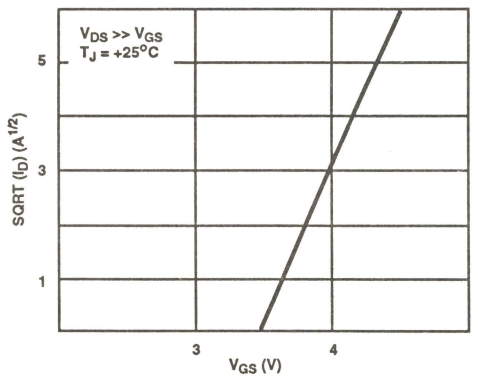

FIGURE 20. SQUARE ROOT OF I_D

STEP 2 - V_{TO}

The threshold voltage is set by fixing the value of V_{TO}. Threshold voltage of a power MOSFET is usually measured in the saturated regime at a low current, typically 1mA. If the PSpice® model is run at 25°C with the gate and drain voltage equal, a voltage will be found to yield 1mA drain current. V_{TO} is this voltage reduced by the measured threshold voltage. The value identified was 0.6 volts.

STEP 3 - R_{SOURCE}

The straight line curve of Figure 20 is modified by a chosen value of R_{SOURCE} in order to better fit the measured data for medium to high currents at 25°C. This is shown in Figure 21, where 2E-3 provided the best fit.

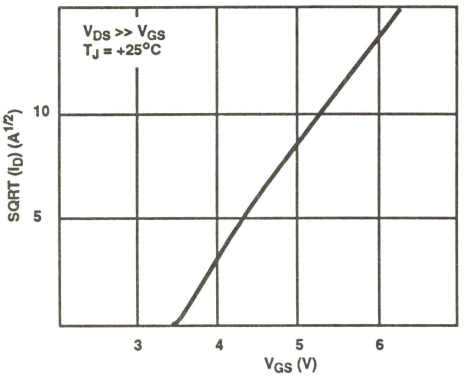

FIGURE 21. SQUARE ROOT OF I_D

STEP 4 - R_{DRAIN}

R_{DRAIN} is chosen to fix the PSpice® calculated $R_{DS(ON)}$ value to the measured value at 25°C when the template is biased to the gate voltage and drain current of the specifications. Do not use the specified maximum of $R_{DS(ON)}$. The value developed was 3.07E-3.

STEP 5 - MODEL RDSMOD (TC1 AND TC2)

R_{SOURCE} and R_{DRAIN} are assumed to have the same temperature coefficients. Although this is not accurate, it is convenient and is deemed to be sufficient for this purpose. If $R_{DS(ON)}$ is measured as a function of temperature, best fit can be obtained by appropriately choosing TC1 and TC2 values of 5.2E-3 and 1.37E-5. $R_{DS(ON)}$ is shown in Figure 22.

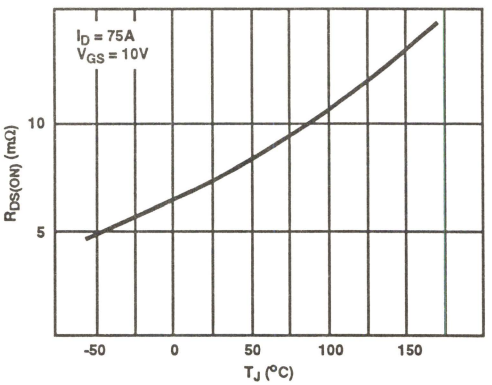

FIGURE 22. $R_{DS(ON)}$ vs TEMPERATURE

STEP 6 - MODEL RVTOMOD (TC1 AND TC2)

The plot of Figure 21 must be modified to add curves at low and high temperature. A temperature sensitive additive or subtractive voltage is placed in series with the gates of Mos1 and Mos2 by use of E_{VTO}. A 1 volt drop equal to It times R_{VTO} is canceled by a 1 volt supply, V_{BAT} and applied to E_{VTO}. By choosing the values of TC1 and TC2 for model RVTOMOD, the voltage of E_{VTO} is made temperature sensitive. The result is shown in Figure 23, where TC1 and TC2 were chosen for best fit at -3.78E-3 and -7.51E-7.

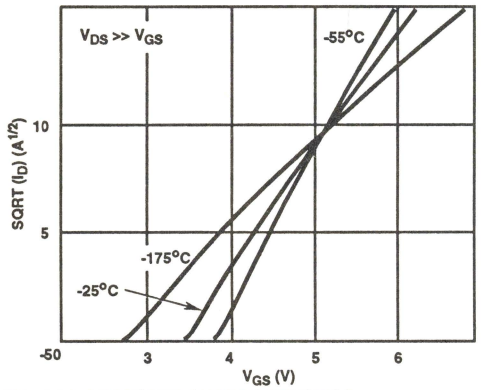

FIGURE 23. TRANSFER CHARACTERISTICS vs TEMPERATURE

STEP 7 - E_{BREAK}

E_{BREAK} derives a thermally variant voltage from the product of I_T and R_{BREAK} equal to 1.00 volt at 25°C. When the drain voltage rises sufficiently, diode D_{BREAK} provides a voltage clamp to E_{BREAK}. The value of the E_{BREAK} multiplier is equal to the low current value of BV_{DSS} less the forward drop of D_{BREAK}. The multiplier was set at 58.4 for the final model.

STEP 8 - MODEL RBKMOD (TC1 AND TC2)

The low current breakdown voltage of the MOSFET may be measured at several temperatures, such that TC1 and TC2 may be determined for model RBKMOD. Figure 24 plots the low current breakdown voltage as a function of temperature as modeled with TC1 and TC2 equal to 9.5E-4 and -1.17E-6.

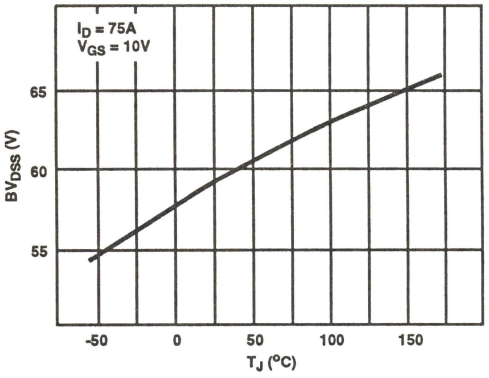

FIGURE 24. BREAKDOWN vs TEMPERATURE

STEP 9 - MODEL DBKMOD (RS, TRS1 AND TRS2)

Although reliable data is difficult to obtain for the breakdown voltage at many tens of amperes, it can be done with a small inductive flyback circuit of very low duty cycle. RS of the diode D_{BREAK} may be determined at 25°C. TRS1 and TRS2 may be determined with similar measurements at several temperatures. The curves of Figure 25 present the modelled behavior for RS, TRS1 and TRS2 equal to 8E-2, 2.5E-3, and 0.

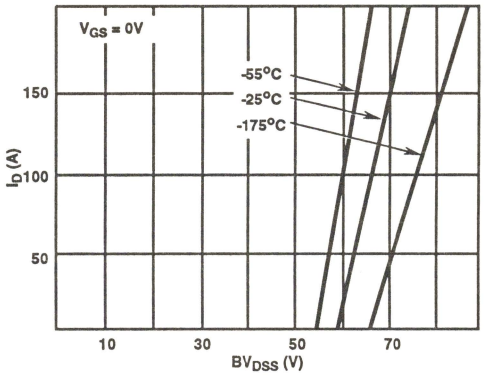

FIGURE 25. BREAKDOWN vs TEMPERATURE

STEP 10(a) - MODEL DBDMOD (IS, RS, TRS1 and TRS2)

When operating D_{BODY} in the forward mode, one may develop IS and RS at 25°C assuming a diode ideality value of 1.0, the default value. Measurements at elevated current levels and several temperatures will define TRS1 and TRS2. Measurements are taken with V_{GS} equal to zero. Figure 26 presents the body diode forward characteristics for several temperatures where IS, RS, TRS1, and TRS2 are found to equal 2.23E-12, 2.28E-3, 2.98-E3, and 2.22E-12.

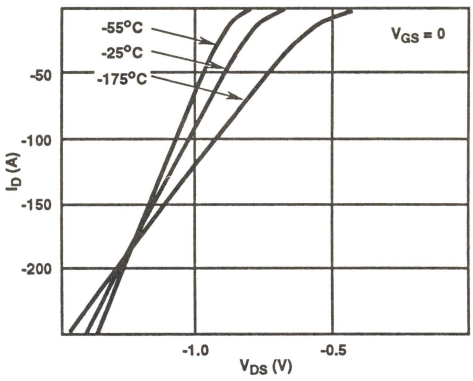

FIGURE 26. BODY DIODE CURVES

STEP 10(b) - MODEL DBDMOD (CJO, TT)

Coss minus C_{RSS} may be determined at 25 volts and 25°C. Then CJO is this value when adjusted to zero drain volts by the factor of the square root of (25+0.7) or 5.07. For the example this equals 7.55E-9.

In order to determine TT, equipment similar to the Bermar SM30 may be used. This equipment forces a forward body diode current (If) for a sufficiently long period of time, after which a linear amplifier with high current capability ramps the diode current off at a constant rate, di/dt. (Feedback control is used.) The diode current equals zero at time T_F, after the ramp off is initiated. The current continues to ramp, extracting charge from the diode, for an added time T_A. At this time, the constant ramp (di/dt) can no longer be maintained and the reverse current has attained a maximum. TT may be solved [12] and entered using:

$$TT = T_A/(1-\exp(-(T_A+T_F)/TT))$$

The value of TT was determined to equal 4E-8.

STEP 11 - L_{GATE}, L_{DRAIN}, L_{SOURCE}, R_{GATE}

L_{GATE}, L_{DRAIN}, L_{SOURCE}, and R_{GATE} may be measured, estimated or calculated and entered. An approximation for the inductances in nH may be calculated using:

$$L = (5)(length)(\log_e(4(length/diam))) \text{ nH}$$

where wire length and diameter are in inches [13]. Values of Lgate, Ldrain, Lsource, and Rgate were approximated at 5E-9, 1E-9, 3E-9, and 1.2 for the final model.

CAPACITANCES

The capacitances are derived from the measured gate charge curve of Figure 27. They will require some iteration and some judgement calls as will be explained.

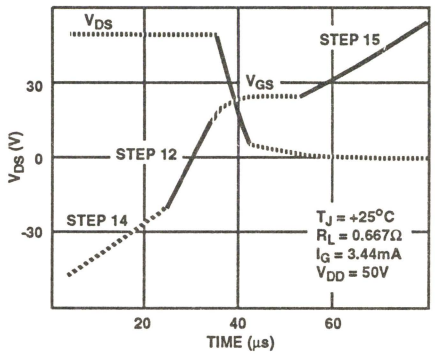

FIGURE 27. GATE CHARGE CURVES

STEP 12 - C_{IN}

The value of C_{IN} should be chosen for best fit to the solid line portion of the V_{GS} curve of Figure 27 labeled step 12. A value of 4.48E-9 was found to provide a good fit.

STEP 13 - MODEL DPLCAPMOD (CJO)

A feedback capacitor is modelled by using the junction capacitance of a reverse biased diode, D_{PLCAP} as defined by model DPLCAPMOD. IS and N of model DPLCAPMOD were chosen to avoid undesired diode effects. CJO is chosen as 2.14E-9 to best fit the solid line portion of the V_{DS} curve of Figure 27.

STEP 14 - C_A, MODELS S1AMOD and S1BMOD (VON and VOFF)

The value of C_A is chosen to be 8.98E-9 to best parallel the dotted line portion of the V_{GS} curve of Figure 27 labelled step 14.

In order to match the dotted line portion it may be necessary to increment VON and VOFF of both model S1AMOD and model S1BMOD. Note that all four values must be incremented by an identical amount before making a PSpice® run. This incremental change will vertically displace the slope provided by C_A. The transition voltages of S1A and S1B must always be negative values.

The sharpness of transition between the dashed line of step 14 and the solid line of step 12 may be adjusted if necessary by changing the increment between VON and VOFF equally for both S1A and S1B.

STEP 15 - C_B, MODELS S2AMOD and S2BMOD (VON and VOFF)

The value of C_B is chosen to be 8.81E-9 to best parallel the solid line portion of the V_{GS} curve of Figure 27 labelled step 15.

In order to match the solid line portion it may be necessary to increment VON and VOFF of both model S2AMOD and model S2BMOD. Note that all four values must be incremented by an identical amount before making a PSpice run. This increment change will horizontally displace the slope provided by C_B.

The sharpness of transition between the solid line and the low voltage dotted line of the V_{DS} curve may be adjusted if necessary by changing the increment between VON and VOFF equally for both S2A and S2B. It is recommended that this increment be small, of the order of several volts.

STEP 16 - R_{IN}

R_{IN} can be set to a very large value such as 1E15. However it is recommended that it be chosen low enough to cause 10nA to flow at a gate bias of moderately high voltage, typically 1E9 ohms. Rin functions to provide an initial gate reference voltage near zero even though the Modeler may choose to drive the MOSFET from a current generator.

EPILOGUE

The final model is completed as shown in Table 3. One may iterate through the steps if desired, but it should not be necessary. Any changes made in the model outside of the above routine should be minimal, if at all.

Anomalies

Some commercially available power MOSFETs exhibit anomalous behavior which is not modelled in this work.

THE VERTICAL JFET PROBLEM

A vertical JFET type of structure exists in the VDMOS device used for the industry standard power MOSFET. Many works describe this portion of the device, including Wheatley, et al [14]. The N^- lightly doped drain region reaches to the surface

of the silicon die, which is bounded by the P doped body. This region of N^- is often called the neck of the MOSFET. As the breakdown voltage of the device is designed for increasing values, the depletion layer extends further within the neck laterally, for relatively low drain voltages. In this manner, the neck or vertical JFET becomes pinched off, causing the $R_{DS(ON)}$ to exhibit excess non-linearity with current. In addition an abrupt limiting of the drain current (at large values of drain voltages) occurs for increasing values of gate voltage. This current limiting has a highly localized thermal assist constrained to the neck with time responses in the microsecond region. This anomaly may be suppressed by increasing the neck width and/or implanting a low dose of N type dopant into the neck, just below the surface.

Devices of this type are not properly modelled.

NON OHMIC CONTACT PROBLEMS

Some commercially available devices exhibit a non-ohmic series contact resistance from the metallization to the silicon. This seldom happens with present day devices, but, when present, it is most likely to occur from source metal to source silicon for N channel devices, and from drain metal to drain silicon for P channel devices. The effect is seen as a low current non-linearity in $R_{DS(ON)}$ vs drain current for the former case and an excessive voltage drop for the body diode for the latter case.

Devices of this type are not properly modelled.

Conclusions

An equivalent circuit model for power MOSFETs that is suitable for use with PSpice® has been demonstrated. The model requires no modifications to the PSpice® algorithms. The model features global temperature representation from -55°C to 175°C for the first time. It addresses static and dynamic behavior over the normal circuit operating range of the device, including 1st and 3rd quadrant MOSFET operation, high current avalanche breakdown operation, body diode stored charge effects, gate charge non-linearities, gate equivalent series resistance (ESR), and package inductances. Gate propagation delay is not modelled [15]. The sub-circuit is empirical in nature and the parameters may be readily extracted by use of terminal measurements. Experimental verification shows excellent agreement between measured and simulated results over the entire thermal, static, and dynamic regimes.

Recommendations For Future Work

A supporting program of algorithms should be written to address the parameter extraction effort.

Accurate testing for characterization of power MOSFETs as a function of temperature is required. Studies should be made to identify and correct methods prone to testing error.

PSpice® algorithms should be modified to refine and incorporate many of the findings of this work into a new MOS level.

If a new MOS level is formed, a modification should be made to the drain current equation in the linear regime to accommodate the non-uniform channel surface concentration of the power MOSFET as described elsewhere. If done, the MOSFET may be more closely modelled in the linear regime of the output characteristic curves and the third quadrant MOSFET regime. (See Figure 9 and Figure 19.) The authors suggest a user defined model value WH to be used in a multiplier which would be applied to Id in the linear regime such that:

$$\text{Multiplier} = (1+WH*(1-V_{DS}/(V_{GS}-V_{TO}))^2)$$

If the multiplier were applied to the MOSFET of Table 3, the 1st and 3rd quadrant characteristics would be approximately as shown in Figure 28 for V_{GS} = 5 volts. Here, WH is shown for values of 0, 1, and 2. The drain and source are interchanged for $V_{DS} < 0$, as is done in PSpice®.

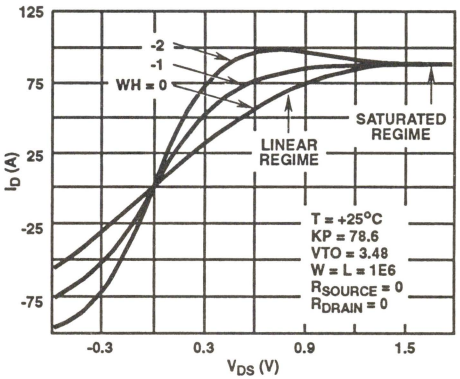

FIGURE 28. THE WH ADJUSTMENT

A value of zero for WH forces the multiplier to equal unity for all values of V_{DS}, thereby retaining the original linear regime equation. Zero should be the default value. Any value of WH greater than 1 results in a negative output resistance and is unacceptable. Therfore WH is bounded by 0 and 1.

If this multiplier option were offered, it would be extracted for the model MOSMOD between steps 3 and 4 of Table 2, probably requiring some iteration between WH and Rdrain.

Acknowledgements

The authors express appreciation to Don Burke, Gene Freeman, Nick Magda, Hal Ronan, and Wally Williams for their support and assistance.

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UNDERSTANDING POWER MOSFETs

Author: Tom McNulty

Power MOSFETs (**M**etal **O**xide **S**emiconductor, **F**ield **E**ffect **T**ransistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the body by silicon contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor present a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Figure 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Figure 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely different from that of a bipolar transistor, which always retain its n-p-n characteristic.

By virtue of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful by-product of the MOSFET process is the internal parasitic diode formed between source and drain, Figure 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

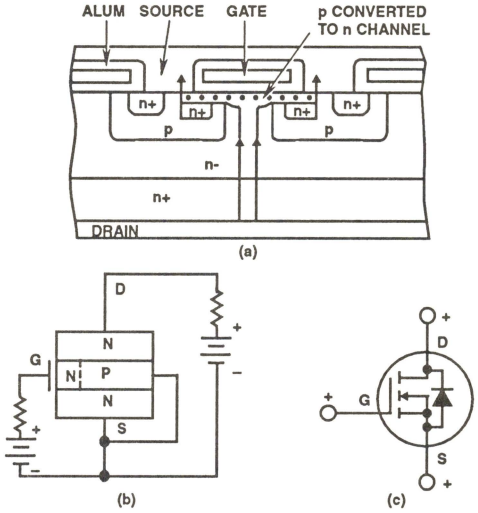

FIGURE 1. THE MOSFET, A VOLTAGE-CONTROLLED DEVICE WITH AN ELECTRICALLY ISOLATED GATE, USES MAJORITY CARRIERS TO MOVE CURRENT FROM SOURCE TO DRAIN (A). THE KEY TO MOSFET OPERATION IS THE CREATION OF THE INVERSION CHANNEL BENEATH THE GATE WHEN AN ELECTRIC CHARGE IS APPLIED TO THE GATE (B). BECAUSE OF THE MOSFETs CONSTRUCTION, AN INTEGRAL DIODE IS FORMED ON THE DEVICE (C), AND THE DESIGNER CAN USE THIS DIODE FOR A NUMBER OF CIRCUIT FUNCTIONS.

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Structure

Harris Power MOSFETs are manufactured using a vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cell varies according to the dimensions of the chip. For example, a 120-mil^2 chip contains about 5,000 cells; a 240-mil^2 chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(ON)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(ON)}$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_N, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(ON)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(ON)}$ value:

$r_{DS(ON)} = R_N/N$, where N is the number of cells.

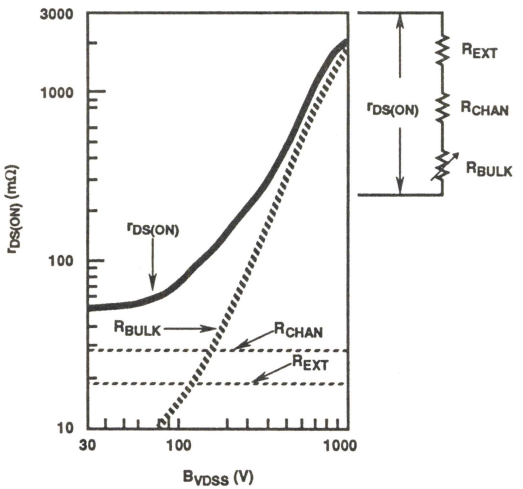

FIGURE 2. THE DRAIN-TO-SOURCE RESISTANCE ($r_{DS(ON)}$ OF A MOSFET IS NOT ONE BUT THREE SEPARATE RESISTANCE COMPONENTS)

TABLE 1. PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

B_{VDSS}	40V	150V	500V
$R_{CHANNEL}$	50%	23%	2.4%
R_{BULK}	35%	70%	97%
$R_{EXTERNAL}$	15%	7%	<1%

In reality, $r_{DS(ON)}$ is composed of three separate resistances. Figure 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(ON)}$. The value of $r_{DS(ON)}$ at any point of the curve is found by adding the values of the three components at that point:

$$r_{DS(ON)} = R_{BULK} + R_{CHAN} + R_{EXT}$$

where R_{CHAN} represents the resistance of the channel beneath the gate, and R_{EXT} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{BULK} represents the resistance resulting from the narrow neck of n material between the two players, as shown in Figure 1(a), plus the resistance of the current path below the neck and through the body of the device to the drain.

Note in Figure 2 that R_{CHAN} and R_{EXT} are completely independent of voltage, while R_{BULK} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(ON)}$ is dominated by the sum of R_{CHAN} and R_{EXT}. Above 150 volts, $r_{DS(ON)}$ is increasingly dominated by R_{BULK}. Table 1 gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(ON)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(ON)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{BULK} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and more resistive to support high voltages, the bulk component of resistance rapidly increases (see Figure 2) and begins to dominate the channel and external resistance. The $r_{DS(ON)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(ON)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(ON)}$ in Figure 2 holds only for a relatively small chip. Using a larger chip results in a lower value for $r_{DS(ON)}$ because a large chip has more cells (See Figure 3). A larger chip also increases MOSFET breakdown voltage capability.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(ON)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the original. Although the cost does not rise exponentially, it is substantially more than the original cost.

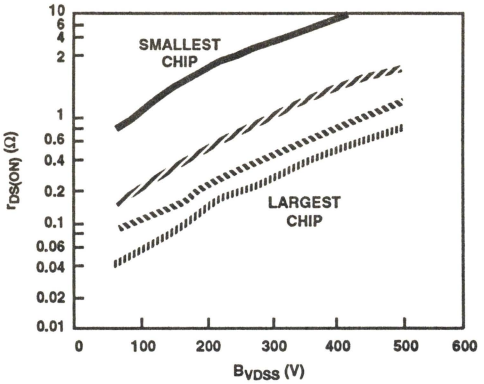

FIGURE 3. AS CHIP SIZE INCREASES, $r_{DS(ON)}$ DECREASES, & VOLTAGE HANDLING CAPABILITY INCREASES

Effects of Temperature

The high operating temperatures of bipolar transistors area frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slowdown as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Figure 4.

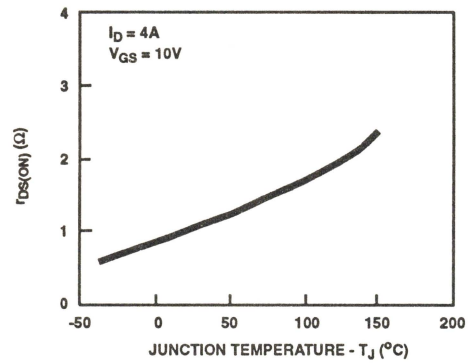

FIGURE 4. MOSFETs HAVE A POSITIVE TEMPERATURE COEFFICIENT OF RESISTANCE, WHICH GREATLY REDUCES THE POSSIBILITY OF THERMAL RUNAWAY AS TEMPERATURE INCREASES

The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Figure 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R, and capacitance, C. The capacitance, called C_{ISS} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

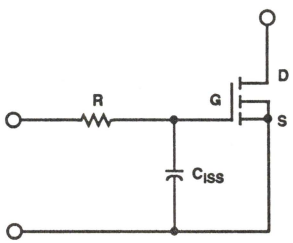

FIGURE 5. A MOSFETs SWITCHING SPEED IS DETERMINED BY ITS INPUT RESISTANCE R AND ITS INPUT CAPACITANCE C_{ISS}

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure (R in Figure 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFET in high-frequency (greater than 20MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from

datasheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20W/□. But whereas the total R value is not found on datasheets, the C value (C_{ISS}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{ISS} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1MHz to 10MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic, shown in Figure 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage (gs). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{GS} level required to operate a MOSFET, note, from Figure 6, that the device is not turned on (no drain current flows) unless V_{GS} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally V_{GS} for many types of DMOS devices is at least 2V. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Figure 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10V, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5V, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of l0V, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

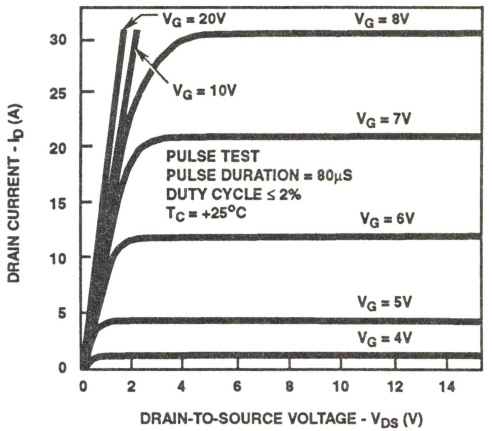

FIGURE 6. MOSFETs REQUIRE A HIGH INPUT VOLTAGE (AT LEAST 10V) IN ORDER TO DELIVER THEIR FULL RATED DRAIN CURRENT

No. AN7254.1 May 1992

SWITCHING WAVEFORMS OF THE L²FET: A 5 VOLT GATE-DRIVE POWER MOSFET

Author: C. Frank Wheatley, Jr. and Harold R. Ronan, Jr.

The switching waveforms of a newly announced series of power MOSFET devices called Logic Level FETs (L^2FETs) and featuring a 5V gate drive are presented and contrasted with those of the more conventional 10V gate drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascade from a low voltage lateral MOS. The 2:1 advantage in rise and fall time and the 4:1 reduction in switching "dynamic $V_{(SAT)}$" dissipation with constant drive power of the L^2FET over the 10V MOSFET are demonstrated and discussed

Background

A new series of power MOSFET devices called Logic Level FETs, or L^2FETs, is compatible with the 5V power supply used for logic circuitry. L^2FETs retain the on resistance, drain current, and blocking voltage ratings of their 10V predecessors, but operate from a much less costly 5V supply.

The reduction in gate drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100nm to 50nm (500Å). Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, halving the insulator thickness halves the applied gate voltage without compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L^2FET over its 100nm predecessor, where gate drive power is the same for both devices. The "dynamic $V_{(SAT)}$" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded gate, depletion mode, vertical JFET driven in cascade by a grounded source, enhancement mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L^2FET Characteristics Compared to Standard Types - A Brief Review

Thirty-two different power MOSFETs of the L^2FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figures 1, 2, and 3, which are comparisons of the industry standard RFM10N15 with its Logic Level FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L^2FET product currently available is limited to n-channel devices handling 200V or less, with 15A ratings or less.)

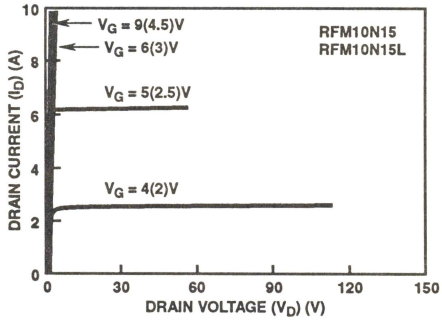

FIGURE 1. DRAIN CURRENT vs. DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES

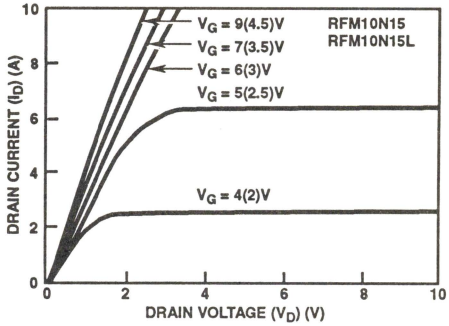

FIGURE 2. DRAIN CURRENT vs. LOW DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES DEMONSTRATING THAT R_{ON} HAS NOT BEEN SACRIFICED IN THE L^2FET

Figures 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L^2FET gate voltage is in parenthesis. The low drain voltage curves of Figure 2 demonstrate that RON has not been sacrificed in the L^2FET. Figure 3 is the transfer characteristic comparison

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for three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, L values are in parenthesis. It is evident from the curve that:

1. The threshold voltage is scaled down by a factor of two for the L^2FET.
2. The threshold voltage temperature coefficient in mV/°C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L^2FETs have similar relationships to their respective predecessors.

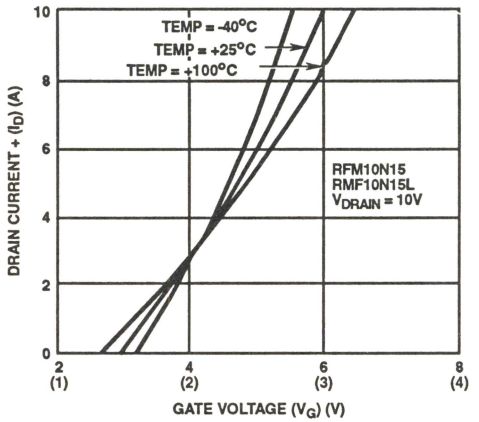


FIGURE 3. TRANSFER CHARACTERISTIC

Switching Waveforms with Conventional Drive

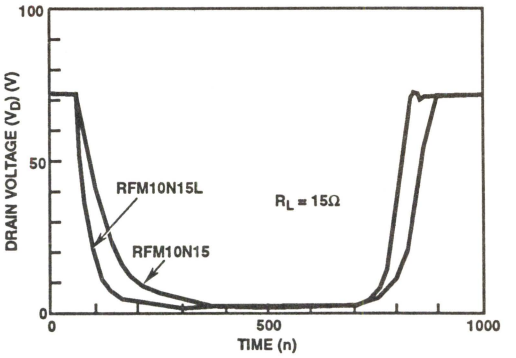
The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal". If the standard device is driven between zero and ten volts with an R_G of 25Ω, impedance transformation dictates that the L^2FET should be driven between zero and five volts with an R_G of $6^1/_4$ Ω, thereby transforming open circuit voltage and short circuit current by factors of 2 (or $^1/_2$). With these parameters, either drive system will supply a peak R_G, or generator dissipation, of one watt.

Figure 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5A, 75V resistive load line. The time scale is 100ns per division. The table under the graph compares on delay time, rise time, off delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input voltage and output voltage waveforms.

Note that:

1. The rise and fall times are not symmetrical
2. The L^2FET is faster
3. There is a "dynamic $V_{(SAT)}$" type of behavior
4. The "dynamic $V_{(SAT)}$" is of a lesser amplitude for the L^2FET

These observations are discussed below.



TYPE	GATE DRIVE	R_G (Ω)	$t_{D(ON)}$ (ns)	$t_{(RISE)}$ (ns)	$t_{D(OFF)}$ (ns)	$t_{(FALL)}$ (ns)
RFM10N15 (100nm)	0-10V	25	15	120	123	73
RFM10N15L (50nm)	0-5V	6.25	11	57	104	62

FIGURE 4. DRAIN VOLTAGE vs. TIME CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES

Switching Waveforms with Constant Current Drive

The power MOSFET is a current driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first order approximation to a constant current where the voltage compliance is determined by ground potential or the drive circuit power supply voltage. The on current may not equal the off current; this situation is addressed below.

Figure 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{G1} = I_{G2}$, with gate voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L^2FET receives less drive power or energy. The value for I_{G1} and I_{G2} was chosen as 5mA; the time scale is 1μs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic $V_{(SAT)}$" even at slow switching speeds.

4. The "dynamic $V_{(SAT)}$" curves are symmetrical during the low drain voltage portion of the turn on and turn off portion.
5. The "dynamic $V_{(SAT)}$" curves are lower in amplitude by a factor of approximately two for the L^2FET.

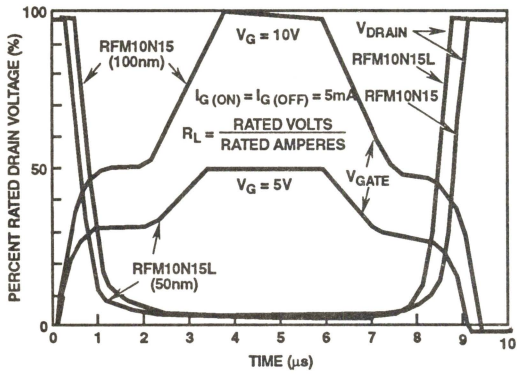


FIGURE 5. CHARACTERIZATION CURVES FOR REPRESENTATIVE DEVICES DRIVEN FROM A CURRENT GENERATOR

Large Signal Equivalent Circuit of the MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional power MOSFET must first be understood. Figure 6 shows a properly proportioned cross sectional view of the power MOSFET.

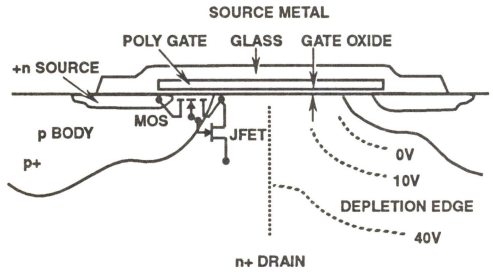


FIGURE 6. CROSS SECTION OF POWER MOSFET

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n+ region usually though of as being the MOSFET drain. This situation is shown in Figure 6, where the cross sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Figure 6. The right half indicates the edge of the depletion width for several drain voltages. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Figure 7. Note that the third quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

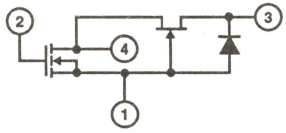


FIGURE 7. SCHEMATIC REPRESENTATION OF THE CROSS SECTION OF FIGURE 6

Interelectrode Capacitance

The equivalent circuit of Figure 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the small signal equivalent circuit of the MOS and JFET. Of course, the MOS and JFET small signal equivalent circuits are nonlinear functions of voltage and current and invariant with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three terminal characterization of this four node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reduces the power MOSFET to the capacitor network of Figure 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

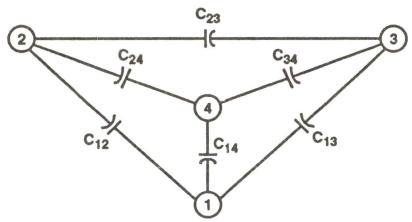


FIGURE 8. CAPACITOR NETWORK REPRESENTATION OF THE POWER MOSFET

When current does flow, node (4) of Figure 7 is a low impedance node due to the source follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate to Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Figure 6 shows that the gate to source capacitance (C_{12}) is that from the poly gate upward through the thick oxide to the source metal. In addition, there is a contribution from the poly gate to the n+ source through the thin gate oxide. Additionally a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate to Drain Capacitance, C_{23}

Capacitor C_{23} exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C_{23} exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate to Internal Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the middle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulation layer ceases to exist when the external drain voltage minus the IR drop through the n- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

Waveforms Expected from the Model

The following discussion relates the prior model discussion to the waveforms of Figure 5. The discussion begins with the gate voltage at +5V or +10V and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to I_D(max) and the drain voltage equals I_D(max) times R_{DS}(ON).

Gate Voltage Slope - t_{OFF} Delay

As time progresses, I_G = -5mA, which must flow through C_{12} + C_{23} + C_{24} of Figure 8 because the MOS and JFET are both heavily biased into conduction. Therefore, $dV_4/dt = dV_3/dt$ = nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_G/dt = I_G/(C_{12} = C_{24}) \quad (1)$$

Gate Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no longer flows from C_{12} during the constant gate voltage plateau.

Drain Voltage Shallow Slope

Since C_{23} is still zero, all gate current must flow from C_{24}. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Figure 7 must ramp at linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_D/dt = I_G/C_{24} \quad (2)$$

Again this curve will approximate a straight line.

Drain Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n- voltage directly beneath the gate oxide, and differs from the drain voltage by an amount nearly equal to $I_D r_{DS}$(on).)

Since the drain voltage is still fairly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_D/dt.

JFET Pinch Off Voltage - Drain Voltage Steep Slope

As the drain voltage approaches the pinch off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET sour-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain voltage waveform.

Gate Voltage Slope - $t_{(ON)}$ Delay

When the drain is totally off, most of the gate current flows from C_{12}. Again, this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_G/dt = I_G/C_{12} \quad (3)$$

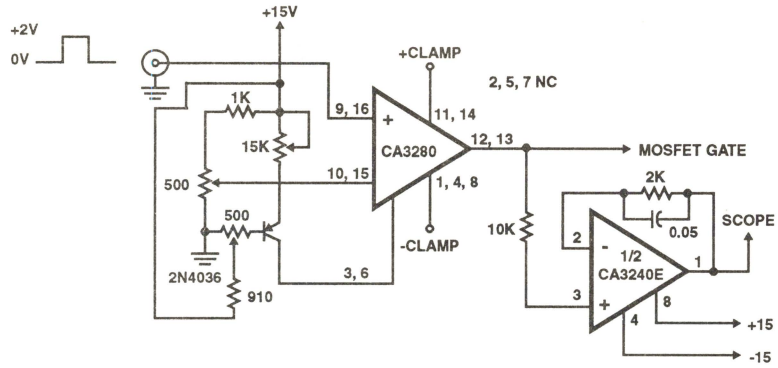


FIGURE 9. TEST CIRCUIT

New Switching Characterization for Power MOSFETs

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive circuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit - Drive

A test circuit is shown in Figure 9. The heart of this circuit is the Harris CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Figure 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximately 0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads parallel to the chips rather than wiring many sockets. However, this arrangement may require an increase in the bypass capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1mΩ or 10mΩ shunting impedance of the scope would load the high impedance circuitry associated with the MOSFET gate.

Testing Conditions

A pulse generator is set for 50µs on time duration and approximately 25ms repetition rate (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several µs exists at the +10V level. Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased to maximum rated value. The L^2FETs would be tested at +5V gate clamp.

Figure 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Figure 10(a) is the 3V signal to the CA3280. Figure 10(b) is the power MOSFET gate current. In this example, the amplitude is ±1mA with a third state of 0mA. Figure 10(c) displays the gate voltage and the drain voltage, 10V peak-to-peak and 150V peak-to-peak. Figure 10(d) is a piece wise linear approximation of Figure 10(c). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Figure 10 is 100µs full scale.

There are some features of the gate and drain voltage waveforms that should be noted. These features are consistent with the equivalent model discussion.

1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time. Exceptions will occur for very fast or very slow switching, and for nonsymetrical current drive. These exceptions are discussed in the following.

2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS}(on)$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

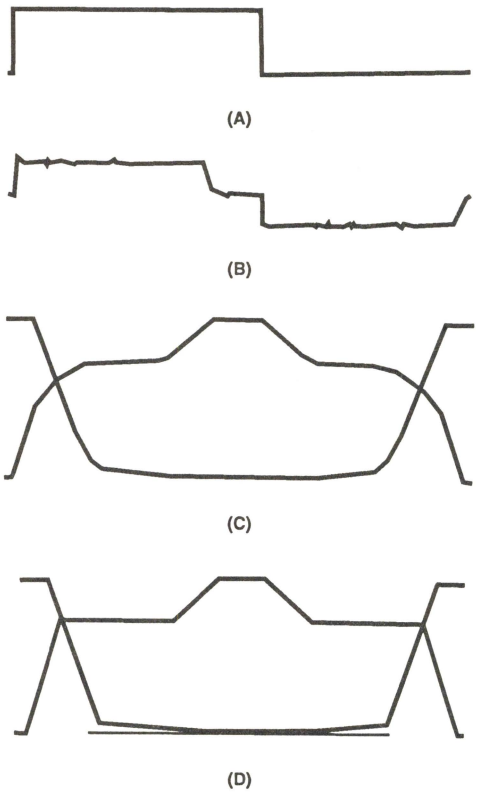


FIGURE 10. (A) 3V SIGNAL TO THE CA3280, (B) POWER MOSFET GATE CURRENT, (C) GATE AND DRAIN VOLTAGE, (D) PIECE WISE LINEAR APPROXIMATION OF 10(C)

Application of the Switching Data

Figure 11 is a family of curves similar to Figure 10(C), where the drain supply voltage is fixed at four values. Note that the ordinate is 10V full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_G) microseconds full scale, where I_G is the actual gate drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

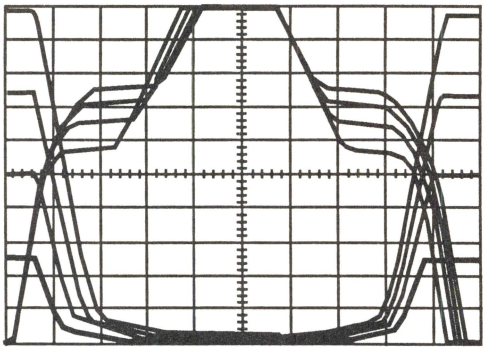


FIGURE 11. CURVES SIMILAR TO THOSE OF FIGURE 10(C) WITH DRAIN SUPPLY VOLTAGE FIXED AT FOUR VALUES

Symmetrical Current Drive

Waveforms of Figure 11 will scale in an inverse manner with gate current. Driving current was varied from ±200mA to ±2μA for the device of Figure 11. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Figure 12 and compared to the inverse scaling suggested by Figure 11.

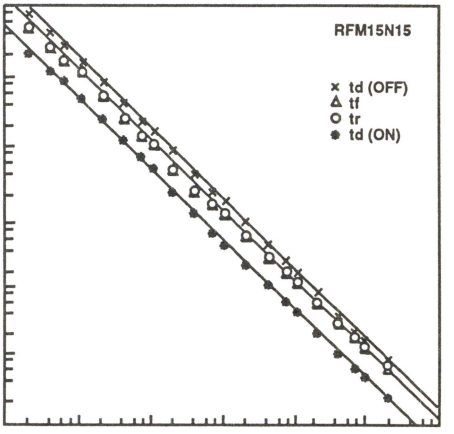


FIGURE 12. VARIOUS TIME MEASUREMENTS COMPARED TO THE INVERSE SCALING SUGGESTED BY FIGURE 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the

inverse scaling. This condition was not noted on Figure 12 for gate currents as low as ±2μA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. As a result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Figure 12, even though the gate current was increased to ±200mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piecewise linear methods will yield the gate current, which will permit the proper piecewise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Figure 11 dividing it into 10 equal voltage segments; for example, V_G = 0, 1, 2, . . . 9, 10V.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piecewise linear gate current for each time segment. I_{G1} = (10 - 0.5)/100 = 95mA, I_{G2} = (10 -1.5)/100 = 85mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Figure 11 corresponding to an average gate voltage of 9.5,8.5, . . . 1.5, 0.5 volts. Call these segments 11,12,... 19,20.
7. In that the pulse-generator voltage is now zero volts, calculate I_G as:
   I_{G11} = (0-9.5)/100 = -95mA, I_{G12} = (0-8.5)/100 = -85mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Figure 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Figure 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

Gate Voltage Propagation Effects

Most power MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage waveform applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figures 13(A), (B), and (C) show the increasing effect of gate voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Figure 13(C).

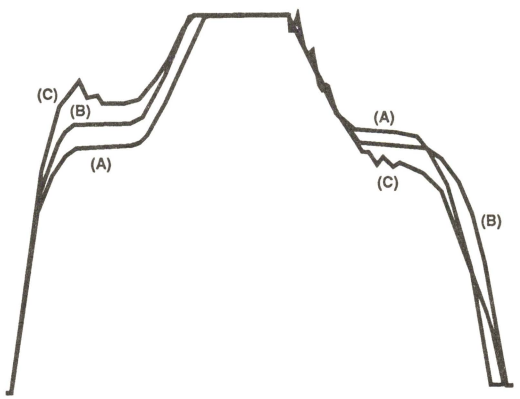


FIGURE 13. CURVES SHOWING THE INCREASING EFFECT OF GATE VOLTAGE PROPAGATION

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher R_{ON}).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield "breakthrough" devices unless used in combination.

Any of the previous methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of R_{ON} per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

References

1. "Power MOSFET Switching Waveforms - A New Insight," H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.
2. "Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed," E. Oxner, Proc. Powercon 9, April 1982.

APPNOTE

No. AN7260.2 September 1993

POWER MOSFET SWITCHING WAVEFORMS: A NEW INSIGHT

Author: Harold R. Ronan, Jr. and C. Frank Wheatley, Jr.

The examination of power MOSFET voltage and current waveforms during switching transitions reveals that the device characterization now practiced by industry is inadequate. In this Note, device waveforms are explained by considering the interaction of a vertical JFET driven in cascode from a lateral MOSFET in combination with the interelectrode capacitances. Particular attention is given to the drain-voltage waveform and its dual-slope nature. The three terminal capacitances now published by the industry are shown to be valid only for zero drain current. For cases where the gate drive is a voltage step generator with internal fixed resistance, the drain voltage characteristics are inferred from the gate current drive behavior and compared to observed waveforms. The nature of the "asymmetric switching times" is explained.

A waveform family is proposed as a more descriptive and accurate method of characterization. This new format is a plot of drain voltage and gate voltage versus normalized time. A family of curves is presented for a constant load resistance with V00 varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

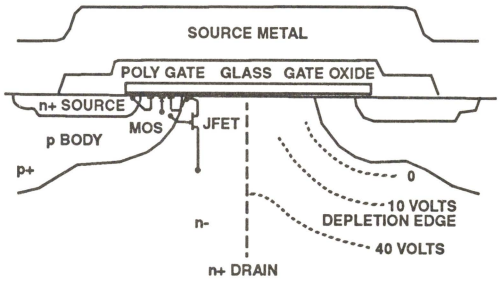


FIGURE 1. CROSS-SECTIONAL VIEW OF MOSFET SHOWING EQUIVALENT MOS TRANSISTOR AND JFET

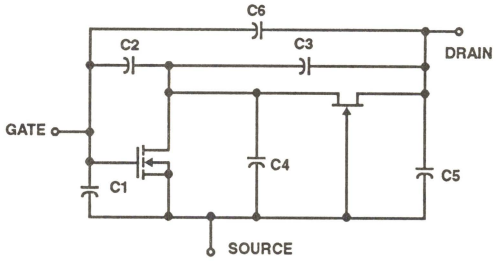


FIGURE 2. MOS TRANSISTOR WITH CASCODE-CONNECTED JFET AND ALL CAPACITORS

Device Models

The keystone of an understanding of power MOSFET switching performance is the realization that the active device is bimodal and must be described using a model that accounts for the dual nature. Buried in today's power MOSFET devices is the equivalent of a depletion layer JFET that contributes significantly to switching speed. Figure 1 is a cross-sectional view of a typical power MOSFET, with MOSFET/JFET symbols superimposed on the structure.

Figure 2 is obtained by taking the lateral MOS and vertical JFET from this conception and adding all the possible node-to-node capacitances. Computed values of the six capacitances for a typical device structure suggest that device behavior may be adequately modeled using only three capacitors in the manner of Figure 3. This is the model to be employed for analysis and study

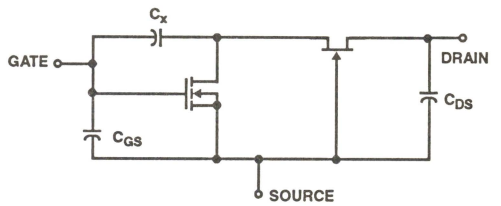


FIGURE 3. FIGURE 2 SIMPLIFIED

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Gate Drive: Constant Voltage or Constant Current

Before moving on to the study of the equivalent circuit states of the model, a gate-drive forcing function which is easy to represent, relates to reality, and best illustrates device behavior must be chosen. The choice may be immediately narrowed to two:

(1) An instantaneous step voltage with internal resistance R, Figure 5.

(2) An instantaneous step current with infinite internal resistance, Figure 6.

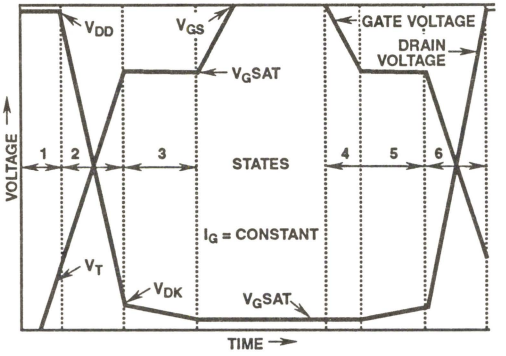


FIGURE 4. IDEALIZED POWER MOSFET WAVEFORMS

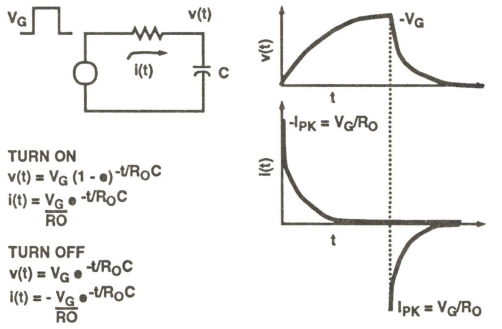


FIGURE 5. STEP-VOLTAGE FORCING FUNCTION

Power MOSFET devices are highly capacitive in nature; hence, simple capacitor responses to the forcing functions offer a good vehicle for comparison. The advantageous choice is immediately obvious: Figure 5. Voltage/time responses dominated by capacitance are straight lines (when constant current is used). The slope of these lines is

proportional to current and inversely proportional to capacitance. Analytically, then, constant current is most convenient. It is quite another matter, however, to build a bidirectional current drive that is accurate across the many decades of both current and time required to establish experimental verification.

Six States

To completely characterize power MOSFET switching waveforms, the six states that a device assumes, Figure 6, must be addressed:

STATE	MOS	JFET
Turn-on 1	Off	Off
Turn-on 2	Active	Active
Turn-on 3	Active	Saturated*
Turn-off 4	Saturated	Saturated
Turn-off 5	Active	Saturated
Turn-off 6	Active	Active

*The term saturated is taken to mean a constant low-voltage drain-source condition.

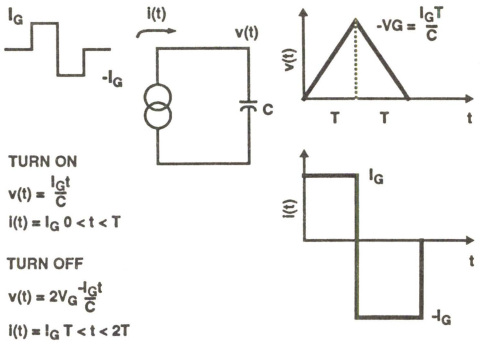
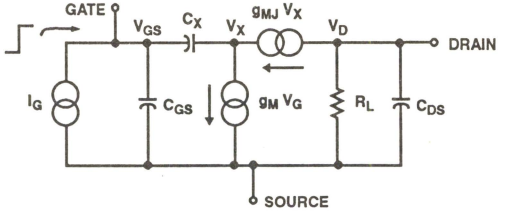


FIGURE 6. STEP CURRENT FORCING FUNCTION

Equivalent Circuit

The lumped-parameter model of Figure 3, with the cascode-connected JFET, can now be reduced to the linear equivalent circuit of Figure 7, and the six device states investigated from full off to full on.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_M	- MOSFET Transconductance
V_D	- Drain Voltage	g_{MJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_X	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE 7. POWER MOSFET EQUIVALENT CIRCUIT

State 1: MOS Off, JFET Off

In a power-MOSFET device, no drain current will flow until the device gate threshold voltage, V_T, is reached. During this time, the gate current drive is only charging the gate source capacitance. More accurately, I_G is charging C_{ISS} ($C_{ISS} = C_{GS} + C_{GD}$, C_{DS} shorted), the capacitance designation published by the industry.

The current generators, $g_M v_G$ and $g_{MJ} V_X$ are open circuits for zero drain current, and R_L is presumed to be so low as to represent a short circuit (generally true for practical applications). This is academic however since C_{GS} is very much larger that C_6. The time to reach threshold, then, is simply:

$$T = \frac{C_{ISS}\, V_T}{I_G}$$

State 2: MOS Active, JFET Active

This state graphically illustrates the dramatic influence that the JFET has on the power MOSFET drain-voltage wave- form. Instead of having to discharge C_x from V_{DD} to ground, the lateral MOSFET need only swing v_X to ground, a much smaller voltage thanks to the grounded gate JFET. Since the interaction of R_L with the device capacitances has a second-order effect on the drain voltage, the equivalent circuit of Figure 7 predicts a drain voltage change of:

$$dv_G/dt = g_M R_L I_G/[C_{GS} + C_X(1 + g_M/g_{MJ})]$$

In all but the smallest power-MOSFET devices, C_x is several thousand picofarads and g_M/g_{MJ} is of the order of 3:1. Power-MOSFET devices exhibit a high dv_D/dt switching rate because of the cascode-connected J FET, not because C_{RSS} ($C_{RSS} = C_{GD}$) is a small value, as zero-drain-current data- sheet capacitance values might lead one to believe. If C_{RSS} were, in actuality, small, long drain voltage tails would not exist. The tail response is a direct result of JFET saturation. In order to delineate the transition from state 2 to state 3, a drain voltage at which the transition occurs must be defined. V_{DK} is the knee voltage at which linear extrapolations of drain-voltage slopes intersect. The time duration of state 2 is:

$$t = (V_{DD} - V_{DK})[C_{GS} + C_X(1 + g_M/g_MJ)]/g_M R_L I_G$$

State 3: MOS Active, JFET Saturated

When the JFET saturates, the $g_{MJ} V_X$ current generator becomes a short circuit and the equivalent circuit predicts:

$$dv_D/dt = g_M R_L I_G/[C_{GS} + C_X(1 + g_M R_L)]$$

This is the Miller effect so often referred to in older texts that describe the behavior of grounded-cathode vacuum-tube amplifier circuits. Allowing for the fact that $1 + g_M R_L$ is approximately equal to $g_M R_L$ and $C_X(1 + g_M R_L)$ is very much larger than C_{GS}, the expression for drain-voltage tail time is:

$$t = (V_{DK} - V_{D[SAT]})C_x/I_G$$

State 4: MOS Saturated, JFET Saturated (Turn-Off)

In this state, in addition to $g_{MJ} V_X$ being shorted, the $g_M V_G$ current generator is shorted, and I_G is occupied with charging C_X and C_{GS}, in parallel, from the peak value of V_G to $V_{G(SAT)}$. The time required for this is:

$$t = (V_G - V_{G(SAT)}(C_{GS} + C_x)/I_G$$

Since a value for C_{GS} may be measured independently of switching time, the method described is the simplest way of determining C_X.

On turn-off, the state time equations are equally applicable, but in reverse order (states 5 and 6); see the idealized waveform of Figure 4.

Experimental Verification

The four switching states just analyzed indicate that for a given device, all four switching state times are inversely proportional to the magnitude of the gate drive current. Figure 8 illustrates the switching performance of a typical power MOSFET across three decades of gate drive current and time. In each case the data slope is almost a perfect -1.

A New Device Characterization

Figure 8 could not be a reasonable device data sheet presentation because it does not give the designer any information on a typical value for C_X, nor does it convey how V_{DK}, g_M, g_M/g_{MJ}, and V_G(sat) vary with drain current. What would be of enormous value to the designer is a plot of $V_D(t)$, $V_G(t)$ for selected values of V_{DD} and I_D within device ratings.

A reasonable characterization would be as follows:

1. The x axis would be normalized in terms of gate current drive.
2. The y axis would be normalized in terms of percent maximum rated V_D (0 to 100%).
3. $R_L = V_D(max)/I_D(max)$ would define the drain load resistance.
4. Four plots of $V_D(t)$, $V_G(t)$ at 100%, 75%, 50%, and 25% $V_D(max)$ would be shown.

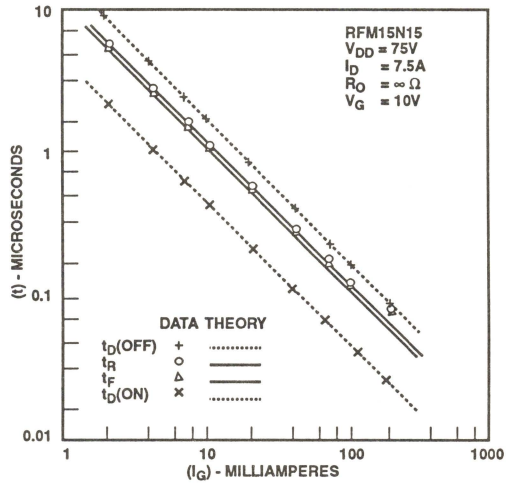


FIGURE 8. CONSTANT GATE CURRENT SWITCHING TIME

Figure 9 is such a plot for the RFM15N15 power MOSFET. With such a plot, a designer can estimate device switching performance under any resistive gate/drain conditions.

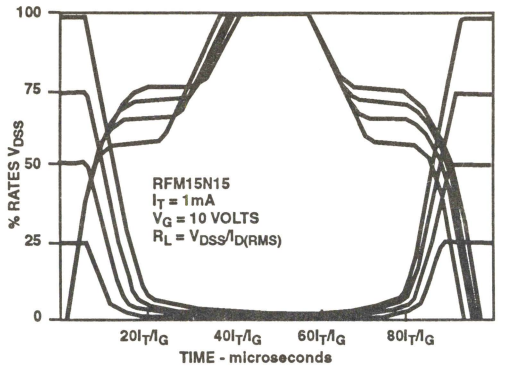


FIGURE 9. NORMALIZED RFM15N15 SWITCHING WAVEFORMS FOR CANSTANT GATE-CURRENT DRIVE.

Step-Voltage Gate Drive

The majority of power MOSFET applications employ a step gate-voltage input with a finite source resistance R_O.Often R_O for turn-on is not the same as R_O for turn-off. How can switching times for these situations be estimated using the switching characterization curves just described? The analysis for resistive step voltage inputs, which is complex because the gate current is no longer constrained to be constant, but is a function of device gate-voltage response, is covered in Appendix A. (A second, shorter appendix, B, has been added to illustrate the estimation of R_O for some practical gate drive circuits.) Table I summarizes the common switching equations, and indicates the appropriate 1G to be used in each state for relating step voltage drives to the characterization curves.

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figs. 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current VU/R_O equalling the constant 1G, t6(on), t, td(off), and t1 will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t, t1 switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

TABLE 1. COMMON SWITCHING EQUATIONS

	CONSTANT CURRENT	STATE 1: MOS OFF, JFET OFF	CONSTANT VOLTAGE
TURN ON	$t = \frac{C_{ISS} V_T}{I_G}$		$t = R_O C_{ISS} \ln \frac{[1]}{[1 - V_T/G_V]}$
	$I_G = I_T$	STATE 2: ACTIVE, ACTIVE	$I_G = (V_G - V_T)/R_O$
	$t = \frac{[V_{DD} - V_D K][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L I_G}$		
	$I_G = I_T$	STATE 3: ACTIVE, SATURATED	$I_G = (V_G - V_{GSAT})/R_O$
	$t = \frac{(V_{DK} - V_{DSAT})C_X}{I_G}$		
TURN OFF	$I_G = I_T$	STATE 4: SATURATED, SATURATED	$I_G = -V_G/R_O$
	$t = \frac{(C_{GS} + C_X)(V_G - V_{GSAT})}{I_G}$		$t = R_O(C_{GS} + C_X) \ln (V_G/V_{GSAT})$
	$I_G = I_T$	STATE 5: ACTIVE, SATURATED	$I_G = (V_G - V_{GSAT})/R_O$
	$t = \frac{(V_{DK} - V_{DSAT})C_X}{I_G}$		
	$I_G = I_T$	STATE 6: ACTIVE, ACTIVE	$I_G = (V_G - V_{GSAT})/R_O$
	$t = \frac{[V_{DD} - V_D K][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L I_G}$		

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figures 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_O equalling the constant I_G, $t_D(on)$, t_R, $t_D(off)$, and t_F will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t_R, t_F switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

$$\frac{t_{TURN\text{-}ON}}{t_{TURN\text{-}OFF}} = \frac{V_{G(SAT)}}{V_G - V_T}$$

For states 3 and 5 the time ratio is:

$$\frac{t_{TURN\text{-}ON}}{t_{TURN\text{-}OFF}} = \frac{V_{G(SAT)}}{V_G - V_{G(SAT)}}$$

Utilization of available maximum gate drive voltage and current can be optimized for fastest power MOSFET switching speed through the use of constant-current gate drive at the expense of increased gate-drive circuit complexity.

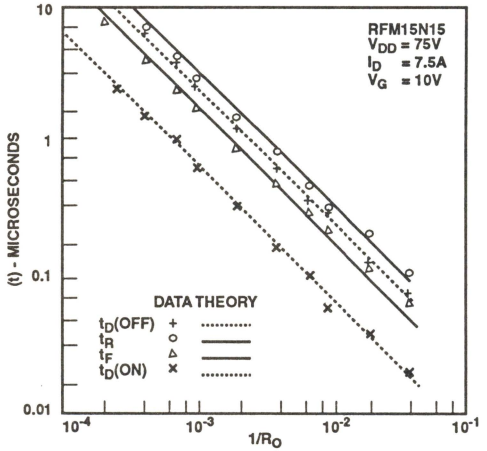


FIGURE 10. CONSTANT GATE VOLTAGE SWITCHING TIME

Using the Characterization Curves, Figure 9

To estimate the switching times for an RFM15N15 power MOSFET under the conditions V_G = 10V, V_{DD} = 75V, R_O = 100 ohms, and R_L = 10 ohms, precedes as follows:

State 1: MOS Off, JFET Off

This time can be estimated without recourse to the curves

$t = 100(1200 \times 10^{-12})$ in [1/(1 - 4/10)]

$t = 61$ ns

State 2: MOS Active, JFET Active

$I_G =$ (10 - 4)/100 = 60mA

$$t = \frac{\text{(curve divisions)} \times I_T\ \mu s}{60} = \frac{9}{60} = 150\text{ ns}$$

State 3: MOS Active, JFET Saturated

$I_G =$ (10 - 7)/100 = 30mA

$$t = \frac{\text{(curve divisions)} \times I_T\ \mu s}{30} = \frac{14}{30} = 467\text{ ns}$$

State 4: MOS Saturated, JFET Saturated

$C_{GS} + C_x$ = (gate voltage slope)(test current)

= $(1.5 \times 10^{-6}$s/5 volts)(10mA)

= 3000pF

$t = 100(3000 \times 10^{-12})$ in [10/6.6]

$t = 125$ns

State 5: MOS Active, JFET Saturated

$I_G =$ 6.6/100 = 66mA

$$t = \frac{\text{(curve divisions)} \times I_T\ \mu s}{66} = \frac{8}{66} = 121\text{ ns}$$

Figure 11 shows RFM15N15 waveforms using the conditions specified in the example.

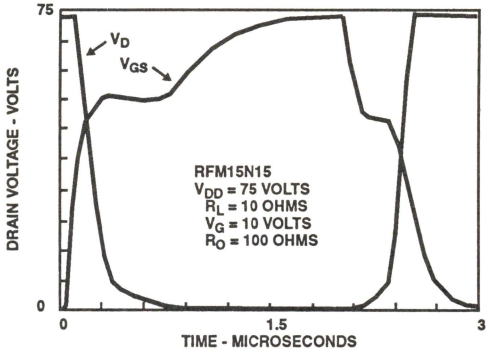


FIGURE 11. STEP GATE VOLTAGE INPUT TO AN RFM15N15

STATE	CALCULATED TIME	MEASURED TIME	RATIO
	(t_C, ns)	(t_M, ns)	(t_C/t_M)
1	61	60	1.02
2 + 3	671	670	0.92
4	125	137	0.91
5 + 6	318	375	0.85

For peak gate voltages other than 10 volts, and load resistances other than $V_{DSS}/I_{D(RMS)}$, the equations of Table 1 may be used in conjunction with slope estimates from the characterization curves for C_X and $C_{GS} + C_X(1 + g_M/g_{MJ})$ at the appropriate drain-current level.

Characterization-Curve Limits

The switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of microamperes, device dissipation is the limiting factor. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. However, as Figure 12 graphically shows, the characterization is valid across five decades of gate current and switching time, allowing all but a very few switching applications to be described by the characterization curves of Figure 9.

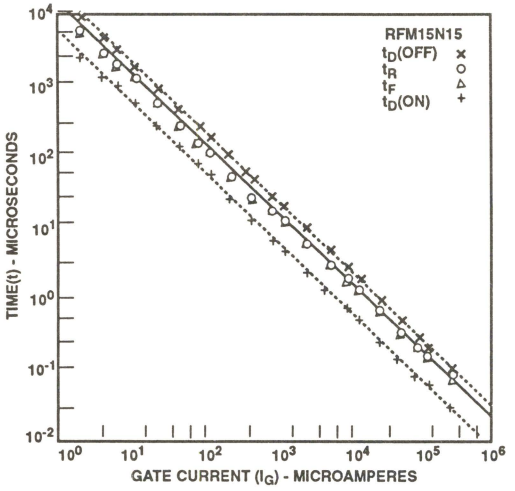


FIGURE 12. FIVE DECADES OF LINEAR RESPONSE

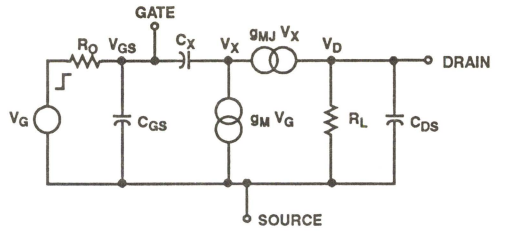
Conclusions

The viability of the proposed characterization curves using constant current has been demonstrated and the limits of application defined. The existence of a vertical JFET in a power MOSFET makes data-sheet capacitances of little use for estimating switching times. The classical method of defining switching time by 10% and 90% is a poor representation for power MOSFETs because of the dual-slope nature of the drain waveforms. Switching influences are masked because the 10% level is controlled by one mechanism and the 90% level by another. Device comparisons based on the classical switching definition can be very misleading.

Appendix A - Analysis for Resistive Step Voltage Inputs

Step Voltage Gate Drive

To obtain the necessary relationships, six device switching states must be examined using the same device equivalent circuit as was used for the constant-gate-current case, but with the forcing function replaced with a step voltage with internal resistance R_O, Figure A-1.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_M	- MOSFET Transconductance
V_D	- Drain Voltage	g_{MJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_X	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE A-1. POWER MOSFET EQUIVALENT CIRCUIT

State 1: Mos Off, JFET Off

As before, both current generators are open circuits, reducing the equivalent circuit to simply charging C_{ISS} through R_O.

$$t = R_O C_{ISS} \ln(1/(1 - V_T/V_G))$$

$$t = V_G/R_O$$

State 2: Mos Active, JFET Active

Before proceeding, it is wise to examine an actual device response and make use of available simplifications. Figure A-2 shows $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage. For truly resistive switching, realize that these waveforms are only mirror images of their voltage counterparts $v_G(t)$ and $v_D(t)$. Using Figure A-2, applicable gate currents for each of the device states may be listed.

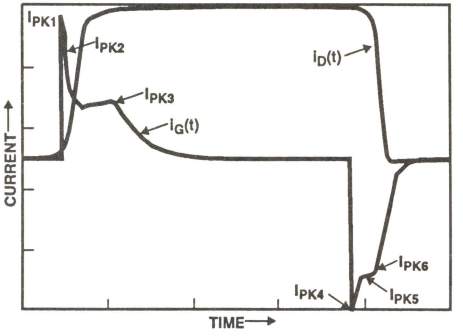


FIGURE A-2. $I_G(t)$ AND $I_D(t)$ FOR A TYPICAL POWER MOSFET DRIVEN BY A STEP GATE VOLTAGE

Turn-On

State 1: MOS Off, JFET Off

$I_{PK1} = V_G/R_O$

State 2: MOS Active, JFET Active

$I_{PK2} = (V_G - V_T)/R_O$

State 3: MOS Active, JFET Saturated

$I_{PK3} = (V_G - V_{G(SAT)})/R_O$

Turn-Off

State 4: MOS Saturated, JFET Saturated

$I_{PK4} = V_G/R_O$

State 5: MOS Active, JFET Saturated

$I_{PK5} = V_{G(SAT)}/R_O$

State 6: MOS Active, JFET Active

$I_{PK6} = V_{G(SAT)}/R_O$

The equivalent circuit of Figure A-1 predicts that:

$$dv_D/dt = -g_M R_L(V_G - V_T)e^{-t/T1}/T1$$

where $T1 = R_O C_{GS} + (1 + g_M/g_{MJ})R_O C_X$

Note that $g_M R_L(V_G - V_T)$ is usually an order of magnitude greater than V_{DD}, indicating that the drain voltage is discharging toward a very large negative value. The device operation, then, is on the early, almost linear, portion of the exponential, where $e^{-t/T1}$ approximates unity. The drain current of Figure A-2, and hence the drain voltage, does indeed exhibit a linear decrease with time.

Thus, for state 2:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L I_{PK2}}$$

where $I_{PK2} = (V_G - V_T)/R_O$

State 3: Mos Active, JFET Saturated

Because of the Miller effect, the gate voltage and, hence, the gate current, is almost constant during the tail time. The equivalent circuit then predicts:

$$\frac{dV_D}{dt} = \frac{g_M R_L I_G}{C_{GS} + (1 + g_M R_L)C_X} = \frac{I_G}{C_X}$$

$I_G = I_{PK3} = (V_G - V_{G(SAT)})/R_O$

and $t = \dfrac{(V_{DK} - V_{D[SAT]})C_x}{I_{PK3}}$

State 4: Mos Saturated, JFET Saturated (Turn-off)

Both equivalent-circuit generators are short circuits, and the gate drive is discharging C_X in parallel with C_{GS} through R_O.

$$t = R_O(C_{GS} + C_X)\ \ln[V_G/V_{G(SAT)}]$$

$I_{PK4} = V_G/R_O$

State 5: Mos Active, JFET Saturated

The JFET current generator $V_x g_{mJ}$, is operative.

$$t = \frac{[V_{DK} - V_{D[SAT]})C_X}{I_{PK5}}$$

$I_{PK5} = V_{G(SAT)}/R_O$

State 6: Mos Active, JFET Active

The Miller effect is now reduced by the activation of $V_G g_{MJ}$, and the equivalent circuit predicts:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L I_{PAK6}}$$

$I_{PAK6} = V_{G(SAT)}/R_O$

Appendix B - Estimating R_O for Some Typical Gate-Drive Circuits

Case 1: Typical Pulse-Generator Drive, Figure B-1

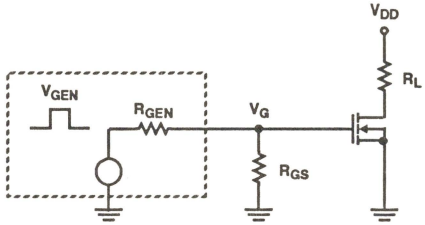


FIGURE B-1. TYPICAL PULSE-GENERATOR DRIVE CIRCUIT

Turn-On and Turn-Off

$$R_O = R_{GEN}R_{GS}/(R_{GEN} + R_{GS})$$

For the typical case where $R_{GEN} = 50\Omega$, and a coaxial-cable termination of 50 ohms, $R_O = 25\Omega$ and $V_G = V_{GEN}/2$.

Case 2: Voltage-Follower Gate Drive, Figure B-2

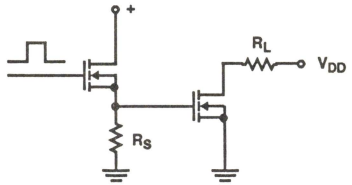


FIGURE B-2. VOLTAGE-FOLLOWER GATE-DRIVE CIRCUIT

Turn-On

R_O is approximately equal to $1/g_M$ for R_S very much greater than $1/g_M$.

gm = transconductance of driving MOSFET transistor.

Turn Off

$R_O = R_S$

Case 3: Common-Source Gate Drive, Figure B-3

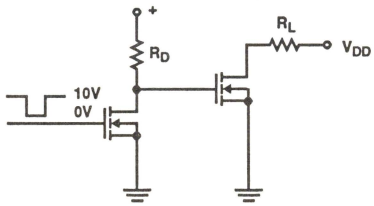


FIGURE B-3. COMMON-SOURCE GATE-DRIVE CIRCUIT

Turn-On

$R_O = R_D$ (drain-to-ground capacitance of driving device adds to C_{GS} of driven MOSFET.)

Turn Off

$R_O = R_{DS}(on)$ of driving MOSFET

R_D is very much greater than $R_{DS}(on)$

Harris Semiconductor

APPNOTE

No. AN9321 February 1994

Harris Power

SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING: A RATING SYSTEM

Author: Harold Ronan

Unexpected transients in electrical circuits are a fact of life. The most potentially damaging transients enter a circuit on the power source lines feeding the circuit. Power control and conversion circuits are vulnerable because of their close proximity to the incoming lines. The circuit designer must provide protection or face frequent field failures. Harris provides extensive information on transient characteristics in support of its line of transient voltage suppression devices (SSD-450). Additionally Harris offers power MOS devices that are avalanche failure resistant. Most semiconductor devices are intolerant of voltage transients in excess of their breakdown rating. Avalanche capable devices are designed to be robust. The Harris MEGAFET product line typifies the best in rugged power devices. To assist the designer in their use, Harris has devised a Rating System that is application specific. This application note is intended to explain and illustrate the use of the single pulse Unclamped Inductive Switching Rating curves.

Failure Mechanisms

Early Power MOSFET devices, not designed to be rugged, failed when the parasitic bipolar transistor indigenous to the vertical DMOS process turned on. Figure 1 shows a cross section of a unit cell from an N-channel enhancement mode device.

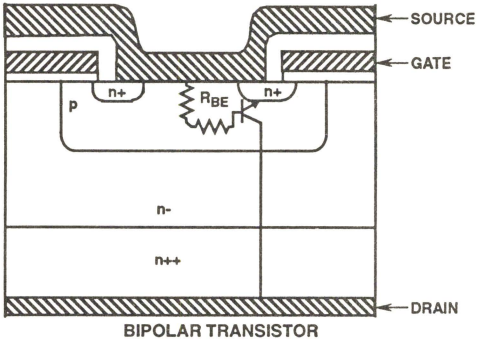


FIGURE 1. VDMOS STRUCTURE WITH PARASITIC BIPOLAR TRANSISTOR

When a unit is in avalanche, the bipolar transistor is in a V_{CER} mode, thus, it will rapidly heat. The avalanche-induced base-emitter voltage rises because of a positive resistive temperature coefficient. Simultaneously, the base emitter voltage at which the transistor will become forward biased decreases because of a negative V_{BE} temperature coefficient. If a forward bias condition is reached, device failure initiates. Blackburn's measurements showed that this failure mode is a function of avalanche current and junction temperature and not energy related.

Ruggedness improvement technology has advanced to such a level that devices fail because of a different mechanism. Devices have been manufactured in which the parasitic bipolar transistor never turns on. The failure is thermally induced. At the start of avalanche, any localized increase in temperature can initiate the formation of a current filament with a current-controlled negative-resistance characteristic. At a high current density, this can lead to the formation of a mesoplasma resulting in second breakdown and device failure. If there is heat transfer from the filament to the bulk material, the time to second breakdown is inversely proportional to the square of the current.

The Harris MEGAFET product line typifies this type of failure mode. UIS capability testing of these devices show that the failure current versus the time in avalanche closely approximates a negative one-half slope when the locus of device destruction points is plotted on a log-log graph. Device failure is not inversely proportional to current only as it would be in the case of constant energy. Harris supplies rating curves at starting junction temperatures of +25°C and +150°C.

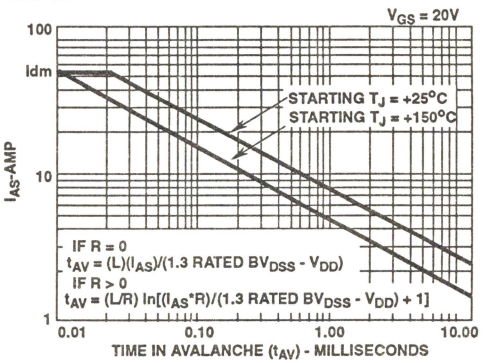


FIGURE 2. UNCLAMPED-INDUCTIVE-SWITCHING SAFE OPERATING-AREA CURVE (SINGLE PULSE UIS SOA). SEE FIGURE 3 FOR TEST CIRCUIT.

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TABLE 1.

ROW #	CIRCUIT CONDITIONS		TIME IN AVALANCHE	AVALANCHE ENERGY	AVERAGE AVALANCHE POWER
	V_{DD}	R	T_{AV}	E_{AS}	$P_{AS(AVE)} = (E_{AS}/TAX)$
1	V_{DD}	R	$(L/R)\ln[1/\ln(1+1/K)-K]$	$(LI_{AS}V_{DSX(SUS)}/R)[1-K\ln(1+1/K)]$	$[I_{AS}V_{DSX(SUS)}][1/\ln(1+1/K)-K]$
-	0	R	-	-	- -
2	V_{DD}	0	$LI_{AS}/(V_{DSX(SUS)}-V_{DD})$	$LI_{AS}^2/2(1-V_{DD}/V_{DSX(SUS)})$	$I_{AS}V_{DSX(SUS)}/2$ -
3	0	0	$LI_{AS}/V_{DSX(SUS)}$	$LI^2_{AS}/2$	$I_{AS}V_{DSX(SUS)}/2$ -

I_{AS} - The peak current reached during device avalanche.
t_{AV} - The time duration of device avalanche.
$V_{DSX(SUS)}$ - The effective (constant) device breakdown voltage during avalanche.
L - Inductance
R - Resistance
V_{DD} - The output circuit supply voltage.
K - $(V_{DSX(SUS)}-V_{DD})/I_{AS}R$ - The ratio of the inductor plus the resistor voltage to the resistor voltage drop.

Test Circuit Equations

The circuit model (Figure 3) used to describe a UIS test is a simple lumped parameter series inductor/resistor circuit in which both the power supply and device avalanche voltage are presumed to be constant. All the equations that result from the mathematical analysis are listed in Table 1 by the V_{DD}, R conditions commonly referenced in the JEDEC test method and commercial data sheets. The equations in Row 1 are for the general case. The factor K is the ratio of the net voltage across the inductor and resistor to the resistor voltage drop. When K is large (K >30), the equations in Row 1 reduce to those in Rows 2 and 3. This can be accomplished mathematically by substituting the series expansion: $\ln(1+X) = X - X^2/2 + \ldots$ Only the first term is needed for t_{AV}, while two terms are required for E_{AS} and $P_{AS(AVE)}$. Time in avalanche, t_{AV}, is the important parameter for a rugged device. Reviewing the expressions for t_{AV} in Table 1, the following observations can be made:

1. Series circuit resistance reduces the device avalanche stress.
2. A supply voltage approaching the device avalanche voltage increases t_{AV}. Stress increases and the allowable avalanche current is reduced.
3. When the supply voltage is zero, t_{AV} varies inversely with the device avalanche voltage.

Integrated Technology Corporation, Tempe, AZ manufactures test equipment that works on this principle. When a device avalanches, the supply voltage is disconnected and current is commutated through an antiparallel diode. Power MOSFETs tested in this manner will receive the same heating energy independently of varying device-to-device avalanche voltages.

The equations of Table 1 presume that the device avalanche voltage is constant. In an actual test it is not. Experiments have been performed using devices with similar low current room temperature BV_{DSS} readings. V_{DD}, L, R, I_{AS} and t_{AV}

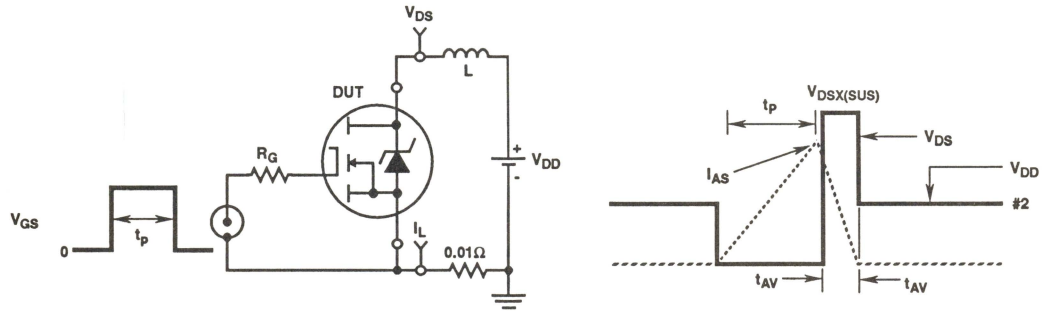

FIGURE 3. UIS TEST CIRCUIT AND WAVEFORMS

were carefully measured and the avalanche breakdown was calculated. All units yielded similar results. The effective avalanche voltage was in all cases 30% larger than BV_{DSS}. $V_{DSX(SUS)}$ is the effective voltage referenced in the JEDEC test method. Harris has chosen to list $V_{DSX(SUS)}$ in the t_{AV} equations on the rating curves for these devices as 1.3 times the rated low current breakdown voltage. It has been industry practice to refer only to B_{VDSS}.

Single point avalanche energy ratings at T_J = +25°C are not application specific nor are they useful for comparing similar devices offered by different manufacturers. To highlight the difficulty, a hypothetical example is in order. Let's attempt to determine the safe single pulse avalanche current for an application that uses L = 100µH and a V_{DD} = 30V. Typical industry data sheet information is as follows:

E_{AS} = 19mJ Maximum
T_J = +25°C (Starting)
BV_{DSS} = 60V
L = 50µH
V_{DD} = 25V
I_{AS} = 21A

Only a starting junction temperature of +25°C can be assessed. In lieu of a rating curve, a failure mode must be assumed.

Parasitic Bipolar Turn-on

There is no basis from which to estimate the safe avalanche current for the intended application.

Constant Energy

To use the relationship $E_{AS} = L\, I^2_{AS}/2(1-V_{DD}/V_{DSX(SUS)})$ we must use $V_{DSX(SUS)} = BV_{DSS}$. The predicted safe I_{AS} would then be equal to 13.8A.

Thermal ($I^2_{AS}\, t_{AV}$ = Constant)

Again using $V_{DSX(SUS)} = BV_{DSS}$ in the relationship $t_{AV} = L\, I_{AS}/(V_{DSX(SUS)}-V_{DD})$ we have t_{AV} = 30µs for the data sheet condition and $I^2_{AS}\, t_{AV}$ = 0.0132. For the intended application then

$I^3_{AS} = 0.0132\ (V_{DSX(SUS)}-V_{DD})L$
where L = 100µH, V_{DD} = 30V and $V_{DSX(SUS)} = BV_{DSS}$
and I_{AS} = 15.8A

It is a simple matter to establish the safe avalanche current for a Harris MegaFET supplied with rating curves. Figure 2 is the rating chart for the RPF22N10, a 100V BV_{DSS} device.

For T_{JS} = +25°C

$I^2_{AS}\, t_{AV}$ = constant = C = 0.06 and $V_{DSX(SUS)} = 1.3\ BV_{DSS}$
and $I^3_{AS} = C\ (V_{DSX(SUS)}-V_{DD})/L$
for the application I_{AS} = 39A

For T_{JS} = +150°C

$I^2_{AS}\, t_{AV} = 0.025$

Thus at the maximum rated starting junction temperature, I_{AS} = 29.2A.

The safe avalanche current for any starting T_J can be established from the Harris rating curves. Stoltenburg showed that for MegaFET devices avalanche failure was a linear function of starting T_J for a fixed inductor. This is also true for a constant t_{AV}. Figure 4 shows the relationship for the RFP22N10 device. It is a simple matter then to establish the $I^2_{AS}\, t_{AV}$ = constant for any starting T_J. T_{JS} = +100°C is a common operating temperature for a practical application.

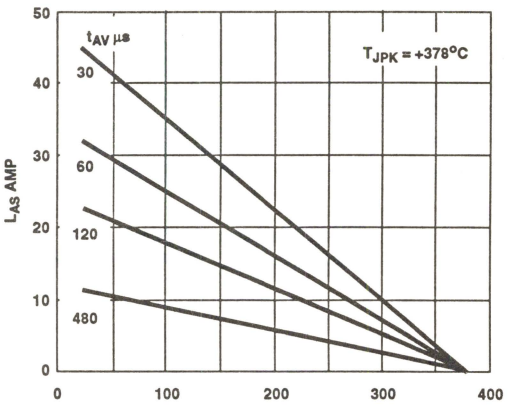

FIGURE 4. RFP22N10 L_{AS} vs T_{JS}

Entering the Harris curves at any convenient t_{AV}, in this case. 0.6ms, the I_{AS} temperature sensitivity is found to be -3.55A/+125°C or -28.4mA/°C. Therefore, I_{AS} = 10-(0.0284) (75) = 7.87A at t_{AV} = 0.6ms and $I^2_{AS}\, t_{AV}$ = 0.0372.

Using $I^3_{AS} = 0.0372\ (V_{DSX(SUS)}-V_{DD})/L$ for the hypothetical application I_{AS} = 33.4A for a starting T_J = +100°C.

Rail Voltage (V_{DD}) Transients

Development of a single pulse UIS rating curve for a specific load inductance and junction temperature has been illustrated. This information can be used to develop the amplitude and duration of rail voltage transients that are within the device rating. Figure 5 shows an idealized rail voltage pulse with the resultant avalanche current waveform. The equations that describe the current waveform are based on a V = Ldi/dt relationship are:
$V_{SPK} - V_{DSX(SUS)} = LI_{AS}/t_{SPK}$ and
$V_{DSX(SUS)} - V_{DD} = LI_{AS}/t_{AV}$

Calculating the junction temperature rise caused by the voltage transient will allow the use of UIS rating curve information to determine a corresponding V_{SPK}, t_{SPK} rating curve for L = 100µH, V_{DD} = 30V and a T_J = +100°C. Under the condition of no die heat loss and constant $V_{DSX(SUS)}$, the temperature at t_{SPK} is:

$T_{SPK} = T_{JS} + HV_{DSX(SUS)}\, I_{AS}\, t_{SPK}/2$
where H is a constant defined by
the rating curves.

The UIS rating curves contain two important items of information. First, each curve regardless of starting T_J, represents the locus of points of a single allowable peak

junction temperature to be reached during avalanche. Second, for any fixed t_{AV}, the +25°C I_{AS} and the +150°C I_{AS} values are two points on a linear Ias versus starting T_J relationship whose intercept at I_{AS} = 0 is that peak junction temperature.

Continuing the analysis, T_{JPK} may be determined from the rating curves at a constant t_{AV} by:

$T_{JPK} = (150 - 25\ I_{AS150}/I_{AS25})/(1 - I_{AS150}/I_{AS25})$
for the RFP22N10, T_{JPK} = +378°C.

A value for H may be found from the time/temperature relationship during t_{AV}.

$$T_J = [HV_{DSX(SUS)}] \int_0^t I(t)dt + T_{SPK} \text{ where}$$

$I(t) = I_{AS}(1 - t/t_{AV})$ and

$T_J = HV_{DSX(SUS)}\ I_{AS}(t - t^2/2t_{AV}) + T_{SPK}$

Stoltenburg has reported that device failure generally occurred between $t_{AV}/3$ and $t_{AV}/2$. If the delay time to second breakdown is proportional to $(T_J/I(t))^2$, then a maximization leads to a $t_{AV}/3$ result. If the delay time is proportional to $T_J/I(t)$ then $t_{AV}/2$ is the result. $t_{AV}/3$ is used here to obtain

$$T_{JPK} = 5H\ V_{DSX(SUS)}\ \frac{I_{AS}t_{AV}}{18} + T_{SPK}$$

Setting $T_{SPK} = T_{JS}$ = +25°C and using T_{JPK} = +378°C, $V_{DSX(SUS)}$ = 130V and entering the +25°C rating curve for I_{AS} and t_{AV}, H is found to be 1.63×10^3 °C/J.

It is now possible to calculate the allowable I_{AS} corresponding to a rail voltage spike using the relationship

T_{SPK}-$T_{JS} = H_{VDSX(SUS)}\ I_{AS}\ t_{SPK}/2$

The rating curve limits T_{SPK} to +150°C. For T_{JS} = +100°C:

$I_{AS150}\ t_{SPK} = 472 \times 10^{-6}$

For each t_{SPK} in this equation there is a circuit defined $t_{AV} = LI_{AS}/(V_{DSX(SUS)} - V_{DD})$ that should not exceed the $t_{AV} = C_{150}/I^2AS$ rating. This in turn defines a maximum spike induced I_{AS} that should not be exceeded. This current is

$I^3_{ASM} = C_{150}\ (V_{DSX(SUS)} - V_{DD})/L$.

For this example I_{ASM} = 29.2A for $t_{SPK} \leq$ 18.2 microseconds. The bounds for the relationship $V_{SPK} = LI_{AS}/t_{SPK} + V_{DSX(SUS)}$ have been defined and V_{SPK} vs t_{SPK} can be plotted. The rating curve is illustrated in Figure 6.

The Application Environment

With a rating curve in hand, the intended application transient environment must be assessed to determine if added protection is required. The expected rail transient voltage amplitude, duration, and frequency of occurrence can vary greatly. Figure 7 illustrates measured results on AC power service. Several organizations such as ANSI/IEEE, IEC, UL, NEMA have and are developing guidelines and test standards to describe what a specific environment is likely to be on the basis of field experience.

Reference 6 contains an overview of voltage transients and provides the means for selecting an appropriate Metal-Oxide Varistor should it be required for an application.

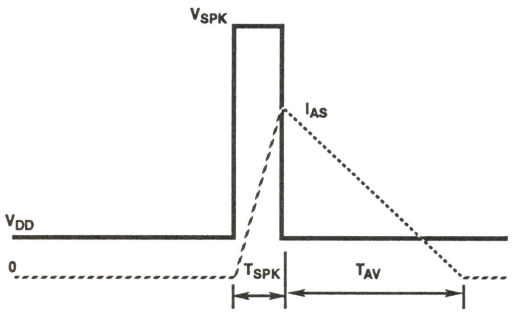

FIGURE 5. IDEALIZED RAIL VOLTAGE TRANSIENT

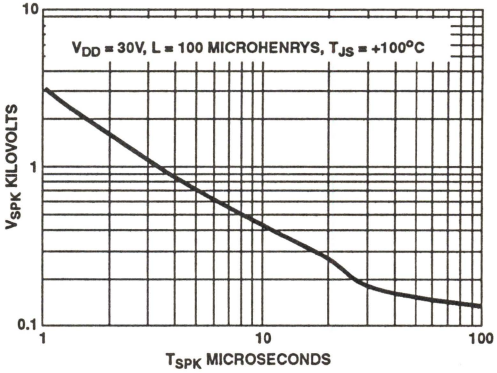

FIGURE 6. RFP22N10 RAIL TRANSIENT RATING

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5. S. K. Ghandhi, SEMICONDUCTOR POWER DEVICES, John Wiley & Sons, New York, pp 15-29, 1977.
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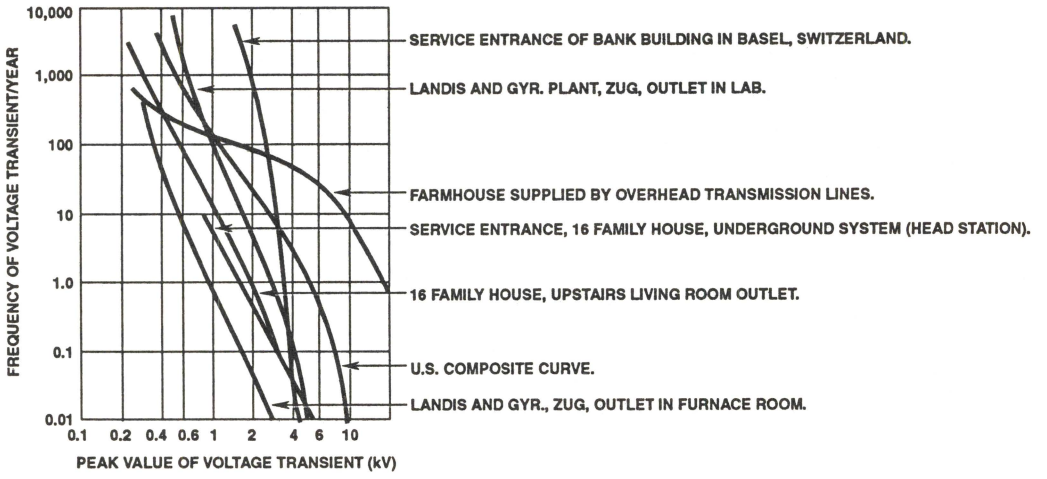

FIGURE 7. FREQUENCY OF OCCURRENCE OF TRANSIENT OVERVOLTAGES IN 220V AND 120V SYSTEMS

A COMBINED SINGLE PULSE AND REPETITIVE UIS RATING SYSTEM

Author: Wallace D. Williams

A rating system for Unclamped Inductive Switching in PowerMOS transistors already widely accepted and implemented on Harris PowerMOS transistor data sheets can be applied to a wide range of applications very easily and expanded to cover repetitive UIS pulses by the simple technique of superposition. This allows PowerMOS transistor users to determine if their application lies within the rated capability of a power transistor. Two examples are given of the analysis of UIS stress level in representative applications.

The ability of PowerMOS transistors to withstand unclamped inductive switching (UIS) has been recognized since 1985. Although Blackburn has clearly shown[1] UIS stress level is not directly related to energy, many manufacturers of PowerMOS transistors persist in rating their devices in terms of energy capability. Since the energy capability varies with the operating conditions, this rating is valid only at the condition specified and the PowerMOS transistor user has no way to calculate whether the particular application exceeds the device rating. Ronan has defined a rating system[3], herein after called simply the UIS Rating System, which allows manufacturers to specify the capability of their PowerMOS transistors for single pulse UIS in such a way that users can easily determine if their application exposes the device to more UIS stress than is guaranteed in the device data sheet.

The Single Pulse UIS Rating System

This UIS Rating System, requires the user to determine only the peak current through the PowerMOS transistor (I_{AS}), the junction temperature at the start of the UIS pulse (T_J) and the time the transistor remains in avalanche (t_{AV}). It allows the easy determination of the conformance of any application to a specified UIS capability where the worst case conditions can be simulated. It is also quite feasible to calculate the UIS stresses for circuits not yet constructed or conditions not easily simulated.

The UIS rating for a PowerMOS transistor (see Figure 1) is presented as a chart with a vertical axis of (I_{AS}) maximum avalanche current vs (t_{AV}) time in avalanche as the horizontal axis. Two lines are shown, one for +25°C and one for the maximum junction temperature. It is fairly easy in most applications to determine the avalanche current and time in avalanche in an existing application by using a current probe. If the time in avalanche and avalanche current plotted on the UIS rating curve fall above and to the right of the +25°C line, the application is beyond the UIS rating of the device and the user stands a risk of device failure. If the time and current plotted on the rating curve fall below and to the left of the maximum junction temperature line the application is within the UIS rating of the device. In either case no further analysis is needed. If the time and current plotted on the rating chart falls between the +25°C and the maximum junction temperature lines further analysis is required.

To analyze those cases where the starting temperature and time in avalanche fall between the +25°C and maximum temperature line, first we must determine the junction temperature of the PowerMOS transistor at the start of the UIS pulse. If the UIS stress occurs after a long period in conduction it may be sufficient to just measure the case temperature of the device and calculate the temperature rise between the case and junction from the dissipation and thermal resistance of the device. Any other approach may be used. Once the junction temperature at the start of the pulse has been determined we can extrapolate between the two published rating curves to determine the UIS capability at that starting junction temperature.

Ronan[3], Stoltenburg[2] and Blackburn[1] have all indicated that the UIS capability $I^2_{AS} \times t_{AV}$ is a simple linear function of temperature. Using this allows a straight line extrapolation of the UIS capability of the device at the calculated junction temperature. Then simply compare the calculated capability to the stress determined to determine if the device is within ratings. This simple approach allows users to find out if their application is safe for any single UIS pulse.

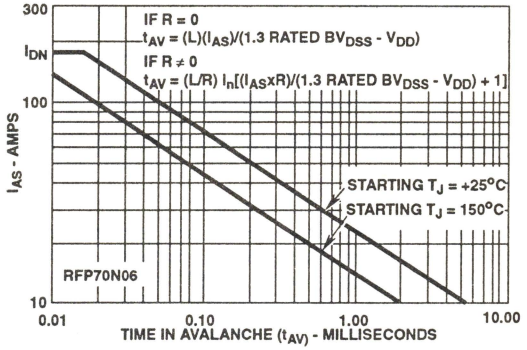

FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING (SINGLE PULSE UIS)

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Multiple or Repetitive UIS

The handling of repetitive UIS pulses has been ignored by the PowerMOS transistor manufacturers except for an attempt by one manufacturer to rate repetitive UIS at 0.01% of the +25°C power rating with no further qualifications. The UIS rating system outlined in Ronan's paper[3] is quite applicable to repetitive pulses by using the technique of superposition as is commonly done in evaluating repetitive SOA pulses. Each UIS pulse is considered a separate event and evaluated as if no other pulse existed. It is necessary only to determine I_{AV} (avalanche current), t_{AV} (time in avalanche) and T_J (junction temperature at the start of the pulse), just as in the single pulse case. Usually the last pulse in a series occurs at the highest junction temperature and is therefore the most severe stress. If the PowerMOS transistor is within the specified UIS rating for that pulse, it is certainly within the UIS ratings for previous pulses which occurred at a lower junction temperature.

Usually the junction temperature variation of a PowerMOS transistor over a full repetitive period is very small. The device has a thermal capacitance and does not change temperature instantaneously, so usually using the average junction temperature for the starting temperature to evaluate the avalanche stress does not result in appreciable error. In those cases where the period is long other means must be used to determine the junction temperature at the start of the UIS pulse.

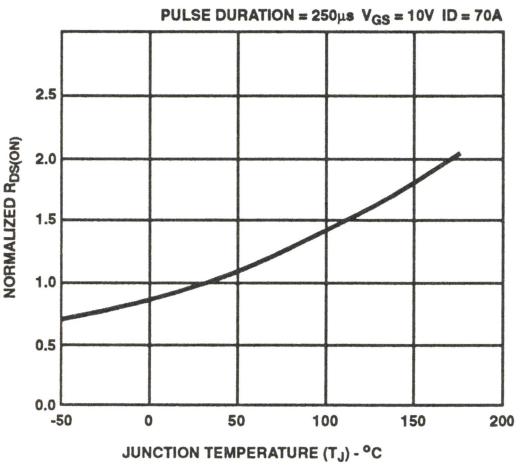
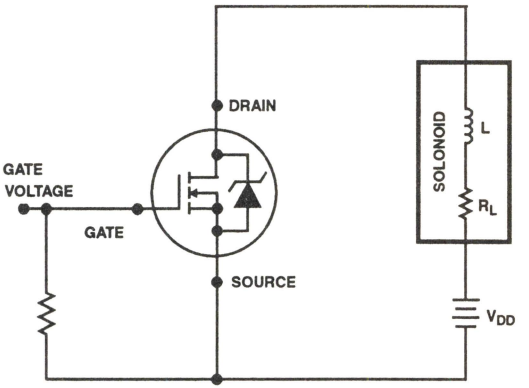


FIGURE 2. NORMALIZED $R_{DS(ON)}$ VS JUNCTION TEMPERATURE

Examples

The two examples shown below are intended only to illustrate the techniques used to calculate whether a PowerMOS transistor is within its UIS rating or not. Since UIS capability is an interactive function of other environmental stresses, it is necessary to include some calculation of other operating conditions as part of this analysis. The operating conditions in both examples are calculated rather than measured since the determination of UIS capability using measured values for I_{AV} and t_{AV} seemed trivial and self explanatory. The first example is a "single" pulse stress with sufficient time between stresses so that there is no interaction between subsequent pulses, and the second has a period short enough so that the temperature variation over a period is small.

Example 1



SCHEMATIC

Solenoid Driver: Single Pulse

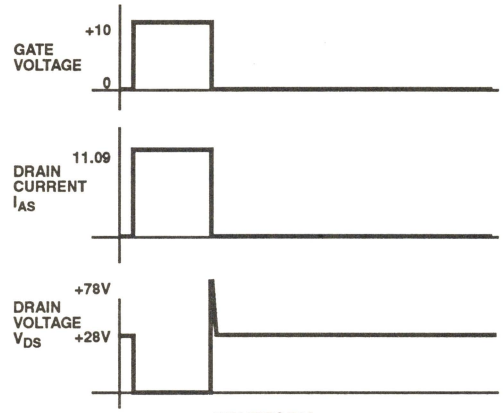
Given:
- V_{DD} = 28 volts
- R_L = 2.5Ω
- Pulse width = Steady state "on"
- Transistor = RFP70N06
- Gate "on" drive = 10 volts
- Maximum T_J = 150°C
- $T_{AMBIENT}$ = 90°C

Calculate:
- L (Maximum allowable inductance)
- θ_{CA} (Required case to ambient thermal resistance)

$R_{TOTAL} = R_L + R_{DS(ON)} = 2.5 + (0.014 \times 1.8)$ See Figure 2
$R_{TOTAL} = 2.525\Omega$
$I_{AVALANCHE} = 28/2.525 = 11.09$ amps
(Peak avalanche current)

Using the rule of thumb that the avalanche voltage is equal to the rated breakdown rating multiplied by 1.3 we can write:

$V_{AVALANCHE} = 60 \times 1.3 = 78$ volts
$t_{AVALANCHE} = (L/R) \times \ln[(I_{AV} \times R)/(V_{AV} - V_{DD}) + 1]$
$t_{AVALANCHE} = (L/2.525) \times \ln[(11.09 \times 2.525)/(78 - 28) + 1]$
$L = t_{AVALANCHE}/0.176$



WAVEFORM

Entering the Unclamped Inductive Switching Chart (See Figure 1) at 150°C and 11.09 amps we read an allowable $t_{AVALANCHE}$ of 1.5 milliseconds. This gives us a maximum allowable L of:

L = (1.5E-3)/0.176 = 8.53mH
maximum allowable inductance

Now to calculate the required heat sink thermal resistance:

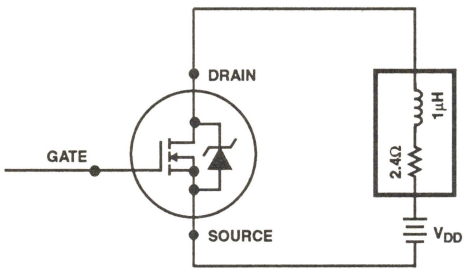
$Pd = (I^2 \times R_{DS(ON)}) = (11.09^2) \times 0.025 = 3.07$ watts

$\theta_{CA} = [T_{JMAX} - P_D \times \theta_{JC} - T_{AMBIENT}]/P_D$

$\theta_{CA} = [150 - (3.07 \times 1.0) - 40]/3.07$

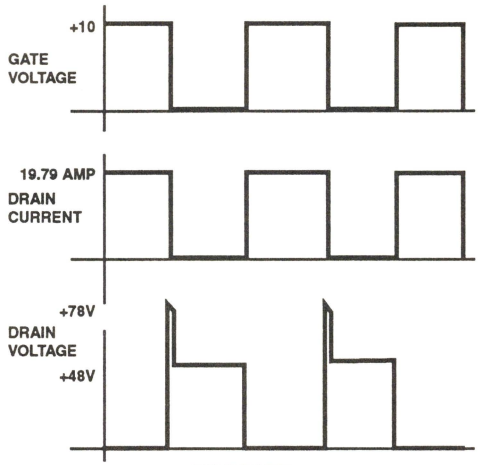
θ_{CA} = 18.5 °C/W required thermal resistance, case to ambient

Example 2



SCHEMATIC

Switching Regulator - 100kHz
Given:
Frequency = 100kHz
Duty Cycle = 50%
$R_L = 2.4\Omega$
V_{DD} = 48 volts
$T_{AMBIENT} = 40°C$
$T_{JUNCTION} = 150°C$ Maximum junction temperature
L = 1µH (Leakage Inductance)
PowerMOS transistor = RFP70N06



WAVEFORM

Determine:
Is the PowerMOS transistor within UIS rating?
What θ_{CA} is required?

$I_{AVALANCHE} = V_{DD}/(R_L + R_{DS(ON)})$

$I_{AVALANCHE} = 48/(2.4 + (0.014 \times 1.8))$ See Figure 2

$I_{AVALANCHE}$ = 19.79 amps

$t_{AVALANCHE} = (L/R) \times \ln[(I_{AV} \times (R_L + R_{DS(ON)}))/V_{AV} - V_{DD}) + 1]$

$t_{AVALANCHE} = (1E\text{-}6/2.425) \times \ln[19.79 \times 2.425/(78 - 48) + 1]$

$t_{AVALANCHE}$ = 0.395µsec

Entering the Unclamped Inductive Switching Curve (See Figure 1) at 19.79 amps, we find the device has a $t_{AVALANCHE}$ capability at 150°C of 500µsec. Obviously this application does not challenge the UIS capability of the RFP70N06.

Now to calculate the required heat sink thermal resistance:

$E_{AVALANCHE} = (L \times V_{AV} \times I_{AV}/R) \times (1 - (V_{AV} - V_{DD})/(I_{AV} \times R) \times \ln[(1 + [I_{AV} \times R)/(V_{AV} - V_{DD})]$

$E_{AV} = ((1e\text{-}6 \times (60 \times 1.3) \times 19.79)/2.4) \ln(1 + 19.97 \times 2.4)/78 - 48)$

E_{AV} = 614.0 µJ per avalanche

$P_{AVALANCHE} = E_{AVALANCHE} \times f$

$P_{AVALANCHE} = 614.0e\text{-}6 * 100e3$

$P_{AVALANCHE}$ = 61.40 watts

$P_{CONDUCTION} = (I_{AV}^2 \times R_{DS(ON)})/2$

$P_C = (19.79^2 \times 0.025)/2$

P_C = 4.90 watts

$P_{TOTAL} = P_{AV} + P_C$

$P_{TOTAL} = 61.40 + 4.90$

P_{TOTAL} = 66.30 watts

$\theta_{CA} = [T_{JMAX} - (P_{TOTAL} \times \theta_{JC}) - T_{AMBIENT}]/P_{TOTAL}$

$\theta_{CA} = [150 - (66.30 \times 1.0) - 40]/66.30$

θ_{CA} = 0.659°C/W Obviously the heat sink is more of a problem than the UIS capability.

Application to Other Circuits

Usually the designer of a circuit has carefully determined the temperature of the devices in his circuit over the entire range of operating conditions. Using only the junction temperature of the device at the start of a UIS pulse, the duration of the pulse and the current level of the pulse the designer can determine whether or not his/her application exceeds the UIS rating on the device. These quantities are easily measured or calculated. By superposition this rating can be applied to multiple or repetitive pulses as illustrated in the two examples shown. Any circuit can be analyzed for UIS stress using this approach. There is no need for a separate repetitive UIS rating.

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2. Rodney R. Stoltenburg, "Boundary of Power-MOSFET Unclamped Inductive Switching (UIS) Avalanche Current Capability," Proc. 1989 Applied Power Electronics Conference, pp 359-364, March 1989
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HARRIS QUALITY AND RELIABILITY

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Quality and Reliability Assurance

The ability to build and maintain the high levels of quality and reliability today, depends on inherent design and process capability, and not the degree of test and inspection. Both the design and production facilities for Power MOSFETs are totally new, with state-of-the-art equipment and process techniques which deliver this needed capability.

In-Process Quality Control

All critical phases of the highly automated power MOSFET manufacturing cycle have been characterized with respect to their intrinsic variability. Statistical limits have been established to give warning of abnormal process trends and fluctuations, based on this intrinsic capability. These limits are constantly tightened as the process improves and are well within the engineering specifications. The emphasis at Harris is to employ statistical methods at the point of control, rather than an inspection point at the end of a process.

Control of Outgoing Product

The quality control lot acceptance sampling of finished product is performed after manufacturing has performed 100% inspection of all specified electrical characteristics. The current sampling level is 0.1% AQL for electrical parameters, and is constantly being improved. However, due to tight parameter distributions gained through process control and inherent design capability, the average outgoing quality level (AOQ) to the customer has been in the order of 100 PPM (0.01%).

Reliability Assurance

Harris Semiconductor has a world-wide reliability program that helps to shape the direction of new product development, assures that the reliability level is maintained throughout the production cycle, and develops specific models to predict the reliability in the end-use application. In order to meet these objectives, a reliability facility is maintained at each manufacturing location for real-time feedback. A centralized reliability engineering organization develops all new test methods and supports new product/process development. Each group is fully trained in the reliability and applied statistics disciplines, as well as failure analysis, and are responsible for using these techniques to monitor and improve product capability.

The Reliability Program

The reliability-assurance program operates at all stages of production, using the following four-pronged approach:

Product Design and Development

During early development, initial product lots are characterized through accelerated reliability tests which establish the product capability. Once the design had been fine-tuned, multiple production runs are initiated and samples are subjected to a full range of standardized accelerated tests. All lots must meet pre-established reliability standards before any new design or process can be released for production.

Wafer HTRB

Harris Semiconductor has developed a totally unique in-line reliability test performed at the wafer level. Samples from each wafer lot receive a 24-hour +150°C bias life test to measure passivation integrity and surface cleanliness.

Real Time Indicators (RTI)

RTI's are short-duration accelerated-stress tests used to control the occurrence of specific failure mechanisms that can significantly affect product reliability. The stress levels are designed to induce failures, so that product-capability shifts can be detected and corrected. They are performed weekly at each manufacturing location. In this real-time method of determining reliability, a continuous flow of data is provided to indicate how well the manufacturing process is performing product.

TABLE 1. TYPICAL MOSFET RTI TESTS

TEST	CONDITIONS	PACKAGE	TYPICAL DURATION
Power Cycling	PD = 4.75W T_J = +35°C - 175°C (approx.)	Plastic	10 - 15K Cycles
Power Cycling	PD = 4.75W T_J = +35°C - 175°C (approx.)	TO-3	20 - 50K Cycles
D-S Bias Life	T_A = +150°C 80% of Drain Source	All	168 Hours
G-S Bias Life	G - S = 16V T_A = +150°C	All	168 Hours

Requalification Program (RQP)

Each product is requalified every six to twelve months to the same matrix of tests required for the initial production release. This operation measures the changes in the total capability of each MOSFET family to meet the original reliability design objectives. Table 2 is typical of the data generated for RQP.

TABLE 2. ACCELERATED POWER MOSFET TEST RELIABILITY SUMMARY

PACKAGE	TEST AND CONDITIONS	DURATION	CUM. HOURS OR CYCLES	% NON-FUNCTIONAL
All	Bias Life Drain-Source = 80% of rated T_A = +150°C	500 Hours	300,000	0.33
All	Bias Life Gate-Source = 16V, T_A = +150°C	500 Hours	270,000	0.00
All	Operating Life T_A = +150°C, Free Air	500 Hours	230,000	0.00
TO-31 TO-39	Thermal Cycling -65°C to +150°C	400 Cycles	133,600	0.30
TO-220	Thermal Shock -65°C to +150°C	400 Cycles	100,000	0.00
TO-31 TO-39	Power Cycling Delta T_J = +78°C PD = 56W (TO-3) or 2W (TO-39)	20,000 Cycles	5,480K	0.73
TO-220	Power Cycling Delta T_J = +135°C, PD = 4.75W	10,000 Cycles	1,850K	0.00
TO-220	Pressure Cooker	24 Hours	3,072	0.00

FAILURE RATE IN %/1000 HOURS AT 60% UCL			
TEST	T_A = +125°C	T_A = +90°C	T_A = +75°C
Bias Life	0.09	0.005	0.001
Operating Life	0.07	0.004	0.001

NOTE: Failure rate based on Nonfunctional performance in an operating mode, extrapolated from +150°C data using 1.0eV activation energy.

Harris Semiconductor

TechBrief

No. TB304 February 1994

Harris Power

ADVANCED POWER PACKAGE CONSTRUCTION METHOD RAISES TO-252 RELIABILITY TO NEW HEIGHTS

This technical backgrounder is intended to show how Harris redesigned the TO-252 surface-mount power package into the most reliable package of its type in the industry.

Surface-Mount Packaging Introduction

The continuing development of surface-mount technology (SMT) as a replacement for conventional through-hole mounting of electronic components on single-sided printed circuit boards has led to a host of advantages for electronics equipment manufacturers. From an integrated circuit standpoint, SMT allows manufacturers to optimize packaging density since ICs can be mounted on both sides of a board. SMT also offers thrifty and efficient use of material resources by permitting circuit boards to be smaller, closer component spacing, lower assembly costs and more compact and lighter system housings. Semiconductor companies have steadily promoted SMT growth by creating a variety of high-density, high lead-count ICs designed to be easily assembled onto the smaller footprints of SM circuit boards.

Most circuit boards perform functions in addition to the signal processing and logic operations handled by ICs. To interface with and drive off-board components such as amplifiers, motors, printer hammers, relays and the like requires power devices mounted on SM boards in close proximity to their signal sources. But SMT power devices are not as simple to use as their IC partners. Because of the reduced size of SM boards, the confined space alloted for the package and the greater dissipation of a power device, attention to thermal management and heat sinking take on greater significance.

To squeeze a power device into the confined area demanded by SM boards, semiconductor manufacturers have developed the plastic TO-252 package, popularly known as the D-pak (see Figure 1). With its gull-wing leads and metal back designed to pull heat from the device inside, the TO-252 offers to designers a high-power SM package. Unlike the variety of IC packages that designers can choose among, the TO-252 has become the workhorse package for SM power MOSFETs and rectifiers. Since it is widely used and applied in applications in which device failure is more probable because of internal heat generation, it is vital that TO-252-packaged power devices meet the highest standards for reliable operation.

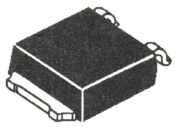

FIGURE 1. TO-252

While today's TO-252-packaged power devices are manufactured to meet extremely high reliability standards, that has not always been the case. In the recent past, all the leading power semi- conductor suppliers of the TO-252 have been hampered by manufacturing problems that are rooted in the package's size, materials and fabrication methods. And these problems can be inadvertently passed on to users who don't detect them until after devices have been assembled into boards.

Like its competitors, Harris Semiconductor has experienced problems with the package. When unexplained problems arose on customer production lines, the company launched an exhaustive year-long investigation into the TO-252 that encompassed every detail of its manufacturing process, materials, fabrication, process control and testing. The result of this comprehensive effort, undertaken with the assistance of a number of customers who produce computer, automotive and cellular telephone products, is a vastly improved method for building and testing TO-252-packaged power devices. Extensive monitoring and testing of tens of thousands of production line devices reveals that the redesigned TO-252 is a robust power package capable of surviving extremely demanding thermal environments during assembly onto boards and under operating conditions.

Since no process is ever perfect, Harris Semiconductor offers this report to power designers and production personnel to increase awareness of problems that may occur using plastic, surface-mount power devices. By understanding the structural foundation of the package and the improvements incorporated in the Harris manufacturing process, users can have increased confidence that the company's TO-252 power devices will provide unmatched service and reliability in any application and environment for which the devices are intended.

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The TO-252 Problem

When a TO-252-packaged power device fails after it has been assembled into a SM circuit board, the most likely conclusion that a user might draw is that the semiconductor die has cracked from thermal stresses induced by their soldering process. However, research indicates that the die was likely damaged during the manufacturing process and that the thermal shock of soldering only exacerbates the problem. There is no evidence to conclude that a user's mounting or assembly methods are the root of the problem. Die cracking is a generic problem in the TO-252 and can affect any manufacturer. The smaller the semiconductor die (its physical dimensions) the less likely it is to crack.

The root cause of die cracking stems from the materials and physical configuration of the TO-252 and the size of the die put into the package. In the manufacturing process, the die is attached to the header by a thin layer of solder (see Figure 2). The solder serves to reduce the thermal coefficient of expansion mismatch between the silicon die and the copper header.

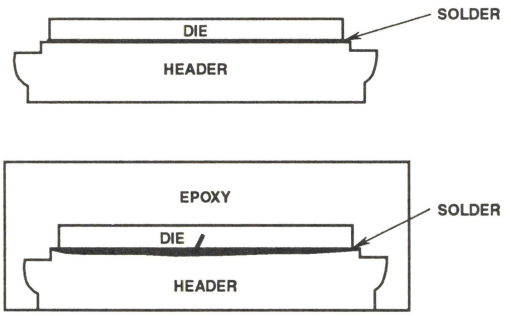

FIGURE 2.

The next step is to put an epoxy encapsulation over the die and header to form the package's molded outer shell (Figure 2). The shrinking of the mold epoxy compound forces the header to deflect, but in the opposite direction from the die attach process (concave on the top, convex on the bottom). This type of stress puts tension on the bottom of the die which can lead to cracking because the die is not as resistant to stress in this direction. Deflection of the header is more pronounced under epoxy curing than during die attach resulting in greater forces on the die.

Slight cracks in the die may result from the shrinking mold compound but they usually do not result in electrical failure of the device. It is the thermal shock of wave soldering during board assembly that forces the cracks to open wider and lead to eventual failure.

The TO-252 Solution

After identifying the primary cause of failed devices, engineers at Harris initiated an extensive program to redesign the TO-252 by changing materials and increasing the strength of mechanical components. This involved experimentation with different components supported by a sophisticated computer-aided design technique called Finite Element Analysis (FEA).

Initial analysis showed that the standard 20-mil thick header could bow by 1- to 2-mils during epoxy curing. This bowing puts excessive tension on the backside of the die, making it more susceptible to cracking. After many experiments, it became clear that the amount of deflection with a 20-mil header could not be compensated for with solder thickness, assembly methods or low-stress epoxies. Through FEA, it was determined that increasing the header thickness to 35-mils would eliminate most of the deflection. To achieve a 35-mil thickness without retooling all the mount and mold equipment, it was decided to use a pedestal of 35-mils under the die.

FEA is an extremely valuable tool that permits the modeling of a device's critical package elements, materials, headers, overcoat material, oxides and others. It provides solutions for reducing stress at dissimilar material junctions, thus minimizing device failure. The real benefit of FEA is its ability to simulate complex packaging relationships in a fast and accurate way. The stress models produced by FEA can be generated faster and at lower cost than by actually constructing and modifying physical models. FEA models point the way to the most favorable solutions which can then be implemented with actual materials.

FEA also came into play to help determine the best epoxy compound to use. The epoxy is probably the most critical element in the problem of cracked die because its curing generates the forces that cause the header to bow. And the bowing of the header produces the tension that cracks the die. To solve the problem, engineers selected an improved epoxy which balances stress vs. power cycling reliability. They then tested the new compound with the largest die that fit in the TO-252 to ensure that no cracking occurred.

At this point, the critical elements for solving the problem had fallen into place: increase the header thickness to 35 mils, go to an improved epoxy to reduce tension on the die and improve the process control over the thickness of the solder between the die and header. One other change in the manufacturing process was made to prevent any unnecessary shock to the die when the completed package is separated from the strip that holds a whole run of devices together. The conventional way to separate devices is called frame shear, a mechanical method that shears the strip away and can transfer forces from the package's heatsink to the die, possibly leading to cracking. In place of frame shear, Harris employs a less stressful method of device separation. In this technique, a shallow groove (10 mils deep) is cut into the heatsink portion of the package to reduce the force on the header and die when separating the package from the strip.

After hundreds of thousands of devices were fabricated with the new process, Harris engineers pulled tens of thousands off the line and subjected them to a grueling reliability test. The test is called solder shock and requires that the devices be fully immersed in a liquid solder bath at a temperature of 260°C for 10 seconds. Solder shock closely simulates the conditions that the package is subjected to when a user wave solders the part into a SM circuit board. The thermal shock of the solder bath is intended to increase the stress on the header and cause sufficient movement to make any existing crack wider detectable via electrical testing.

Harris has run solder shock tests on over 24,000 TO-252-packaged devices during the past year and no device has ever failed. Over 15,000 devices were chemically decapsulated and correlated to solder shock results. No die cracks were ever found when examined under high-power magnification. In addition, the company has sold more than 4.7 million devices without having any reports or returns due to a cracked die. This record of reliability is unmatched by any other manufacturer of TO-252-packaged power semiconductors and should give users confidence that the company offers the manufacturing and engineering capabilities to produce the highest quality products for today's complex electronic systems.

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PACKAGING AND ORDERING INFORMATION

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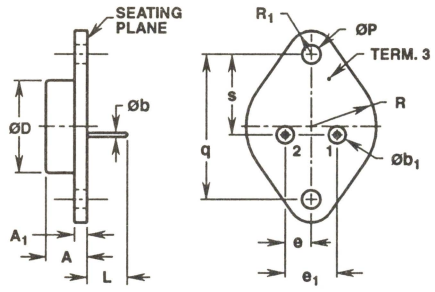
ORDERING INFORMATION

To order any part in this databook use full part number on the datasheet.

Hermetic Steel Packages



NOTES:

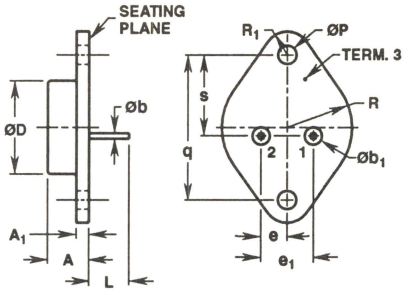
1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-204AA outline dated 11-82.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of seating plane.
5. Controlling dimension: Inch.
6. Revision 2 dated 6-93.

TO-204AA

JEDEC TO-204AA HERMETIC STEEL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.310	0.330	7.88	8.38	-
A_1	0.060	0.065	1.53	1.65	-
Øb	0.038	0.042	0.97	1.06	2, 3
$Øb_1$	0.138	0.145	3.51	3.68	-
ØD	-	0.800	-	20.32	-
e	0.215 TYP		5.46 TYP		4
e_1	0.430 BSC		10.92 BSC		4
L	0.430	-	10.93	-	-
ØP	0.155	0.160	3.94	4.06	-
q	1.187 BSC		30.15 BSC		-
R	0.495	0.525	12.58	13.33	-
R_1	0.131	0.185	3.33	4.69	-
s	0.655	0.675	16.64	17.14	-

Hermetic Steel Packages (Continued)



NOTES:

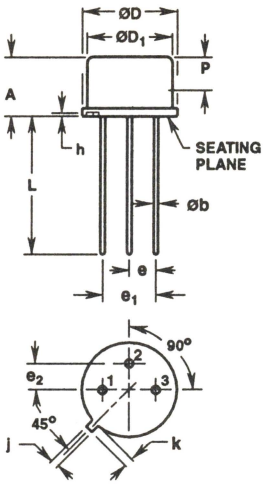
1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-204AE outline dated 11-82.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of seating plane.
5. Controlling dimension: Inch.
6. Revision 2 dated 6-93.

TO-204AE

JEDEC TO-204AE HERMETIC STEEL PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.310	0.330	7.88	8.38	-
A_1	0.060	0.065	1.53	1.65	-
Øb	0.057	0.063	1.45	1.60	2, 3
$Øb_1$	0.138	0.145	3.51	3.68	-
ØD	-	0.800	-	20.32	-
e	0.215 TYP		5.46 TYP		4
e_1	0.430 BSC		10.92 BSC		4
L	0.440	0.480	11.18	12.19	-
ØP	0.155	0.160	3.94	4.06	-
q	1.187 BSC		30.15 BSC		-
R	0.495	0.525	12.58	13.33	-
R_1	0.131	0.185	3.33	4.69	-
s	0.655	0.675	16.64	17.14	-

Metal Can Packages



TO-205AB

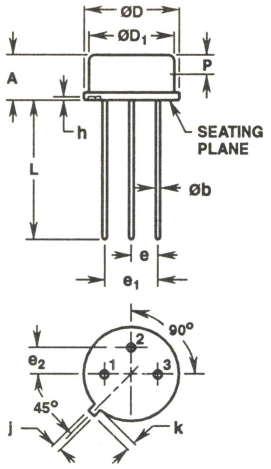
3 LEAD JEDEC TO-205AB HERMETIC METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.240	0.260	6.10	6.60	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
$ØD_1$	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e_1	0.190	0.210	4.83	5.33	4
e_2	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.560	12.70	14.22	3
P	0.100	-	2.54	-	5

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AB outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inches (0.254mm).
6. Controlling dimension: Inch.
7. Revision 1 dated 6-93.

Metal Can Packages (Continued)



TO-205AF

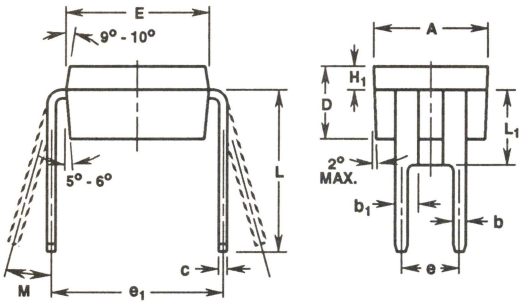
3 LEAD JEDEC TO-205AF HERMETIC METAL CAN PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.160	0.180	4.07	4.57	-
Øb	0.016	0.021	0.41	0.53	2, 3
ØD	0.350	0.370	8.89	9.39	-
$ØD_1$	0.315	0.335	8.01	8.50	-
e	0.095	0.105	2.42	2.66	4
e_1	0.190	0.210	4.83	5.33	4
e_2	0.095	0.105	2.42	2.66	4
h	0.010	0.020	0.26	0.50	-
j	0.028	0.034	0.72	0.86	-
k	0.029	0.045	0.74	1.14	-
L	0.500	0.560	12.70	14.22	3
P	0.075	-	1.91	-	5

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-205AF outline dated 11-82.
2. Lead dimension (without solder).
3. Solder coating may vary along lead length, add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of seating plane.
5. This zone controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 inches (0.254mm).
6. Controlling dimension: Inch.
7. Revision 2 dated 6-93.

Plastic Packages



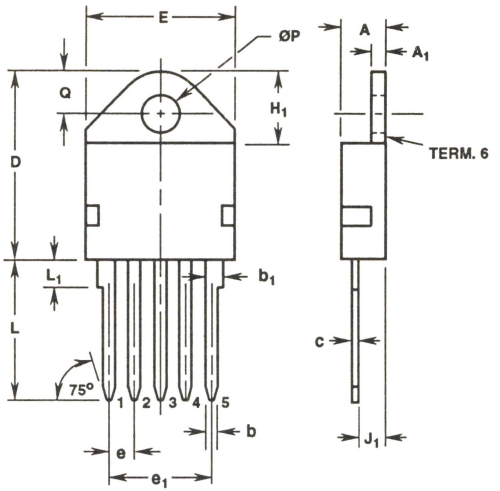
4 PIN DIP

4 PIN DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.194	0.198	4.93	5.02	-
b	0.020	0.024	0.51	0.60	1, 2
b_1	0.035	0.045	0.89	1.14	1, 2
c	0.013	0.017	0.34	0.43	1, 2
D	0.126	0.134	3.21	3.40	-
E	0.242	0.248	6.15	6.29	-
e	0.100 BSC		2.54 BSC		3
e_1	0.300	-	7.62	-	3
H_1	0.038	0.042	0.97	1.06	-
L	0.266	0.296	6.76	7.51	-
L_1	0.126	0.136	3.21	3.45	-
M	0°	15°	0°	15°	-

1. Lead dimension (without solder).
2. Add typically 0.0006 inches (0.015mm) for solder coating.
3. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
4. Controlling dimension: Inch.
5. Revision 1 dated 1-93.

Plastic Packages (Continued)



MO-093AA

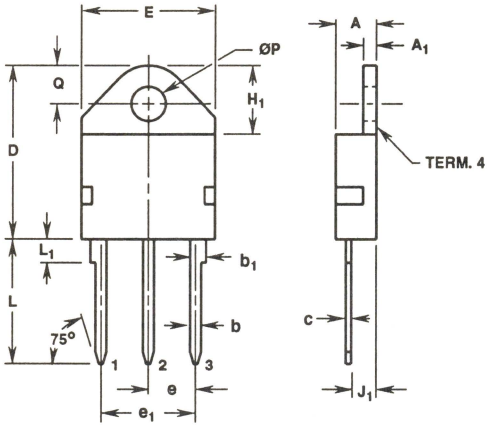
5 LEAD JEDEC MO-093AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.195	4.70	4.95	-
A_1	0.058	0.062	1.48	1.57	-
b	0.049	0.053	1.25	1.34	3, 4, 5
b_1	0.070	0.080	1.78	2.03	3, 4
c	0.018	0.022	0.46	0.55	3, 4, 5
D	0.800	0.820	20.32	20.82	-
E	0.615	0.625	15.63	15.87	2
e	0.110 TYP		2.80 TYP		7
e_1	0.438 BSC		11.12 BSC		7
H_1	-	0.330	-	8.38	-
J_1	0.115	0.125	2.93	3.17	8
L	0.575	0.600	14.61	15.24	-
L_1	-	0.130	-	3.30	3
ØP	0.159	0.163	4.04	4.14	-
Q	0.176	0.186	4.48	4.72	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC MO-093AA outline dated 2-90.
2. Tab outline optional within boundaries of dimensions E and Q.
3. Lead dimension and finish uncontrolled in L_1.
4. Lead dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder coating.
6. Maximum radius of 0.050 inches (1.27mm) on all body edges and corners.
7. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
8. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
9. Controlling dimension: Inch.
10. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-218AC

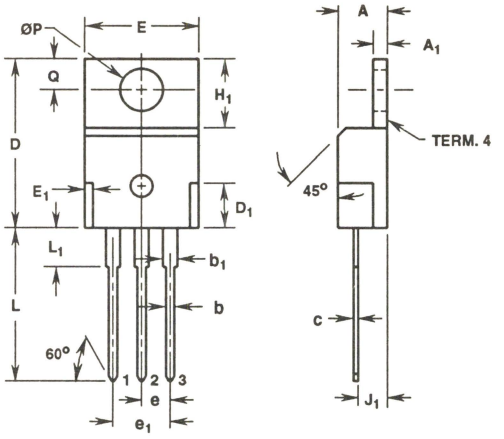
3 LEAD JEDEC TO-218AC PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.195	4.70	4.95	-
A_1	0.058	0.062	1.48	1.57	-
b	0.049	0.053	1.25	1.34	3, 4, 5
b_1	0.070	0.080	1.78	2.03	3, 4
c	0.018	0.022	0.46	0.55	3, 4, 5
D	0.800	0.820	20.32	20.82	-
E	0.615	0.625	15.63	15.87	2
e	0.219 TYP		5.56 TYP		7
e_1	0.438 BSC		11.12 BSC		7
H_1	-	0.330	-	8.38	-
J_1	0.115	0.125	2.93	3.17	8
L	0.575	0.600	14.61	15.24	-
L_1	-	0.130	-	3.30	3
ØP	0.159	0.163	4.04	4.14	-
Q	0.176	0.186	4.48	4.72	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-218AC outline dated 6-86.
2. Tab outline optional within boundaries of dimensions E and Q.
3. Lead dimension and finish uncontrolled in L_1.
4. Lead dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder coating.
6. Maximum radius of 0.050 inches (1.27mm) on all body edges and corners.
7. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
8. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
9. Controlling dimension: Inch.
10. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-220AB

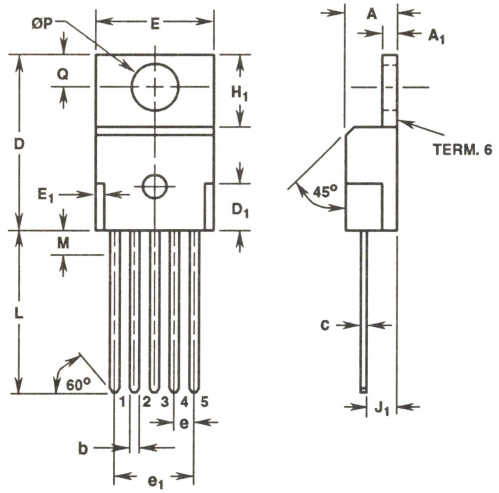
3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

Plastic Packages (Continued)



TS-001AA

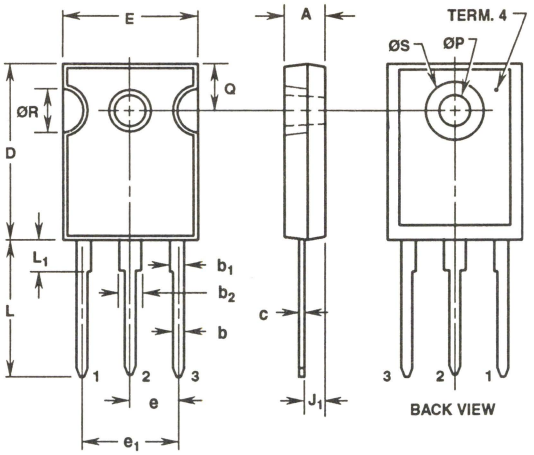
5 LEAD JEDEC TS-001AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.067 TYP		1.70 TYP		5
e_1	0.268 BSC		6.80 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
M	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TS-001AA outline dated 8-89.
2. Lead finish uncontrolled in zone M.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 3 dated 12-93.

Plastic Packages (Continued)



TO-247

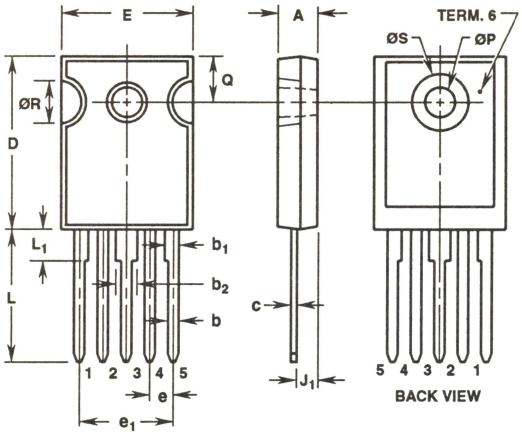
3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-247

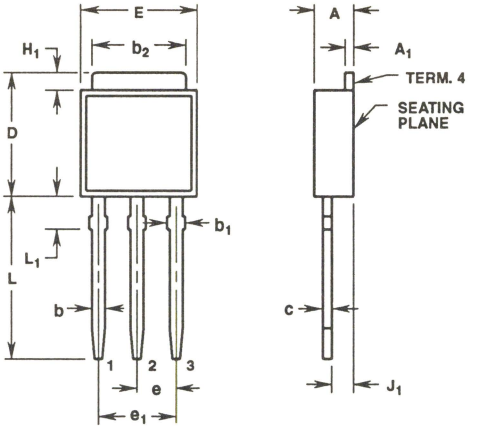
5 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.110 TYP		2.79 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-251AA

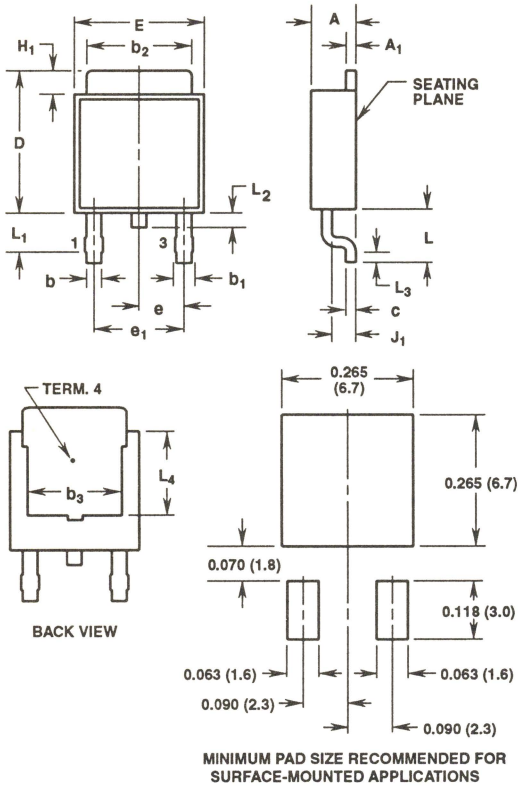
3 LEAD JEDEC TO-251AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled.
3. Dimension (without solder).
4. Add typically 0.0006 inches (0.015mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

Plastic Packages (Continued)



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-252AA

2 LEAD JEDEC TO-252AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.075	0.090	1.91	2.28	3
L_2	0.025	0.040	0.64	1.01	-
L_3	0.020	-	0.51	-	4, 6
L_4	0.170	-	4.32	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_4 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled.
4. Dimension (without solder).
5. Add typically 0.0006 inches (0.015mm) for solder coating.
6. L_3 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 2 dated 6-93.

POWER MOSFETs 14

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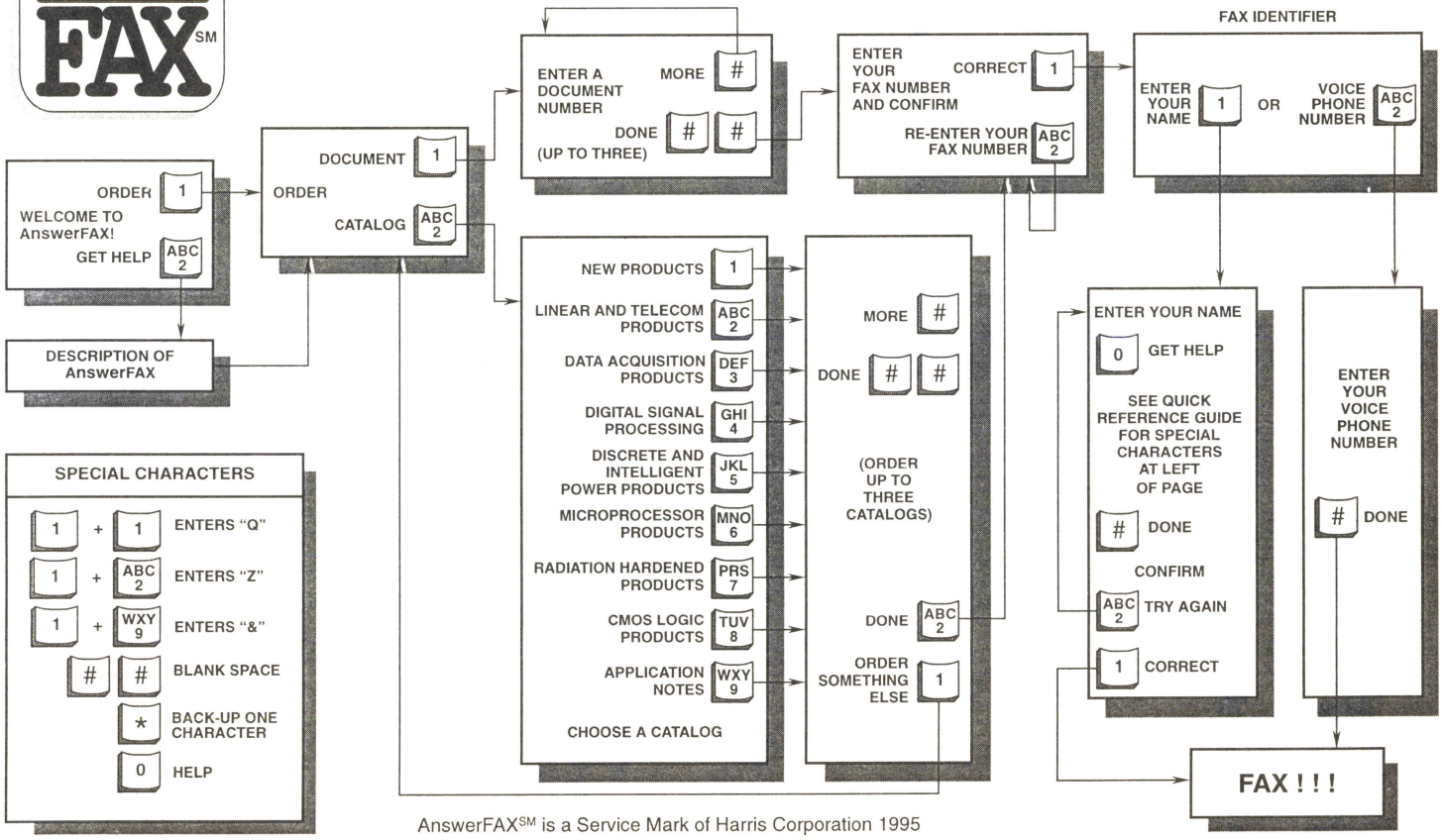

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	DB316	**POWER MOSFET DATA BOOK SUPPLEMENT** (1996: 380pp) This data book contains the data sheets of recently introduced products and also updates some of the data sheets in the Power MOSFET Data Book DB223B. These data sheets contain the detailed specification for these products.
	DB235B	**RADIATION HARDENED** (1993: 2,232pp) The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
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	DB321	**APPLICATIONS FOR COMMUNICATION ICs** (1997: 392pp) Application Notes and Tech Briefs for Harris communication products that range from wireless PRISM™ 2.4GHz WLAN chip set to Telecom HC5517 ringing SLIC. Also Data Acquisition and Digital Signal Processing.
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	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
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Melville, NY 11747
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TEL: (918) 660-5105
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Salt Lake City
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FAX: (408)451-1600

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IS - 43100 Ra'anana
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